EE230: Lab 2.
Voltage Regulator using Zener Diode and BJT

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1 Overview of the experiment

1.1 Aim of the experiment

To understand the limits of performance of a Zener regulator and BJT based series voltage regulator to appreciate the basic blocks of an integrated circuit voltage regulator.

1.2 Methods

The netlists for the Zener regulator and BJT voltage regulator were made in NGSPICE, subcircuits for Zener diode and SL100 and BC547 BJTs were directly used in the netlists. Plots for various dependencies were made as per the handout. The variation of V_{out} and I_Z, I_S, I_L with the resistance R_L were obtained by varying R_L from 1Ω to 1kΩ via the `.dc` operation in NGSPICE. After obtaining the plots, the answers to the questions provided in the handout were answered.

2 Design

2.1 Circuit Diagrams

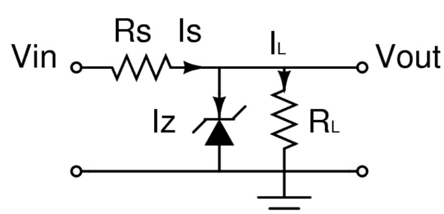

Figure 1.1: Zener Diode Based Voltage Regulator

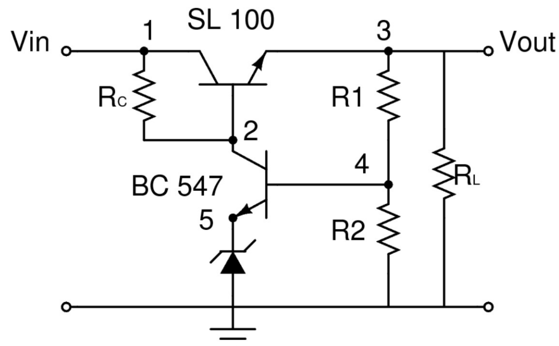

Figure 1.2: BJT Based Voltage Regulator

3 Simulation results

3.1 Code snippets

3.1.1 Operating Point Analysis for Zener Diode

```
DC Power Supply with Zener Diode Regulator
*Rohan Rajesh Kalbag - 20D170033

.SUBCKT ZENER_12 1 2
D1 1 2 DF
DZ 3 1 DR
VZ 2 3 10.8
.MODEL DF D(IS =27.5p RS=0.620 N=1.10 CJO =78.3p VJ=1.00 M =0.330
TT =50.1n)
.MODEL DR D(IS =5.49f RS=50 N=1.77 )
.ENDS

v1 1 0 dc 20
r1 1 3 470
vr1 3 2 0
x1 5 2 ZENER_12
r2 2 4 1k
vr2 4 0 0
vx1 5 0 0


.op
.control
run
print v(3) i(vx1) i(vr1) i(vr2)
.endc
.end
```

3.1.2 DC Analysis for Zener Diode

```
DC Power Supply with Zener Diode Regulator
*Rohan Rajesh Kalbag - 20D170033

.SUBCKT ZENER_12 1 2
D1 1 2 DF
DZ 3 1 DR
VZ 2 3 10.8
.MODEL DF D(IS =27.5p RS=0.620 N=1.10 CJO =78.3p VJ=1.00
M =0.330 TT =50.1n)
.MODEL DR D(IS =5.49f RS=50 N=1.77 )
.ENDS

v1 1 0 dc
r1 1 3 470
vr1 3 2 0
x1 5 2 ZENER_12
r2 2 4 1k
vr2 4 0 0
vx1 5 0 0


.dc v1 15 25 0.5
.control
run
print v(3) i(vx1) i(vr1) i(vr2)
plot v(3) vs v(1)
plot i(vx1) vs v(1)
.endc
.end
```

3.1.3 Behaviour of Zener regulator with variation in R_L

```
DC Power Supply with Zener Diode Regulator
*Rohan Rajesh Kalbag - 20D170033

.SUBCKT ZENER_12 1 2
D1 1 2 DF
DZ 3 1 DR
VZ 2 3 10.8
.MODEL DF D(IS =27.5p RS=0.620 N=1.10 CJO =78.3p VJ=1.00
M =0.330 TT =50.1n)
.MODEL DR D(IS =5.49f RS=50 N=1.77 )
.ENDS

v1 1 0 dc 20
r1 1 3 470
vr1 3 2 0
x1 5 2 ZENER_12
r2 2 4 1k
vr2 4 0 0
vx1 5 0 0


.dc r2 1 1k 50
.control
run
print v(3) i(vx1) i(vr1) i(vr2)
plot i(vx1) i(vr1) i(vr2)
plot v(3)
.endc
.end
```

3.1.4 Operating Point Analysis of BJT based voltage regulator

```
DC Power Supply with a BJT Series Regulator
*Rohan Rajesh Kalbag - 20D170033

.model bc547a NPN IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3
+ BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40
+ tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7
mjc=0.33 kf=2f

.model SL100 NPN IS=100f BF=80 ISE=10.3f IKF=50m NE=1.3
+ BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=100 RE=1 RC=10
+ tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7
mjc=0.33 kf=2f

.SUBCKT ZENER_12 1 2
D1 1 2 DF
DZ 3 1 DR
VZ 2 3 4.4
.MODEL DF D(IS =27.5p RS=0.620 N=1.10 CJO =78.3p VJ=1.00
M =0.330 TT =50.1n)
.MODEL DR D(IS =5.49f RS=50 N=1.77 )
.ENDS

v1 1 0 dc 20
rc 1 2 1k
q1 1 2 3 SL100
q2 2 4 5 bc547a
x1 0 5 ZENER_12
r1 3 4 10.21k
r2 4 0 14.79k
rl 3 0 1k
.op
.control
run
print v(1) v(2) v(3) v(4) v(5)
.endc
.end
```

3.1.5 DC Analysis of BJT based voltage regulator

```
DC Power Supply with a BJT Series Regulator
*Rohan Rajesh Kalbag - 20D170033

.model bc547a NPN IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3
+ BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40
+ tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7
mjc=0.33 kf=2f
.model SL100 NPN IS=100f BF=80 ISE=10.3f IKF=50m NE=1.3
+ BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=100 RE=1 RC=10
+ tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7
mjc=0.33 kf=2f

.SUBCKT ZENER_12 1 2
D1 1 2 DF
DZ 3 1 DR
VZ 2 3 4.4
.MODEL DF D(IS =27.5p RS=0.620 N=1.10 CJO =78.3p VJ=1.00 M =0.330
TT =50.1n)
.MODEL DR D(IS =5.49f RS=50 N=1.77 )
.ENDS

v1 1 0 dc
rc 1 2 1k
q1 1 2 3 SL100
q2 2 4 5 bc547a
x1 0 5 ZENER_12
r1 3 4 10.21k
r2 4 0 14.79k
rl 3 0 1k
.dc v1 15 25 0.5
.control
run
print v(3)
plot v(3) vs v(1)
.endc
.end
```

3.2 Simulation results

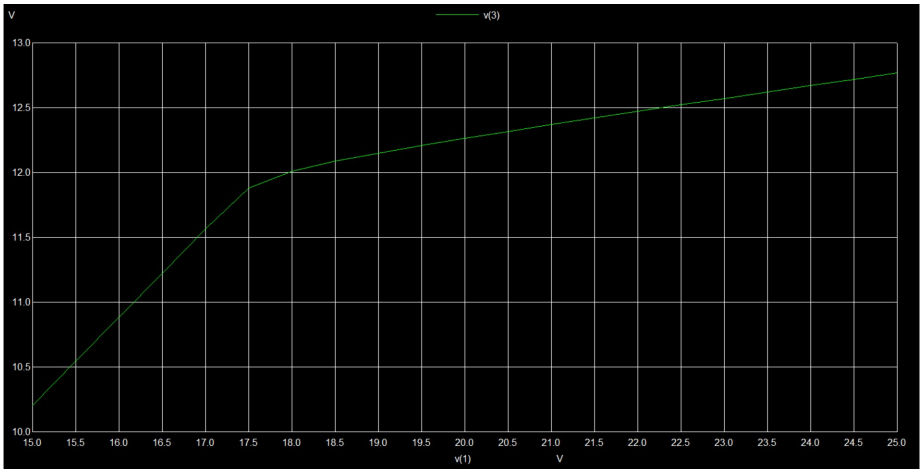

Fig 2.1
Variation of output DC voltage with input DC voltage for Zener regulator
v(3): V_{out}, v(1): V_{in}

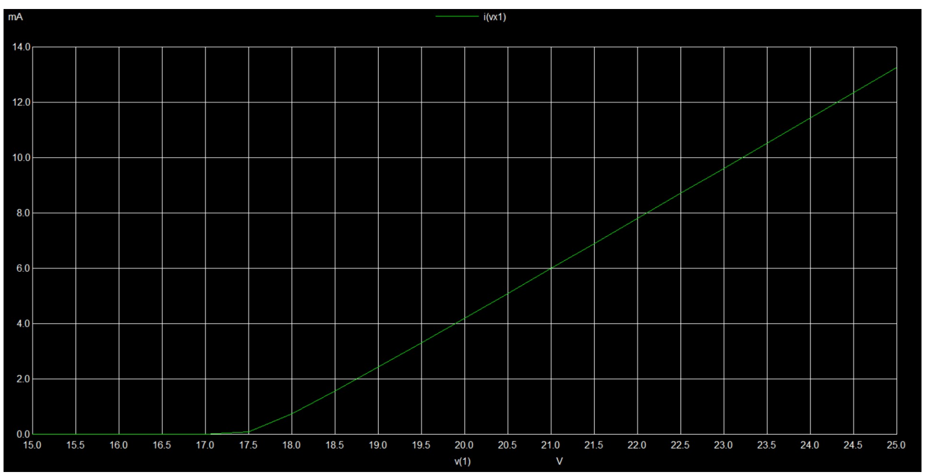

Fig 2.2
Variation of I_z with input DC voltage for Zener regulator
i(vx1): I_z(Current through Zener), v(1): V_{in}

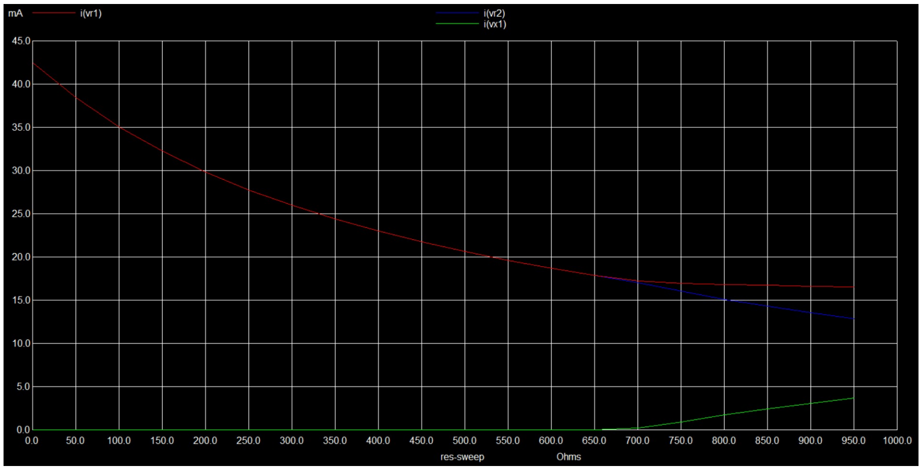

Fig 2.3
Variation of I_Z, I_S, I_L with change in R_L
i(vx1): I_z(Current through Zener)
i(r1): Current through R_S
i(r2): Current through R_L
res-sweep: Resistance R_L

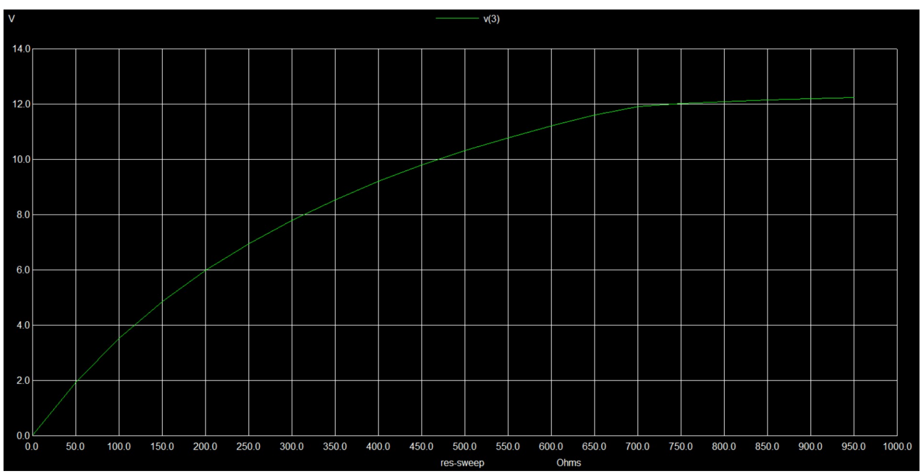

Fig 2.4
Variation of V_{out} with change in R_L
v(3): V_{out}, res-sweep: Resistance R_L

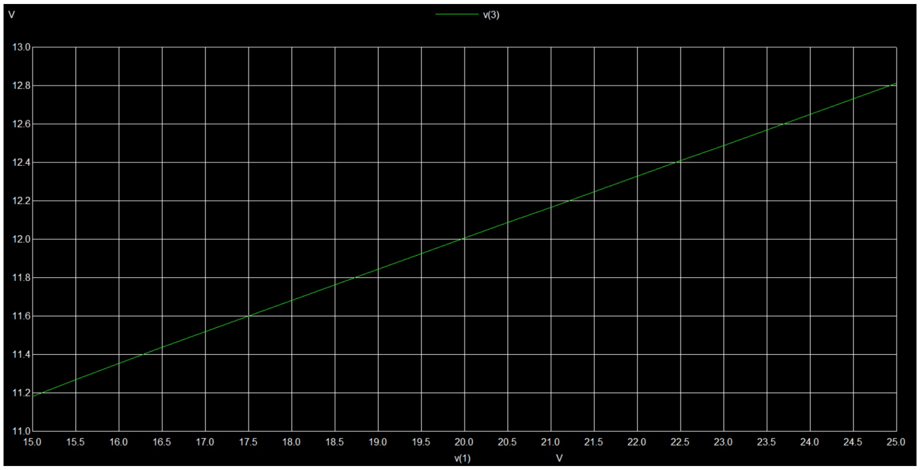

Fig 3.1
Variation of V_{out} with change in V_{in} for BJT based voltage regulator
v(3): V_{out}, v(1): V_{in}

4 Experimental results

4.1 DC Power Supply with Zener Diode Regulator

4.1.1 Part 1.1.2(a)

The values obtained from Operating Point NGSPICE simulation for $V_{in} = 20$V and $R_S = 470\Omega, R_L = 1k\Omega$ were

```
v(3) = 1.226269e+01
i(vx1) = 4.199669e-03
i(vr1) = 1.646236e-02
i(vr2) = 1.226269e-02
```

where v(3) denotes V_{out}, i(vx1) denotes I_Z, i(vr1) denotes I_S and i(vr2) denotes I_L

4.1.2 Part 1.1.2(b)

The plots obtained for DC analysis were Figures 2.1 and 2.2. The value of I_Z for $V_{in} \leq 17V$ is ≈ 0. Which is evident from Fig 2.2

4.1.3 Part 1.1.2(c)

The variation of V_{out} and I_Z, I_S, I_L with the resistance R_L can be seen in the plots shown in Fig 2.3 and 2.4. We notice in Fig 2.4 that the Zener diode behaves like a voltage regulator giving an output dc voltage of $\approx$ 12V only for around $R_L \geq 700\Omega$. We also observe that $I_Z \approx 0$ for $R_L < 700\Omega$ in Fig 2.3.

The theoretical minimum for R_L given $V_{in} = 20V, R_S = 470\Omega$ is when the Zener diode has $V_Z = 12V$, which can be achieved if $R_L \geq 705\Omega$. Hence the observed results match with the theoretical results.

4.2 DC Power Supply with a BJT Series Regulator

4.2.1 Part 1.2.1 Case(i)

All the node voltages obtained from Operating Point NGSPICE simulation for V_{in} = 20V and $R_L = 1k\Omega, R_1 = R_2 = 12.5k\Omega$ were

```
v(1) = 2.000000e+01
v(2) = 1.449511e+01
v(3) = 1.378716e+01
v(4) = 6.645576e+00
v(5) = 5.929149e+00
```

v(3) denotes V_{out} and v(1) denotes V_{in}

4.2.2 Part 1.2.1 Case(ii)

Upon varying R_1 and R_2 the value for which V_{out} was $\approx$ 12V is $R_1 = 10.21k\Omega$ and $R_2 = 14.79k\Omega$. The node voltages obtained for the Operating Point analysis of this circuit were. The nodes have been labelled according to the diagram

```
v(1) = 2.000000e+01
v(2) = 1.270274e+01
v(3) = 1.200561e+01
v(4) = 6.767221e+00
v(5) = 6.035238e+00
```

Thus we notice that v(3) $= V_{out} \approx$ 12V $=$ 12.0056V for the chosen values of R_1 and R_2.

4.2.3 Part 1.2.1 Case(iii)

The plots obtained after DC analysis was Fig 3.1. We notice that the V_{out} vs V_{in} characteristics of the BJT based regulator has an increasing linear behaviour at achieves 12V output at exactly 20V DC input. Meanwhile the Zener diode based regulator has an increasing non linear behaviour. The Zener regulator achieves 12V output at around 18V and not exactly 20V DC input.