EE 230 – Analog Lab - 2021-22/2 (Spring)

Lab 2: DC Power Supply

Unregulated DC Power Supply Learning

Objectives

1. Understanding the limits of performance of a Zener regulator
2. Understanding a BJT based series voltage regulator to appreciate the basic blocks of an IC voltage regulator.

1.1 DC Power Supply with Zener Diode Regulator

1.1.1 Zener Regulator - Analysis

Analyse the Zener diode regulator circuit given below.

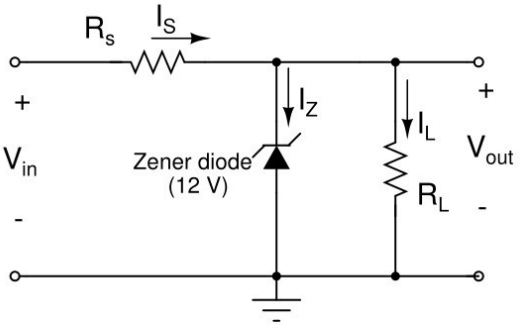

Fig.1 Zener regulator

Case (i): For $V_{in} = 20V$ (dc). Choose $R_s = 470\Omega$, $R_L = 1k\Omega$. Assume Zener voltage = 12 V and Zener region diode resistance = 125 Ω. Calculate V_{out}, I_s, I_z and I_L.

Case (ii): For V_{in} varying from 15V to 25V, $R_s = 470\Omega$, $R_L = 1k\Omega$. (Zener voltage = 12V and Zener region diode resistance = 125Ω). Consider a few V_{in} values between 15V and 25V.

Hint: For a given V_{in} value, apply Thevenin's theorem and represent the Zener regulator by its equivalent Thevenin voltage and resistance. This would make it easier to calculate V_{out}, and I_L, and then I_s and I_z.

1.1.2 NGSPICE Simulation

a) For $V_{in} = 20V, R_s = 470\Omega$, $R_L = 1k\Omega$, simulate and print V_{out}, I_s, I_z and I_L. Compare your simulation results with your earlier calculations. Best to use **.op** command for this.
(For obtaining currents I_L , and then I_s and I_z, you need to put a series voltage source with zero voltage and then print the currents).

Zener Diode Model

The best way to model a Zener diode is to consider it as a sub-circuit consisting of a forward diode connected in parallel with a reverse diode with a dc offset. The dc offset is typically chosen to be about 1 to 1.2V lower than the Zener voltage. We shall use the following sub-circuit for the 12V Zener diode.

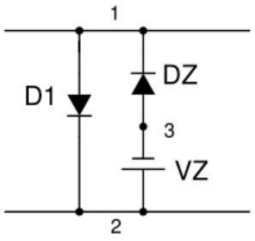

Fig.2 Zener Sub Circuit

```
.SUBCKT ZENER_12 1 2
D1 1 2 DF
DZ 3 1 DR
VZ 2 3 10.8
.MODEL DF D ( IS=27.5p RS=0.620 N=1.10 CJO=78.3p VJ=1.00 M=0.330
TT=50.1n)
.MODEL DR D ( IS=5.49f RS=50 N=1.77 )
.ENDS
```

You may key in the above sub-circuit in your .CIR file and then use it through the sub-circuit command:

x1 A K ZENER_12

where A and K are the anode and cathode nodes of the Zener diode, respectively.

b) See how well the Zener regulator regulates Vout for a range of V_{in} values. You should use the **.dc** command for this purpose. Format for the .dc command:

.dc source startval stopval stepsize

Obtain the Vout, I_S, I_Z and I_L values when Vin is varied from 15 to 25 V in steps of 0.5 V. (Assume $R_s = 470\Omega$, $R_L = 1k\Omega$). Observe I_Z values for $V_{in} \leq 17$V and explain the results.

c) For $V_{in} = 20V$, and $R_s = 470\ \Omega$, simulate for different values of R_L lower than 1 kΩ. For the given values, verify the simulation results with the theoretical value for the lowest value of R_L allowed for a Zener regulator.

1.2 DC Power Supply with a BJT Series Regulator

The circuit diagram of the BJT series regulator is shown below in Fig.3. You could think of this as the next step towards better regulation of output voltage against changes in V_{in} and R_L. This circuit has the basic blocks of a sophisticated IC regulator, such as 7812 (fixed 12V regulator). A general-purpose adjustable Voltage regulator IC essentially has about four parts, viz. a reference voltage, an error amplifier, a series active element and a resistor network for adjusting V_{out}.

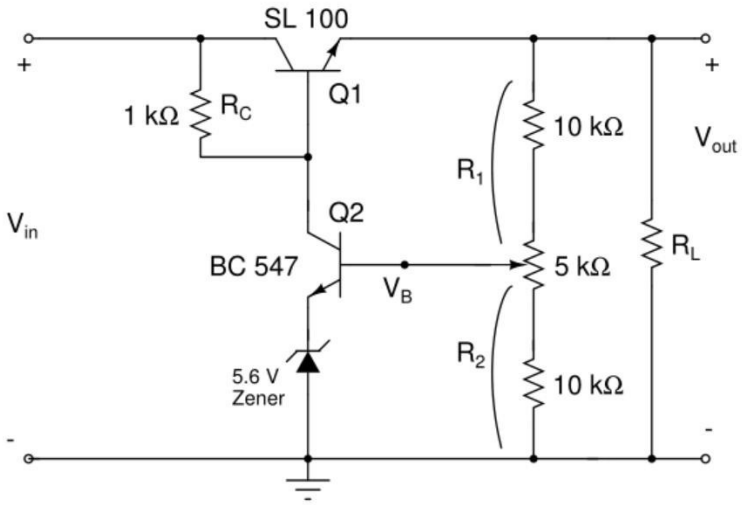

Fig.3 BJT series voltage regulator

In the circuit shown, Q_1 (SL100) is a medium power BJT with β of about 100, whereas Q_2 (BC547) is a low power BJT having β > 200, which is commonly used in amplifier circuits.

Operation of the BJT Series Regulator

The BJT series regulator is a combination of a reference voltage, error amplifier, a series element for regulating the voltage and a resistor network for sampling Vout. In Fig 3, Zener diode acts as the reference voltage, Q_2 acts as the error amplifier and Q_1, the series regulating element, and R_1, R_2 and the potentiometer as the resistive network. The circuit is essentially a negative-feedback amplifier.

Note that $V_B = V_{out}.R_2/(R_1 + R_2)$, it is directly proportional to Vout. Assume that Vout increases from the steady-state value due to $R_L\uparrow$ (or less load current). This would result in V_B also increasing proportionately, which would cause more base current to flow in Q_2 and consequently more collector current in Q_2, which would then drain away some of the base current flowing into Q_1, resulting in increased V_{CE} drop in Q_1, which would reduce Vout. A similar argument can be given for corrections when Vout decreases. Hence, we see that the circuit continuously samples Vout and corrects any voltage variations.

1.2.1 NGSPICE Simulation

BJT Models

The series regulator circuit has two BJTs, a medium power BJT and a low power BJT commonly used for small-signal amplifier applications. Their model files (sample model values) are given below. Since ours is a dc application, many small-signal parameters are not very important for our analysis. However, the ac parameters would be required to check whether the circuit is stable or not.

```
.model bc547a NPN IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3
+ BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40
+ tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7 mjc=0.33 kf=2f

.model SL100 NPN IS=100f BF=80 ISE=10.3f IKF=50m NE=1.3
+ BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=100 RE=1 RC=10
+ tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7 mjc=0.33 kf=2f
```

Format for BJTs: Q1 C B E bc547a, where C, B and E are the Collector, Base and Emitter nodes of the BJT.

Refer to the Common Emitter amplifier example given in Chapter 21 (page 451) of the NGSPICE-34-manual. There a 'generic npn' model is used. Here we are specifying the model parameters.

Simulation

Create a .CIR file to simulate the BJT series regulator circuit of Fig.3. Use Vin = 20 V, R_L = 1 kΩ. Note that in Fig 3, the value of R_1 is: 10kΩ + part of the 5 kΩ potentiometer; similarly, R_2 is: 10 kΩ + the remaining part of the 5 kΩ potentiometer). Hence, $R_1 + R_2$ = 25 kΩ.

Case (i) For Vin = 20 V, R_L = 1 kΩ, keep $R_1 = R_2$ = 12.5 kΩ. Print all the node voltages.

Case (ii) Vary R_1 and R_2 (while keeping $R_1 + R_2$ = 25 kΩ), so as to get Vout = 12 V approximately.

Case iii) for the R_1 and R_2 values you got for Vout = 12 V, perform a **.dc** analysis. (Keep R_L = 1 kΩ, and vary Vin from 15 V to 25 V in steps of 0.5 V). Compare these results with the ones you got for the Zener regulator.