EE230- Analog lab (Homework-3)
Spring Semester: Year 2021-22

January 21, 2022

Instructions:

- Show your netlists and simulation results of each question to the evaluating TA.
- **No Additional time will be given.**
- **You can refer:** NGSPICE tutorial, model files uploaded on the course moodle / MS Teams channel and your written netlists of previous experiments.

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1. Simulate the inverting amplifier circuit shown in the figure [1] with $R_1 = 1k\Omega$, $R_2 = 10k\Omega$. Don't forget to apply the supply voltage of $\pm 15V$.
2. Apply a sinusoidal input with a peak of $0.1V$ and frequency $1kHz$. Plot V_i and V_o with respect to time.
3. Now, change the input amplitude from 0.1 V to 2 V and observe the output waveform.
4. Plot the frequency response for $R_1 = 1k\Omega$, $R_2 = 10k\Omega$ and $R_1 = 1k\Omega$, $R_2 = 100k\Omega$, together on the same plot, with the gain in dB and frequency on log scale for the amplitude of $0.1V$ and frequency range of $10Hz$ to $10MHz$. Comment on the plots?
5. Repeat the above (steps 1 to 4) for Non-inverting amplifier circuit in the figure [1].
6. Simulate the Integrator circuit shown in the figure [1] with $R = 10k\Omega$, $C = 0.01\mu F$, $R' = 470k\Omega$. Note that R' is used to prevent the op-amp from entering saturation (because of a non-zero DC component in the input voltage or the op-amp bias current). Verify that your output waveform is triangular for a square wave input ($\pm 2V$, $1kHz$).
7. Simulate the differentiator circuit shown in the figure [1] with a triangular wave input ($\pm 2V$, $2.5kHz$), $R = 10k\Omega$, $C = 0.01\mu F$ and plot the output? Now, connect a small capacitor $C' = 0.001\mu F$ in parallel with R, and observe $V_o(t)$. Explain your observation.

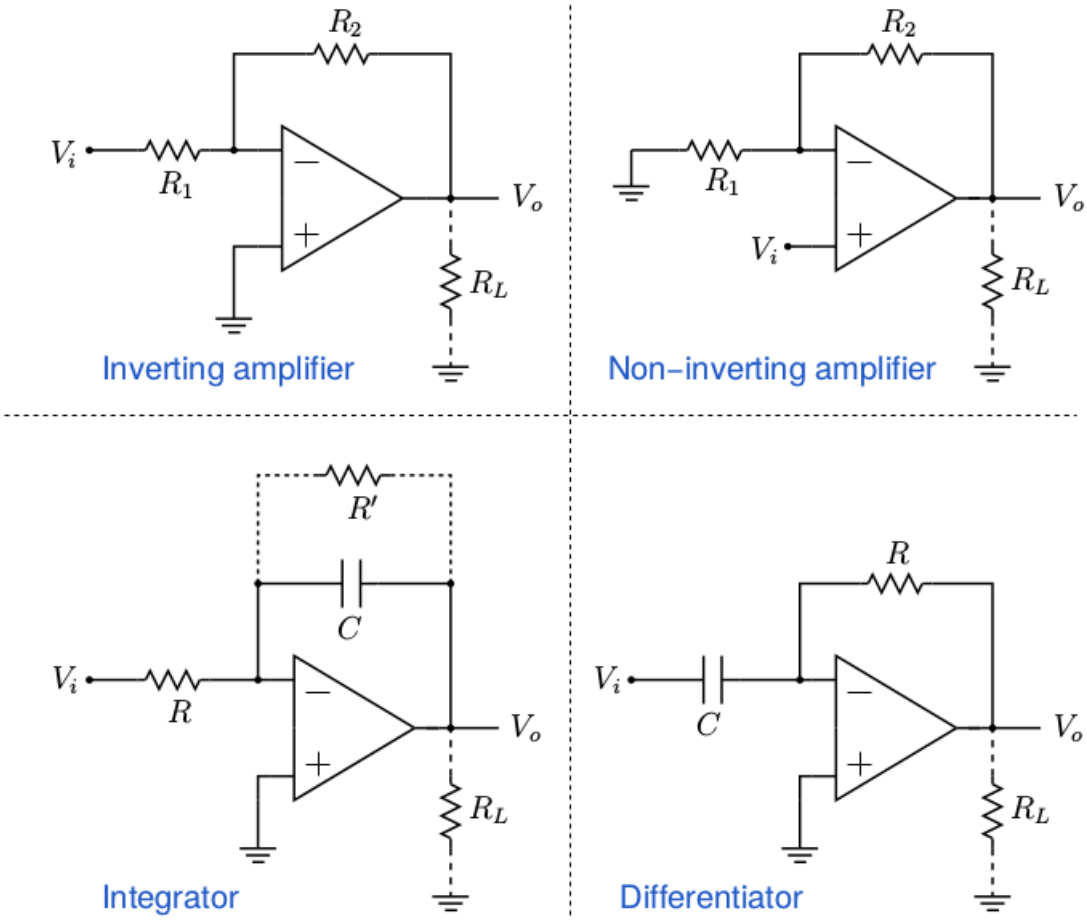

Figure 1: Basic OP-AMP based Circuits