EE230- Analog lab (Homework-4)
Spring Semester: Year 2021-22

January 29, 2022

Instructions:

- Show your netlists and simulation results of each question to the evaluating TA.
- **Deadline: Feb 3, 2:00 pm.**
- **You can refer:** NGSPICE tutorial, model files uploaded on the course moodle / MS Teams channel and your written netlists of previous experiments.

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1. Write NGSPICE netlist for the circuit shown in Figure [1]. For the given circuit, use a single supply of $+5V$ for the op-amp LM324. Sweep the input voltage (V_{in}) from $0.1V_{dc}$ to $5V_{dc}$ in the steps of $0.1V$ and comment on the relationship between V_{in} and V_{out}.

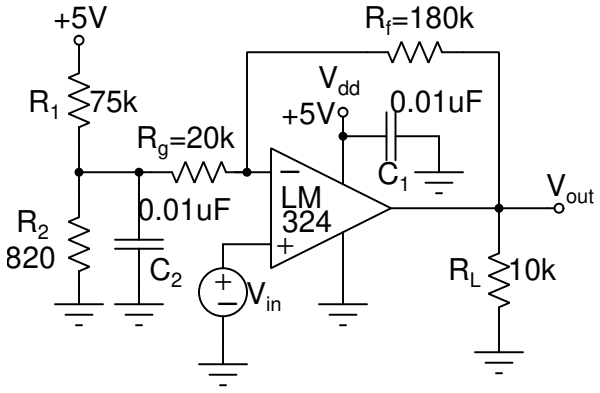

Figure 1: OP-AMP based Circuit-1

2. Write NGSPICE netlist of the circuit shown in Figure [2]. Use op-amp 741 and supply voltage of $\pm 15V$.

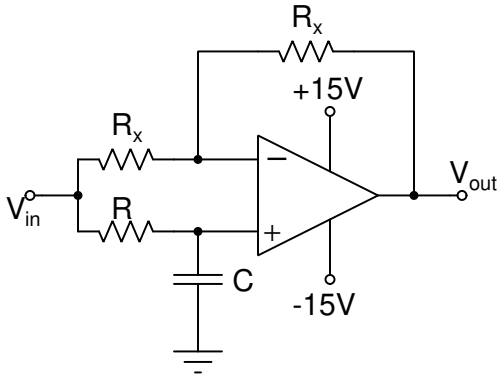

Figure 2: OP-AMP based Circuit-2

(a) Simulate the circuit, where $R_x = 10k\Omega$, $R = 10k\Omega$ and $C = 47nF$. Perform the AC analysis and observe the phase and gain plots for the circuit. Make sure that the dc component is $0V$ and ac signal should be $1V_{pp}$ for the V_{in} source.

(b) Now, repeat above step for $R_x = 10k\Omega$, $R = 1k\Omega$ and $C = 1nF$.

(c) Write your observations in the gain plots and phase plots for part (a) and (b)?

(d) What is the gain value in linear scale for part (a) and (b)?

(e) What is the above circuit called and what are the applications of the circuit you could think of?

3. (a) Write NGSPICE netlist for the circuit shown in Figure [3]. Use op-amp 741 and supply voltage of $\pm 15V$. In a single window, plot V_{out} v/s V_{in} for $-5V \leq V_{in} \leq +5V$. Find the values of V_{in} for which V_{out} trips.

Upper trip point $V_T^+ =$ ——

Lower trip point $V_T^- =$ ——

(b) Write NGSPICE netlist for the circuit shown in Figure [4]. Use the same op-amp and power supplies as in Part (a). Observe the input and steady state output from 100 ms to 110 ms.

(c) Write NGSPICE netlist which interconnects the circuits in Figure [3] and [4] to form a closed loop without any external input.

Hint: An output of Figure [4] in part (b), let's call it ($V_{out}^{'}$), will be an input to Figure [3] in part (a). Also, an output of Figure [3] in part (a) will be an input to Figure [4] in part (b). **Output of Figure [3] will be your final output (V_{out}).**

You should re-use the existing netlists from part (a) and (b). **You can use the existing netlists as sub-circuits in writing the netlist for part (c) (optional).**

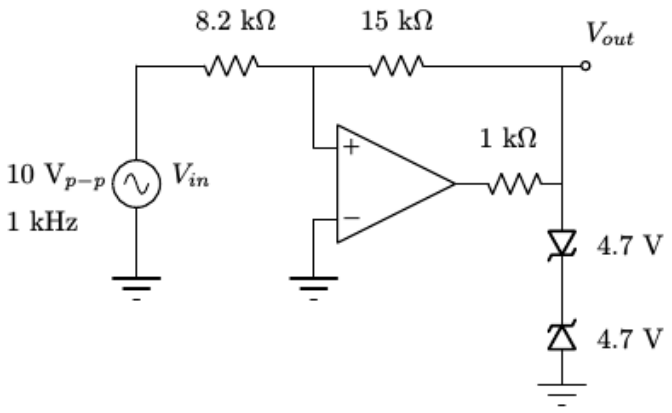

Figure 3: OP-AMP based Circuit-3

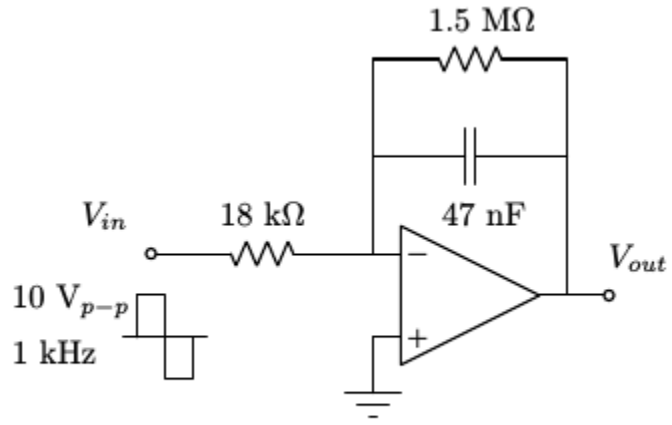

Figure 4: OP-AMP based Circuit-4

i. Observe the steady state outputs V_{out} and $V_{out}^{'}$ from 99 ms to 101 ms.
ii. Write the frequency of V_{out} = ——

Positive peak of $V_{out}^{'}$= ——

Negative peak of $V_{out}^{'}$ = ——