EE 230 - Analog Lab - 2021-22/2

Homework 2

Part A – Unregulated DC Power Supply

Learning Objectives

1. Understanding the problems associated with increasing the capacitor value in an unregulated power supply so as to reduce the ripple.
2. Understanding the limits of performance of a Zener regulator
3. Understanding a BJT based series voltage regulator to appreciate the basic blocks of an IC voltage regulator.

1.1 Step Down Transformer (15-0-15)

We will use a 15-0-15V step-down transformer. (See Fig.1), i.e. a transformer with a centre tap, hence the name 15-0-15 V transformer.

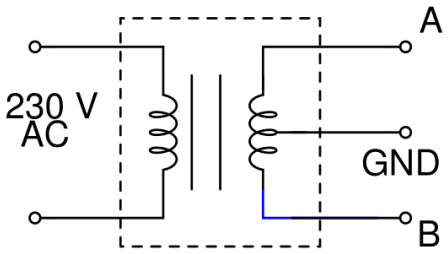

Fig 1 230 V to 15-0-15V Step-down transformer

1.2 Unregulated DC Power Supply (using Bridge Rectifier)

A) Unregulated Supply – without and with a Capacitive Filter

Fig.2 shows the circuit diagram of the unregulated DC power supply. In the absence of a Capacitor, the V_{out} waveform will be a pulsating DC waveform. Diodes used are IN4007 (Peak current = 1 A, Breakdown voltage = 1000V).

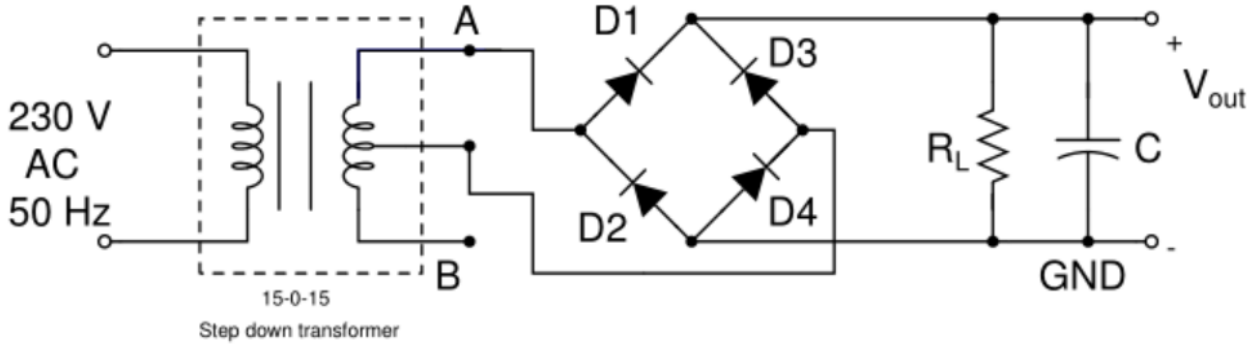

Fig. 2 Unregulated DC Power supply using a Bridge Rectifier

1.2.1 NGSPICE Simulation

Simulate the Bridge rectifier circuit. Plot the V_{out} waveform as one plot; plot the currents through the diodes D1 and D3 as the second plot. Choose R_L = 1 kΩ. Do not connect any Capacitor for this part. Note that the transformer output voltage of 15 V is its RMS value. Choose a voltage source as appropriate.

Hint: You need to use the **.tran** command for analysis. Also, choose a sine waveform with the correct amplitude and frequency. Use appropriate voltage sources for obtaining the currents through D1 and D2.

Diode Model:

You need to use an appropriate diode model for the diodes used. Note that the diodes used (1N4007) are not switching diodes, but power diodes. 1N4007 has a peak current rating of 1 A and breakdown voltage 1000 V. Model for 1N914 switching diode is given below (taken from WEL Lab site).

```
.MODEL 1N914 D (IS=6.2229E-9  N=1.9224  RS=0.33636  IKF=42.843E-3  CJO=764.38E-15
+ M=0.1001 VJ=0.99900  BV=100.14  IBV=0.25951  TT=2.8854E-9)
```

Modify the above model parameters appropriately for your simulations.
(Please refer to the Spice_3f3_Users_Manual.pdf. Available in the Google drive location shared for Expt 1. We shall discuss more on this in the Lab Lecture).

B) Unregulated Supply - with a Capacitive Filter

Once a Capacitor is connected across R_L as in Fig.2, the V_{out} waveform will become smoother, i.e. a large dc with a ripple voltage riding on it. The ripple voltage will depend on: i) the load current (or R_L), and ii) the value of C.

For a given load R_L, one solution employed by some to reduce the ripple voltage is to increase C. In the following NGSPICE simulations you should investigate and decide for yourself whether this strategy is right or not.

1.2.2 NGSPICE Simulation

Simulate and plot the V_{out} waveform of the unregulated power supply with C. Observe and estimate the approximate peak-to-peak ripple voltage. Plot the currents through the diodes D1 and D3 separately. Try simulations for the following combinations of R_L and C values.

Obtain the above plots for the following cases:
Cases (i) to (iii) : R_L = 1kΩ, and C = 100 μF, 470 μF, and 1000 μF
Cases (iv) to (vi) : R_L = 500 Ω, and C = 100 μF, 470 μF, and 1000 μF

Observation and comments:

Note the changes in the voltage and current waveforms as R_L and C are varied. Note also, the approximate ratio of peak diode current to the load current. Comment as to why for a given value of R_L, the diode currents are different for different C values.

Note: Learning objectives 2 and 3 will be part of your classwork.

Part B - Plotting and Data Representation/Analysis Exercise

The measured forward bias current-voltage characteristics of a pn junction diode are given at the end of this file. Plot current versus voltage in a semilog graph. For an example of the semilog graph, please see Fig. 3 [1]. Outline a methodology to obtain the ideality factor, "n" by **visual inspection** of the semilog graph. What details should be visible in the graph to enable such a quick analysis? Do not say that you would calculate it and put the text "n = N" in the graph!
"n" is defined in the following equation.

$$I = I_0\left(e^{qV/nkT} - 1\right)$$

Where k is the Boltzmann constant, T is the temperature in Kelvin and q is the elementary charge. *I* is the current in Amperes, I_0 is the reverse saturation current in Amperes, and *V* is the voltage applied to the diode in Volts.

V (V)	I (A)
0.464	1.30E-06
0.486	3.10E-06
0.515	8.00E-06
0.536	2.00E-05
0.553	4.00E-05
0.571	8.10E-05
0.59	1.65E-04
0.597	2.19E-04
0.604	2.85E-04
0.615	4.35E-04
0.632	8.30E-04
0.647	0.00145
0.663	0.00257
0.678	0.00448
0.687	0.00596
0.706	0.0111
0.731	0.0212
0.743	0.0269
0.756	0.033
0.77	0.0427
0.796	0.0594
0.803	0.0638
0.807	0.0681
0.875	0.132

Note: Students are encouraged to discuss the problem in peer groups.

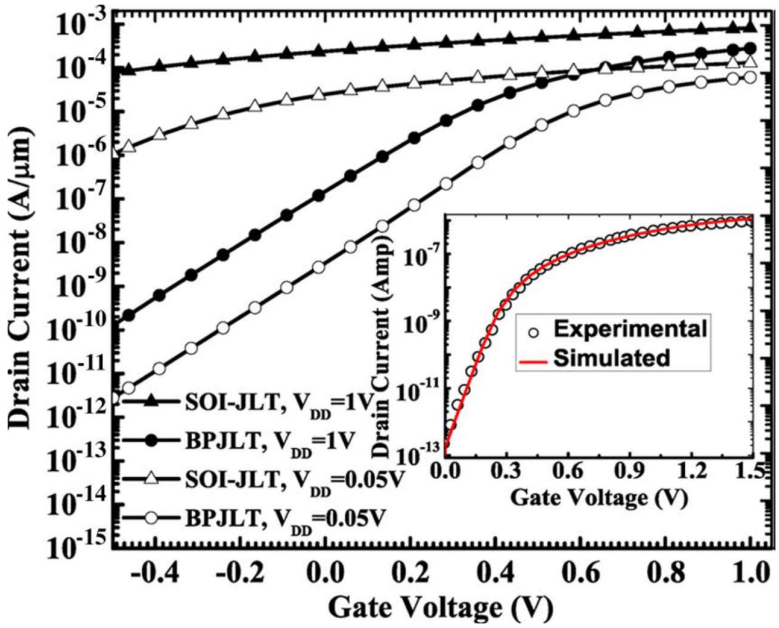

Fig. 3 $I_D - V_{GS}$ characteristics

References:

[1] S. Gundapaneni, S. Ganguly and A. Kottantharayil, "Bulk Planar Junctionless Transistor (BPJLT): An Attractive Device Alternative for Scaling," in IEEE Electron Device Letters, vol. 32, no. 3, pp. 261-263, March 2011, doi: 10.1109/LED.2010.2099204.