EE671 VLSI Design - Assignment 2

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1 Question 1(a)

My roll number ends with 33 hence the load capacitances are 133 fF.

1.1 Approach

The capacitances in the `swmat` subckt were changed to 133 fF. Also the Unit Inverter designed by me in the first assignment was included into the netlist. An instance of `swmat x1` was created for the XOR logic. The inputs In1, In2, In3, In4 were mapped to B, Bbar, Bbar and B. Also con was assigned A and conbar was assigned Abar. To each of the outputs an inverter (instances `x2` and `x3`) was connected to invert the output. The current through the inverters were plotted and also all the required voltages. The average value of the current was measured using the `meas` command.

1.2 NGSPICE Simulation

1.2.1 Code Snippet

```
.include models-180nm

*Name: Rohan Rajesh Kalbag
*Roll 20D170033 : nn = 33

* Switch Matrix
.subckt swmat In1 In2 In3 In4 con conbar Out1 Out2
MN1 In1 con Out1 0 cmosn
```

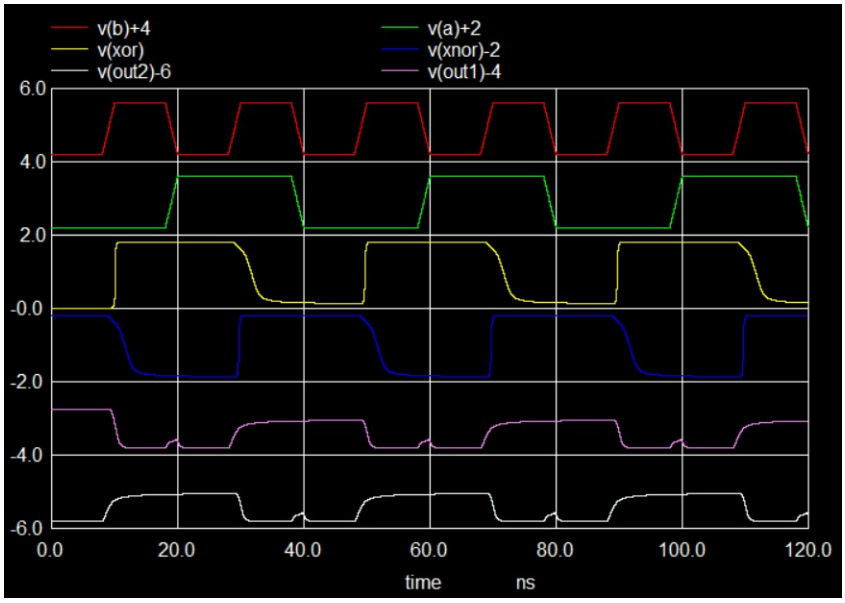
```
+ L=0.18U W=0.24U AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U
MN2 In2 conbar Out1 0 cmosn
+ L=0.18U W=0.24U AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U
MN3 In3 con Out2 0 cmosn
+ L=0.18U W=0.24U AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U
MN4 In4 conbar Out2 0 cmosn
+ L=0.18U W=0.24U AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U
* Loads representing wiring capacitance
C1 Out1 0 133fF
C2 Out2 0 133fF
.ends

* Unit Inverter

* Geometry Parameters for Inverter which was designed by me in
   ↪ Assignment 1
.param pw = 1.505U
.param pl = 0.18U
.param pad = {2*pw*pl}
.param pas = {2*pw*pl}
.param ppd = {2*(pw + 2*pl)}
.param pps = {2*(pw + 2*pl)}

.param nw = 0.502U
.param nl = 0.18U
.param nad = {2*nw*nl}
.param nas = {2*nw*nl}
.param npd = {2*(nw + 2*nl)}
.param nps = {2*(nw + 2*nl)}


.subckt inv supply Inp Output
MP1 Output Inp Supply Supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MN1 Output Inp 0 0 cmosn
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
.ends
```

```
.param Trep1= 40n
.param Trep2 = {Trep1/2.0}
.param Trf = {Trep1/20.0}
.param Tw1 = {Trep1/2.0 - Trf}
.param Tw2 = {Trep2/2.0 - Trf}
.param hival=1.6
.param loval=0.2

V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {
   ↪ Trep1})
V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1} {Trf} {Trf} {Tw1} {
   ↪ Trep1})
V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {
   ↪ Trep2})
V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2} {Trf} {Trf} {Tw2} {
   ↪ Trep2})
V5 vdd 0 DC 1.8

vinv1 vdd top1 dc 0
vinv2 vdd top2 dc 0

x1 B Bbar Bbar B A Abar out1 out2 swmat
x2 top1 out1 xor inv
x3 top2 out2 xnor inv

.tran 1pS {3*Trep1} 0nS
.control

run
plot V(A)+2 V(B)+4 V(xnor)-2 V(xor) V(out1)-4 V(out2)-6
plot I(vinv1)
plot I(vinv2)

meas tran averagecurr1 AVG I(vinv1) from=0 to={3*Trep1}
meas tran averagecurr2 AVG I(vinv2) from=0 to={3*Trep1}
.endc
.end
```

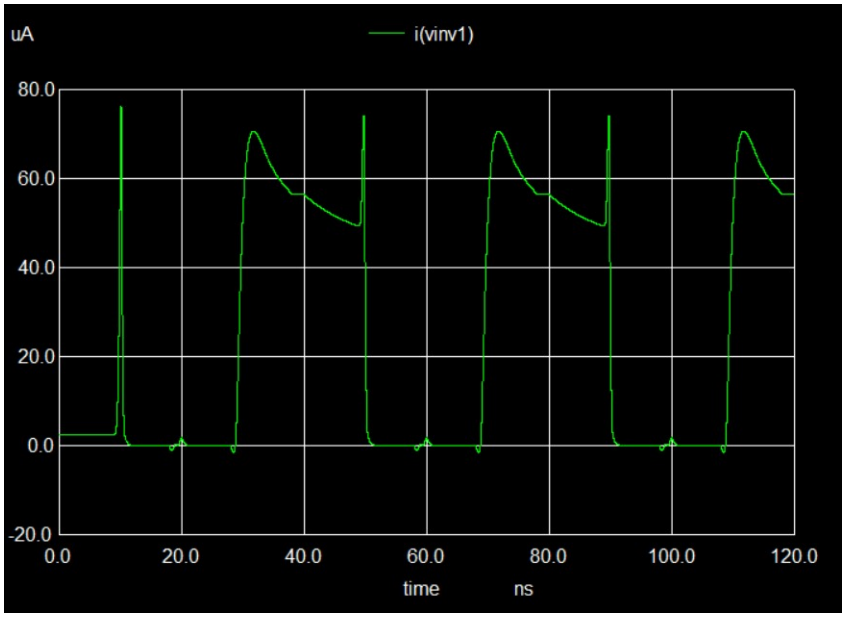
1.3 Results Obtained

The average current through the first inverter (for the XOR output) was obtained as 25.75 μA.

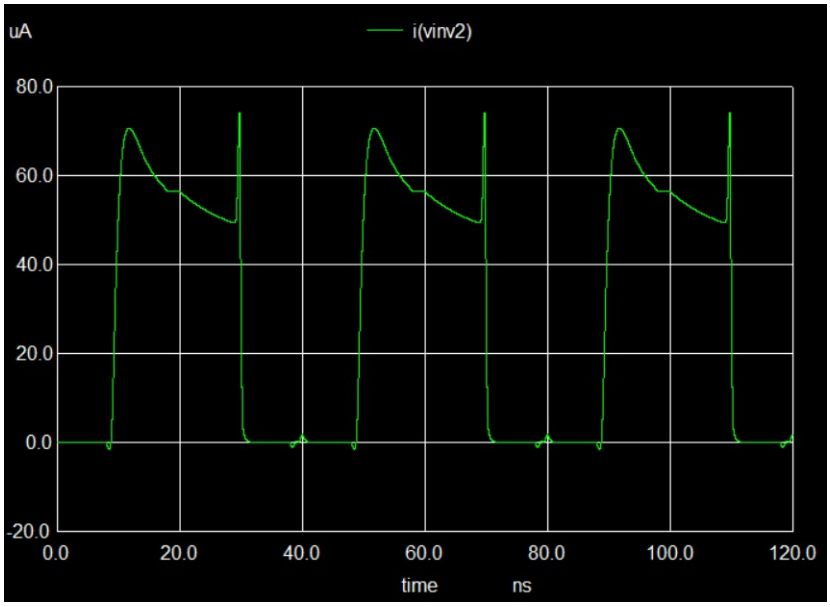
The average current through the second inverter (for the XNOR output) was obtained as 29.64 μA.



Logic Voltage Waveforms Obtained



Current through First Inverter



Current through Second Inverter

1.4 Inferences of Waveforms

We see that the voltage at output nodes before the inverters (pink and white) waveforms are not exactly the complemented values of required waveforms(XOR and XNOR), the inverters serve their purpose of **noise margin reduction** and give rise to the correct waveforms which are the (yellow and blue) waveforms.

We also see that there is a significant amount of static current drawn from V_{DD} as the circuit is not purely CMOS, but has only NMOS. We can try and reduce this current by using a PMOS feedback as in the next part of this question.

2 Question 1(b)

2.1 Approach

Two feedback PMOS transistors were connected to reduce the static current loss. These two lines were additionally added to previous code

```
m1 out1 xor vdd vdd cmosp
+ L=0.18U W=0.24U AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U

m2 out2 xnor vdd vdd cmosp
+ L=0.18U W=0.24U AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U
```

2.2 NGSPICE Simulation

2.2.1 Code Snippet

```
.include models-180nm

*Name: Rohan Rajesh Kalbag
*Roll 20D170033 : nn = 33

* Switch Matrix
.subckt swmat In1 In2 In3 In4 con conbar Out1 Out2
MN1 In1 con Out1 0 cmosn
```

```
+ L=0.18U W=0.24U AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U
MN2 In2 conbar Out1 0 cmosn
+ L=0.18U W=0.24U AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U
MN3 In3 con Out2 0 cmosn
+ L=0.18U W=0.24U AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U
MN4 In4 conbar Out2 0 cmosn
+ L=0.18U W=0.24U AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U
* Loads representing wiring capacitance
C1 Out1 0 133fF
C2 Out2 0 133fF
.ends

* Unit Inverter

* Geometry Parameters for Inverter which was designed by me in
   ↪ Assignment 1
.param pw = 1.505U
.param pl = 0.18U
.param pad = {2*pw*pl}
.param pas = {2*pw*pl}
.param ppd = {2*(pw + 2*pl)}
.param pps = {2*(pw + 2*pl)}

.param nw = 0.502U
.param nl = 0.18U
.param nad = {2*nw*nl}
.param nas = {2*nw*nl}
.param npd = {2*(nw + 2*nl)}
.param nps = {2*(nw + 2*nl)}


.subckt inv supply Inp Output
MP1 Output Inp Supply Supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MN1 Output Inp 0 0 cmosn
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
.ends
```

```
.param Trep1= 40n
.param Trep2 = {Trep1/2.0}
.param Trf = {Trep1/20.0}
.param Tw1 = {Trep1/2.0 - Trf}
.param Tw2 = {Trep2/2.0 - Trf}
.param hival=1.6
.param loval=0.2

V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {
   ↪ Trep1})
V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1} {Trf} {Trf} {Tw1} {
   ↪ Trep1})
V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {
   ↪ Trep2})
V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2} {Trf} {Trf} {Tw2} {
   ↪ Trep2})
V5 vdd 0 DC 1.8

vinv1 vdd top1 dc 0
vinv2 vdd top2 dc 0

x1 B Bbar Bbar B A Abar out1 out2 swmat
x2 top1 out1 xor inv
x3 top2 out2 xnor inv

*PMOS for leakage current reduction

m1 out1 xor vdd vdd cmosp
+ L=0.18U W=0.24U AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U

m2 out2 xnor vdd vdd cmosp
+ L=0.18U W=0.24U AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U

.tran 1pS {3*Trep1} 0nS
.control

run
```

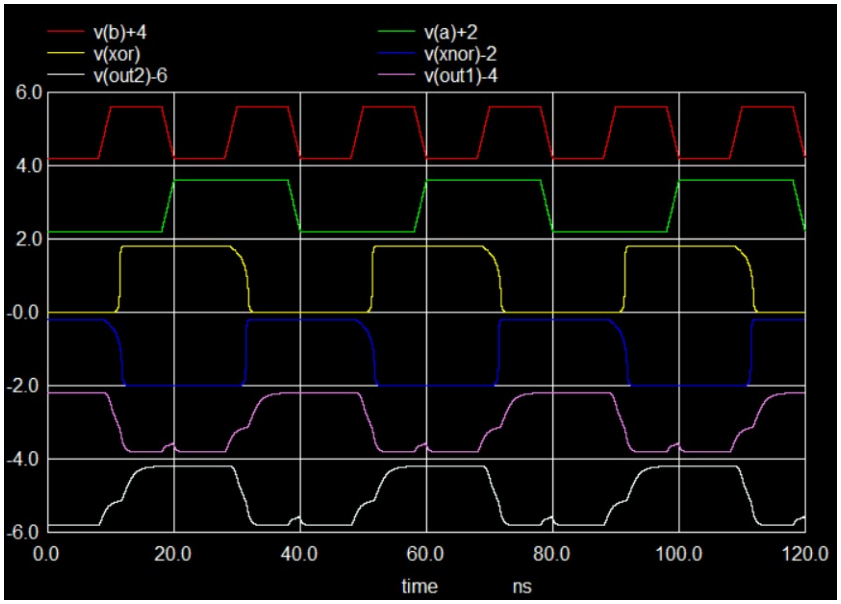
```
plot V(A)+2 V(B)+4 V(xnor)-2 V(xor) V(out1)-4 V(out2)-6
plot I(vinv1)
plot I(vinv2)

meas tran averagecurr1 AVG I(vinv1) from=0 to={3*Trep1}
meas tran averagecurr2 AVG I(vinv2) from=0 to={3*Trep1}
.endc
.end
```

2.3 Results Obtained

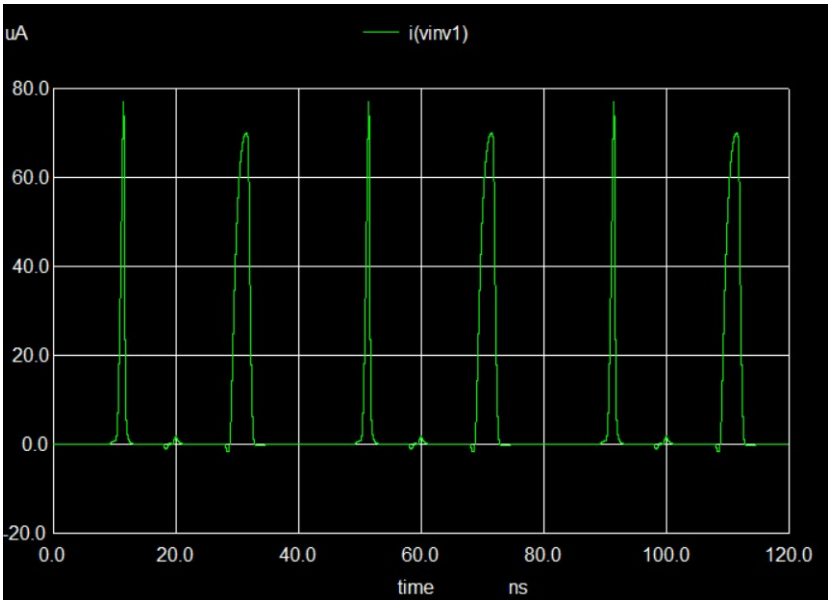
The average current through the first inverter (for the XOR output) was obtained as 5.697 μA.

The average current through the second inverter (for the XNOR output) was obtained as 5.692 μA.

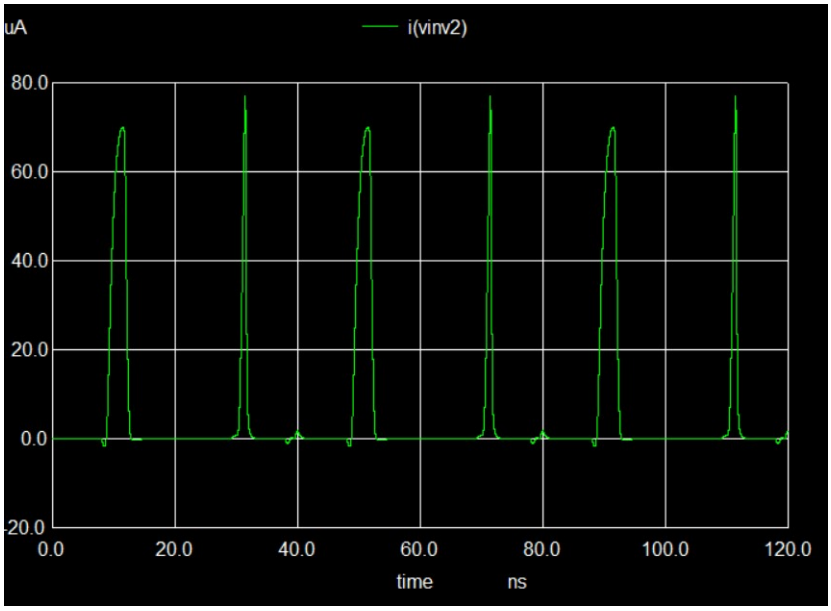
Thus we see that it is nearly **4** times smaller than the previous case indicating that PMOS was successfully able to reduce static leakage current



Logic Voltage Waveforms Obtained



Current through First Inverter



Current through Second Inverter

2.4 Inferences of Waveforms

After adding PMOS we see that there is **nearly zero static current loss**, we only see short impulses in the current waveforms corresponding to the dynamic current.

We also see that the voltage waveforms have **larger amplitude** in comparison to the previous case. The generated XOR and XNOR output waveforms are very similar to what we had got in the CMOS case.

3 Question 1(c)

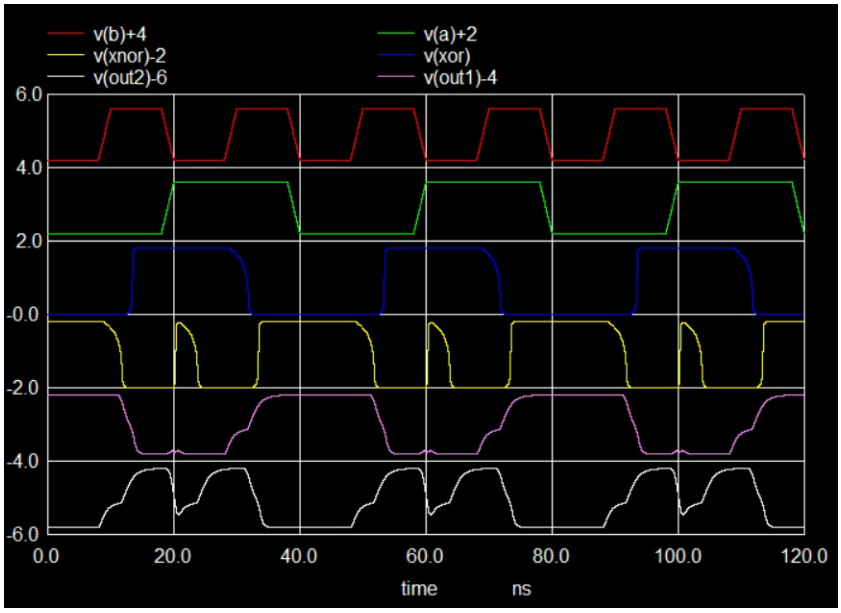
3.1 Approach

As instructed 2ns delay was added to the Abar and Bbar waveforms using the following two lines

```
V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1 + 2ns} {Trf} {Trf
    ↪ } {Tw1} {Trep1})

V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2 + 2ns} {Trf} {Trf
    ↪ } {Tw2} {Trep2})
```

3.2 Results Obtained

We notice that the XOR waveform is as in the previous experiment. But we see that there is distortion in the XNOR output waveform. The delay in the Abar and Bbar signals leads to the out2 waveform to decrease in value to lesser than V_{IH} for the times when A=1 and B=0 for a short duration of time, is interpreted as LOW by the inverter and is turned to HIGH.



Voltage Waveform When Delay in Complementary Signals

4 Question 1(d)

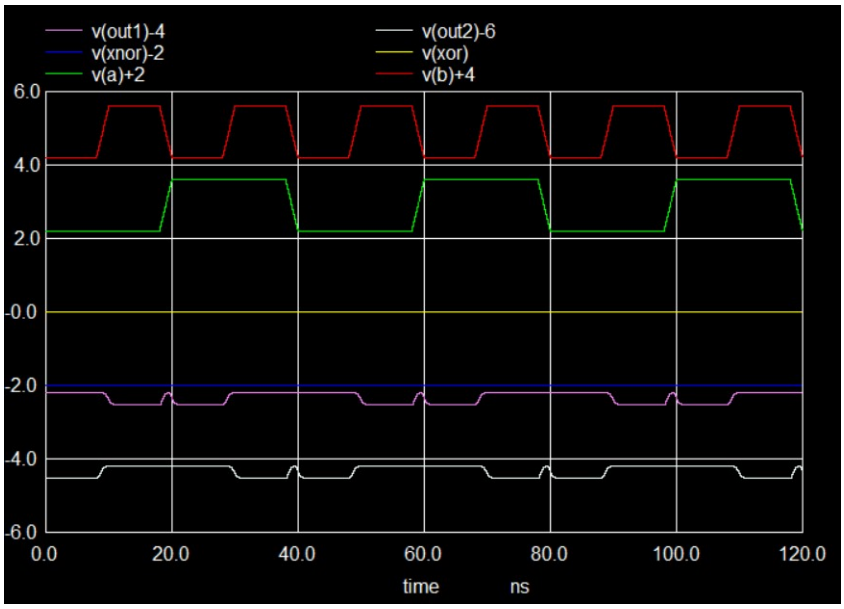
4.1 Approach

The 2ns delay was removed and the width of the PMOS transistors used in feedback was made **4** times the one used in **Question 1(b)** using these

```
m1 out1 xor vdd vdd cmosp
+ L=0.18U W={0.24U*4} AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U

m2 out2 xnor vdd vdd cmosp
+ L=0.18U W={0.24U*4} AD = 86.4f AS = 86.4f PD = 1.2U PS = 1.2U
```

4.2 Results Obtained

The waveform produced at out1 and out2 have really large dc offset due to the pull up by pMOS transistor because of the pseudo NMOS effect and the reduction in amplitude isn't sufficient in terms of noise margin to be read as LOW by the inverter hence the output for both XOR and XNOR waveforms is a constant LOW output.



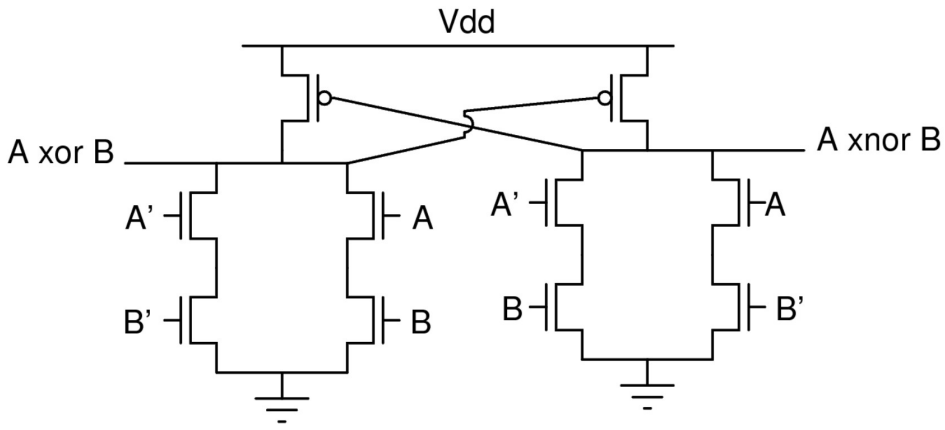
Voltage Waveform With Wide PMOS Feedback

5 Question 2

5.1 Approach

The **CVSL XOR Gate** was designed in the following way, two blocks one for XOR and XNOR were created using Pseudo NMOS style of designing and then the Gates of the pullup PMOS transistors were connected to the outputs of the opposite blocks. A subckt `cvsllogic` was created and the following circuit was modelled in NGSPICE. The parameters used for PMOS and NMOS in Assignment 1 were used. The width of NMOS was taken twice that of PMOS because of series-parallel rules

5.2 Circuit Diagram



Design of the CVSL XOR Gate

5.3 Simulation in NGSPICE

5.3.1 Code in NGSPICE

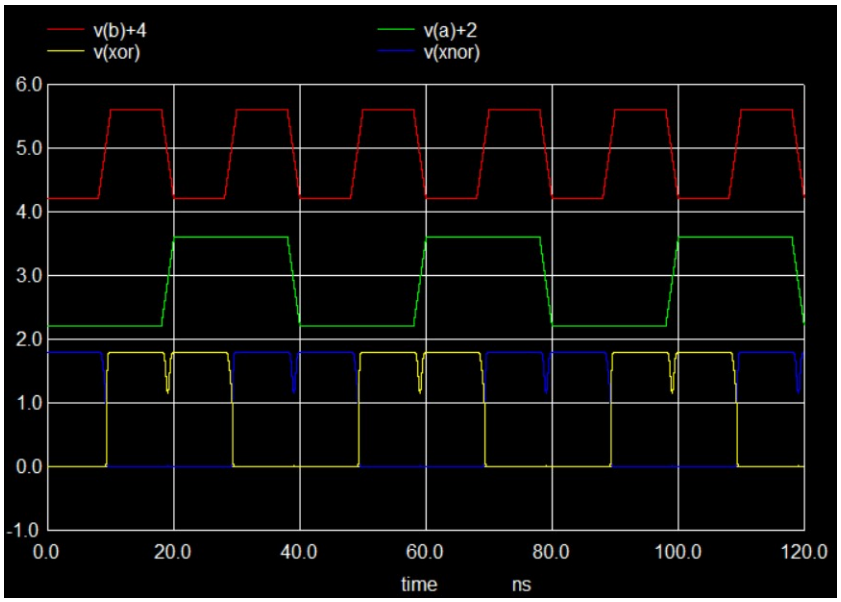
```
.include models-180nm
*Name: Rohan Rajesh Kalbag
*Roll 20D170033 : nn = 33

.param pw = 1.505U
.param pl = 0.18U
.param pad = {2*pw*pl}
.param pas = {2*pw*pl}
.param ppd = {2*(pw + 2*pl)}
.param pps = {2*(pw + 2*pl)}
.param nw = 0.502U
.param nl = 0.18U
.param nad = {2*nw*nl}
.param nas = {2*nw*nl}
.param npd = {2*(nw + 2*nl)}
.param nps = {2*(nw + 2*nl)}

.subckt cvsllogic supply A B Adash Bdash Out1 Out2
```

```
MP1 Out1 Out2 supply supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MN1 Out1 Adash n1 n1 cmosn
+ L={nl} W={2*nw} AD={nad} AS={nas} PD={npd} PS={nps}
MN2 n1 Bdash 0 0 cmosn
+ L={nl} W={2*nw} AD={nad} AS={nas} PD={npd} PS={nps}
MN3 Out1 A n2 n2 cmosn
+ L={nl} W={2*nw} AD={nad} AS={nas} PD={npd} PS={nps}
MN4 n2 B 0 0 cmosn
+ L={nl} W={2*nw} AD={nad} AS={nas} PD={npd} PS={nps}

MP2 Out2 Out1 supply supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MN5 Out2 Adash n3 n3 cmosn
+ L={nl} W={2*nw} AD={nad} AS={nas} PD={npd} PS={nps}
MN6 n3 B 0 0 cmosn
+ L={nl} W={2*nw} AD={nad} AS={nas} PD={npd} PS={nps}
MN7 Out2 A n4 n4 cmosn
+ L={nl} W={2*nw} AD={nad} AS={nas} PD={npd} PS={nps}
MN8 n4 Bdash 0 0 cmosn
+ L={nl} W={2*nw} AD={nad} AS={nas} PD={npd} PS={nps}
.ends

.param Trep1= 40n
.param Trep2 = {Trep1/2.0}
.param Trf = {Trep1/20.0}
.param Tw1 = {Trep1/2.0 - Trf}
.param Tw2 = {Trep2/2.0 - Trf}
.param hival=1.6
.param loval=0.2

V1 A 0 DC 0 PULSE({loval} {hival} {Tw1} {Trf} {Trf} {Tw1} {
   ↪ Trep1})
V2 Abar 0 DC 0 PULSE({hival} {loval} {Tw1} {Trf} {Trf} {Tw1} {
   ↪ Trep1})
V3 B 0 DC 0 PULSE({loval} {hival} {Tw2} {Trf} {Trf} {Tw2} {
   ↪ Trep2})
V4 Bbar 0 DC 0 PULSE({hival} {loval} {Tw2} {Trf} {Trf} {Tw2} {
```

```
    ↪ Trep2})
V5 vdd 0 DC 1.8

x1 vdd A B Abar Bbar xor xnor cvsllogic
.tran 1pS {3*Trep1} 0nS
.control

run
plot V(A)+2 V(B)+4 V(xnor) V(xor)

.endc
.end
```

5.4 Results Obtained

The output waveform on performing transient analysis gave the following waveform which behaves nearly like an XOR/XNOR gate pair. The waveform decreases for a short pulse of time when both A and B make transitions from 0-1 or 1-0 at the same time which can be seen at ≈ 20 ns, ≈ 40ns .etc



Output Waveforms for CVSL based XOR/XNOR Gate