EE671 VLSI Design - Assignment 1

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1 Question 1

My roll number ends with 33 hence the value of $nn = 33$, thus required rise and fall time are 266 ps.

1.1 Approach

I created parameters for each of the following geometry variables such as pad, pas, ppd, pps for PMOS and nad, nas, npd, nps for NMOS then changed the value of pw and nw and accordingly measured the output rise and fall times using the meas command. I varied the values via hit and trial method and noticed that rise time is linearly dependent on the width of PMOS and fall time

1.2 NGSPICE Simulation

1.2.1 Code Snippet

```
CMOS Inverter Rise and Fall Time

.include models-180nm

*Name: Rohan Rajesh Kalbag
*Roll 20D170033 : nn = 33

* required outrise = 200 + 66 = 266 ps = 2.66e-10 s
* required outfall = 200 + 66 = 266 ps = 2.66e-10 s
```

```
* measured outrise = 2.66286e-10 s
* measured outfall = 2.66096e-10 s

*geometry parameters
.param pw = 1.505U
.param pl = 0.18U
.param pad = {2*pw*pl}
.param pas = {2*pw*pl}
.param ppd = {2*(pw + 2*pl)}
.param pps = {2*(pw + 2*pl)}

.param nw = 0.502U
.param nl = 0.18U
.param nad = {2*nw*nl}
.param nas = {2*nw*nl}
.param npd = {2*(nw + 2*nl)}
.param nps = {2*(nw + 2*nl)}

* unit inverter
.subckt inv supply Inp Output
MP1 Output Inp Supply Supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MN1 Output Inp 0 0 cmosn
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
.ends

vdd supply 0 dc 1.8
* device under test
x3 supply Ck dutout inv
* load capacitor
C3 dutout 0 0.05pF
*transient analysis with pulse inputs
VCk Ck 0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8nS)

.tran 1pS 35nS 0nS
.control
run
```

```
plot 4.0+V(Ck) V(dutout)

* 20ps input rise and fall time
meas tran risetime TRIG v(ck) VAL=0.001 RISE=2 TARG v(Ck) VAL
    ↪ =1.799 RISE=2
meas tran falltime TRIG v(ck) VAL=1.799 FALL=2 TARG v(Ck) VAL
    ↪ =0.001 FALL=2

* input 10% - 80% rise and fall time
meas tran inprise TRIG v(ck) VAL=0.18 RISE=2 TARG v(Ck) VAL
    ↪ =1.62 RISE=2
meas tran inpfall TRIG v(ck) VAL=1.62 FALL=2 TARG v(Ck) VAL
    ↪ =0.18 FALL=2

* output 10% - 80% rise and fall time
meas tran outrise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout)
    ↪  VAL=1.62 RISE=2
meas tran outfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout)
    ↪  VAL=0.18 FALL=2
.endc
.ends
```

1.3 Results Obtained

Expected Output Rise Time	Obtained Output Rise Time
266ps	266.286ps

Expected Output Fall Time	Obtained Output Fall Time
266ps	266.096ps

2 Q-2

2.1 Approach

I performed a DC sweep of V(Ck) from 0 to 1.8V. Then plotted the V(dutout) as a function of the sweep voltage, defined a variable der to store the derivative of V(dutout). To find the noise margins, I made use of the meas command to find the points where der was becoming -1. Using this approach

I found $V_{OL}, V_{OH}, V_{IL}, V_{OL}$. Then I printed out the values of the high noise margin and the low noise margin.

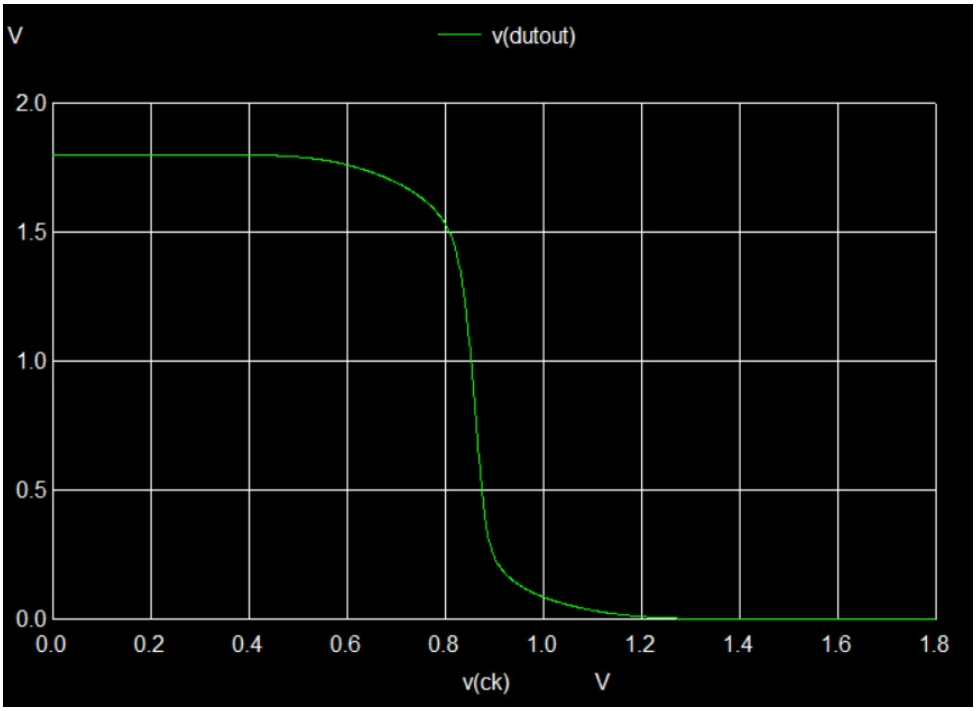
2.2 NGSPICE Simulation

2.2.1 Code Snippet

```
CMOS Inverter Transfer Characteristics

.include models-180nm

*Name: Rohan Rajesh Kalbag
*Roll 20D170033 : nn = 33

*geometry parameters
.param pw = 1.505U
.param pl = 0.18U
.param pad = {2*pw*pl}
.param pas = {2*pw*pl}
.param ppd = {2*(pw + 2*pl)}
.param pps = {2*(pw + 2*pl)}

.param nw = 0.502U
.param nl = 0.18U
.param nad = {2*nw*nl}
.param nas = {2*nw*nl}
.param npd = {2*(nw + 2*nl)}
.param nps = {2*(nw + 2*nl)}

* unit inverter
.subckt inv supply Inp Output
MP1 Output Inp Supply Supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MN1 Output Inp 0 0 cmosn
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
.ends

vdd supply 0 dc 1.8
```

```
* device under test
x3 supply Ck dutout inv
* load capacitor
C3 dutout 0 0.05pF
*transient analysis with pulse inputs
VCk Ck 0 DC

.dc VCk 0 1.8 0.001
.control
run

*plotting of graphs
plot V(dutout) vs V(Ck)
plot deriv(V(dutout)) vs V(Ck)

*calculation of noise margin
let der = deriv(V(dutout))
meas dc VIL find V(Ck) when der = -1
meas dc VIH find V(Ck) when der = -1 rise = last
meas dc VOH find V(dutout) when V(ck) = VIL
meas dc VOL find V(dutout) when V(ck) = VIH

let highnoisemargin = VOH - VIH
let lownoisemargin = VIL - VOL

print highnoisemargin
print lownoisemargin
.endc
.end
```

2.3 Results Obtained

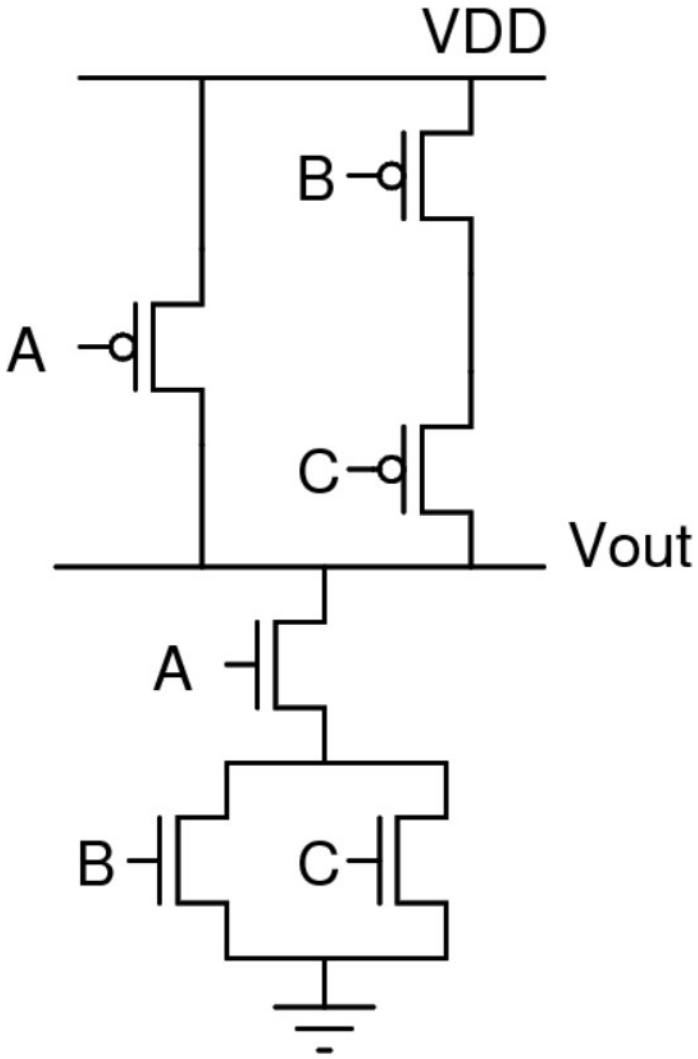


Parameter	Value Obtained
V_{IL}	0.708 V
V_{IH}	0.968 V
V_{OH}	1.683 V
V_{OL}	1.123 V
High Noise Margin	0.7157 V
Low Noise Margin	0.596 V

3 Q-3

3.1 Approach

To design the required boolean logic, the series-parallel approach was used as per the content covered in the lectures. A subckt block was created by me in the NGSPICE netlist called logic where I used 3 NMOS and PMOS transistors in the following configuration. The configuration was created using XCircuit, and the .ps file is also attached



3.2 NGSPICE Simulation

I simulated the logic gates for the following three cases of transitions

- B = 1, C = 1 if A = 0 then Y = 1 else Y = 0
- A = 1, B = 0 if C = 0 then Y = 1 else Y = 0
- A = 1, C = 0 if B = 0 then Y = 1 else Y = 0

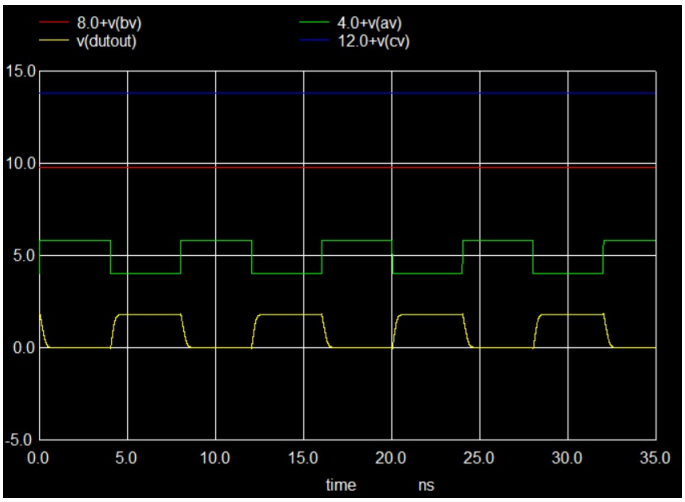
```
CMOS Logic

.include models-180nm

*Name: Rohan Rajesh Kalbag
*Roll 20D170033 : nn = 33

*geometry parameters
.param pw = 1.505U
.param pl = 0.18U
.param pad = {2*pw*pl}
.param pas = {2*pw*pl}
.param ppd = {2*(pw + 2*pl)}
.param pps = {2*(pw + 2*pl)}

.param nw = 0.502U
.param nl = 0.18U
.param nad = {2*nw*nl}
.param nas = {2*nw*nl}
.param npd = {2*(nw + 2*nl)}
.param nps = {2*(nw + 2*nl)}

* logic unit to implement (A.(B+C))'
* the circuit diagram of the design can be found in
   ↪ q3_cmos_logic_design.jpg
.subckt logic supply A B C Y
MP1 Y A supply supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MP2 mid1 B supply supply cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}
MP3 Y C mid1 mid1 cmosp
+ L={pl} W={pw} AD={pad} AS={pas} PD={ppd} PS={pps}

MN1 Y A mid2 mid2 cmosn
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
MN2 mid2 B 0 0 cmosn
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
MN3 mid2 C 0 0 cmosn
```

```
+ L={nl} W={nw} AD={nad} AS={nas} PD={npd} PS={nps}
.ends

vdd supply 0 dc 1.8
* device under test
x3 supply av bv cv dutout logic
* load capacitor
C3 dutout 0 0.05pF

*Desired Transitions

* a) B = 1, C = 1 if A = 0 then Y = 1 else Y = 0

* measured rise time = 276ps
* measured fall time = 341ps

*for a) uncomment next three lines and comment them while
   ↪ simulating others
* VA av 0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8nS)
* VB bv 0 DC 1.8
* VC cv 0 DC 1.8

* b) A = 1, B = 0 if C = 0 then Y = 1 else Y = 0

* measured rise time = 518ps
* measured fall time = 426ps

*for b) uncomment next three lines and comment them while
   ↪ simulating others
* VC cv 0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8nS)
* VA av 0 DC 1.8
* VB bv 0 DC 0

* c) A = 1, C = 0 if B = 0 then Y = 1 else Y = 0

* measured rise time = 518ps
* measured fall time = 443ps
```

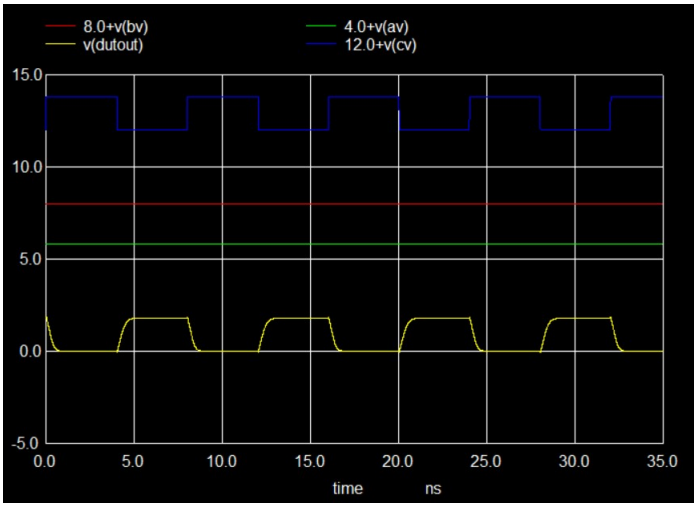
```
*for c) uncomment next three lines and comment them while
    ↪ simulating others
* VB bv 0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8nS)
* VA av 0 DC 1.8
* VC cv 0 DC 0

*transient analysis
.tran 1pS 35nS 0nS
.control
run
plot 4.0+V(av) 8.0+V(bv) 12.0+V(cv) V(dutout)

* output 10% - 80% rise and fall time
meas tran outrise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout)
    ↪  VAL=1.62 RISE=2
meas tran outfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout)
    ↪  VAL=0.18 FALL=2
.endc
.end
```

3.3 Results Obtained

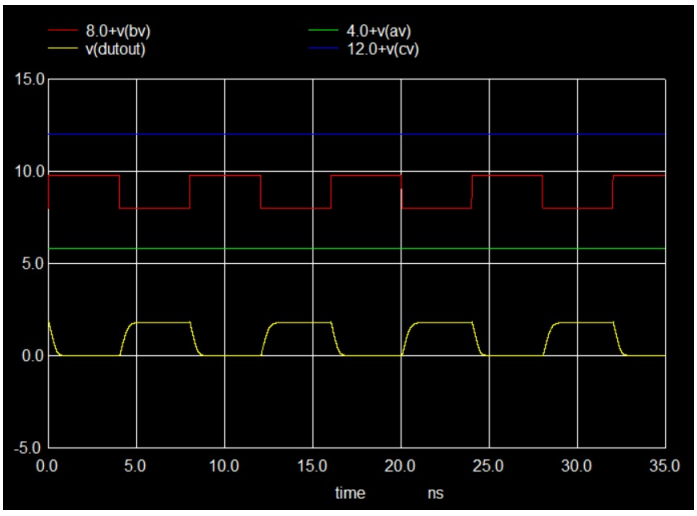
3.3.1 For Case 1



3.3.2 For Case 2



3.3.3 For Case 3



3.3.4 Timing Characteristics

Transition	Rise Time	Fall Time
B = 1, C = 1, A varying	276ps	341ps
A = 1, B = 0, C varying	518ps	426ps
A = 1, C = 0, B varying	518ps	443ps