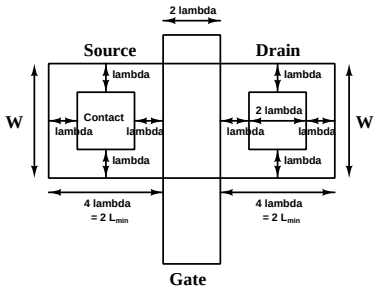
Monday	EE 671: VLSI Design	Due on
Aug. 08, 2022	Assignment 1	Aug. 16, 2021

We want to design CMOS logic gates using a 180 nm CMOS process.
Transistor models for this process are attached in a separate file called models-180nm.

The n and p channel transistors in your solution should use a channel length of 0.18μm and their channel width should be $\geq 0.24\mu$m. The supply voltage for this inverter should be 1.8V and the external load capacitance should be 0.05pF. In addition to this, include the drain and source capacitances for all transistors by specifying the source/drain area and perimeter values. These will depend on transistor geometry:

Width of either diffused region is W while its length is 4λ.
Since $\lambda = L_{min}/2, 4\lambda = 2L_{min}$. Therefore:
as = ad = $W \times 2L_{min}$
and source/drain perimeter is:
ps = pd = $2 \times (W + 2L_{min})$.



When as, ad, ps and pd are specified, the capacitance contributed by these diffused regions is incorporated by the transistor models (and need not be specified separately as a circuit component).

A template file to simulate the inverter is given below. It uses minimum widths for n as well as p channel transistors. Your solution should replace these with appropriate values to meet the delay specification. Notice that the values of area and perimeter of source and drain regions will have to be recalculated when you change the widths.

The .include statement in the template input file given below imports the models from the file models-180nm.

```
* Unit Inverter
.subckt inv supply Inp Output
*  This subcircuit defines a CMOS inverter with equal n and p widths
MP1 Output Inp Supply Supply cmosp
+ L=0.18U W=0.24U AD = 0.0864P AS = 0.0864P PD = 1.2U PS = 1.2U
MN1 Output Inp 0      0      cmosn
+ L=0.18U W=0.24U AD = 0.0864P AS = 0.0864P PD = 1.2U PS = 1.2U
.ends

vdd supply 0 dc 1.8

*  Device under test
x3  supply Ck dutout inv

* Load Capacitor
C3 dutout 0 0.05pF
```

```
.include models-180nm

*TRANSIENT ANALYSIS with pulse inputs
VCk  Ck   0 DC 0 PULSE(0 1.8 0nS 20pS 20pS 4nS 8.0nS)
.tran 1pS 35nS 0nS

.control
run
plot 4.0+V(Ck) V(dutout)
meas tran inrise TRIG v(ck) VAL=0.18 RISE=2 TARG v(Ck) VAL=1.62 RISE=2
meas tran infall TRIG v(ck) VAL=1.62 FALL=2 TARG v(Ck) VAL=0.18 FALL=2
meas tran drise TRIG v(dutout) VAL=0.18 RISE=2 TARG v(dutout) VAL=1.62 RISE=2
meas tran dfall TRIG v(dutout) VAL=1.62 FALL=2 TARG v(dutout) VAL=0.18 FALL=2
.endc
.end
```

Q–1 Design the CMOS inverter by choosing appropriate widths for n and p channel transistors such that it has equal rise/fall times of $200 + 2 \times nn$ ps, where nn represents the last two digits of your roll number. The input should be a rail to rail square wave with rise/fall times of 20 ps. Measure the rise/fall times of the output by finding the time taken to traverse between 10% of V_{DD} and 90% of V_{DD}.

Q–2 Use ng-spice to plot the static transfer characteristics of this inverter by using a DC sweep on the input from 0 to V_{DD} and determine the static noise margins for it.

Q–3 Using the above inverter as the base design, apply series-parallel rules to design a logic gate which produces $\overline{A \cdot (B + C)}$ at its output. Find the rise and fall times of this gate for different input combinations in which two of the inputs are held at an enabling value, such that a transition on the third input produces a transition at the output.