Monday	**EE 671: VLSI Design**	Due on Wednesday
Oct. 24, 2022	**Assignment 5**	Nov. 2, 2022

Q–1 Describe a multiplier accumulator circuit in VHDL which multiplies two 8 bit operands and adds a 16 bit number to the product. The MAC circuit should use:

1. An 8x8 array of AND gates to generate partial product bits,
2. Full and half adders as required using Dadda scheme to reduce the number of bits to 2 each in every column
3. A logarithmic adder (you can use the tree adder designed by you in assignment 4) as the final adder.

You can re-use the basic logic gates from assignment-4 to construct full and half adders required for the wire reduction stage. Your description should use `std_logic` types for various signals.

Your description should include a test bench which reads input data and expected results from a file. The test bench will be the top level entity which verifies correct operation of the circuit.

Verify correct operation of the MAC circuit with 10 inputs inclusive of boarder values (maximum values, values which are complements of each other).