FPGAspeaks

Level-1
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September 2023

Contents

1 Introduction

This Level will give a brief intro of the all the Basic logic gates which will be used in our upcoming levels.

2 Tools/Requirements

Xilinx Vivado

3 Basic Logic Gates

- **OR Gate:** A logic gate that produces a HIGH output when one or more inputs are HIGH.
- **AND Gate:** A logic gate that produces a HIGH output only when all the inputs are HIGH.
- **NOT Gate:** A logic gate that produces a HIGH output when input is LOW and Vice versa.
- **XOR Gate:** A logic gate that produces a HIGH output only when inputs are NOT equal.
- **NAND Gate:** A logic gate that produces a LOW output only when all the inputs are HIGH.
- **NOR Gate:** A logic gate that produces a LOW output when one or more inputs are HIGH.
- **XNOR Gate:** A logic gate that produces a HIGH output only when the inputs are equal.

4 What have I done in this Level?

I have implemented the verilog programs of all the Basic logic gates using Xilinx Vivado.

5 Links

Link to my Github