IC2K1749
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Q4

Ans In simple processors a task is executed in set of instructions which involved read from memory, performing an arithmatic and logical operation, and then again write to memory / register.

~~White~~

Pipelining is introduced to achieve multitasking in single processor systems.

Pipeling is the process of ~~accumulating instruction~~ arrangement of hardware elements of the CPU such that is overall performance is increased. Execution of multiple operation can be done at the same time in a pipelined processor.

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Q3

Super pipelining	Super Scalar pipelining
1. Instruction issue style is dynamic	2. Instruction issue style is dynamic
2. It issues one instruction at	
2. Instruction issue is 1	2 Instruction issue rate is one.
3. Divides long latency stages of a pipeline into several shorter stages	3. Dyramicaly issuing multiple instruction per cycle.
4. It effects on clock cycle time of equation	4. It effects on CPI of

Q1

Given pipeline stage latency = 3ns, 9ns, 4ns, 8 ns and 2ns
pipline latency = 1ns other
Max latency is 9ns. {all latencies are cleared within 9ns).

Total cycle time of resulting processor
= Max latency + pipeline latch delay
= 9ns + 1ns
= 10 ns