**International Institute of Professional Studies**

**Devi Ahilya University**

**M.C.A. VII Semester**

**Computer Architecture Test-2**

**Date 15-01-2021**

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| **Q:-1** | **Suppose a non-pipelined processor with a 25 ns cycle time is divided into 5 pipeline stages with latencies of 3,9,4,8 & 2 ns. If the pipeline latch (buffer) latency is 1 ns, what is the cycle time of resulting processor and why?** | **5** |
| **Q:-2** | **In which situations delayed load and delayed branch are suitable? Explain.** | **5** |
| **Q:-3** | **Compare and contrast super pipelining and super scalar pipelining.** | **5** |
| **Q:-4** | **What causes a processor pipeline to be under pipelined?** | **5** |

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