avsd_opamp **Circuit Netlist**

- *R.V.Rohinth Ram*

```
.lib "sky130_fd_pr/models/sky130.lib.spice"  tt

* Stage 1 - Differential amplifier
xm1 net-_m1-pad1_ in1 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm2 out1 in2 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm3 net-_m1-pad1_ net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10
xm4 out1 net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10

* Current Mirror
xm5 net-_m1-pad3_ ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=20
xm6 ref ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=10

* Stage 2 - PMOS Common Source Amplifier
xm7 out2 out1 vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=62.83
xm8 out2 ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=62.83


* Circuit Bias
v1  vdd gnd dc 1
v2  vss gnd dc -1
xR1 vdd ref gnd sky130_fd_pr__res_high_po_0p69  l=100


v3 in1 gnd sine(0 1m 60)
v4 in2 gnd sine(0 -1m 60)

.end
```

Netlist Simulated to find characteristics of avsd_opamp

Gain

```
.lib "sky130_fd_pr/models/sky130.lib.spice"  tt

* Stage 1 - Differential amplifier
xm1 net-_m1-pad1_ in1 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm2 out1 in2 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm3 net-_m1-pad1_ net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10
xm4 out1 net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10

* Current Mirror
xm5 net-_m1-pad3_ ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=20
xm6 ref ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=10

* Stage 2 - PMOS Common Source Amplifier
xm7 out2 out1 vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=62.83
xm8 out2 ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=62.83



* Circuit Bias
v1  vdd gnd dc 1
v2  vss gnd dc -1
xR1 vdd ref gnd sky130_fd_pr__res_high_po_0p69  l=100



v3 in1 gnd ac 1
v4 in2 gnd dc 0

*Simulation Command
.ac dec 101 1 1g

* ngspice control statements
.control

run
print allv > plot_data_v.txt
print alli > plot_data_i.txt

*For AC Analysis

plot db(V(out2)/V(in1))
plot 180/PI*phase(v(out2))

let gain = db(V(out2)/V(in1))
let phase = 180/PI*phase(v(out2))
```

```
let max_gain = maximum(gain)

print gain > gain_values.txt
print phase > phase_values.txt

.endc

*results
*max_gain = 33.36db
*3db cutoff freq =  1.314655e+06
*Phase Margin
*180 - 134.08 = 45.92

.end
```

Common Mode Gain

```
.lib "sky130_fd_pr/models/sky130.lib.spice"  tt

* Stage 1 - Differential amplifier
xm1 net-_m1-pad1_ in1 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm2 out1 in2 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm3 net-_m1-pad1_ net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10
xm4 out1 net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10

* Current Mirror
xm5 net-_m1-pad3_ ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=20
xm6 ref ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=10

* Stage 2 - PMOS Common Source Amplifier
xm7 out2 out1 vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=62.83
xm8 out2 ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=62.83



* Circuit Bias
v1  vdd gnd dc 1
v2  vss gnd dc -1
xR1 vdd ref gnd sky130_fd_pr__res_high_po_0p69  l=100

v3 in1 gnd ac 1
v4 in2 gnd ac 1

*Simulation Command
.ac dec 101 1 1g

* ngspice control statements
.control

run
print allv > plot_data_v.txt
print alli > plot_data_i.txt

*For AC Analysis
plot db(V(out2)/V(in1))

let gain = db(V(out2)/V(in1))
let max_gain = maximum(gain)
print max_gain

.endc
*results
*Acm = -8.399db
.end
```

Offset Voltage

```
.lib "sky130_fd_pr/models/sky130.lib.spice"  tt

* Stage 1 - Differential amplifier
xm1 net-_m1-pad1_ in1 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm2 out1 in2 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm3 net-_m1-pad1_ net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10
xm4 out1 net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10

* Current Mirror
xm5 net-_m1-pad3_ ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=20
xm6 ref ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=10

* Stage 2 - PMOS Common Source Amplifier
xm7 out2 out1 vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=62.83
xm8 out2 ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=62.83


* Circuit Bias
v1  vdd gnd dc 1
v2  vss gnd dc -1
xR1 vdd ref gnd sky130_fd_pr__res_high_po_0p69  l=100


v3 in1 gnd dc 0
v4 in2 gnd dc 0

.tran 0.1e-3 10e-3 0


* ngspice control statements
.control

run
print allv > plot_data_v.txt
print alli > plot_data_i.txt

plot v(out2)
print maximum(v(out2))

.endc

.end
```

Power Dissipation

```
.lib "sky130_fd_pr/models/sky130.lib.spice"  tt

* Stage 1 - Differential amplifier
xm1 net-_m1-pad1_ in1 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm2 out1 in2 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm3 net-_m1-pad1_ net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10
xm4 out1 net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10

* Current Mirror
xm5 net-_m1-pad3_ ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=20
xm6 ref ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=10

* Stage 2 - PMOS Common Source Amplifier
xm7 out2 out1 vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=62.83
xm8 out2 ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=62.83



* Circuit Bias
v1  vdd gnd dc 1
v2  vss gnd dc -1
xR1 vdd ref gnd sky130_fd_pr__res_high_po_0p69  l=100
*Load
xR2 out2 ny gnd sky130_fd_pr__res_high_po_0p69  l=1

v3 in1 nx sine(0 1m 60)
v4 in2 gnd dc 0

v_u1 nx gnd 0
v_u2 ny gnd 0

.tran 0.1m 1 0.5

* ngspice control statements
.control
run
print allv > plot_data_v.txt
print alli > plot_data_i.txt
let pd = v(in1)*i(v_u1)-v(out2)*i(v_u2)
plot pd
let res = v(out2)[0] / i(v_u2)[0]
print res
.endc
*results
*pd = 13uW @ sine(0 1m 60) and 1k load

.end
```

Input Noise Spectrum

```
.lib "sky130_fd_pr/models/sky130.lib.spice"  tt

* Stage 1 - Differential amplifier
xm1 net-_m1-pad1_ in1 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm2 out1 in2 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm3 net-_m1-pad1_ net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10
xm4 out1 net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10

* Current Mirror
xm5 net-_m1-pad3_ ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=20
xm6 ref ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=10

* Stage 2 - PMOS Common Source Amplifier
xm7 out2 out1 vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=62.83
xm8 out2 ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=62.83



* Circuit Bias
v1  vdd gnd dc 1
v2  vss gnd dc -1
xR1 vdd ref gnd sky130_fd_pr__res_high_po_0p69  l=100



v3 in1 gnd ac 1
v4 in2 gnd dc 0


.noise v(out2) v3 dec 101 1 1g


* ngspice control statements
.control

run
*setplot noise1
*plot onoise_spectrum

.endc

.end
```

Slew Rate

```
.lib "sky130_fd_pr/models/sky130.lib.spice"  tt

* Stage 1 - Differential amplifier
xm1 net-_m1-pad1_ in1 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
*xm2 out1 in2 net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm2 out1 gnd net-_m1-pad3_ net-_m1-pad3_ sky130_fd_pr__nfet_01v8  l=1 w=1.79
xm3 net-_m1-pad1_ net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10
xm4 out1 net-_m1-pad1_ vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=10

* Current Mirror
xm5 net-_m1-pad3_ ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=20
xm6 ref ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=10

* Stage 2 - PMOS Common Source Amplifier
xm7 out2 out1 vdd vdd sky130_fd_pr__pfet_01v8  l=1 w=62.83
xm8 out2 ref vss vss sky130_fd_pr__nfet_01v8  l=1 w=62.83



* Circuit Bias
v1  vdd gnd dc 1
v2  vss gnd dc -1
xR1 vdd ref gnd sky130_fd_pr__res_high_po_0p69  l=100



v3 in1 gnd PULSE(-1 1 0 0 0 1m 2m)

.tran 0.1m 10m



* ngspice control statements
.control

run
print allv > plot_data_v.txt
print alli > plot_data_i.txt
plot v(out2)
print v(out2) > output_v.txt

.endc
*results
*7                      4.038271e-07      9.450754e-01
*8                      5.326329e-07      -9.98075e-01
*diff 0.1u for 2 change
.end
```