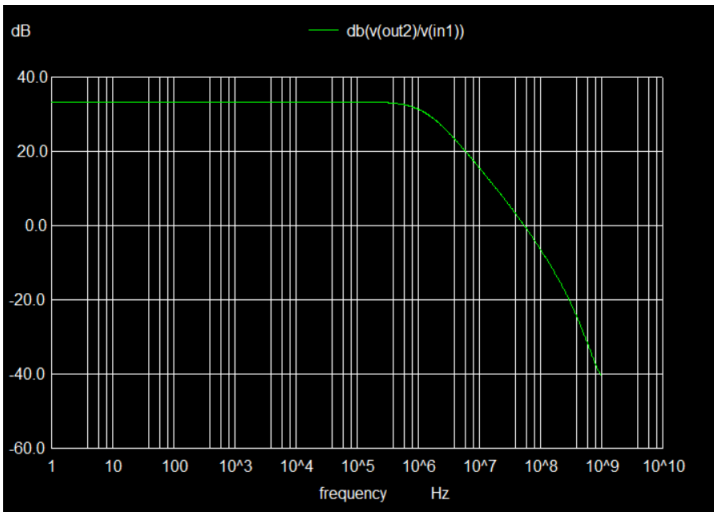
Simulation Results – **avsd_opamp**

(Two Stage CMOS Operational Amplifier)

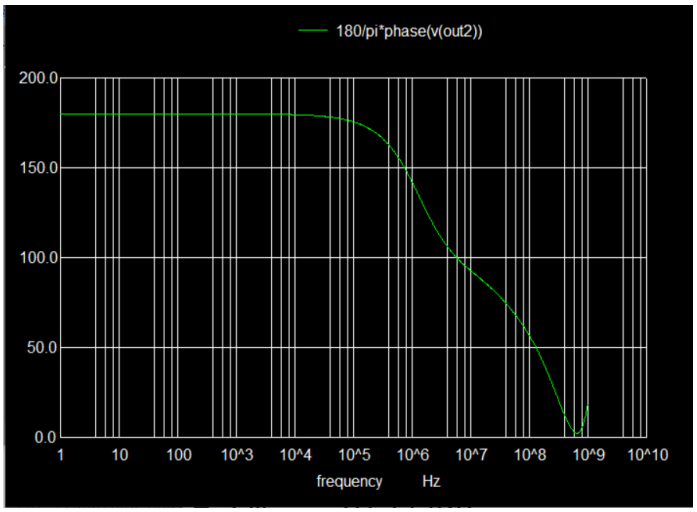
- *R.V.ROHINTH RAM*

Frequency Response(Differential Mode)

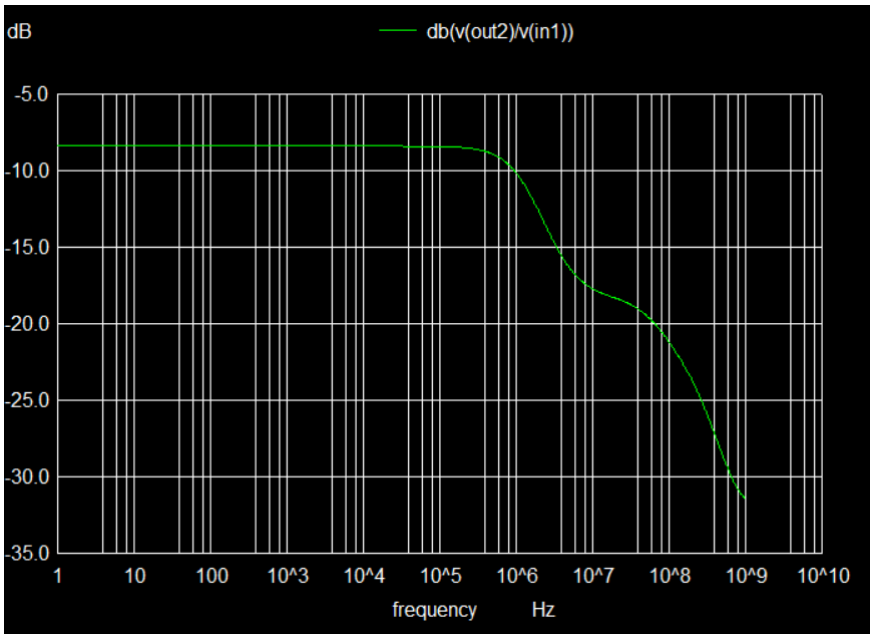
Magnitude(db)



Phase

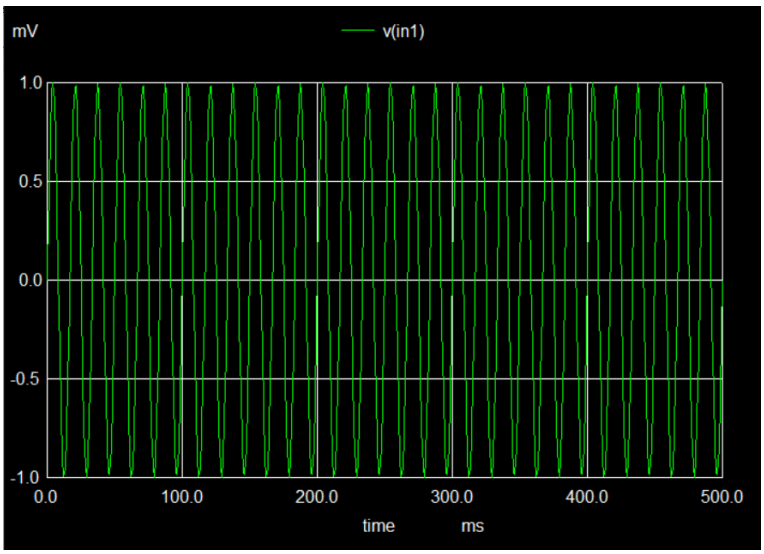


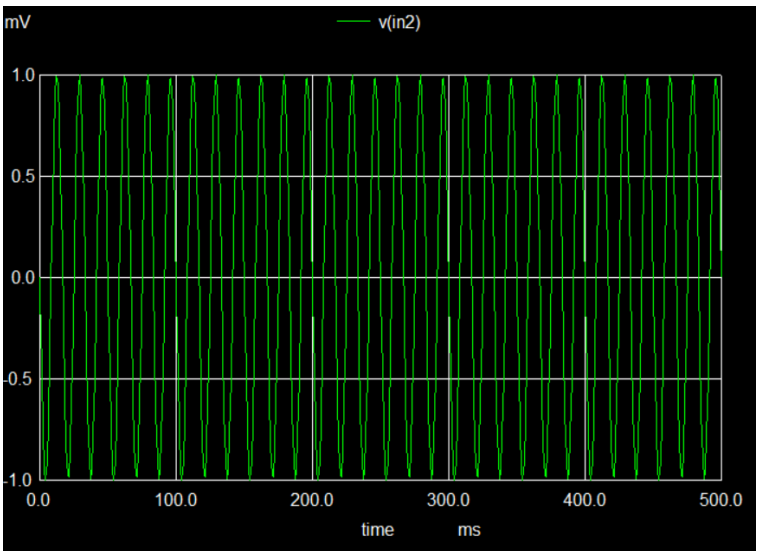
Frequency Response(Common Mode)



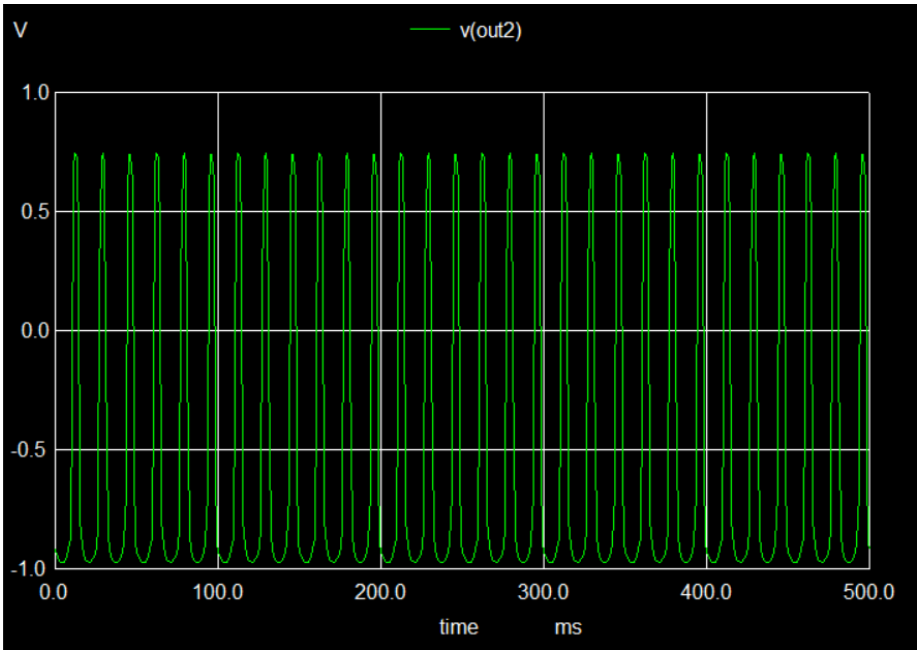
Transient Analysis

Input

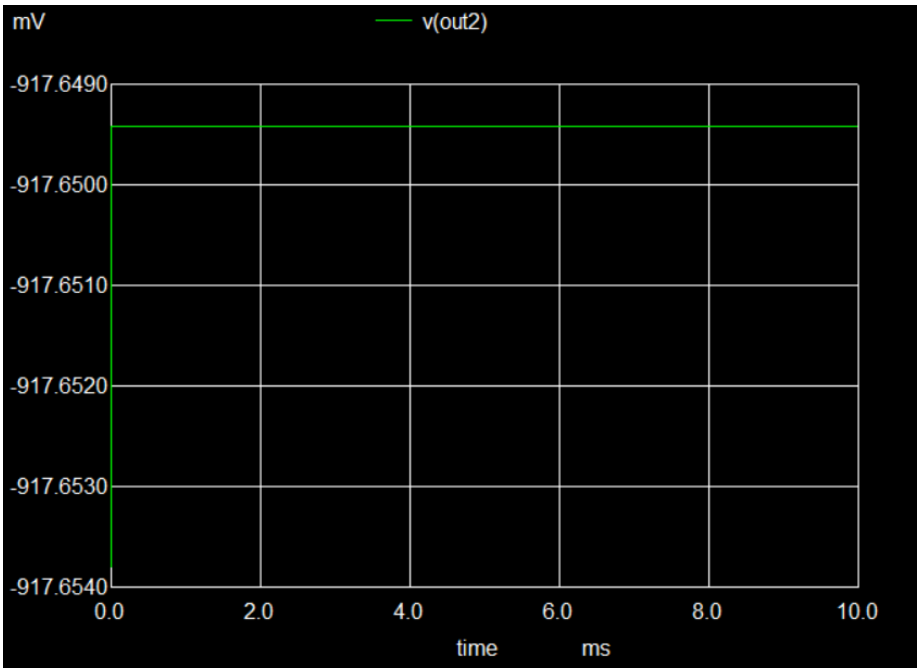




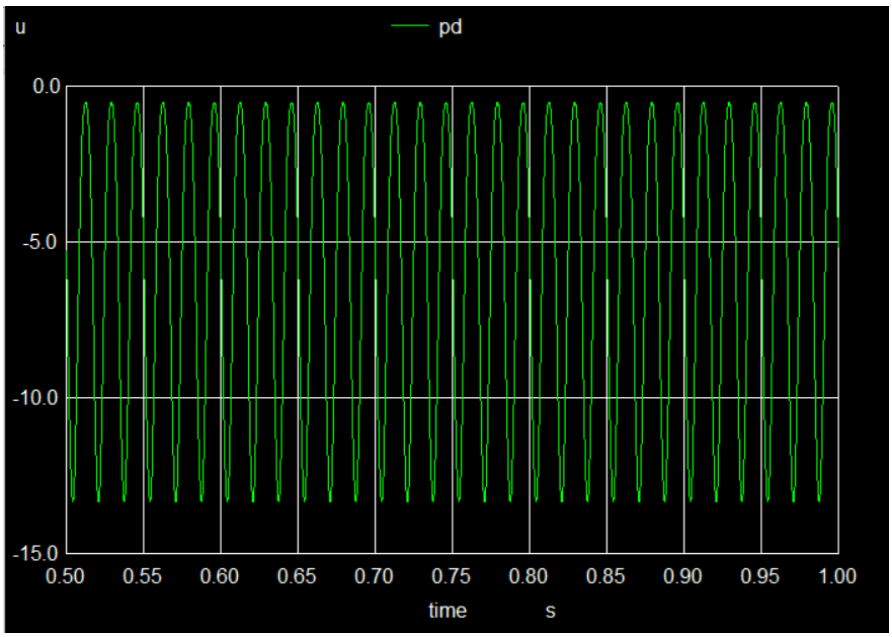
Output



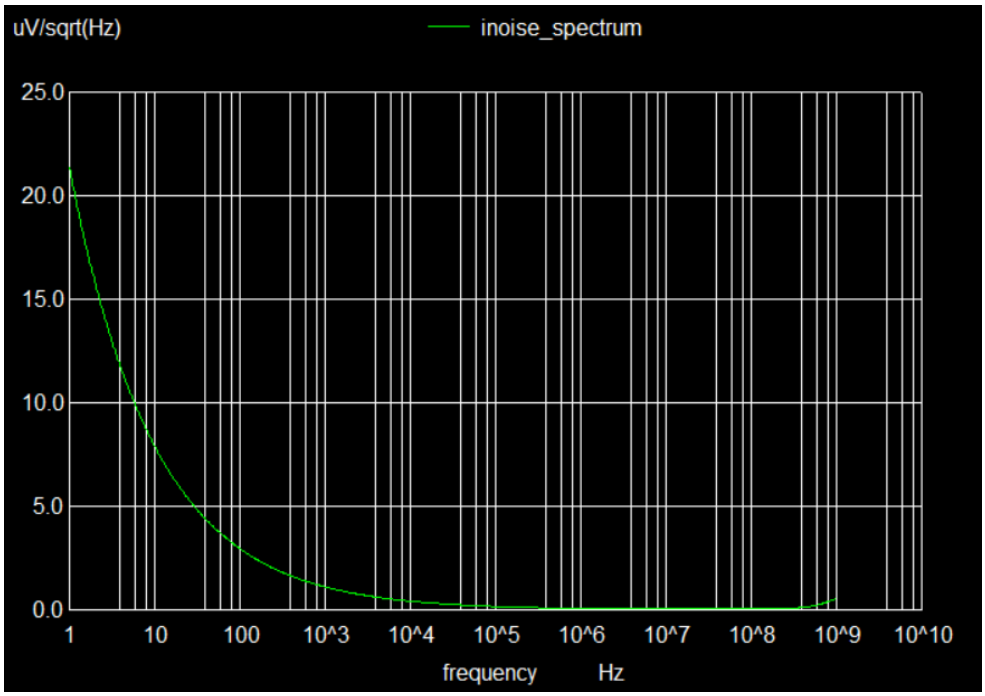
Offset Voltage



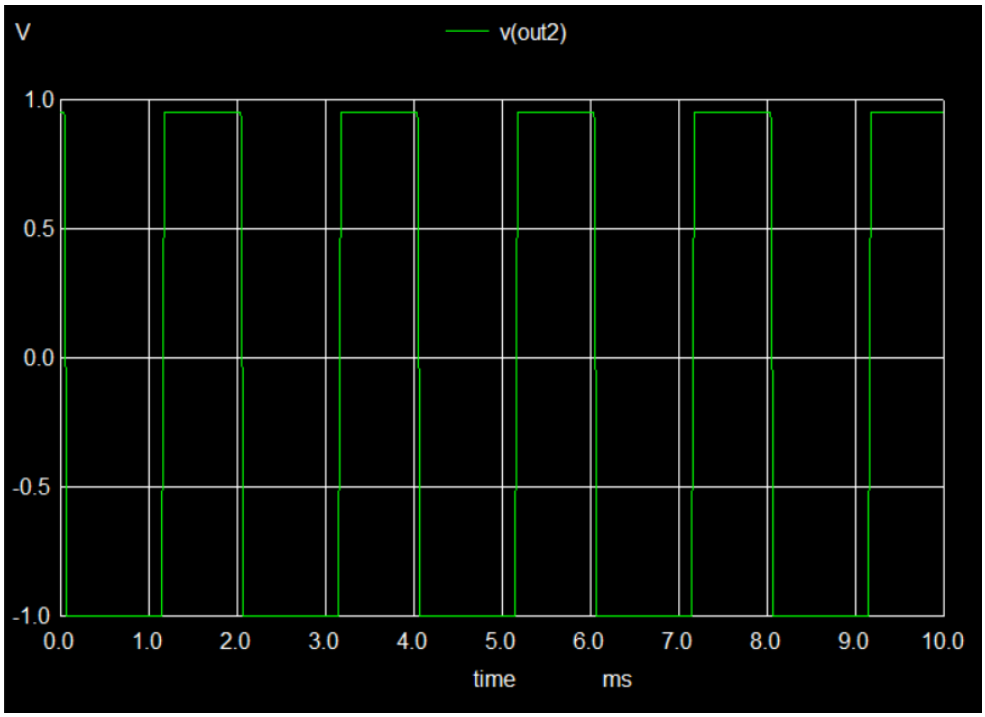
Power Dissipation (For sine(0 1m 60) and 1k load)



Input Noise Spectrum



Slew Rate



Specifications

Specification	Value
Differential Gain	33.36dB
CMRR	41.759dB
Phase Margin	$45.92°$
Input Offset Voltage	$20.85mV$
Power Disspation (at *sine(0 1m 60)* & *1k load*)	$13\ \mu W$
Slew Rate	$20\ V/\mu s$