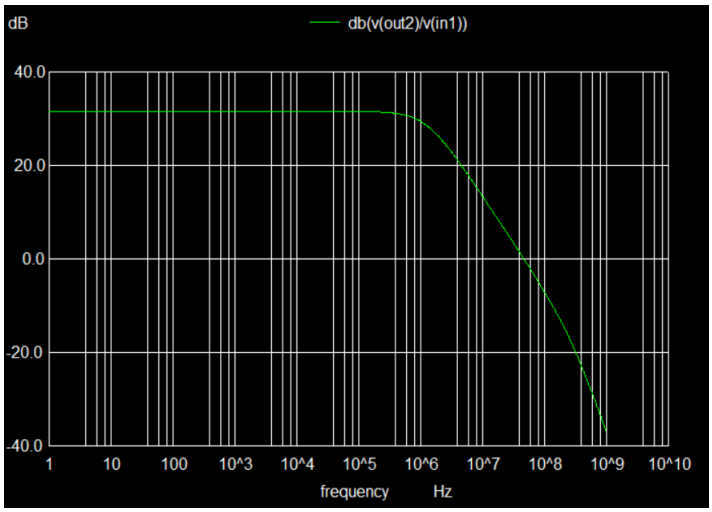
Simulation Results – **avsd_opamp**

(Two Stage CMOS Operational Amplifier)

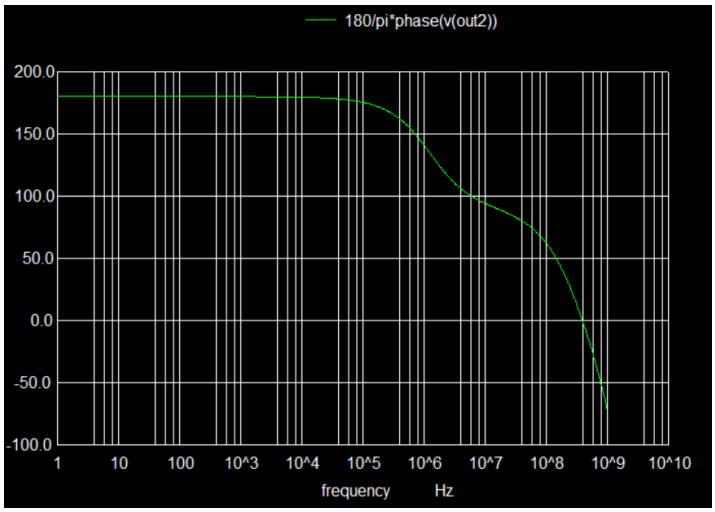
- *R.V.ROHINTH RAM*

Frequency Response (Differential Mode)

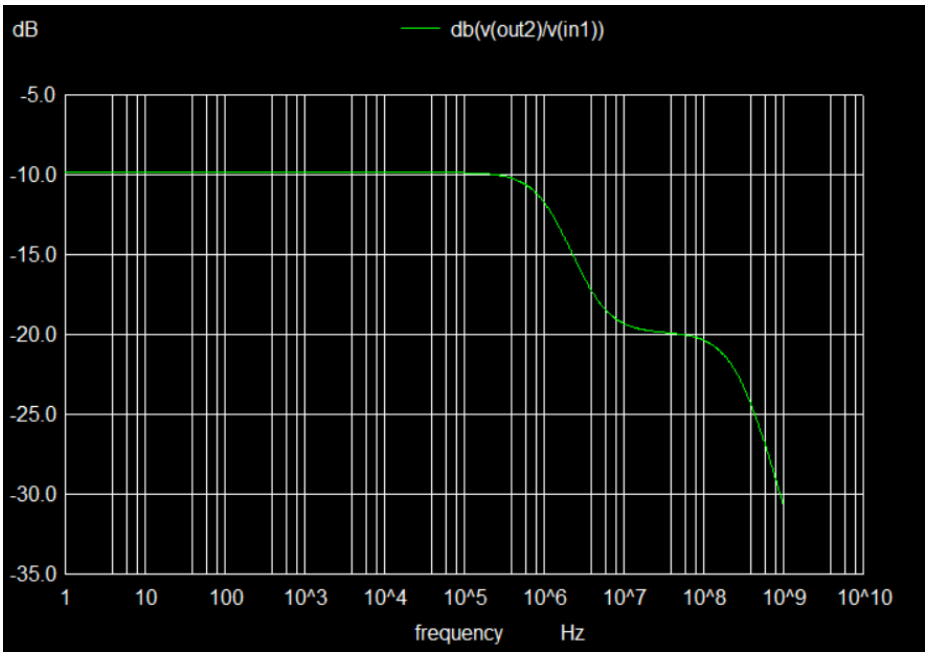
Magnitude(dB)



Phase

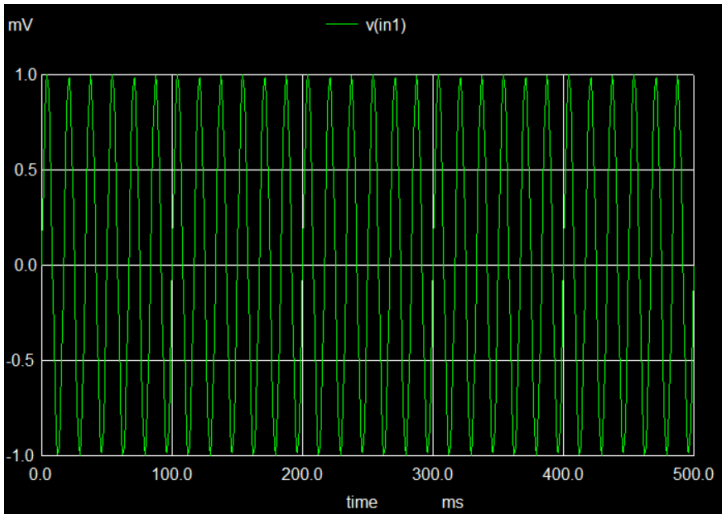


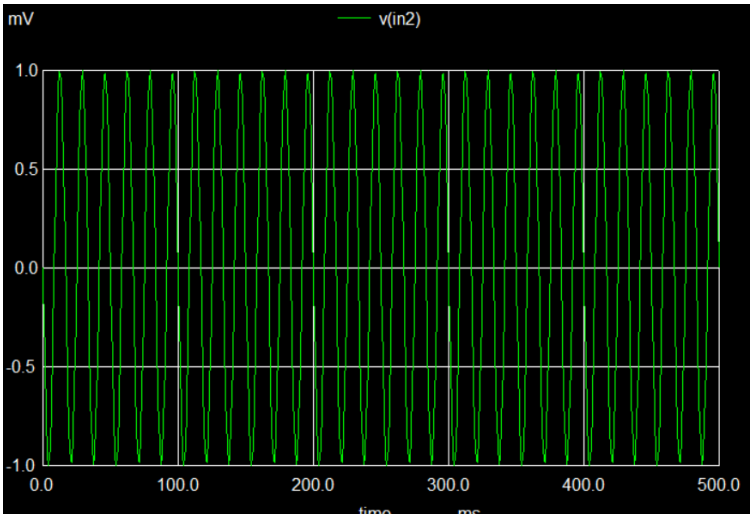
Frequency Response (Common Mode)



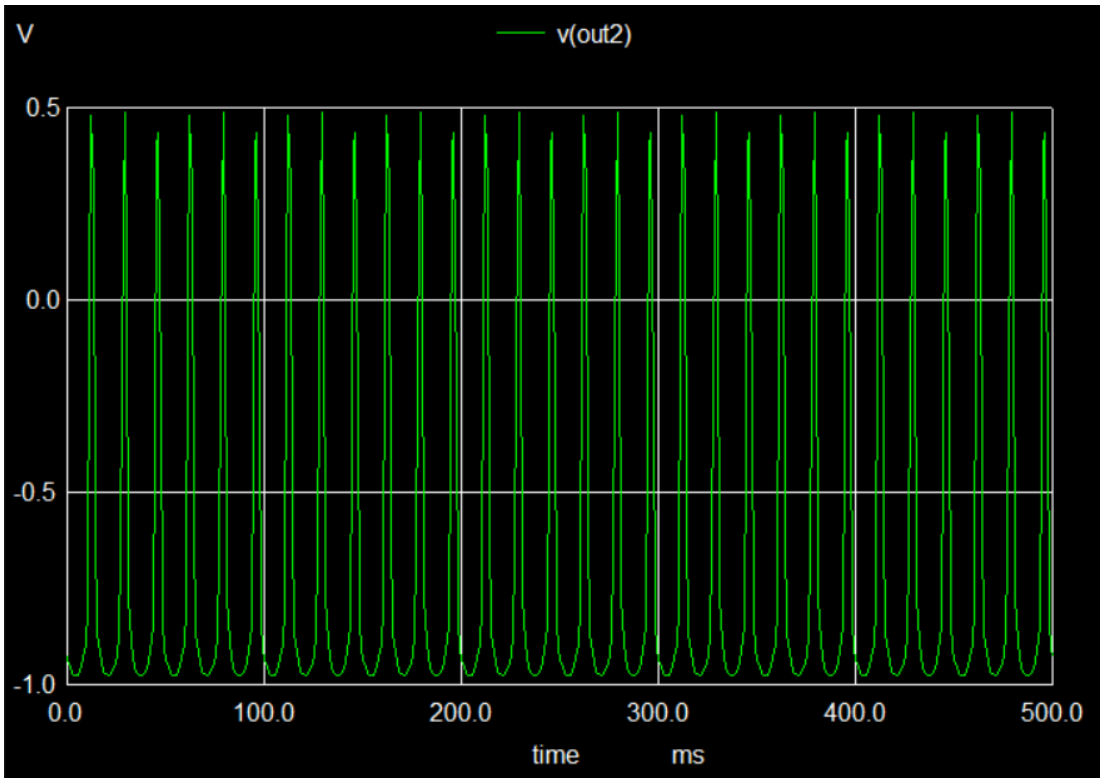
Transient Analysis

Input

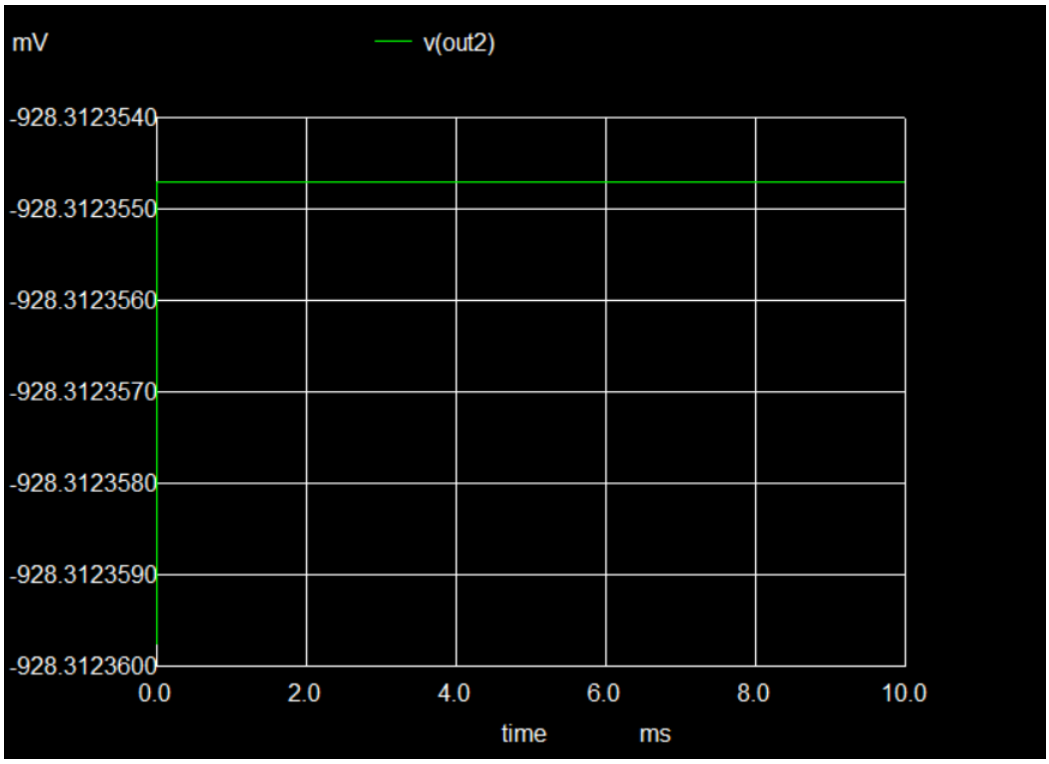




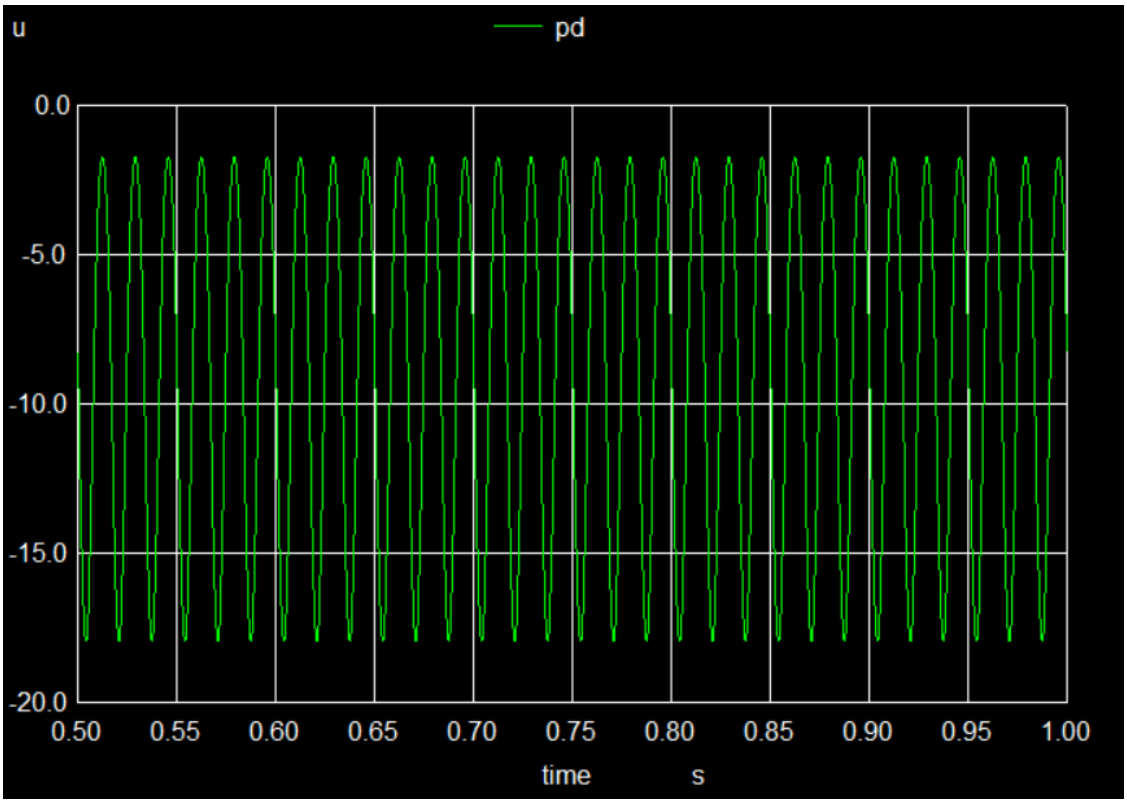
Output



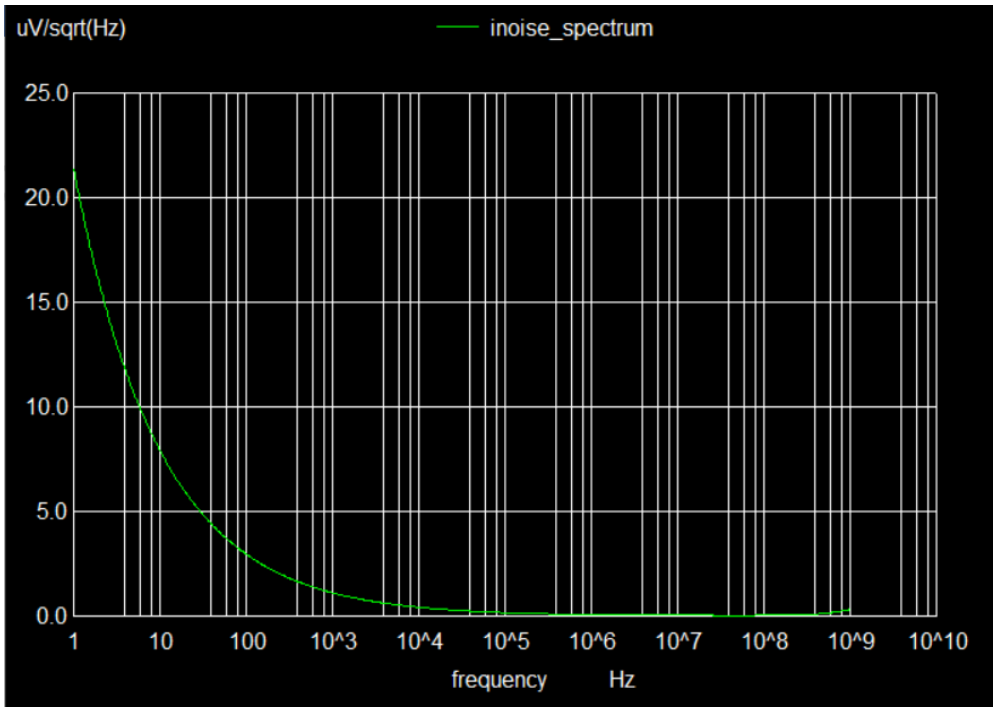
Offset Voltage



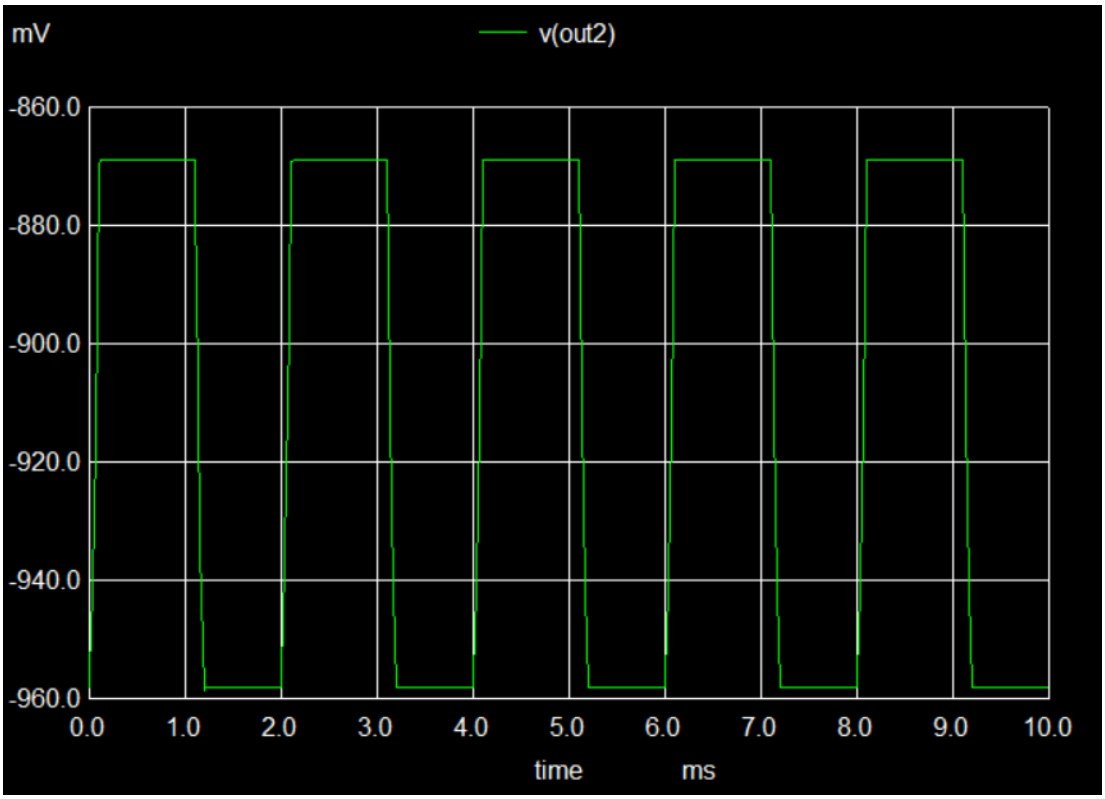
Power Dissipation (For sine(0 1m 60) and 1k load)



Input Noise Spectrum



Slew Rate



Specifications

Specification	Value
Differential Gain	31.55dB
CMRR	41.4dB
Gain Bandwidth Product	46MHz
Phase Margin	101.93°
Input Offset Voltage	-24.55mV
Power Dissipation (at *sine (0 1m 60)* & *1k load*)	17 μW
Slew Rate	0.5 V/ms