

KPIT

An Introduction to Multicore System Design

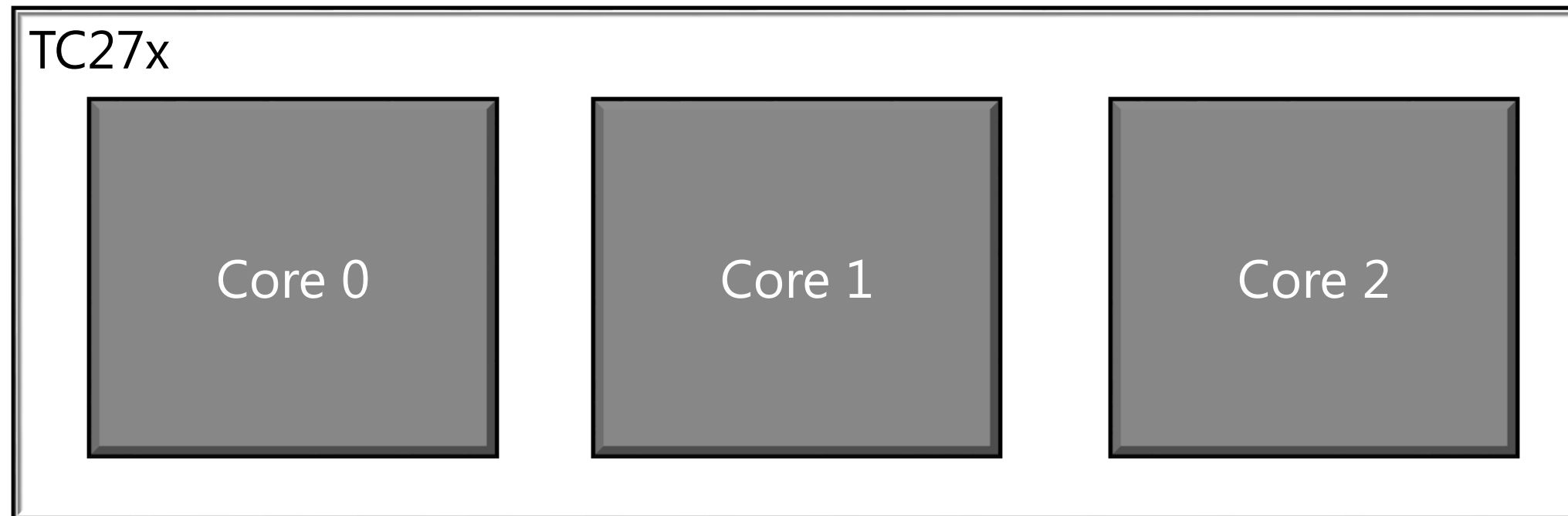
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Agenda

- Multicore concepts
- Hardware requirements for multicore
- AUTOSAR treatment for multicore
- Synchronous procedures for AUTOSAR multicore systems
- Typical AUTOSAR Multicore System Example
- BSW Partitioning in Multicore environment
- Core assignment principles
- Design Hints for Application Development

Multicore Concepts

- Multicore implies presence of more than one cores on the same silicon chip
- The processing speed of the chip increases and processing time is reduced
- TC27x (Aurix) is an example of such microcontroller. It is a high-performance microcontroller with three TriCore CPUs.



Hardware requirements for multicore

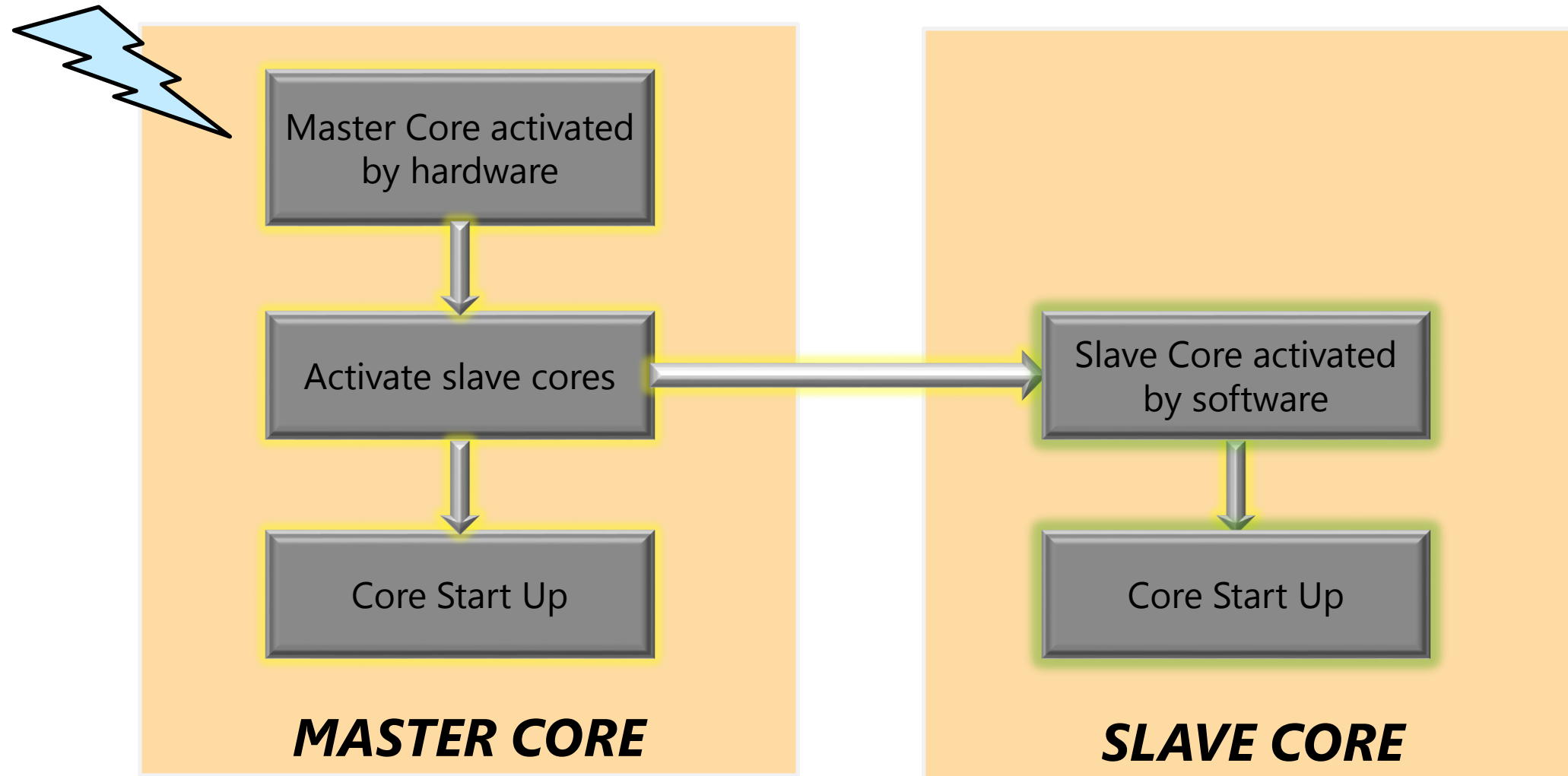
Hardware CPU and Memory requirements :

- More than one CPU on a same piece of silicon
 - Provision of a method to identify core through software
 - All cores on the chip shall have same instruction set and shall have same endianness
 - Inter-core interrupts supported for notifications
 - Shareable memory between all the cores
 - Memory protection unit preferred on the chip.
- ✓ The Infineon TC27x TriCore microcontroller supports all the mentioned features above

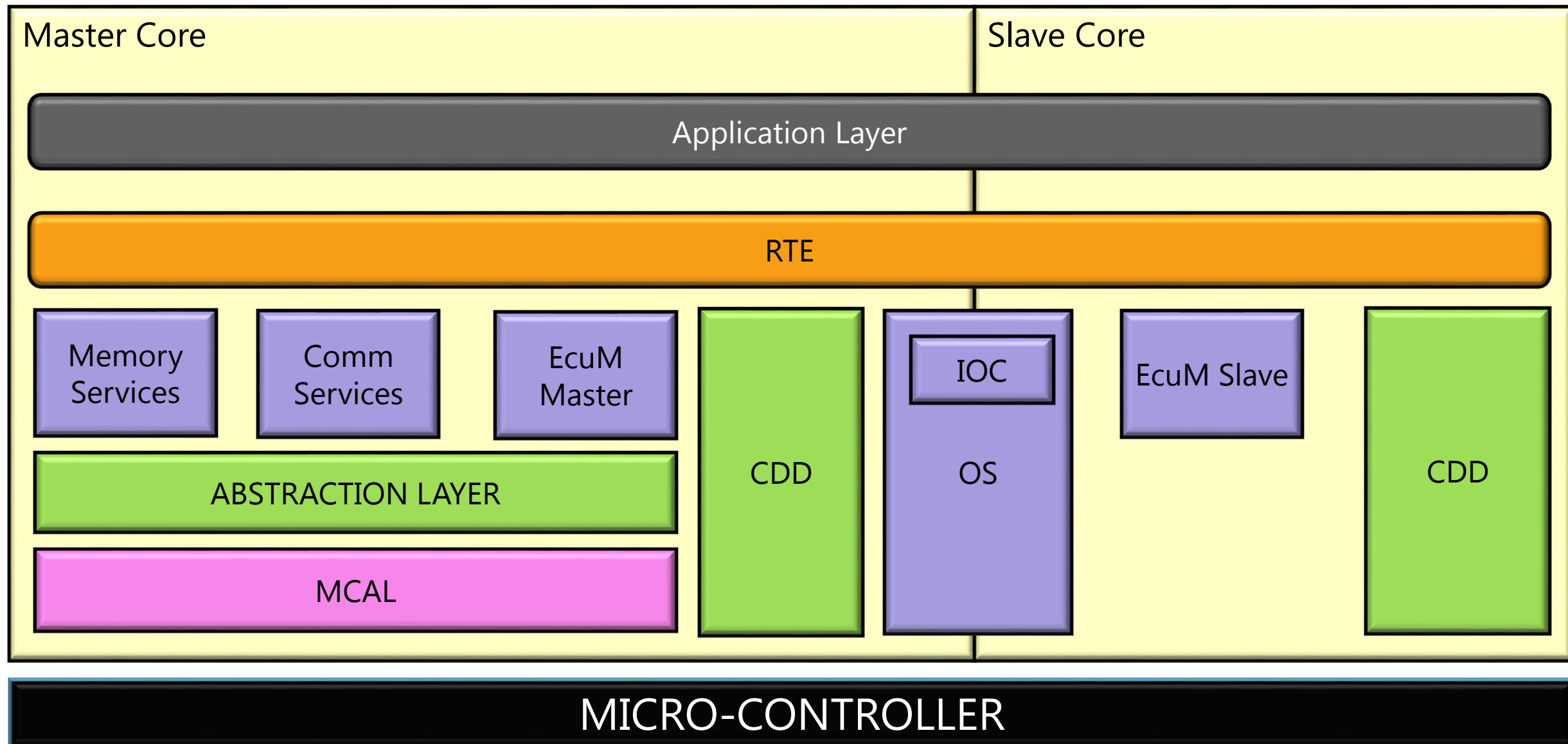
AUTOSAR treatment for multicore

- AUTOSAR specifications require a system with a master-slave start-up behavior. This could be hardware supported or either emulated in software
- Master core shall be the one that requires no activation by software, whereas, the slave cores shall be activated by software
- Upon activation, master core shall activate all the slave cores. This should happen before starting Operating system on the master core
- Synchronous start up and shut down of the multicore system shall be ensured by AUTOSAR BSW modules

Synchronous procedures for AUTOSAR multicore systems (Start up)



Typical AUTOSAR Multicore System Example



BSW Partitioning in Multicore environment

Master Core contains :

- Entire set of BSW modules similar to a single-core system. e.g. BswM, COM, PduR, OS, RTE etc
- EcuM "Master" Module

Slave Core contains :

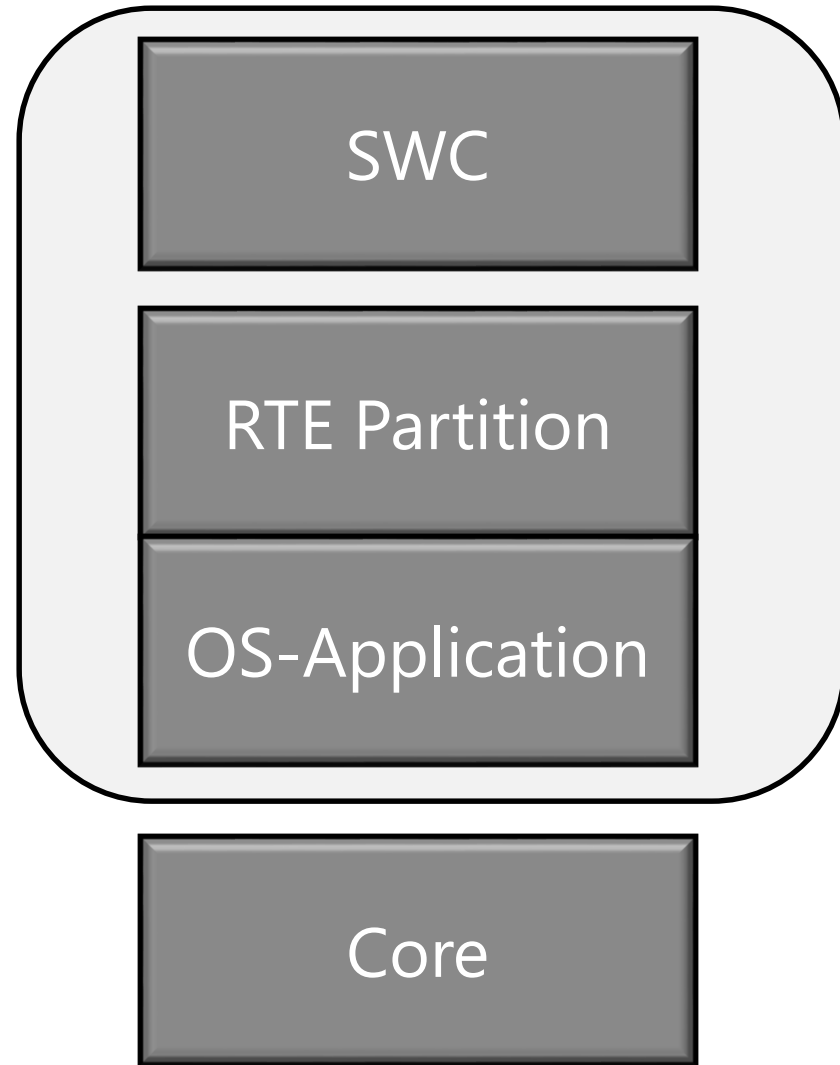
- Operating System(+ IOC)
- Run Time Environment(RTE)
- EcuM "Slave" Module
- Complex Device Drivers(CDD)

Core assignment principles

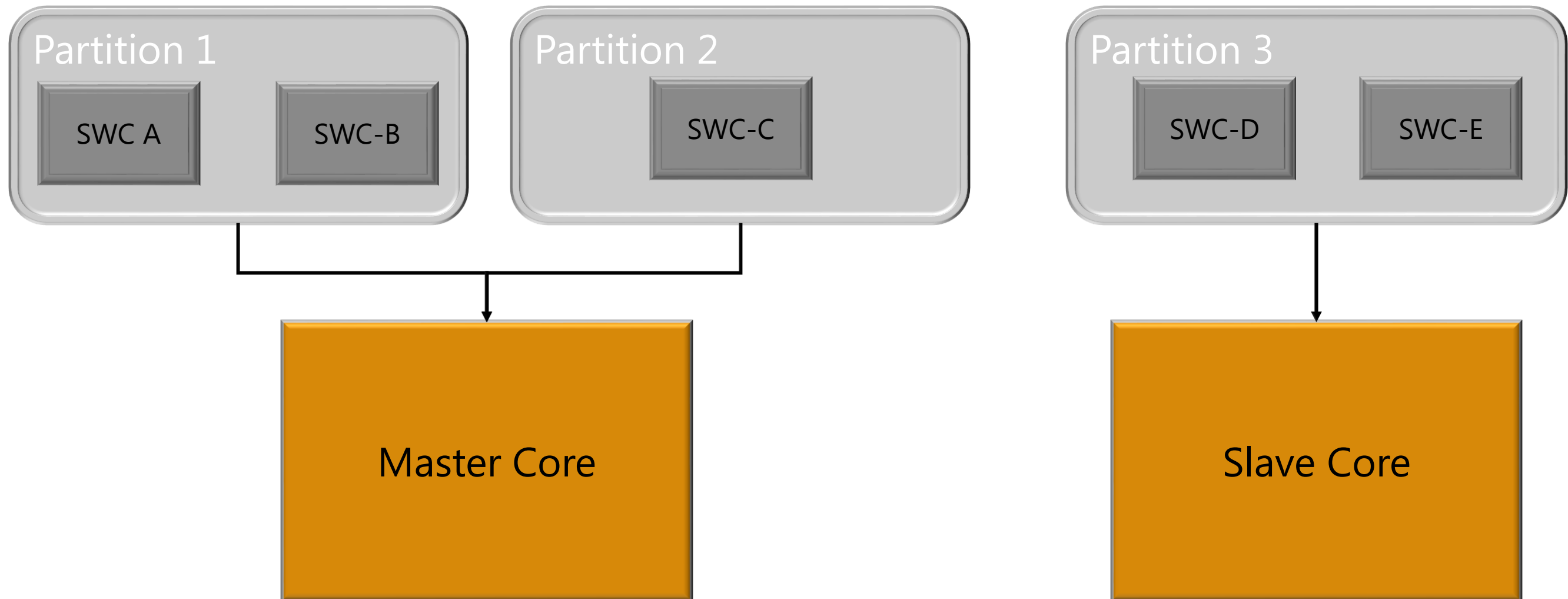
- Core assignment to Application Software Components(SWC) is done through Operating System
- Locatable Entity(LE) shall be represented in OS context as a partition, known as OS-Application
- LE is an entity that has to be located entirely on one core
- One LE can contain multiple Application SWCs but an application SWC cannot be part of multiple LE
- AUTOSAR supports such partitioning only for SC3/SC4 (single core) or SC1/SC2/SC3/SC4(multi core) OS configurations

Core Assignment Principles

- Mapping of Software Component(SWC) to a core

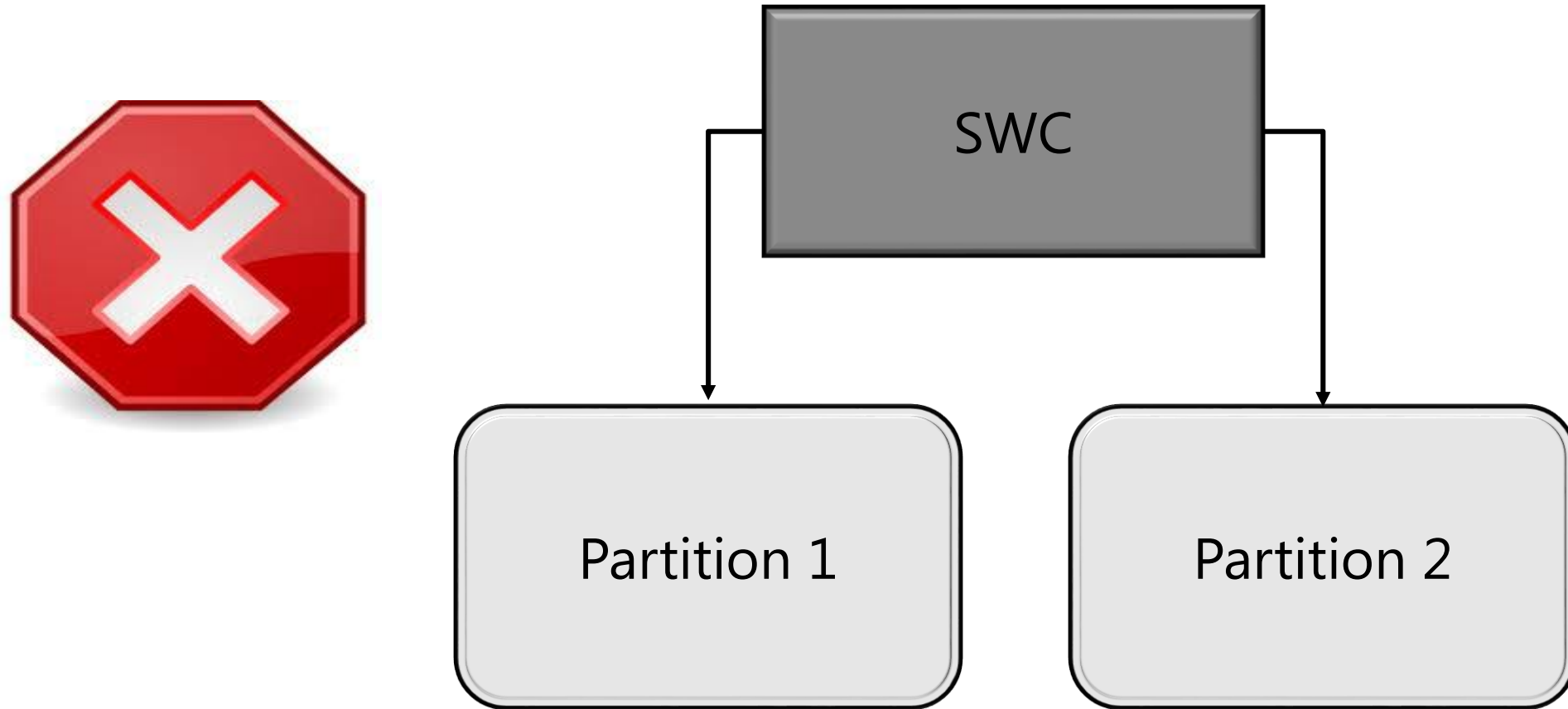


Core assignment example



Core Assignment Example

- One SWC cannot be a part of two partitions or Locatable entities(LE)



Design Hints for Application Development

- Classify runnables that can operate and function independently without dependency from other runnables
- Such runnables should be equally distributed among cores using OS-partitions known as Locatable Entities(LE)
- As entire configuration is static in AUTOSAR environment, it is necessary to consider load division among cores while designing partitions



Questions

Thank You

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