Introduction to logic gates

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***Abstract*—In this lab experiment Half-Adder logic circuits and Full Adder logic circuits was designed using Basic logic gates Like OR gate, XOR gate and AND gate. And we also calculate sum and carry of each logic circuit and we made the Truth table for Half Adder and Full Adder . The design of circuit was based on our requirement of output. The theory behind logic gates and circuit are explained in detail.**

***Index Terms*—Exclusive-OR logic gate(EXOR gate),Carry (C),Ground (GND), Intigrated Circuits (IC) .**

I. Introduction

Digital Electronics is totally based on logic gates, so in this lab we introduced with various logic gates. In digital electronics we concentrate on binary signal that is 0 and 1 and logic gates work on binary algebra and do some operations.

A. Logic Gate

In electronics logic gate is a device with many number of inputs and one output. There are three basic Logic gates namely AND gate, OR gate and NOT gate. And other gates are derived by the combination of these three logic gates and they are NAND gate , NOR gate , EXCLUSIVE-OR gate and EXCLUSIVE-NOR gate.And input of logic gate there is a binary signal that is one or zero at a time. And output is also a binary signal.

Here are the gates that we got introduced in the lab.

1) OR gate: OR gate gives 1 logic as output when either of input is 1 logic and gives 0 logic as output when both of inputs have 0 logic. This logic gate can be implemented by using IC- 7432.

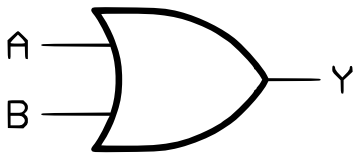

Fig. 1. OR-Logic gate

2) AND logic gate: AND gate gives output as 1 logic when both inputs are 1 and logic 0 as output in all other cases.This logic gate can be implemented by using IC- 7408.

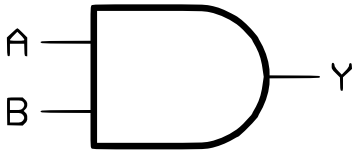

Fig. 2. AND-Logic gate

3) XOR logic gate: XOR(Exclusive OR gate) This gate gives 1 as output when both input is not same and gives output as 0 when both inputs are same. This logic gate can be implemented by using IC-7486

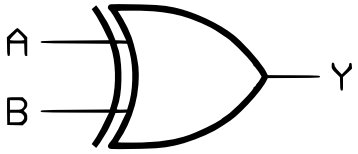

Fig. 3. XOR-Logic gate

B. Adder

Adder is a combination of logic gates that performs an operation on binary number. There are two type of Adder

- Half Adder
- Full Adder

1) Half Adder: The half adder adds two binary digits A and B and produces two outputs as sum and carry. XOR gate is applied to both inputs to produce sum and AND gate is applied to both inputs to produce carry. Half adeer is used to design simple addition with the help of logic gates.

2) Full Adder: This Full adder is obtain by using two half-adders. The difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs, whereas half adder has only two inputs and two outputs. The first two inputs are A and B and the third input is an input carry as Cin.The output carry is designated as C-out and the output sum is designated as S. We can implement a full adder circuit by two half adder circuits. At first, half adder will be used to add A and B to produce a partial Sum and a second half adder logic can be used to add C to the Sum produced by the first half adder to get the final S output.

II. Appartues Required

1) Electronic Trainer Kit

2) IC 7408

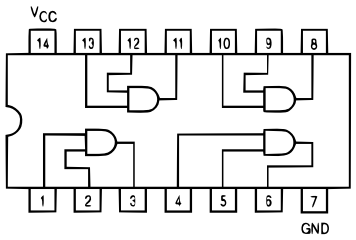

Fig. 4. 7408 Quad 2 Input AND Gates

3) IC 7432

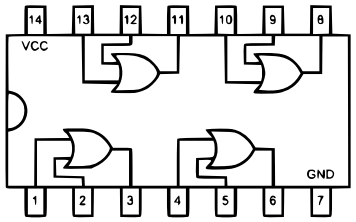

Fig. 5. 7432 Quad 2 Input OR Gates

4) IC 7486

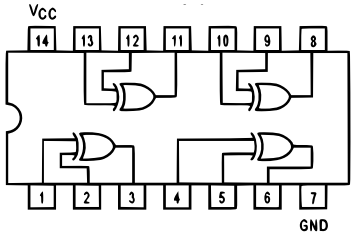

Fig. 6. 7486 Quad 2 Input XOR Gates

5) Some copper wire to have connection between circuit

III. Procedure

A. Half Adder

We assembled the circuit of half Adder by connecting AND gate IC and ExOR gate IC with input A and B on breadboard of Electronic trainer kit. And then we connected point 1 and 2 of 7408 AND gate with input A and B respectively for output of carry. And we connected point 1 and 2 of 7486 ExOR gate with input A and B respectively for sum. And then we connected point 14 ($_{cc}$) with 5V power supply and point 7 (GND) with 0V of both 7408 and 7486 ICs. And then we connected point 3 (output) of 7486 ExOR gate IC and 7408 AND gate IC for output sum(S) and carry(C) respectively.And we noted all the observation and made a Truth table for it.

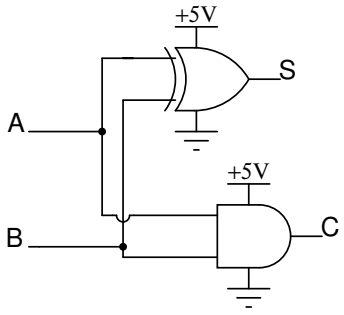

Fig. 7. Circuit of Half Adder

B. Full Adder

We assembled the circuit of Full Adder by connecting AND gate IC and ExOR gate IC with input A and B on breadboard of Electronic trainer kit. And then we connected point 14 (V cc) with 5V power supply and point 7 (GND) with 0V of all three 7408, 7486 and 7432 ICs. And then we connected point 1 and 2 of 7408 AND gate and 7486 ExOR with input A and B respectively . And then we connected point 3 of 7486 IC with point 4(one of the input of another ExOR gate) of same 7486 IC. And we connected point 5 of above 7486 IC with new input $Carry_{In}$ (C_{IN}). And point 4 and 5 of 7408 AND gate IC with point 3 of 7486 IC and $Carry_{In}$ (C_{IN}) respectively. And we connected point 1 of 7432 OR gate IC with point 6 of 7408 IC and point 2 of 7432 IC with point 3 of 7408 AND gate IC. And then we connected point 6 (output) of 7486 IC with output sum(S) and point 3 of 7432 OR gate IC with output carryout(C out). And we noted all the output with respect to all inputs and made a truth table.

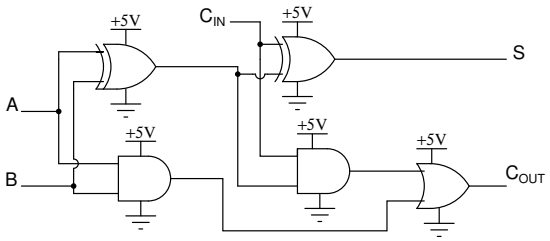

Fig. 8. Circuit of Full Adder

IV. Precautions

1) All ICs should be checked before experiment.
2) Proper grounding should be done in order to protect equipments.
3) All connections should be proper there should not be any short circuit.
4) Switch off the power supply while making circuit.
5) There should be minimal use of copper wires in order to avoid noise in the reading.

V. Observations and Results

After noted observation we made Truth table. And match all the results.And they all correct as we expected. Table 1 is

Truth table for half adder and Table 2 is Truth table for Full Adder. And we found the expression for sum and Carry. Results of half Adder circuit :

$$Sum = A \bigoplus B$$
$$Carry = A.B$$

Results for Full Adder circuit :

$$Sum = A \bigoplus B \bigoplus C_{IN}$$
$$Carry = BC_{IN} + AC_{IN} + AB$$

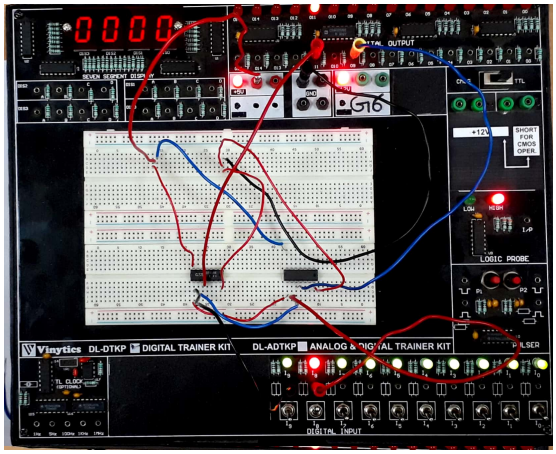

Fig. 9. Observed result when A = 0 and B = 1 and we get results as sum =1 and carry =0

TABLE I
TRUTH TABLE FOR HALF ADDER

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

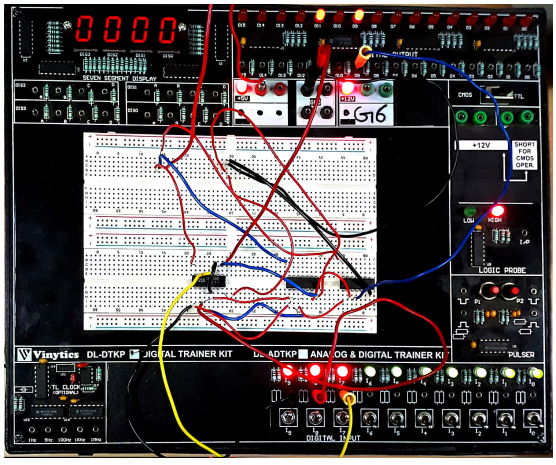

Fig. 10. Observed result when A =1 and B = 1 and C=1 we get results as sum =1 and carry =1

TABLE II
TRUTH TABLE FOR FULL ADDER

A	B	C_{IN}	S	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

VI. CALCULATION

We calculated the sum and carry using some mathematical approch and Boolean Algebra. Like we Assumed X $= B \bigoplus C_{IN}$

$$\begin{aligned} Sum &= \bar{A}\bar{B}C_{IN} + \bar{A}B\overline{C_{IN}} + A\bar{B}\overline{C_{IN}} + ABC_{IN} \\ &= \bar{A}(\bar{B}C_{IN} + B\overline{C_{IN}}) + A(\overline{B\overline{C_{IN}}} + BC_{IN}) \\ &= \bar{A}(B \bigoplus C_{IN}) + A(\overline{B \bigoplus C_{IN}}) \\ &= \bar{A}X + A\bar{X} \\ &= A \bigoplus B \bigoplus C_{IN} \end{aligned}$$

$$\begin{aligned} C_{OUT} &= \bar{A}BC_{IN} + A\bar{B}C_{IN} + AB\overline{C_{IN}} + ABC_{IN} \\ &= BC_{IN}(\bar{A} + A) + AC_{IN}(\bar{B} + B) + AB(\overline{C_{IN}} + C) \\ &= BC_{IN} + AC_{IN} + AB \end{aligned}$$

VII. CONCLUSION

In half adder and full adder we got desired output as we calculated theoritically.These logic gates prove very useful for calculation purposes and can be used in digital electronics to achieve different purposes. And we got a little bit idea of how binary system work practically. And we also got to know how to use logic gates.

ACKNOWLEDGMENT

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REFERENCES

[1] Behzad. Razavi, *Design of Analog CMOS Integrated Circuits*, Mc Graw Hill Education Pvt. Ltd, 2nd Edition 2017.

[2] Lecture Slides of Dr. Kunal Ghosh (Assistant Professor,IIT Mandi) and Instructions of Dr. Hitesh Shrimali (Assistant Professor,IIT Mandi).

[3] Previous year's report and guidence of Aanand Ramrakhyani. *and various report of various groups*. [*https://insite.iitmandi.ac.in/moodle/*]. IC 161P course, 2017.

[4] *Stefan M. Moser, for balancing to equaiton* . [*http://moser-isi.ethz.ch/docs/typeset$_e$quations.pdf*].