Experiment: 5
MOS Technology and CMOS Incveter

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***Abstract*—This weeks experiment aimed at implementing a CMOS invertor in order to observe the input-output characteristics of CMOS invertor. Also we were required to measure the N_{MH} and N_{ML} i.e. Noise Margin High and Noise Margin Low respectively and tr and tf i.e Rise Time and Fall Time are also measured. Also we were required to analyze and then subsequently remove the various problems encountered in circuits in the laboratory. Going through this experiment we encountered several unexpected results which we solved and analyzed by help of our instructor Hitesh sir and TAs.**

I. Introduction

A. CMOS

CMOS stands for Complimentary Metal Oxide Semiconductor. The inverter is universally accepted as the most basic logic gate doing an Boolean operation on a single input variable. The simple structure of a CMOS contain a combination of an p-MOS inverter at the top and a n-MOS inverter at the bottom.
Two important characteristics of CMOS inverter are high noise immunity and low static power consumption.
CMOS inverter has many applications. It is used in RF circuits, signal devices, in cameras and as transmission gates.

B. Noise Margin

It is a parameter related to the transfer characteristics . It allows us to estimate the allowable noise voltage at the input of the gate so that the output will not be affected. It is basically specified in two parameters i.e. N_{MH}andN_{ML}.

II. Apparatus Required

A. Digital Storage Oscilloscope (DSO)-1

Agilent Technologies DSO1052B (50MHz,1GSa/s)

B. CD4007UBE Dual Complimentary Pair Plus Inverter

Fig. 1. IC

C. Function Generator-1

scientific SM5070 (3 MHz)

Fig. 2. function generator

D. Bread Board

Fig. 3. Breadboard

E. Oscilloscopic Probes with BNC Connector-3

One-X probe

F. Some copper wire to have connection between circuit

III. Procedure

A. An Integrated Chip(IC) was used and the circuit was assembled by connecting the IC with V_{dd} and V_{ss} at proper points.

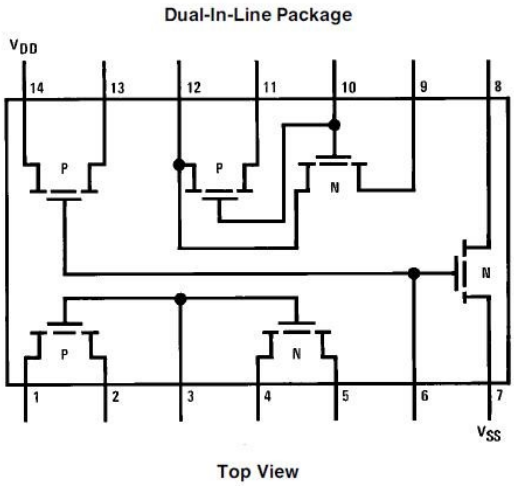

Fig. 4. Internal circuit in IC

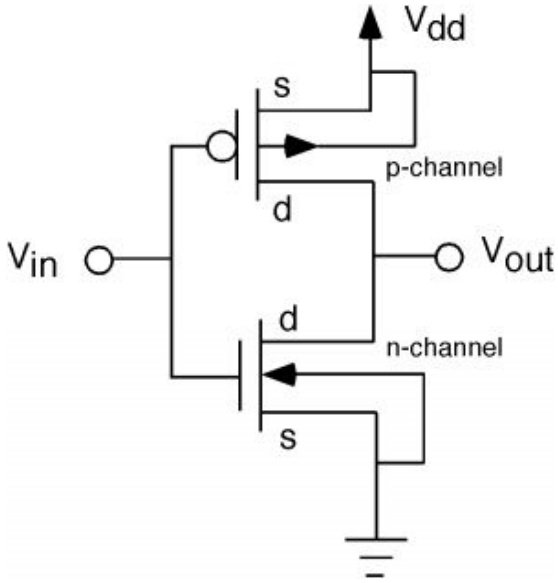

Fig. 5. CMOS

B. Connect point 8 and 13 with a wire as shown in figure.

C. connect point 14 with a $5V$ power supply from breadboard as V_{DD} as shown.

D. Connect point 7 with ground as V_{SS}.

E. Connect function generator to 6 as input with $1X$ probes and give square wave of appropriate frequency.

F. We took the output from 8 in DSO and noted the observations.

IV. Experimental Results and Discussion

A. Square wave was given of frequency $29.66Hz$ in function generator as input to the circuit.

B. All blue lines in graph figures are input and all pink lines are output.

C. Input square wave is given and output is taken in DSO.

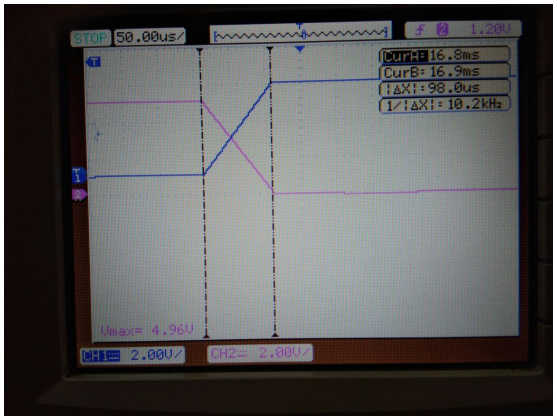

Fig. 6. represents high to low propagation delay (t_{pHL}).

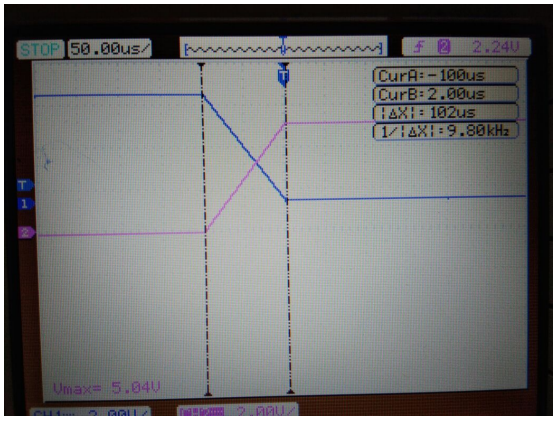

Fig. 7. represents low to high propagation delay (t_{pLH}).

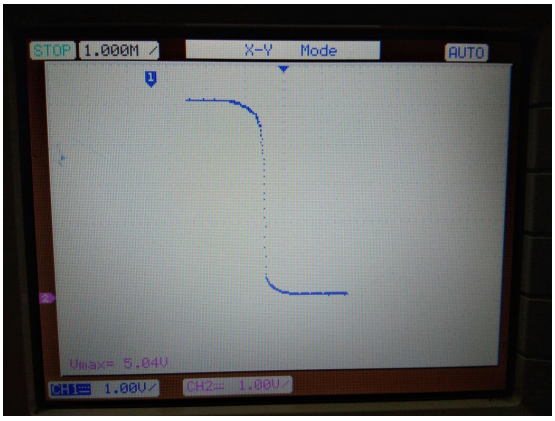

Fig. 8. graph of input vs output wave observed in DSO.

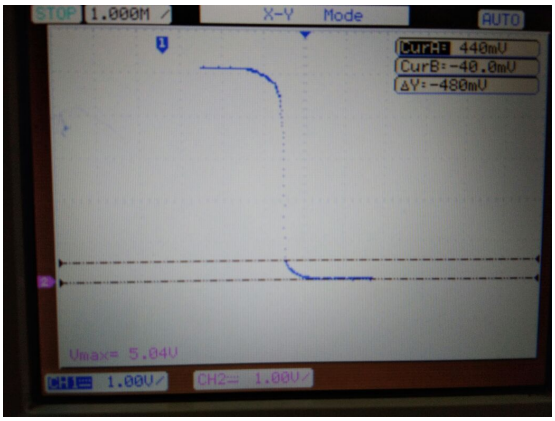

Fig. 9. Observed $\delta Y = 480mV$ for N_{ML}.

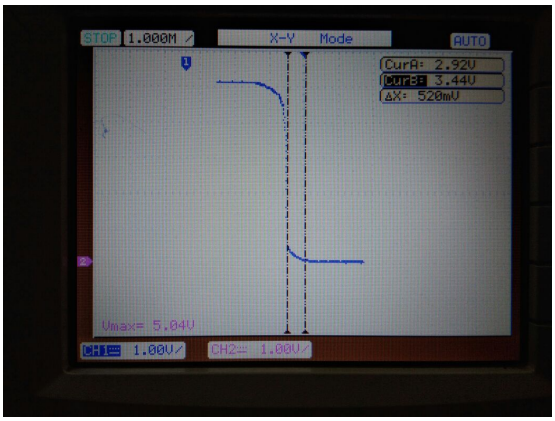

Fig. 10. Observed $\delta X = 520mV$ for N_{ML}.

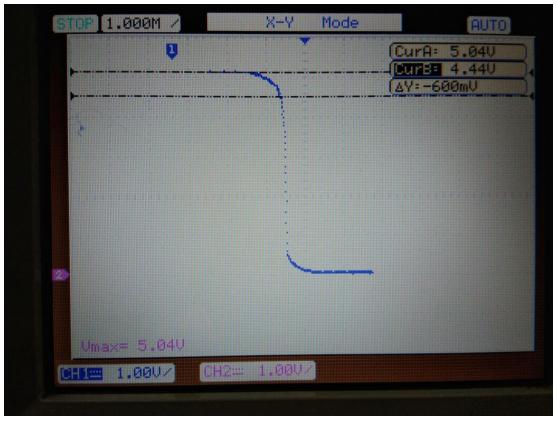

Fig. 11. Observed $\delta Y = 600mV$ for N_{MH}.

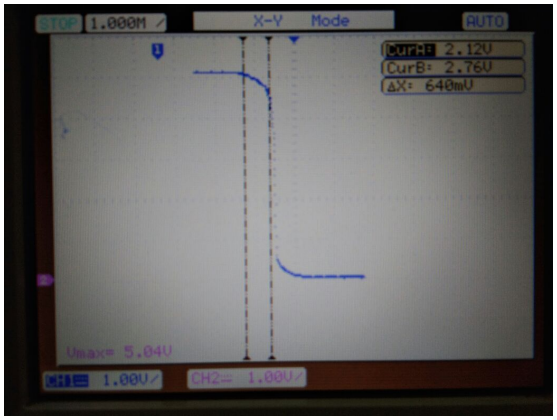

Fig. 12. Observed $\delta X = 640mV$ for N_{MH}.

V. Calculation

A. Propagation Delay

$t_{pHL} = 98\mu s$

$t_{pLH} = 102\mu s$

therefore,

Average propagation delay $t_p = \frac{t_{pHL}+t_{pLH}}{2}$

so $t_p = 100\mu s$

B. Noise Margin

slope of $NM_H = \frac{\delta Y}{\delta X} = \frac{600}{640} = 0.9357$

slope of $NM_L = \frac{\delta Y}{\delta X} = \frac{480}{520} = 0.923$

therefore Noise Margin $(NM) = \frac{NM_H+NM_L}{2} = \frac{1.861}{2} = 0.93$

VI. Precaution

A. Before using the prob cross check that probe con-figuration selected in DSO is the same as the probe using in the circuit (usually 1-X probe).

B. Do not allow the crocodile clips to touch each other.

C. Don't let touch your hand while measuring the resistor, it will give wrong result or measurement.

D. Copper wires used should be minimum to avoid unnecessary error in readings.

E. Proper Grounding should be done in order to protect equipements from damaging.

F. Select the DC coupling in DSO.

References

[1] Lecture Slides of Dr. Kunal Ghosh (Assistant Professor,IIT Mandi) and Instructions of Dr. Hitesh Shirmali (Assistant Professor,IIT Mandi).

[2] Previous year's report and guidance of Aanand Ramrakhyani. *and various report of various groups*. [*https://insite.iitmandi.ac.in/moodle/*]. IC 161P course, 2017.

[3] IIT GUWAHATI VIRTUAL LABS
http://iitg.vlab.co.in/