Batch: A2 **Roll No.: 16010122041**

Experiment / assignment / tutorial No. 9

TITLE: Study of RISC and CISC Architecture

AIM: Understanding RISC and CISC Architecture

Expected OUTCOME of Experiment: CO2

Books/ Journals/ Websites referred:

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization", Fifth Edition, TataMcGraw-Hill.
2. William Stallings, "Computer Organization and Architecture: Designing for Performance", Eighth Edition, Pearson.
3. Dr. M. Usha, T. S. Srikanth, "Computer System Architecture and Organization", First Edition, Wiley-India.

Pre Lab/ Prior Concepts:

Reduced Set Instruction Set Architecture (RISC)

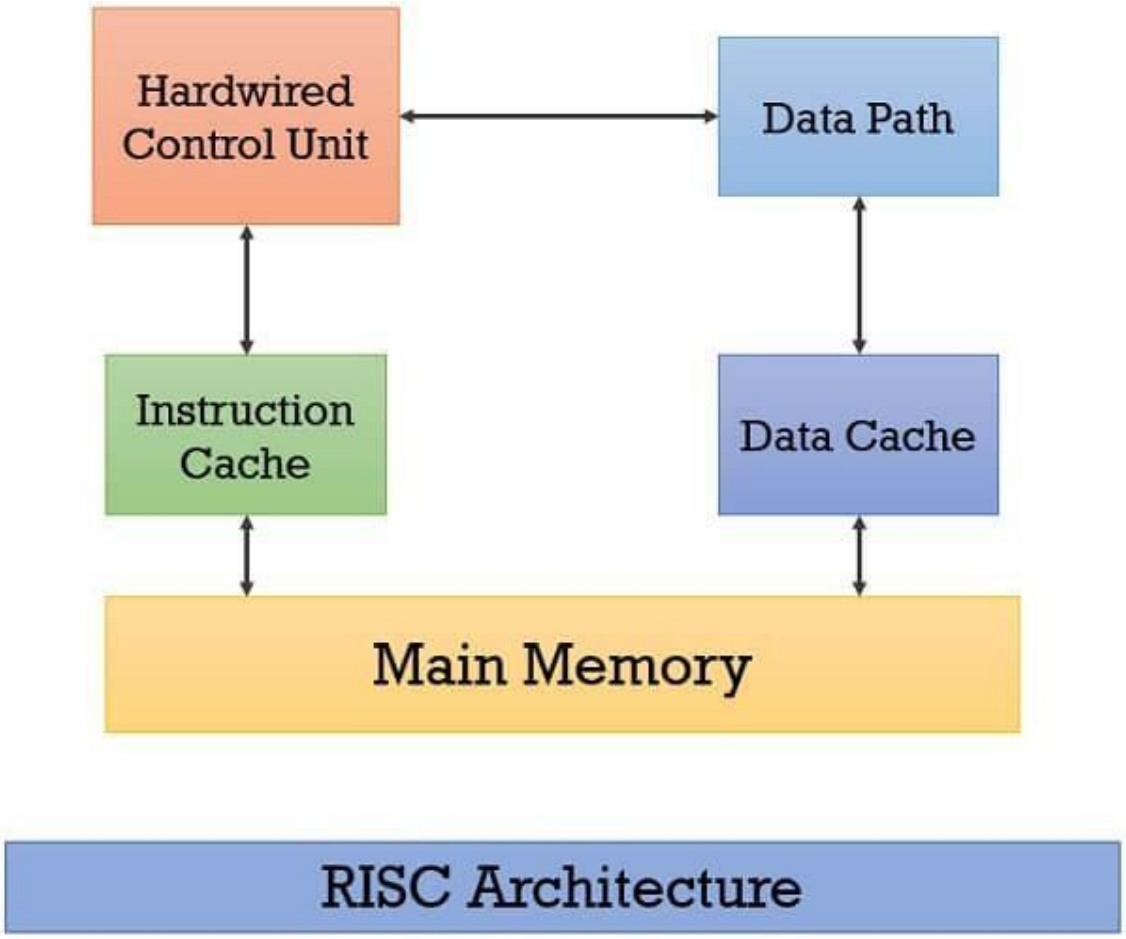
The main idea behind is to make hardware simpler by using an instruction set composed of a few basic steps for loading, evaluating and storing operations just like a load command will load data, store command will store the data.

Complex Instruction Set Architecture (CISC)

The main idea is that a single instruction will do all loading, evaluating and storing operations just like a multiplication command will do stuff like loading data, evaluating and storing it, hence it's complex.Both approaches try to increase the CPU performance

RISC Architecture

1. Diagram of RISC Architecture:



2. Brief Explanation of each component

- Hardwired Control Unit: The hardwired control unit is responsible for generating the necessary control signals to direct the data path and execute instructions. It interprets the opcode of each instruction and activates the appropriate hardware components to carry out the instruction's operation.

- Data Path: The data path is the component that performs arithmetic and logic operations on data. It includes components like the Arithmetic Logic Unit (ALU) and a set of registers.

- Instruction Cache: The instruction cache is a small, high-speed memory that stores frequently used program instructions. It is responsible for quickly fetching instructions that the CPU needs to execute. Caching instructions in this way reduces the time it takes to fetch instructions from the main memory.

- Data Cache: Similar to the instruction cache, the data cache is a high-speed memory that stores frequently accessed data. It is used to speed up the retrieval of data required for executing instructions, such as loading values from memory or writing results back to memory.

- Main Memory: Main memory is the primary storage where both program instructions and data are stored. The data path and control unit work together to transfer data between the main memory and registers in the data path. Main memory is slower than the caches, so efficient memory management is crucial for overall system performance.

3. RISC Processor Instruction Set Examples with explanation (Any 2)

Add (ADD):

Operation: The ADD instruction is used to add the values of two registers.

Example: ADD R1, R2, R3

Explanation: In this example, the values in registers R2 and R3 are added together, and the result is stored in register R1. This instruction is straightforward and aligns with the simplicity and efficiency goals of RISC architectures. It performs a basic arithmetic operation and stores the result.

Load Word (LW):

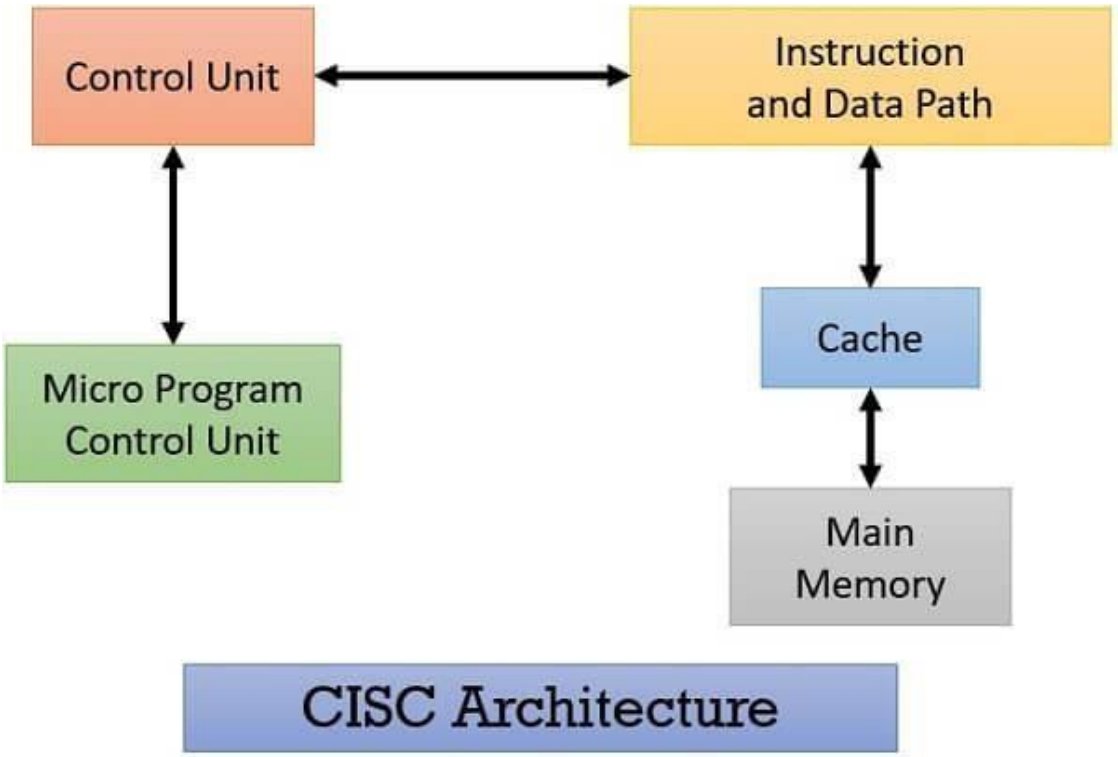
Operation: The LW instruction is used to load a 32-bit word from memory into a register.

Example: LW R4, 100(R5)

Explanation: In this example, the LW instruction loads a 32-bit word from the memory address at offset 100 from the value in register R5. The loaded data is stored in register R4. This instruction is essential for data transfer between memory and registers, a common operation in computing. RISC architectures emphasize simple, load-store instructions like this one to maintain efficiency.

CISC Architecture

1. Diagram of CISC Architecture:



2. Brief Explanation of each component

- You have a special microprogram control unit that uses a series of microinstructions of the microprogram stored in the "control memory" of the microprogram control unit and generates the control signals.
- The control units access the control signals produced by the microprogram control unit & operate the functioning of processors hardware.
- Instruction and data path fetches the opcode and operands of the instructions from the memory.
- Cache and main memory is the location where the program instructions and operands are stored.

3. CISC Processor Instruction Set Examples with explanation (Any 2)

String Move (MOVS):

Operation: The MOVS instruction is used to move a block of data from one memory location to another.

Example: MOVS ECX, DS:[ESI], ES:[EDI]

Explanation: This instruction copies data from the memory location pointed to by the source index register (ESI) to the memory location pointed to by the destination index register (EDI). The ECX register specifies the number of bytes to be moved. CISC processors often feature specialized instructions like MOVS for common operations, which can save on coding effort and execution time.

Multiply (MUL):

Operation: The MUL instruction is used to multiply two values and store the result.

Example: MUL AX, BX

Explanation: This instruction multiplies the values in registers AX and BX and stores the result in AX. CISC processors tend to offer a wide range of instructions, including complex arithmetic instructions like MUL, which can handle more sophisticated operations compared to RISC architectures. This complexity can be useful for reducing the number of instructions required to perform certain tasks.

Post Lab Descriptive Questions

Write a tabular comparative analysis of RISC v/s CISC

CISC	RISC
Emphasis on hardware	Emphasis on software
Multiple instruction sizes and formats	Instructions of same set with few formats
Less registers	Uses more registers
More addressing modes	Fewer addressing modes
Extensive use of microprogramming	Complexity in compiler
Instructions take a varying amount of cycle time	Instructions take one cycle time
Pipelining is difficult	Pipelining is easy

Conclusion: We get an overall view and understanding of RISC and CISC architecture and their differences.

Date: **Signature of faculty in-charge**