Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:		**Batch No:**	**A2**
Faculty Name:	**Dr. Kiran Ajetrao**	**Roll No:**	**16010122041**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 7

Title: Asynchronous Counter

Aim and Objective of the Experiment:

To design and implement 3 bit Asynchronous up counter using JK Flip Flop

COs to be achieved:

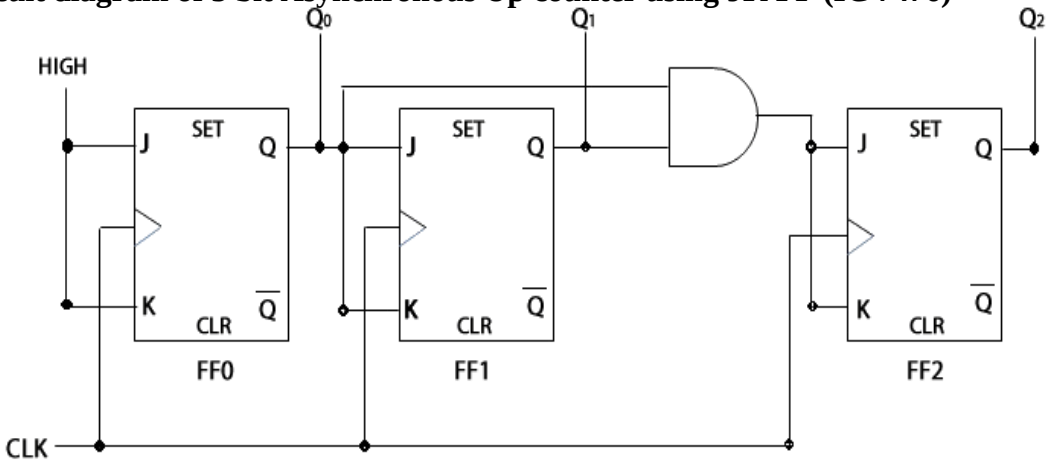
CO3: Design synchronous and asynchronous sequential circuits.

Tools used:

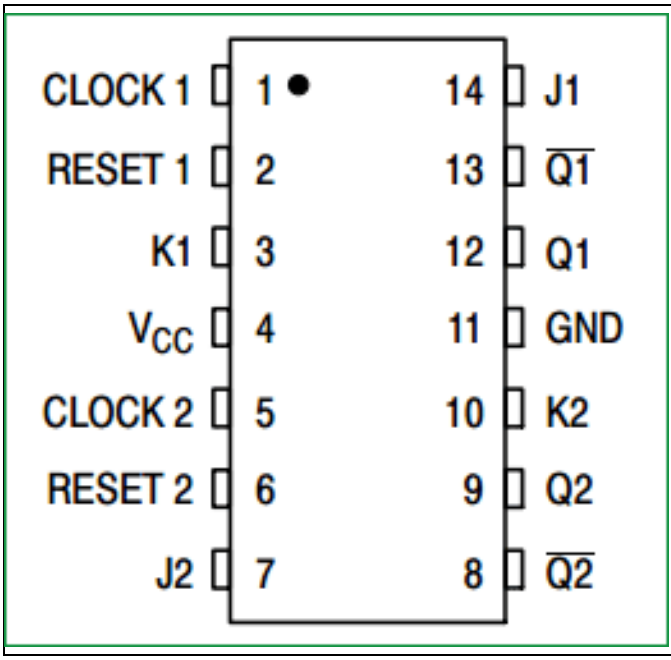
Trainer kits

Theory:

Circuit diagram of 3 bit Asynchronous Up counter using JK FF (IC 7476)



Pin diagram of JK FF (IC 7476)



Implementation Details

Procedure

1) Locate IC 7476 JK FF on Digital trainer kit
2) Apply various inputs to appropriate pins as per the circuit diagram of the 3 bit Asynchronous up counter with reference to the pin configuration of the IC.
3) Make sure of Reset and Clear Pins connections with reference to data sheet information.
4) Connect a pulsar switch to the clock input.
5) Verify the working and prepare a truth table.

Post Lab Subjective/Objective type Questions:

1. **How does JK FF need to be configured to use for counter operation?**

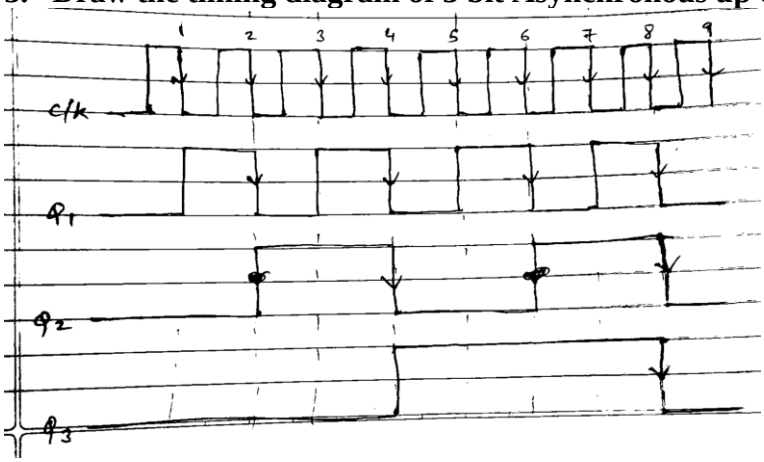
To configure JK flip-flops for counter operation, connect their clock inputs to a shared clock signal, set the initial state, and create feedback loops using the Q outputs to establish the desired counting sequence. For example, in a 3-bit binary counter, connect the Q outputs as needed to count from 000 to 111. This configuration is essential for creating digital counters in various applications.

2. **What changes are required to use the same counter as a 3 bit asynchronous down counter?**

To convert the same counter to a 3-bit asynchronous down counter, provide individual clock inputs for each flip-flop, set the initial state to 111 (the highest count), and reconfigure the

feedback connections for a down-counting sequence. Optionally, use clear or preset inputs to initialize the flip-flops.

3. Draw the timing diagram of 3 bit Asynchronous up counter.



4. What is the mod n concept used in counters?

The "mod n" concept is a fundamental aspect of counter design. It refers to the counting sequence's maximum count value, where "n" represents the modulus or the number of unique states the counter can reach before it resets to zero. For example, in a 4-bit counter, the mod 16 concept means the counter can count from 0 to 15 (16 unique states) before rolling over to zero. This concept helps in determining the counter's maximum count and is crucial for various applications, including binary, decade, or any specific counting sequences.

5. For Mod-5 counter how many JK FFs are required?

For a Mod-5 counter, you would need a minimum of three JK flip-flops to count through all five unique states (0, 1, 2, 3, and 4). Each flip-flop represents one bit on the counter. So, a 3-bit counter, with each bit represented by a JK flip-flop, would be sufficient for counting in a modulo-5 (Mod-5) sequence.

Conclusion:

We learnt the concept of Asynchronous Count and its implementation with IC 7476

Signature of faculty in-charge with Date: