Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**21/08/2023**	**Batch No:**	**A2**
Faculty Name:	**Dr. Kiran Ajetrao**	**Roll No:**	**16010122041**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 4

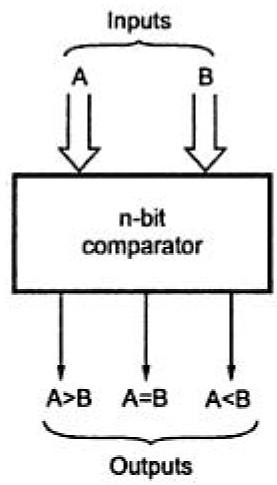
Title: 4-bit magnitude comparator

Aim and Objective of the Experiment:
To design and implement 1-bit comparator using logic gates and verify 4-bit magnitude comparator using IC 7485

COs to be achieved:
CO2: Use different minimization techniques and solve combinational circuits.

Tools used:
Trainer kits

Theory:
Comparator: The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B, A=B (or) A<B.



1-bit Comparator Implementation Details:
Truth Table

A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

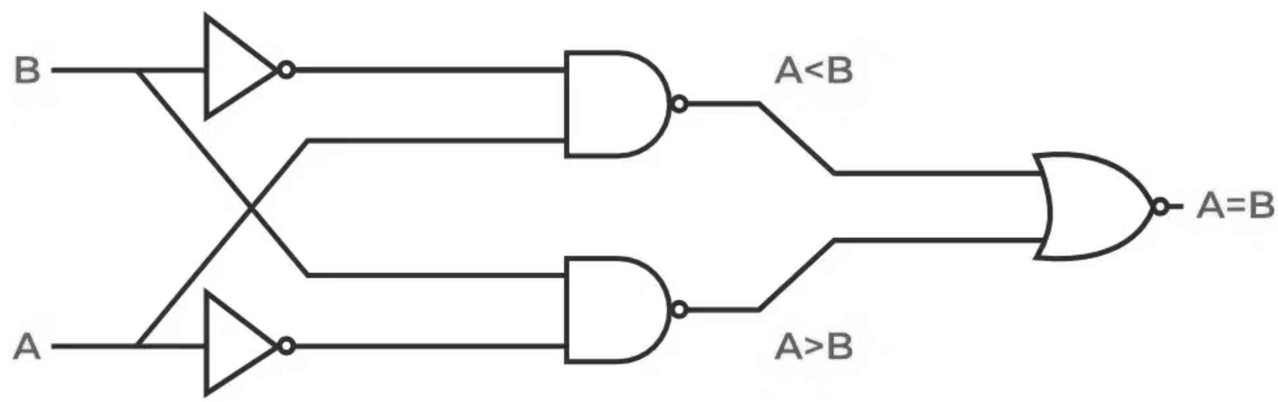
From the Truth Table:

(A<B) = 0, 1, 0 ,0

(A=B)= 1, 0, 0, 1

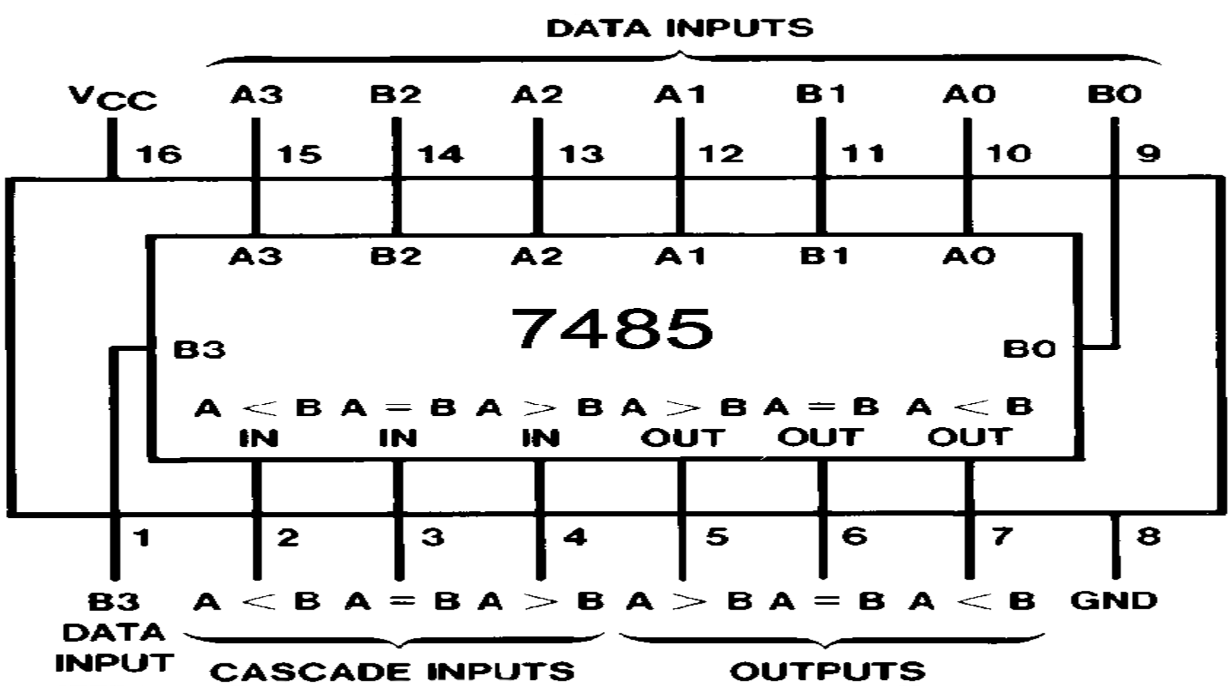
(A>B)= 0, 0, 1, 0

Logic Diagram of 1-bit Comparator

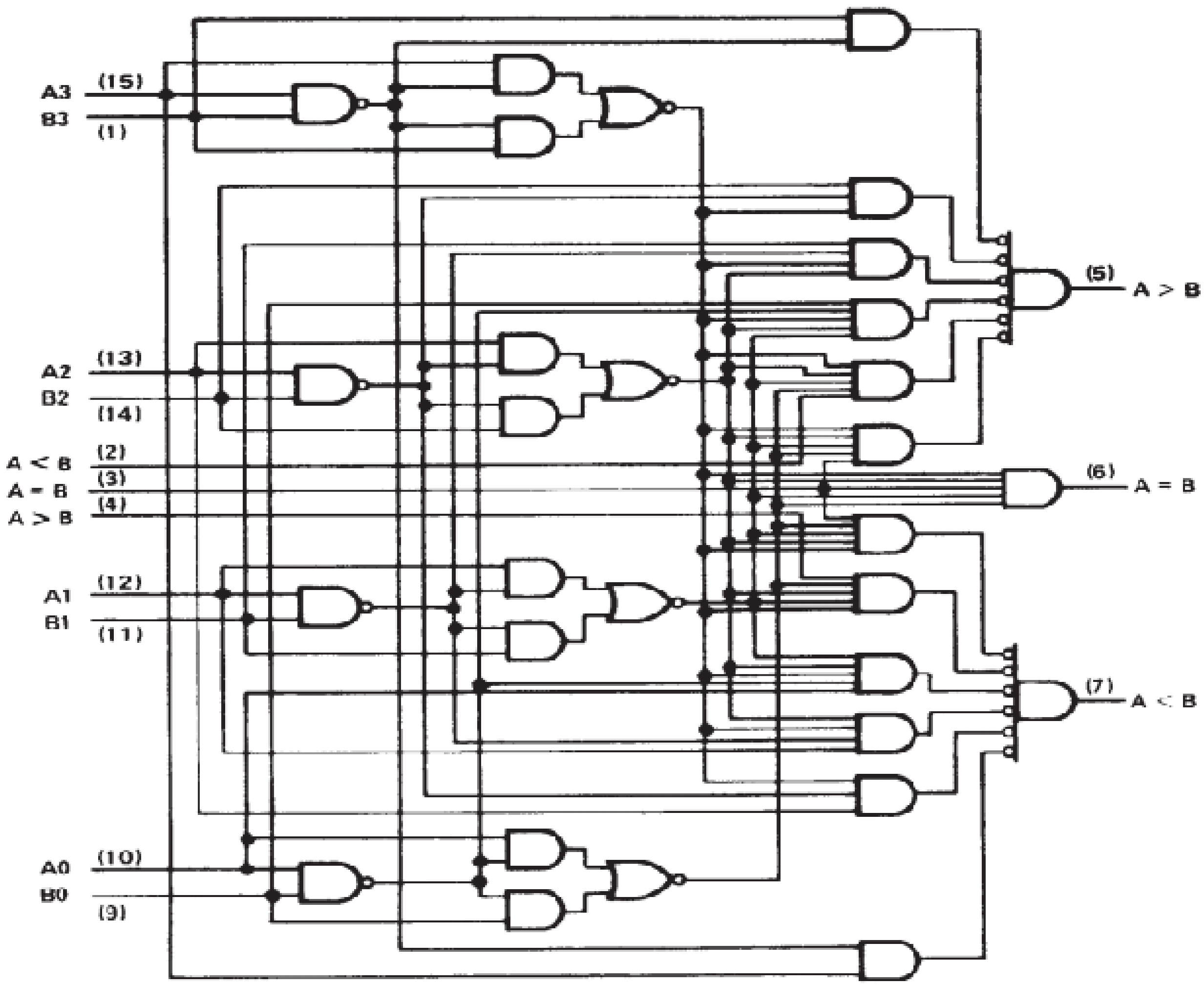


Four Bit Magnitude Comparator Implementation Details

Pin Diagram of IC 7485



Logic Diagram of IC 7485


A3
B3
(15)
(1)
A2
B2
(13)
(14)
A < B
A = B
A > B
(2)
(3)
(4)
A1
B1
(12)
(11)
A0
B0
(10)
(9)
(5)
A > B
(6)
A = B
(7)
A < B

Comparing Table

COMPARING INPUTS				OUTPUT		
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**A > B**	**A < B**	**A = B**
A3 > B3	X	X	X	H	L	L
A3 < B3	X	X	X	L	H	L
A3 = B3	A2 >B2	X	X	H	L	L
A3 = B3	A2 < B2	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H
H = High Voltage Level, L = Low Voltage, Level, X = Don't Care						

Implementation Details

Procedure:

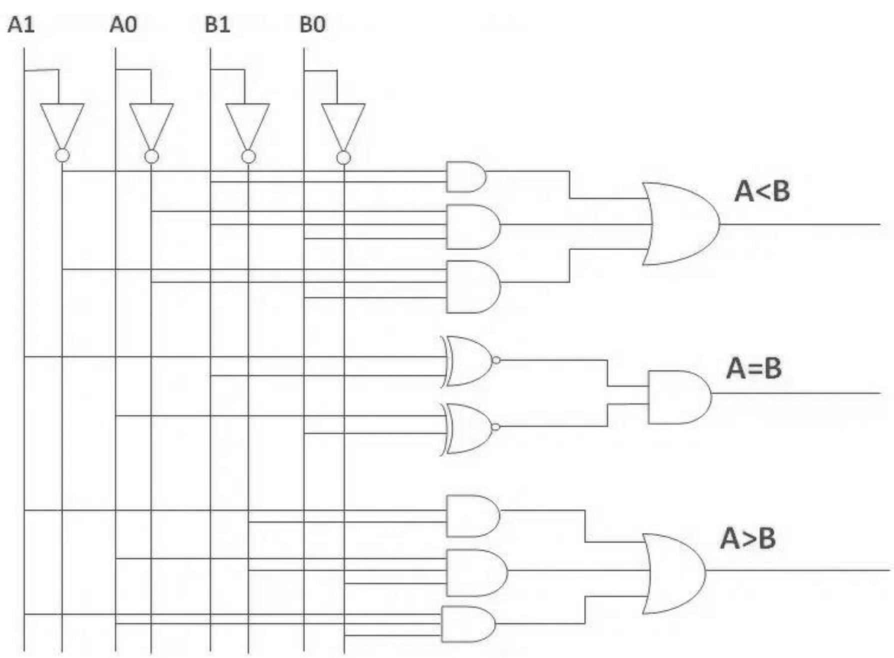
1) Locate the IC 7485 on the trainer kit.
2) Connect 1st input no. to A3-A0 input slot and 2nd to B3-B0.
3) Connect the output $Y_{A>B}$, $Y_{A<B}$ and $Y_{A=B}$ to the output indicators.
4) Switch ON the power supply and monitor the output for various input combinations.

Post Lab Subjective/Objective type Questions:

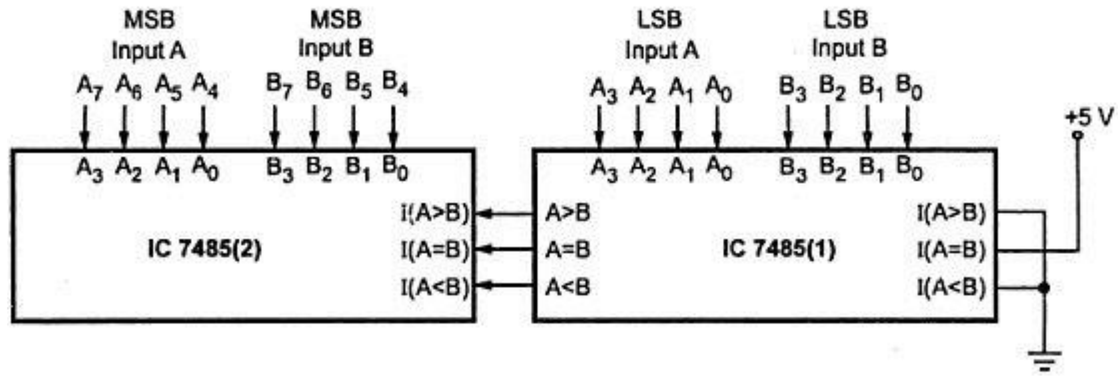
1. Design 2-bit magnitude comparator.

Table 1. Truth Table of 2-Bit Magnitude Comparator

INPUT				OUTPUT		
A1	A0	B1	B0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0



2. How can we implement a 5-bit magnitude comparator using IC 7485.



Conclusion:

In conclusion, this experiment has provided us with a rich and comprehensive experience in the realm of digital design and combinational logic circuits, with a primary focus on designing and implementing a 1-bit comparator using logic gates and verifying the functionality of a 4-bit magnitude comparator using the versatile IC 7485. Throughout this lab, we aimed to gain a deep understanding of comparator design, explore various minimization techniques, and develop problem-solving skills for complex combinational circuits.

The integration of IC 7485 into our experiments was pivotal. This integrated circuit streamlined the verification of our designs and underscored the practical significance of integrated components in digital circuitry. The IC 7485 efficiently handled 4-bit binary comparisons, demonstrating the efficiency and accuracy that integrated circuits bring to complex digital circuits. The lab also introduced us to various minimization techniques, such as Karnaugh maps aka K-maps.

Signature of faculty in-charge with Date: