Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**28 / 8 / 2023**	**Batch No:**	**A2**
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Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 5
Title: Flip Flops

Aim and Objective of the Experiment:
To Verify truth table of JK Flip flop using IC 7476 and study conversion of JK FF to D FF and T FF

COs to be achieved:
CO3: Design synchronous and asynchronous sequential circuits.

Tools used:
Trainer kits

Theory:

Flip-flop is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data.

JK-flip flop: has two inputs, traditionally labeled J and K. IC 7476 is a dual JK master slave flip flop with preset and clear inputs. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge, then the output will toggle from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states.

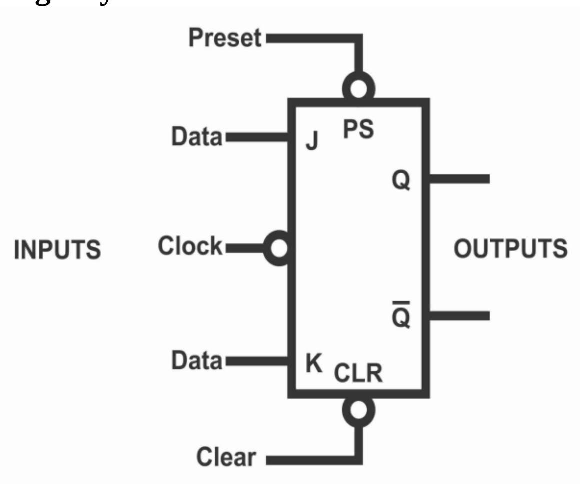
D Flip Flop: tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. D flip-flop can be made from J-K flip-flop by connecting both inputs through a not gate.

T Flip Flop: T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

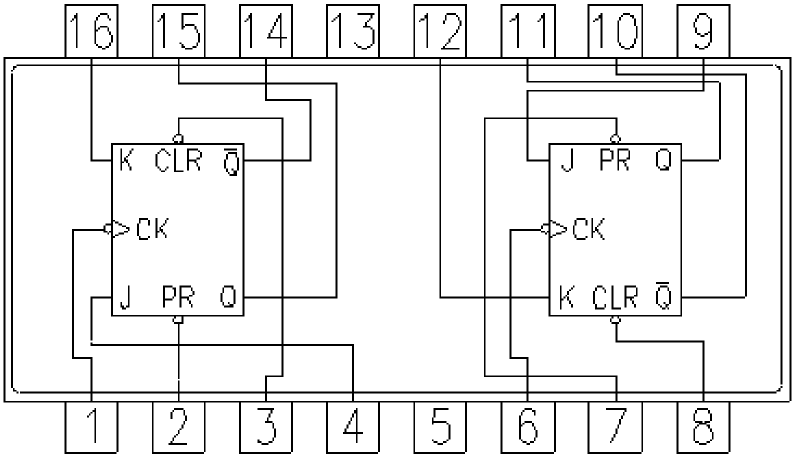
Implementation Details:
Procedure

1) Locate IC 7476 on Digital trainer kit
2) Apply various inputs to J & K pins by means of the output on logic output indicator.
3) Connect a pulsar switch to the clock input.
4) Connect the J&K as D and T flip flop as shown in diagrams and verify the respective truth tables.

Logic Symbol of IC 7476



Pin Diagram of IC 7476



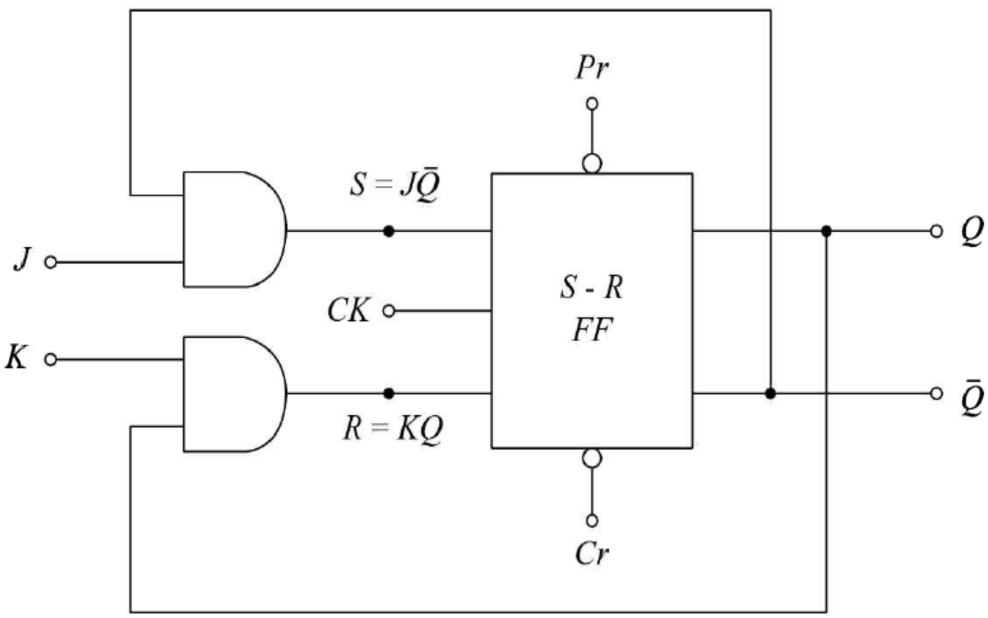


Fig. 7.8 ***An S–R* FLIP-FLOP *Converted into J–K* FLIP-FLOP**

Truth Table of JK FF

Data inputs		Outputs		Inputs to S–R FF		Output
J_n	K_n	Q_n	$\bar{Q}_n$	S_n	R_n	Q_{n+1}
0	0	0	1	0	0	$\left.\begin{matrix}0\\1\end{matrix}\right] = Q_n$
0	0	1	0	0	0	
1	0	0	1	1	0	$\left.\begin{matrix}1\\1\end{matrix}\right] = 1$
1	0	1	0	0	0	
0	1	0	1	0	0	$\left.\begin{matrix}0\\0\end{matrix}\right] = 0$
0	1	1	0	0	1	
1	1	0	1	1	0	$\left.\begin{matrix}1\\0\end{matrix}\right] = \bar{Q}_n$
1	1	1	0	0	1	

Conversion of FFs

1) JK to D FF

Conversion Diagram

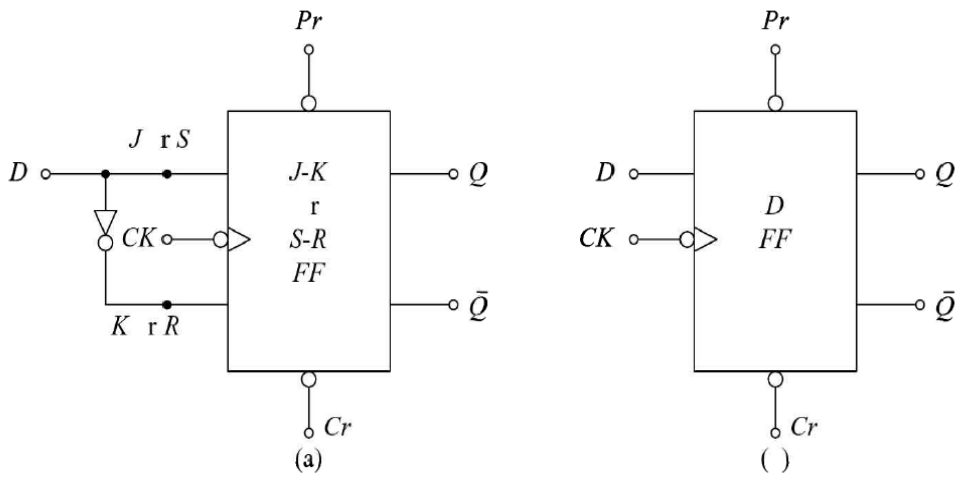


Fig. 7.14 ***(a) A J–K or S–R* FLIP-FLOP *Converted into a D-type* FLIP-FLOP *(b) its Logic Symbol***

Truth Table of D FF

Input	Output
D_n	Q_{n+1}
0	0
1	1

2) JK to T FF

Conversion Diagram

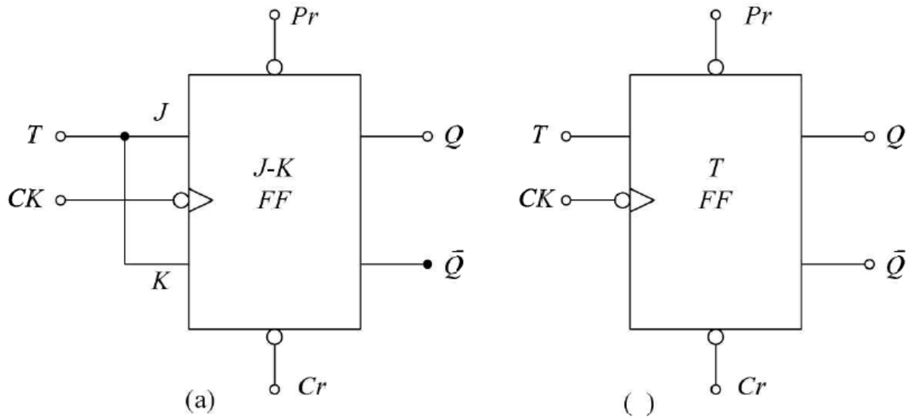


Fig. 7.15 ***(a) A J–K* FLIP-FLOP *Converted into a T-type* FLIP-FLOP *(b) its Logic Symbol***

Truth Table of T FF

Input T_n	Output Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

Implementation Details

Procedure:

1) Locate the IC 7476 and place the IC on trainer kit.
2) Connect VCC and ground to respective pins of IC trainer kit.
3) Implement the circuit as shown in the circuit diagram.
4) Connect the inputs to the input switches provided in the trainer kit.
5) Connect the outputs to the switches of O/P LEDs
6) Apply various combinations of inputs according to the truth table and observe the condition of LEDs.
7) Note down the corresponding output readings for various combinations of inputs.

Post Lab Subjective/Objective type Questions:

How does a JK flip-flop differ from an SR flip-flop in its basic operation?

Input Signals:
- SR Flip-Flop: The SR (Set-Reset) flip-flop has two inputs: S (Set) and R (Reset). It can be in one of four states: S=0, R=0 (no change), S=1, R=0 (set to 1), S=0, R=1 (reset to 0), and S=1, R=1 (undefined behavior or toggle, depending on the implementation).
- JK Flip-Flop: The JK flip-flop has two inputs: J (set) and K (reset). It can be in one of two states: J=0, K=0 (no change), and J=1, K=0 (set to 1), J=0, K=1 (reset to 0), and J=1, K=1 (toggle).

Operation:
- SR Flip-Flop: The SR flip-flop is sensitive to both the S and R inputs. When both S and R are set to 0, the output remains in its previous state. When S is set to 1 and R is set to 0, it sets the output to 1, and when R is set to 1 and S is set to 0, it resets the output to 0. When both S and R are set to 1, it may lead to unstable behavior or toggling, which is typically avoided in practical designs.
- JK Flip-Flop: The JK flip-flop is more versatile and can be used for various purposes. When J and K are both set to 0, it holds its previous state. When J is set to 1 and K is set to 0, it sets the output to 1, and when K is set to 1 and J is set to 0, it resets the output to 0. When both J and K are set to 1, it toggles the output, which means it switches the output state to its complement.

Race Condition Avoidance:
- SR Flip-Flop: SR flip-flops can suffer from race conditions when both S and R inputs change simultaneously, potentially leading to unpredictable behavior.
- JK Flip-Flop: JK flip-flops can be designed to avoid race conditions because of their toggle functionality. When both J and K inputs are set to 1, the flip-flop toggles, ensuring stable operation.

In summary, while both JK and SR flip-flops can be used for similar tasks in digital circuits, JK flip-flops offer more predictable behavior and are often preferred in practical designs due to their ability to toggle and their potential for avoiding race conditions when properly implemented.

1. What is the use of characteristic and excitation tables?

Characteristic Tables:
Characteristic tables, also known as truth tables for flip-flops, are used to describe the relationship between the inputs and the corresponding outputs of a flip-flop or sequential circuit.
These tables list all possible input combinations and show the corresponding output states of the flip-flop or circuit. The outputs are typically represented as the next state (Q_next) and the current state (Q), making it easy to understand how the flip-flop responds to different inputs.
Use Cases: Characteristic tables are essential for analyzing the behavior of flip-flops and

sequential circuits, especially when you want to determine how different input conditions affect the current and next states of the circuit. They are useful for design verification and debugging.

Excitation Tables:
Excitation tables provide a different perspective by focusing on the inputs required to produce a desired next state transition in a flip-flop or sequential circuit.
These tables specify the required present state (Q) and input conditions to achieve a particular next state (Q_next). It lists all possible Q and Q_next combinations and the corresponding input conditions (usually D or JK inputs for flip-flops) that would lead to the desired transition.
Excitation tables are particularly useful during the design and analysis of flip-flops and sequential circuits. They help determine how to set the inputs to achieve a specific state change or sequence, ensuring that the circuit functions as intended. They are essential for implementing finite state machines and designing control logic.

2. How many flip flops do you require storing the data 1101?
   To store the binary data "1101," you would need four flip-flops, one for each bit in the data. Each flip-flop can store one bit of information. Each flip-flop represents one of the binary digits in the sequence.

Conclusion:

By working with the IC 7476 JK flip-flop, we were able to validate its truth table, which details the relationship between its inputs (J and K) and outputs (Q and Q-bar). This hands-on experience helped us understand the behavior of the JK flip-flop and its various operational modes, including Set, Reset, Toggle, and No-Change.

We also delved into the conversion of the JK flip-flop to the D flip-flop and the T flip-flop, which are essential concepts in digital electronics. These conversions allowed us to explore how different flip-flops can be used to achieve specific functionality and how they can be interchanged while preserving the core behavior of the circuit.

Signature of faculty in-charge with Date: