| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| --- | --- | --- | --- |
| **Date of Performance:** | **23/ 10/2023** | **Batch No:** | **A2** |
| **Faculty Name:** |  | **Roll No:** |  |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 8**

**Title: 1-bit adder on VHDL**

| **Aim and Objective of the Experiment:** |
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| To implement 1-bit adder on VHDL |

| **COs to be achieved:** |
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| **CO4**: Implement digital networks using VHDL |

| **Tools used:** |
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| Quartus, ModelSim |

| **Theory:** |
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| A 1-bit adder, a fundamental component of digital circuits, performs binary addition of two 1-bit numbers. It utilizes logic gates to generate the sum and carry-out outputs. A half-adder adds two bits without considering the carry from the previous stage, while a full-adder accounts for the carry input.  Using VHDL, a hardware description language, the 1-bit adder can be designed as a combinational circuit. VHDL facilitates the creation of a structural and behavioral description of the adder. In practice, this simple unit serves as a building block for constructing larger multi-bit adders, enabling arithmetic operations in microprocessors and digital systems. |

| **Implementation Details** |
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| **Screenshots:** |
| **Post Lab Subjective/Objective type Questions:** |
| 1. How can 1-bit adder be used to implement a 4-bit adder? 2. What is VHDL used for? |

| **Conclusion:** |
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| **Signature of faculty in-charge with Date:** |
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