Rohit Dureja, PhD

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EDUCATION

Ph.D. Computer Science, Iowa State University, USA — 2016–2020
Thesis: Model Checking Large Design Spaces: Theory, Tools, and Experiments

M.S.E. Embedded Systems, University of Pennsylvania, USA — 2013–2015

B.E. Instrumentation and Control, University of Delhi, India — 2009–2013

EXPERIENCE

Research and Development Engineer, *Full-time*, IBM, Austin, TX — Aug 2020 – present
Formal Verification Algorithms and Tools
1. Develop algorithms and tools to improve formal verification scalability on complex hardware designs.
2. Benchmark and evaluate performance of state-of-the-art verification algorithms and software.
3. Improve the orchestration, and automation of formal verification algorithms and tools.

Graduate Research Assistant, *Part-time*, Iowa State University — Aug 2015 – Aug 2020
Symbolic Model Checking of Large Design Spaces
1. Designing algorithms for checking "sets" of models and properties, and
2. Developing novel extensions to the NuSMV model checker, and new model-set checkers.

Research and Development Engineer, *Internship*, IBM, Austin, TX — Sep 2019 – Aug 2020
Sequential Equivalence Checking and Abstraction
1. Develop techniques for equivalence checking by efficient multi-property abstraction, and
2. Design algorithms for parallel orchestration in sequential equivalence checking.

Formal Verification Engineer, *Internship*, Apple, Cupertino, CA — May 2019 – Aug 2019
Formal Verification of SoC Designs
1. Formally verified critical cryptography hardware designs in Apple SoCs, and
2. Performed equivalence checking between Haskell-generated C code and Verilog RTL.

Research and Development Engineer, *Internship*, IBM, Austin, TX — Aug 2018 – May 2019
Formal Verification of Multi-Property Testbenches
1. Developed techniques to group and partition properties for formal verification, and
2. Improved multiple property verification support in IBM's model checker.

Formal Verification Engineer, *Internship*, Apple, Cupertino, CA — May 2018 – Aug 2018
Software Verification and Theorem Proving
1. Formally verified C code using Isabelle/HOL theorem prover, and
2. Developed a custom SMT tactic for word-level and non-linear integer arithmetic.

Researcher, *Internship*, Fondazione Bruno Kessler, Trento, Italy — May 2015 – Aug 2015
Formal Verification of NextGen Air Traffic Controller
1. Added extensions to include asymmetric information sharing between aircraft,
2. Developed a contract-based design case-study of a sample railroad system, and
3. Analyzed extraction of SMV models from LLVM bitcode and control flow graphs.

Embedded Systems Programmer, *Part-time*, University of Pennsylvania — Jan 2014 – Apr 2015
Wireless and Invasive Brain-Computer Interfaces
1. Designed a wireless brain-sensor interface system to control prosthetics, and
2. Researched the use of compressive sensing and learning to minimize data outflow.

Hardware Designer, *Internship*, Texas Instruments, New Delhi, India   Dec 2011 – Apr 2013
ARM-based Microcontroller Development Platforms
1. Responsible for complete hardware/software design of ARM-based learning kits,
2. Commercially launched two learning kits, Stellaris Guru and Stellaris Shuru, and
3. Composed pedagogy materials and co-authored an undergraduate lab manual.

PUBLICATIONS *Peer-Reviewed Conferences*

C1 Rohit Dureja, Arie Gurfinkel, Alexander Ivrii, and Yakir Vizel. IC3 with Internal Signals. In *Proceedings of Formal Methods in Computer-Aided Design (FMCAD)*, New Haven, Connecticut, USA, October 2021. IEEE/ACM

C2 Rohit Dureja, Jason Baumgartner, Robert Kanzelman, Mark Williams, and Kristin Y. Rozier. Accelerating Parallel Verification via Complementary Property Partitioning and Strategy Exploration. In *Proceedings of Formal Methods in Computer-Aided Design (FMCAD)*, Haifa, Israel, September 2020. IEEE/ACM

C3 Rohit Dureja, Jason Baumgartner, Alexander Ivrii, Robert Kanzelman, and Kristin Y. Rozier. Boosting Verification Scalability via Structural Grouping and Semantic Partitioning of Properties. In *Proceedings of Formal Methods in Computer-Aided Design (FMCAD)*, San Jose, California, USA, October 2019. IEEE/ACM

C4 Rohit Dureja, Jianwen Li, Geguang Pu, Moshe Y. Vardi, and Kristin Y. Rozier. Intersection and Rotation of Assumption Literals Boosts Bug-Finding. In *Proceedings of Verified Software: Theories, Tools, and Experiments (VSTTE)*, New York, USA, July 2019. Springer, Cham

C5 Jianwen Li, Rohit Dureja, Geguang Pu, Kristin Y. Rozier, and Moshe Y. Vardi. SimpleCAR: An Efficient Bug-Finding Tool Based On Approximate Reachability. In *Proceedings of Computer Aided Verification (CAV)*, Oxford, United Kingdom, July 2018. Springer, Cham

C6 Rohit Dureja and Kristin Y. Rozier. More Scalable LTL Model Checking via Discovering Design-Space Dependencies (D^3). In *Proceedings of Tools and Algorithms for the Construction and Analysis of Systems (TACAS)"*, Thessaloniki, Greece, April 2018. Springer, Cham

C7 Rohit Dureja and Kristin Y. Rozier. FuseIC3: An Algorithm for Checking Large Design Spaces. In *Proceedings of Formal Methods in Computer-Aided Design (FMCAD)*, Vienna, Austria, October 2017. IEEE/ACM

C8 Rohit Dureja, Eric W. D. Rozier, and Kristin Y. Rozier. A Case Study in Safety, Security, and Availability of Wireless-Enabled Aircraft Communication Networks. In *Proceedings of AIAA Aviation Technology, Integration, and Operations Conference (AVIATION)*, Denver, Colorado, USA, June 2017. AIAA

C9 Pei Zhang, Rohit Dureja, Matthew Cauwels, Philip Jones, Joseph Zambreno, and Kristin Y. Rozier. Model Predictive Runtime Verification for Embedded Platforms with Real-Time Deadlines. (under submission)

Journals

J10 Rohit Dureja and Kristin Y. Rozier. Incremental Design-Space Model Checking via Resuable Reachable State Approximations. *Formal Methods in System Design*, (to appear)

J11 Rohit Dureja and Kristin Yvonne Rozier. Formal framework for safety, security, and availability of aircraft communication networks. *Journal of Aerospace Information Systems*, 17(7):322–335, 2020

Patents

P12 Rohit Dureja, Jason Baumgartner, Alexander Ivrii, and Robert Kanzelman. *Grouping and Partitioning of Properties for Logic Verification*. U.S. Patent 10,789,403

Miscellaneous

M13 Rohit Dureja and Kristin Y. Rozier. Scalable Verification of Designs with Multiple Properties. In *Formal Methods in Computer-Aided Design (FMCAD) Student Forum*, San Jose, California, USA, October 2019

M14 Rohit Dureja and Kristin Y. Rozier. From One to Many: Checking A Set of Models. In *Formal Methods in Computer-Aided Design (FMCAD) Student Forum*, Vienna, Austria, October 2017

M15 Rohit Dureja and Kristin Y. Rozier. Comparative Safety Analysis of Wireless Communication Networks in Avionics. In *Formal Methods in Computer-Aided Design (FMCAD) Student Forum*, Mountain View, California, USA, October 2016

Books and Book Chapters

B16 Dhananjay V. Gadre, Rohit Dureja, and Shanjit S. Jajmann. *Getting Started with Stellaris ARM Cortex-M Embedded Processors*. Number 8173718814. Universities Press, 1st edition edition, 2013

Theses

T17 Rohit Dureja. *Model Checking Large Design Spaces: Theory, Tools, and Experiments*. Ph.D. Thesis, Iowa State University, 2020

AWARDS AND
HONORS
- Research Excellence Award by Iowa State University 2019.
- Best Student Contribution Award at Formal Methods in Computer-Aided Design (FMCAD) 2019.
- National Science Foundation travel grant to Verification Mentoring Workshop (VMW) and Computer Aided Verification (CAV) Conference 2016, 2018.
- Travel grant to Formal Methods in Computer-Aided Design (FMCAD) Conference 2016, 2017, 2019.
- Travel grant and registration waiver to Marktoberdorf Summer School 2016.
- Carnegie Mellon University travel grant to CPS V&V Workshop 2016.
- National Science Foundation travel grant to CPS Week 2016.
- *Best Design* and *Top 10 hack* at HackPrinceton 2013.
- University of Delhi academic scholarship, 2009–2013.

PROFESSIONAL
SERVICE
Artifact Evaluation Committee:
- Tools and Algorithms for Construction and Analysis of Systems (TACAS) 2018

Conference Review:
- Foundation of Software Engineering (FSE) 2021
- Computer-Aided Verification (CAV) 2021, 2020
- NASA Formal Methods Symposium (NFM) 2021, 2019, 2018, 2016
- Autonomous Agents and Multi-agent Systems (AAMAS) 2021
- International Colloquium on Theoretical Aspects of Computing (ICTAC) 2020
- Automated Software Engineering (ASE) 2020
- Tools and Algorithms for Construction and Analysis of Systems (TACAS) 2020, 2018, 2017
- Quantitative Evaluation of SysTems (QEST) 2019
- International Conference on Cyber-Physical Systems (ICCPS) 2019
- Design, Automation, and Test in Europe (DATE) Conference 2019

Journal Review:
- Innovations in Systems and Software Engineering (ISSE)
- Journal of Aerospace Information Systems (JAIS)

Grant Proposal Review:
- Semiconductor Research Corporation (SRC) Computer-Aided Design annd Test (CADT)

TECHNICAL PRESENTATIONS	• "Grouping and Partitioning of Properties for Formal Verification", IBM, Austin, TX, May 7, 2019.
	• "Formal Verification of Designs with Multiple Properties", IBM, Austin, TX, December 19, 2018.
	• "Theoretical Foundations of the UAS in the NAS Problem." *Lightning Talk*, NSF CPS PI Meeting, Washington, DC, November 15, 2018.
	• "Design-Space Analysis via SAT-based Model Checking." *Guest Lecture*, COMS 512 - Formal Methods in Software Engineering, Iowa State University, Ames, IA, February 20–22, 2018.
	• "Scalable Design Space Analysis for Future Traffic Management." CPS Challenges for Unmanned and Autonomous Systems Workshop, Washington, DC, November 14, 2017.
	• "Making Undecidable Problems Decidable in Practice." Software Engineering Seminar, Department of Computer Science, Iowa State University, Ames, IA, October 12, 2017.

SELECTED COURSE PROJECTS	• *UAV Security Exploit.* Designed a one-click man-in-the-middle (MITM) attack with ARP poisoning to acquire unauthenticated control of a drone.
	• *Modeling and Verification of a Pacemaker.* Modeled a pacemaker using UPPAAL and synthesized code to run on a 32-bit ARM microcontroller.
	• *Veterinary Patient Records.* Gathered requirements for a patient record system; culminated in a complete requirements specification document, and a prototype.
	• *Network Sniffer.* Designed a powerful network packet sniffer capable of collecting socket-connection information and data, SMTP messages and profile connections.
	• *Viral Marketing.* Experimentally evaluated the correlation between social network and spread of influence models to maximize information spread.
	• *US Presidential Elections.* Designed a predictor model to predict popular vote and electoral college winner of 2016 US presidential elections.

EXTERNAL TRAINING	• Marktoberdorf School on Dependable Software Systems Engineering, 2016.
	• SRI International Sixth Summer School on Formal Techniques, 2016
	• RiSE & LogiCS Spring School on Logic and Verification, 2016

REFERENCES	Available upon request.