

EDUCATION	<i>Ph.D. Computer Science</i> , Iowa State University, USA	2016– ongoing
	<i>M.S.E. Embedded Systems</i> , University of Pennsylvania	2013–2015
	<i>B.E. Instrumentation and Control</i> , University of Delhi, India	2009–2013
EXPERIENCE	Graduate Research Assistant , Iowa State University <i>Symbolic Model Checking of Large Design Spaces</i> Mentor: Kristin Yvonne Rozier	Aug 2015 – present
	1. Designing algorithms for checking “sets” of models and properties, and 2. Developing novel extensions to the NuSMV model checker, and new model-set checkers.	
	Research Intern , IBM, Austin, TX <i>Equivalence Checking and Abstraction</i> Mentors: Jason Baumgartner and Alexander Ivrii	Sep 2019 – present
	1. Develop techniques for equivalence checking by efficient multi-property abstraction, and 2. Design algorithms for parallel orchestration in sequential equivalence checking.	
	Formal Verification Engineer Intern , Apple, Cupertino, CA <i>Formal Verification of SoC Designs</i> Mentor: Tim Pruss	May 2019 – Aug 2019
	1. Formally verified critical cryptography hardware designs in Apple SoCs, and 2. Performed equivalence checking between Haskell-generated C code and Verilog RTL.	
	Research Intern , IBM, Austin, TX <i>Formal Verification of Multi-Property Testbenches</i> Mentors: Jason Baumgartner and Alexander Ivrii	Aug 2018 – May 2019
	1. Developed techniques to group and partition properties for formal verification, and 2. Improved multiple property verification support in IBM’s model checker.	
	Formal Verification Engineer Intern , Apple, Cupertino, CA <i>Software Verification and Theorem Proving</i> Mentor: John Matthews	May 2018 – Aug 2018
	1. Formally verified C code using Isabelle/HOL theorem prover, and 2. Developed a custom SMT tactic for word-level and non-linear integer arithmetic.	
	Summer Intern , Fondazione Bruno Kessler, Trento, Italy <i>Formal Verification of NextGen Air Traffic Controller</i> Mentor: Alessandro Cimatti	May 2015 – Aug 2015
	1. Added extensions to include asymmetric information sharing between aircraft, 2. Developed a contract-based design case-study of a sample railroad system, and 3. Analyzed extraction of SMV models from LLVM bitcode and control flow graphs.	
	Embedded Systems Programmer , University of Pennsylvania <i>Wireless and Invasive Brain-Computer Interfaces</i> Mentor: Jan Van der Spiegel	Jan 2014 – Apr 2015
	1. Designed a wireless brain-sensor interface system to control prosthetics, and 2. Researched the use of compressive sensing and learning to minimize data outflow.	

1. Responsible for complete hardware/software design of ARM-based learning kits,
2. Commercially launched two learning kits, Stellaris Guru and Stellaris Shuru, and
3. Composed pedagogy materials and co-authored an undergraduate lab manual.

PUBLICATIONS *Peer-Reviewed Conferences*

- C1 Rohit Dureja, Jason Baumgartner, Alexander Ivrii, Robert Kanzelman, and Kristin Y. Rozier. Boosting Verification Scalability via Structural Grouping and Semantic Partitioning of Properties. In *Proceedings of Formal Methods in Computer-Aided Design (FMCAD)*, San Jose, California, USA, October 2019. IEEE/ACM
- C2 Rohit Dureja, Jianwen Li, Geguang Pu, Moshe Y. Vardi, and Kristin Y. Rozier. Intersection and Rotation of Assumption Literals Boosts Bug-Finding. In *Proceedings of Verified Software: Theories, Tools, and Experiments (VSTTE)*, New York, USA, July 2019. Springer, Cham
- C3 Jianwen Li, Rohit Dureja, Geguang Pu, Kristin Y. Rozier, and Moshe Y. Vardi. SimpleCAR: An Efficient Bug-Finding Tool Based On Approximate Reachability. In *Proceedings of Computer Aided Verification (CAV)*, Oxford, United Kingdom, July 2018. Springer, Cham
- C4 Rohit Dureja and Kristin Y. Rozier. More Scalable LTL Model Checking via Discovering Design-Space Dependencies (D^3). In *Proceedings of Tools and Algorithms for the Construction and Analysis of Systems (TACAS)*, Thessaloniki, Greece, April 2018. Springer, Cham
- C5 Rohit Dureja and Kristin Y. Rozier. FuseIC3: An Algorithm for Checking Large Design Spaces. In *Proceedings of Formal Methods in Computer-Aided Design (FMCAD)*, Vienna, Austria, October 2017. IEEE/ACM. Talk video: <https://goo.gl/Gs92G2>
- C6 Pei Zhang, Rohit Dureja, Matthew Cauwels, Philip Jones, Joseph Zambreno, and Kristin Y. Rozier. Model predictive runtime verification for embedded platforms with real-time deadlines. (under submission)
- C7 Rohit Dureja, Jason Baumgartner, Raj Kumar Gajavelly, Robert Kanzelman, and Kristin Y. Rozier. Scalable property grouping and partitioning for efficient sequential redundancy removal. (under submission)

Journals

- J8 Rohit Dureja and Kristin Y. Rozier. A Case Study in Safety, Security, and Availability of Wireless-Enabled Aircraft Communication Networks. *AIAA Journal of Aerospace Information Systems (JAIS)*, (to appear), 2020
- J9 Rohit Dureja and Kristin Y. Rozier. Incremental Design-Space Model Checking via Resuable Reachable State Approximations. (under submission)
- J10 Dhananjay V. Gadre and Rohit Dureja. An Inexpensive Approach to Integrate Physical Computing Curriculum in the Classroom. (in preparation)

Patents

- P11 Rohit Dureja, Jason Baumgartner, Alexander Ivrii, and Robert Kanzelman. *Grouping and Partitioning of Properties for Logic Verification*. U.S. Patent Application 16/411193 (Pending)

Miscellaneous

- M12 Rohit Dureja and Kristin Y. Rozier. Scalable Verification of Designs with Multiple Properties. In *Formal Methods in Computer-Aided Design (FMCAD) Student Forum*, San Jose, California, USA, October 2019
- M13 Rohit Dureja and Kristin Y. Rozier. From One to Many: Checking A Set of Models. In *Formal Methods in Computer-Aided Design (FMCAD) Student Forum*, Vienna, Austria, October 2017
- M14 Rohit Dureja, Eric W. D. Rozier, and Kristin Y. Rozier. A Case Study in Safety, Security, and Availability of Wireless-Enabled Aircraft Communication Networks. In *Proceedings of AIAA Aviation*

Technology, Integration, and Operations Conference (AVIATION), Denver, Colorado, USA, June 2017. AIAA

M15 Rohit Dureja and Kristin Y. Rozier. Comparative Safety Analysis of Wireless Communication Networks in Avionics. In *Formal Methods in Computer-Aided Design (FMCAD) Student Forum*, Mountain View, California, USA, October 2016

Books and Book Chapters

B16 Dhananjay V. Gadre, Rohit Dureja, and Shanjit S. Jajmann. *Getting Started with Stellaris ARM Cortex-M Embedded Processors*. Universities Press, 2013

AWARDS AND
HONORS

- Research Excellence Award by Iowa State University 2019.
- Best Student Contribution Award at Formal Methods in Computer-Aided Design (FMCAD) 2019.
- National Science Foundation travel grant to Verification Mentoring Workshop (VMW) and Computer Aided Verification (CAV) Conference 2016, 2018.
- Travel grant to Formal Methods in Computer-Aided Design (FMCAD) Conference 2016, 2017, 2019.
- Travel grant and registration waiver to Marktoberdorf Summer School 2016.
- Carnegie Mellon University travel grant to CPS V&V Workshop 2016.
- National Science Foundation travel grant to CPS Week 2016.
- *Best Design* and *Top 10 hack* at HackPrinceton 2013.
- University of Delhi academic scholarship, 2009–2013.

TECHNICAL
PRESENTATIONS

- “Grouping and Partitioning of Properties for Formal Verification”, IBM, Austin, TX, May 7, 2019.
- “Formal Verification of Designs with Multiple Properties”, IBM, Austin, TX, December 19, 2018.
- “Theoretical Foundations of the UAS in the NAS Problem.” *Lightning Talk*, NSF CPS PI Meeting, Washington, DC, November 15, 2018.
- “Design-Space Analysis via SAT-based Model Checking.” *Guest Lecture*, COMS 512 - Formal Methods in Software Engineering, Iowa State University, Ames, IA, February 20–22, 2018.
- “Scalable Design Space Analysis for Future Traffic Management.” CPS Challenges for Unmanned and Autonomous Systems Workshop, Washington, DC, November 14, 2017.
- “Making Undecidable Problems Decidable in Practice.” Software Engineering Seminar, Department of Computer Science, Iowa State University, Ames, IA, October 12, 2017.

PROFESSIONAL SERVICE *Artifact Evaluation Committee:*

- Tools and Algorithms for Construction and Analysis of Systems (TACAS) 2018

Conference Review:

- Computer-Aided Verification (CAV) 2020
- Quantitative Evaluation of SysTems (QEST) 2019
- International Conference on Cyber-Physical Systems (ICCPs) 2019
- Design, Automation, and Test in Europe (DATE) Conference 2019
- NASA Formal Methods Symposium (NFM) 2019, 2018, 2016
- Tools and Algorithms for Construction and Analysis of Systems (TACAS) 2020, 2018, 2017

Journal Review:

- Innovations in Systems and Software Engineering (ISSE)
- Journal of Aerospace Information Systems (JAIS)

SELECTED
COURSE
PROJECTS

- *UAV Security Exploit*. Designed a one-click man-in-the-middle (MITM) attack with ARP poisoning to acquire unauthenticated control of a drone.
- *Modeling and Verification of a Pacemaker*. Modeled a pacemaker using UPPAAL and synthesized code to run on a 32-bit ARM microcontroller.
- *Veterinary Patient Records*. Gathered requirements for a patient record system; culminated in a complete requirements specification document, and a prototype.
- *Network Sniffer*. Designed a powerful network packet sniffer capable of collecting socket-connection information and data, SMTP messages and profile connections.
- *Viral Marketing*. Experimentally evaluated the correlation between social network and spread of influence models to maximize information spread.
- *US Presidential Elections*. Designed a predictor model to predict popular vote and electoral college winner of 2016 US presidential elections.

EXTERNAL
TRAINING

- Marktoberdorf School on Dependable Software Systems Engineering, 2016.
- SRI International Sixth Summer School on Formal Techniques, 2016
- RiSE & LogiCS Spring School on Logic and Verification, 2016