Rohit Dureja

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EDUCATION

Ph.D. Computer Science, Iowa State University, 2016– present

M.S.E. Embedded Systems, University of Pennsylvania, 2013–2015

B.E. Instrumentation and Control, University of Delhi, 2009–2013

EXPERIENCE

Graduate Research Assistant Aug 2015 – present
Laboratory for Temporal Logic, Iowa State University

1. Design of tools & techniques for checking sets of system models, using
   (a) graph-theoretic and SMT techniques to reduce order of model sets,
   (b) preprocessing scripts and novel extensions to the NuSMV model checker, and design of new model-set checkers.
2. Formally verified migration of hardware-based systems to software-based systems.
3. Developing an intermediate language for modeling language translation.

Research Intern May 2015 – Aug 2015
Fondazione Bruno Kessler, Trento, Italy

1. Formal verification of NASA NextGen air traffic controller.
   (a) Added extensions to include asymmetric information sharing between aircraft.
2. Developed a contract-based design case-study of a sample railroad system.
3. Analyzed extraction of SMV models from LLVM bitcode and control flow graphs.

Embedded Systems Programmer Jan 2014 – Apr 2015
Center for Sensor Technologies, University of Pennsylvania

1. Designed a wireless brain-sensor interface system to control prosthetics.
2. Researched the use of compressive sensing and learning to minimize data outflow.

Undergraduate Intern Dec 2011 – Apr 2013
Texas Instruments, New Delhi, India

1. Responsible for complete hardware/software design of ARM-based learning kits.
2. Wrote CMSIS compliant low-level systems programs and bootloaders.
3. Commercially launched two learning kits, Stellaris Guru and Stellaris Shuru.

PUBLICATIONS

Peer-Reviewed Conferences

C1 Rohit Dureja and Kristin Y. Rozier. "Combinatorial Model Checking Reduction" (under submission).

C2 Rohit Dureja and Kristin Y. Rozier. "FuseIC3: An Algorithm for Checking Large Design Spaces" (under submission).

Miscellanea

M3 Rohit Dureja, Eric Rozier and Kristin Y. Rozier. "A Case Study in Safety, Security, and Availability of Wireless-Enabled Aircraft Communication Networks." In AIAA AVIATION, June 5–9, 2017.

M4 Rohit Dureja and Kristin Y. Rozier. "Comparative Safety Analysis of Wireless Communication Networks in Avionics." In *Formal Methods in Computer-Aided Design (FMCAD 2016) Student Forum*, Mountain View, California, USA, October 3–6, 2016.

Books and Book Chapters

B5 Dhananjay V. Gadre, Rohit Dureja and Shanjit S. Jajmann. "Getting Started with Stellaris ARM Cortex-M Embedded Processors." 1st Edition, 2013, Universities Press, ISBN: 8173718814.

SELECTED COURSE PROJECTS

1. *UAV Security Exploit.* Designed a one-click man-in-the-middle (MITM) attack with ARP poisoning to acquire unauthenticated control of a drone.
2. *Modeling and Verification of a Pacemaker.* Modeled a pacemaker using UPPAAL and synthesized code to run on a 32-bit ARM microcontroller.
3. *Veterinary Patient Records.* Gathered requirements for a patient record system; culminated in a complete requirements specification document, and a prototype.
4. *Network Sniffer.* Designed a powerful network packet sniffer capable of collecting socket-connection information and data, SMTP messages and profile connections.
5. *Viral Marketing.* Experimentally evaluated the correlation between social network and spread of influence models to maximize information spread.
6. *US Presidential Elections.* Designed a predictor model to predict popular vote and electoral college winner of 2016 US presidential elections.

TECHNICAL SKILLS

Languages & Software: C/C++, Python, Haskell, LaTeX, Matlab.
Technologies: Git, CMake, HTML/CSS, SQL, MongoDB.

SERVICE

Reviewer: TACAS 2017, NFM 2016

EXTERNAL TRAINING

1. Marktoberdorf School on Dependable Software Systems Engineering, 2016.
2. SRI International Sixth Summer School on Formal Techniques, 2016
3. RiSE & LogiCS Spring School on Logic and Verification, 2016

AWARDS & HONORS

- Travel grant and registration waiver to Marktoberdorf School.
- Microsoft Research travel grant to Verification Mentoring Workshop (VMW) 2016 and Computer Aided Verification (CAV) Conference 2016.
- Carnegie Mellon University travel grant to CPS V&V Workshop 2016.
- National Science Foundation travel grant to CPS Week 2016.
- *Best Design* and *Top 10 hack* at HackPrinceton 2013.
- University of Delhi academic scholarship, 2009-2013.