Rohit Dureja dureja@iastate.edu

Education

Ph.D. Computer Science, Iowa State University, Ames, IA, USA 2016– ongoing
Cumulative GPA 3.83/4.00

M.S.E. Embedded Systems, University of Pennsylvania, Philadelphia, PA, USA 2013–2015
Cumulative GPA 3.53/4.00

B.E. Instrumentation and Control, University of Delhi, New Delhi, India 2009–2013
Cumulative percentage 77.08%

Experience

Research Assistant, Iowa State University Aug 2015 – present
Symbolic Model Checking of Large Design Spaces
Mentor: Kristin Yvonne Rozier

1. Designing algorithms for checking "sets" of models and properties, and
2. Developing novel extensions to the NuSMV model checker, and new model-set checkers.

Research Intern, Fondazione Bruno Kessler, Trento, Italy May 2015 – Aug 2015
Formal Verification of NextGen Air Traffic Controller
Mentor: Alessandro Cimatti

1. Added extensions to include asymmetric information sharing between aircraft.
2. Developed a contract-based design case-study of a sample railroad system.
3. Analyzed extraction of SMV models from LLVM bitcode and control flow graphs.

Embedded Systems Programmer, University of Pennsylvania Jan 2014 – Apr 2015
Wireless and Invasive Brain-Computer Interfaces
Mentor: Jan Van der Spiegel

1. Designed a wireless brain-sensor interface system to control prosthetics.
2. Researched the use of compressive sensing and learning to minimize data outflow.

Undergraduate Intern, Texas Instruments, New Delhi, India Dec 2011 – Apr 2013
ARM-based Microcontroller Development Platforms
Mentor: Dhananjay Gadre

1. Responsible for complete hardware/software design of ARM-based learning kits.
2. Commercially launched two learning kits, Stellaris Guru and Stellaris Shuru.
3. Composed pegagogy materials and co-authored an undergraduate lab manual.

Publications

Peer-Reviewed Conferences

C1 Rohit Dureja and Kristin Y. Rozier. More Scalable LTL Model Checking via Discovering Design-Space Dependencies (D^3). In *Proceedings of Tools and Algorithms for the Construction and Analysis of Systems (TACAS)"*, Thessaloniki, Greece, April 2018. Springer-Verlag

C2 Rohit Dureja and Kristin Y. Rozier. FuseIC3: An Algorithm for Checking Large Design Spaces. In *Proceedings of Formal Methods in Computer-Aided Design (FMCAD)*, Vienna, Austria, October 2017. IEEE/ACM. Talk video: `https://goo.gl/Gs92G2`

Workshops and Posters

P3 Rohit Dureja and Kristin Y. Rozier. From One to Many: Checking A Set of Models. In *Formal Methods in Computer-Aided Design (FMCAD) Student Forum*, Austria, Vienna, October 2017

W4 Rohit Dureja, Eric W. D. Rozier, and Kristin Y. Rozier. A Case Study in Safety, Security, and Availability of Wireless-Enabled Aircraft Communication Networks. In *Proceedings of AIAA Aviation Technology, Integration, and Operations Conference (AVIATION)*, Denver, Colorado, USA, June 2017. AIAA

P5 Rohit Dureja and Kristin Y. Rozier. Comparative Safety Analysis of Wireless Communication Networks in Avionics. In *Formal Methods in Computer-Aided Design (FMCAD) Student Forum*, Mountain View, California, USA, October 2016

Books and Book Chapters

B6 Dhananjay V. Gadre, Rohit Dureja, and Shanjit S. Jajmann. *Getting Started with Stellaris ARM Cortex-M Embedded Processors*. Universities Press, 2013

Under Submission

C7 Jianwen Li, Rohit Dureja, Geguang Pu, Kristin Y. Rozier, and Moshe Y. Vardi. SimpleCAR: An Efficient Bug-Finding Tool Based On Complementary Approximate Reachability

Technical Presentations

- "Scalable Design Space Analysis for Future Traffic Management." CPS Challenges for Unmanned and Autonomous Systems Workshop, Washington, DC, November 14, 2017.
- "Making Undecidable Problems Decidable in Practice." Software Engineering Seminar, Department of Computer Science, Iowa State University, Ames, IA, October 12, 2017.

Selected Course Projects

1. *UAV Security Exploit.* Designed a one-click man-in-the-middle (MITM) attack with ARP poisoning to acquire unauthenticated control of a drone.
2. *Modeling and Verification of a Pacemaker.* Modeled a pacemaker using UPPAAL and synthesized code to run on a 32-bit ARM microcontroller.
3. *Veterinary Patient Records.* Gathered requirements for a patient record system; culminated in a complete requirements specification document, and a prototype.
4. *Network Sniffer.* Designed a powerful network packet sniffer capable of collecting socket-connection information and data, SMTP messages and profile connections.
5. *Viral Marketing.* Experimentally evaluated the correlation between social network and spread of influence models to maximize information spread.
6. *US Presidential Elections.* Designed a predictor model to predict popular vote and electoral college winner of 2016 US presidential elections.

Skills

Languages & Software: C/C++, Python, LaTeX, Matlab.
Technologies: Git, CMake, HTML/CSS, SQL, MongoDB.

Professional Service

Artifact Evaluation Committee: TACAS 2018
Reviewer: NFM 2018, TACAS 2018, TACAS 2017, NFM 2016

External Training

1. Marktoberdorf School on Dependable Software Systems Engineering, 2016.
2. SRI International Sixth Summer School on Formal Techniques, 2016
3. RiSE & LogiCS Spring School on Logic and Verification, 2016

Awards and Honors

- Travel grant to Formal Methods in Computer Aided Design (FMCAD) Conference 2016, 2017.
- Travel grant and registration waiver to Marktoberdorf School.
- Microsoft Research travel grant to Verification Mentoring Workshop (VMW) 2016 and Computer Aided Verification (CAV) Conference 2016.
- Carnegie Mellon University travel grant to CPS V&V Workshop 2016.
- National Science Foundation travel grant to CPS Week 2016.
- *Best Design* and *Top 10 hack* at HackPrinceton 2013.
- University of Delhi academic scholarship, 2009-2013.