**AIM** – To simulate Verilog programs for binary multiplier.

**SOFTWARE REQUIRED** – ModelSim XE II 5,7c

**PROGRAM** -

module multiplier(a,b,q);

input [1:0]a;

input [1:0]b;

output [3:0]q;

wire t1,t2,t3,t4;

and and12(q[0],a[0],b[0]);

and and22(t1,a[1],b[0]);

and and32(t2,a[0],b[1]);

halfadder\_struct h1(q[1],t3,t1,t2);

and and4(t4,a[1],b[1]);

enfmodule