

Phase Noise Analysis of Phase Frequency Detector using Time-Domain Jitter

A thesis report (Course Code:EE699) submitted in partial fulfillment of
the requirements for the degree of

Master of Technology

by

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November 22, 2024

Declaration

I hereby affirm that this written submission is a reflection of my original ideas and work. Where I have incorporated ideas, words, or data from others, I have appropriately cited and acknowledged the original sources. I further confirm that I have upheld the principles of academic honesty and integrity, ensuring that no information, data, or facts have been misrepresented, fabricated, or falsified. I fully understand that any breach of these principles may result in disciplinary action by the Institute and potential legal consequences from improperly cited sources or those from whom prior permission was required.

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Date:22/11/2024

Acknowledgement

I extend my heartfelt gratitude to my supervisor, Dr. Mahendra Sakare, for granting me the opportunity to work under his guidance and for providing essential support throughout the project. I am also thankful to my PhD mentor Hirensh Mehra whose technical support has helped to complete the project. I would also like to acknowledge the authors of various papers that I have referenced in building this project.

Finally, I extend my appreciation to my family and friends whose encouragement has been invaluable in completing this project.

Abstract

This study examines the phase noise characteristics of Phase Frequency Detectors (PFDs), comparing the noise performance of NAND-based PFD and True Single Phase Clock (TSPC) PFD architectures. Both architectures are evaluated under identical conditions of frequency and power consumption. The noise analysis is conducted using approximations derived from a CMOS inverter model. A key finding of this work is the impact of operating frequency on phase noise, emphasizing the significant influence of frequency scaling on noise performance.

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Chapter 1

Introduction

A Phase-Locked Loop (PLL) is a feedback control system designed for various applications like clock generation, frequency synthesis, modulation and demodulation of signal. There are various blocks of the PLL like phase-frequency detector (PFD), charge-pump (CP), loop filter, voltage-control oscillator (VCO) and frequency divider. By continuously comparing the VCO output with a reference signal it adjust the VCO frequency to maintain synchronization with reference signal, resulting in a highly stable output. Every one of these block contribute noise which contribute to the overall noise of PLL.

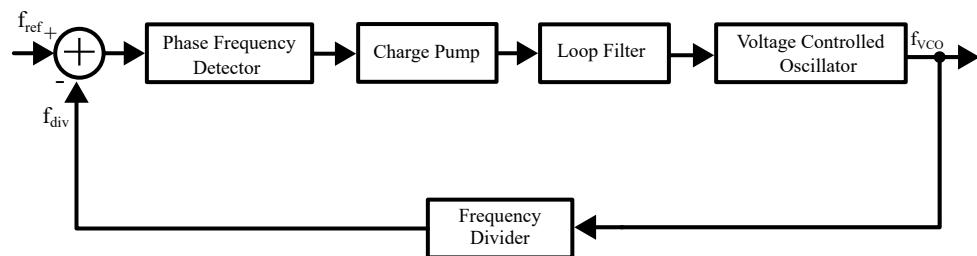


Figure 1.1: PLL Architecture

PFD is one of the main component of PLL whose phase noise impacts the overall performance of the system. In general phase noise of VCO is taken with great importance and seen in most of the research work so the phase noise of PFD is often ignored. In-band phase noise of PFD creates issues in PLL design and in obtaining the desired output.

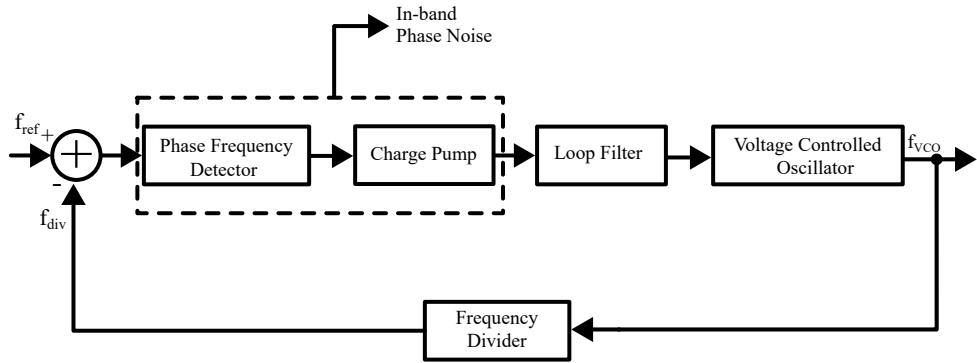


Figure 1.2: Blocks analysed for inband phase noise of PLL

1.1 PFD

PFD detects phase difference between the two pulses and noise present in the pulses affect the output of the PFD. Various designs of PFD has evolved over time as per the applications. D-FlopFlop based PFD is the conventional type of PFD which has been used for various applications but as the requirement of high speed applications various designs of PFD has been developed. For the high speed PLL applications true single phase clock (TSPC) PFD is used. When phase noise causes unequal modulation of the Up and Down pulse widths, it results in fluctuations at the VCO input. The factor that changes or modulates the width of the pulse is noise present in signal which creates random disturbance to the ideal pulse by either increasing or decreasing the pulse width.

1.2 Noise

The unwanted disturbance present in circuit is called noise. There are various types of noise but mainly we consider two types of noise Thermal Noise and Flicker Noise.

Thermal Noise: It is the noise generated by the random motion of charge carriers, caused by the thermal agitation of electrons within the material. This type of noise is frequency-independent, and its spectrum remains constant across frequencies. The noise of the MOS transistor is given as:

$$S_I(f) = 4kT\gamma g_m \quad (1.1)$$

Flicker Noise: Flicker noise is frequency-dependent noise which is dominant in the lower

frequency range. The flicker noise theory states that flicker noise occurs due to the random trapping and de-trapping processes of charges in the oxide traps near the Silicon(Si) and Silicon-Oxide(SiO_2) interface.

$$S_{1/f} = \frac{K}{WLC_{\text{ox}}} \frac{1}{f} \quad (1.2)$$

Based on Hung's model [1], in MOS transistors, the drain current directly influences the flicker noise current (I_D). In the unified model present in the paper noise results from fluctuations in the number of carriers and surface mobility due to charge trapping and scattering mechanisms. As the drain current in the inverter stage is carried by the MOS transistor, any noise in the channel affects the drain current of the inverter. In the switching operation of the inverter the MOSFET continuously transitions between strong inversion, weak inversion and cutoff region and flicker noise arises predominantly in the strong inversion region where current fluctuations are influenced by the number of carrier and mobility fluctuations which contribute to variations in the drain current during switching.

Flicker noise analysis involves capturing and evaluating of low frequency components of a signal often requiring Fourier analysis but direct applying it can lead to spectral leakage. Using windowing techniques it helps to mitigate spectral leakage by shaping the signal at the edges and making it smoother and reducing discontinuities.

kT/C Noise :

When the transistor turns off it injects kT/C noise. When the transistor is in triode region, its combination with node capacitance generates noise whose value is equal to kT/C . The noise produced by the transistor is independent of the value of resistor.

Then noise is given as:

$$P_{n,\text{out}} = \frac{kT}{C} \quad (1.3)$$

1.3 Jitter

Jitter can be defined as the timing uncertainties in comparison with the ideal clock. These jitter can be deterministic or random depending upon the source producing jitter. The noise present in the circuit produces random jitter at the output. These random timing variations impact

the performance of PLL in the high speed applications. There are different kinds of jitter like absolute jitter, relative jitter, and periodic jitter.

1.4 Phase Noise

Phase noise can be defined as the ratio of power of the signal in 1Hz bandwidth at offset f from the carrier divided by the power of the carrier [2]:

$$S_\phi(f) = \frac{S_v(f_0 + f)}{P}. \quad (1.4)$$

It depicts the signal's instability in the frequency domain. In spectrum analysis, it appears as sidebands around the main carrier. Let us relate the concept of phase noise and jitter with basic CMOS inverter circuit.

1.5 Phase Noise of Inverter

As CMOS inverter is foundational block for every circuits of CMOS logic implementation. When a signal is applied to the inverter's input, the PMOS device charges the load capacitor, while the NMOS device discharges it. The rms value of the jitter is proportional to the delay of the inverter. So strong inverter has small jitter as it has less propagation delay.

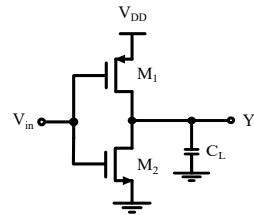


Figure 1.3: CMOS inverter

The on-resistance of a transistor decreases when the W/L ratio of the device is increased which increases power consumption so size and power trade-off should be balanced during design. Propagation delay t_{pHL} and t_{pLH} is,

$$t_{pHL} = 0.69 R_{eqn} C_L \quad (1.5)$$

The rate at which the transistor rises and falls directly influences the phase noise. There are various ways to decrease the rise and fall time by reducing load capacitance C_L , increasing the load capacitance of the transistors and increasing power supply (V_{DD}).

This report is structured in following way. Chapter 1 provides an introduction to the topic. Chapter 2 reviews the literature on different architectures of PFD Design and phase noise analysis. Chapter 3 focuses on the analysis of phase noise and jitter in inverter, NAND PFD and TSPC PFD. Chapter 4 presents the hand calculation and simulation results, and finally, Chapter 5 concludes the work with key findings and insights.

Chapter 2

Literature survey

In the design of PLL, PFD plays important role as it is critical and foundational block which detects phase and frequency differences between input and feedback signal. The PFD generates control signal for subsequent stages and ensure that PLL attain lock stage. To meet the needs of PLL in different applications different design of PFD had evolved from analog to digital PFDs which has distinct advantages and limitations. With advancement in PFD architectures various designs have evolved to enhance it's speed, noise performance and power efficiency.

With advancement in the design of PFD there are various factors affecting its output like phase noise. PFD is one of the important block of PLL so the phase noise of the PFD affects the output of the PLL. So it is one of the important issue to analyze the phase noise of PFD and its contribution in the overall output of the PLL. The noise in PFD affects the VCO control voltage through charge pump. For phase noise analysis spectral density of current and voltage is evaluated. In this work jitter contribution from each transistor is calculated and related to voltage spectral density through slew rate to calculate the total in-band phase noise of the PLL.

The main role of PFD is to generate an error signal by detecting the difference between two signals. For this purpose, a simple XOR-gate can be used which detects the difference between two signals. Its limited frequency sensitivity and dead zone restrict its use in a wide variety of applications.

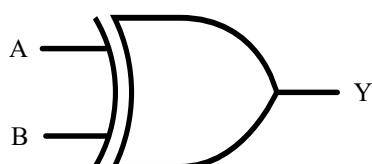


Figure 2.1: XOR gate

In 1962, [3] C.J BYRNE proposed a paper that analyses properties of the phase-controlled oscillator where sawtooth comparator is used. In this work, sawtooth comparator is compared with sinusoidal comparator and observed that it has advantages over sinusoidal comparator for many applications as its gain remains constant for a wide range. After the introduction of Digital PFD, D flipflop-based PFD was widely used for various applications.

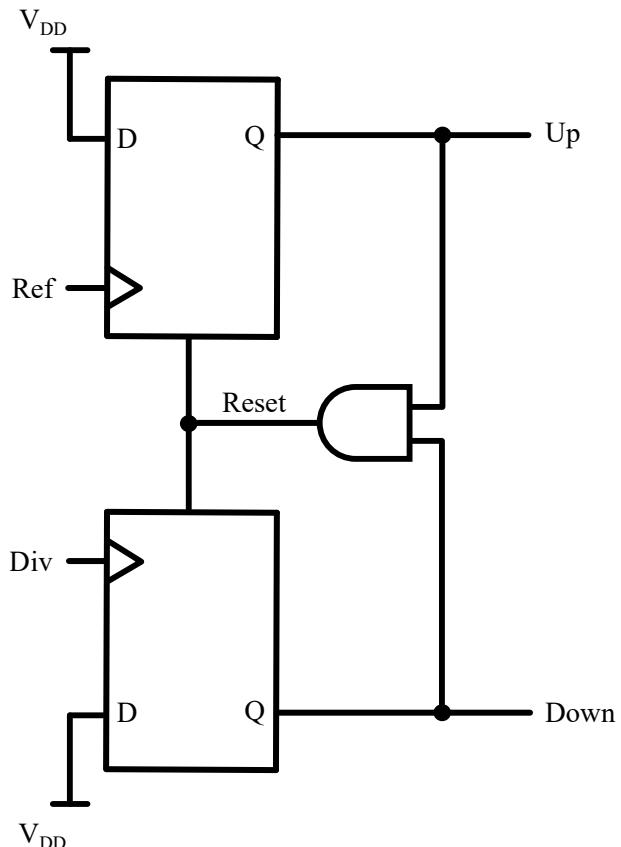


Figure 2.2: D-Flip flop based PFD

In 1967, [4] Kalevi Kalliomaki proposed phase and frequency detector where bistable multivibrator is used. PFD was used using D Flipflop. Nand based PFD is also other form of representation of conventional D-Flipflop PFD. In CMOS logic implementation we require two phase clocks and two transistors are in series and parallel which require more power and area. For low power and high speed applications we require less transistor area and minimize clock distribution requirement which gave rise to the idea of using single clock in the circuit. [5] states first about the 3 state phase detector. In 1989, [6] Yuan proposed a technique for high speed CMOS circuit technique called TSPC which uses only single clock with less no transistors to implement the same logic which were previously done using CMOS logic. Later, TSPC (True Single Phase Clock) based PFD is proposed which requires less number of transistor and higher

operating frequency.

In 2003, [7] Thompson and Brennon explained in their about the phase noise of PFD in digital frequency synthesizer where they focused about the in-band noise in PLL which is contributed by the PFD. In this paper, they explore how phase noise of the PFD impacts Digital PLL Frequency Synthesizer and established a theoretical model to quantify the phase noise contribution of the PFD which includes the effects of timing jitter originating from thermal noise within PFD. They have highlighted how timing jitter introduces uncertainty in the timing of the output pulses impacting the accuracy of the PLL's output phase. The study concluded that PFD is critical contributor of in-band phase noise of digital PLL synthesizer so to improve phase optimization of PFD's operating frequency, switching threshold and input circuitry can be done.

In Abidi's paper [8], analysis of single inverter is done to understand its noise characteristics and the contribution of these noise sources at the output of CMOS ring oscillators. Noise analysis in this paper provides fundamental understanding of noise behavior at the inverter level which later extended to CMOS multi-stage ring oscillators. It also demonstrates the effect of thermal as well as flicker noise in a single inverter stage and its contribution to jitter and phase noise at the oscillator output. It derives various mathematical expressions which links jitter and phase noise and provides ways to design ring oscillators.

In 2005, [9] in this paper an advanced model for phase noise in Fractional-N Phase-Locked Loops (Frac-N PLLs) is presented focusing on the effects of non idealities of components like charge pump and PFD. Noise modeling is done in time and frequency domain model which captures phase disturbance due to multiple sources like error in Charge Pump, reset delay of PFD, prescalar noise and DSM (Delta-Sigma Modulator) noise. Non-uniform propagation delays in the reset path create timing offsets leading to phase noise of PFD which adds to the total noise of pll. In 2013, a paper was published on the analysis of phase noise of PFD where the concept of jitter in time domain is related to phase disturbance and was compared with two different architectures. The PFD with less number of transistors had better noise as less jitter was embedded on pulses [10].

Chapter 3

Phase Noise Analysis

The phase noise in Up and Down signal affect the current injected into the loop filter through CP translates to random fluctuation which introduces noise into the loop filter. When phase noise affects both Up and Down signals equally then both pulses are modulated by same amount of phase noise so the symmetrical modulation has no net effect on the charge pump output and the total charge transferred by the Charge Pump to the loop filter remains unchanged. Modulating the position of the Up and Down pulses has a minimal effect on the performance of the loop filter. However, when noise is present, the widths of the Up and Down pulses become modulated unevenly, leading to random fluctuations in the net current injected by the charge pump. This, in turn, introduces phase disturbance and degrades the overall phase stability of the PLL. The variations in pulse width are a result of jitter occurring on the rising and falling edges of the pulses.

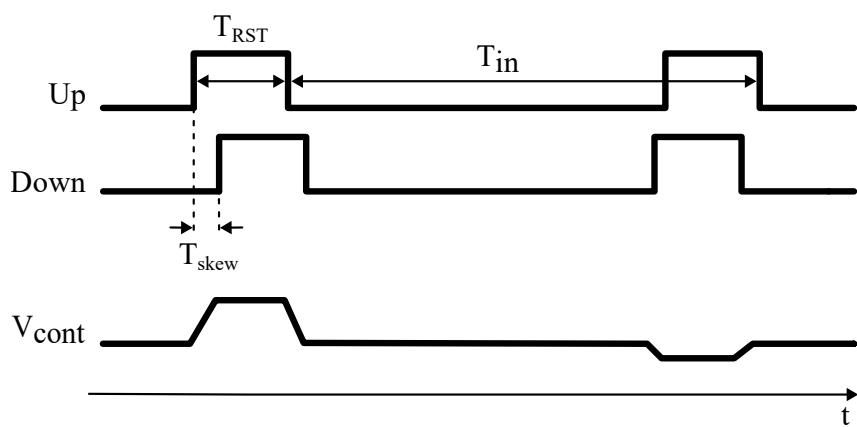


Figure 3.1: Pulse position modulation

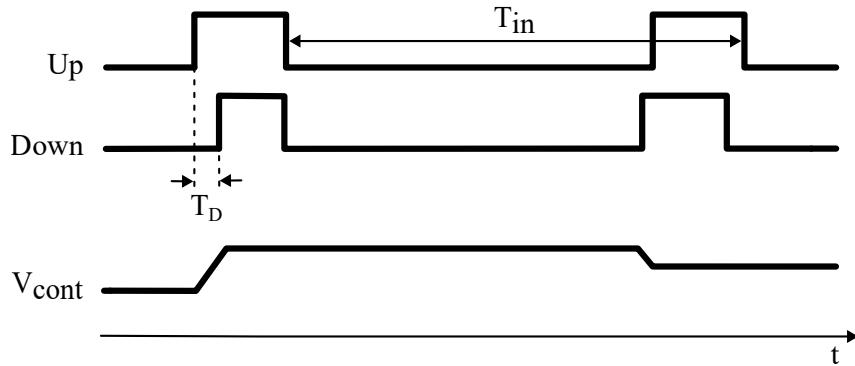


Figure 3.2: Pulse width modulation

When there is a time displacement of ΔT between the edges of the pulses, this displacement in phase domain is given as, $2\pi\Delta T/T_{in}$. If there is constant disturbance of ΔT occurs at the pulse then phase change is also constant but as we know that jitter is random component which effect edges differently.

Let us begin our analysis by first evaluating deterministic sinusoidal jitter and then correlating it with random jitter and phase noise. Consider a ideal square wave $p(t)$ where the sinusoidal jitter $T_m \cos \omega_m t$ is applied on its rising edges which displaces the rising edges by its width of $T_m \cos \omega_m k T_{in}$. As jitter is provided on each cycle on rising edges so we can express this waveform as sum of ideal square wave $p(t)$ and train of impulse occurring at kT_{in} with a width of $T_m \cos \omega_m k T_{in}$ which is denoted by $q(t)$ and represented as: Consider a impulse $\delta(t)$ which is shifted by the time period T_s from time period infinity to -infinity. Then the signal can be represented as

$$\delta(t) = \sum \delta(t - nT_s) \quad (3.1)$$

Now the sinusoidal jitter is sampled as

$$q(t) \approx \sum T_m \cos(\omega_m t) \delta(t - k T_{in}) \quad (3.2)$$

$$q(t) \approx T_m \sum \cos(\omega_m k T_{in}) \delta(t - k T_{in})$$

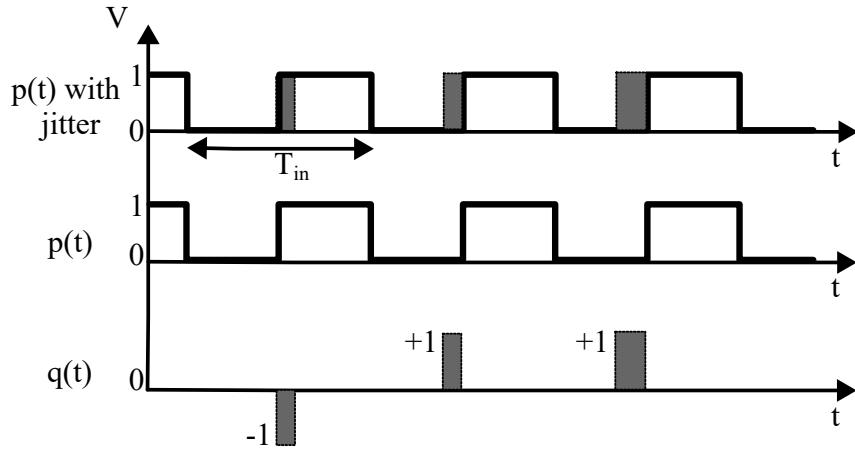


Figure 3.3: Square wave with modulated rising edges

Fourier Transform of $p(t)$ and $q(t)$:

For $p(t)$: DC value (C_0) = 1/2

Let us consider a function $p'(t)$ which is obtained by differentiating the function $p(t)$. The ideal square wave is now impulse where they have positive impulse at rising edges and negative impulse at the falling edges.

$$\begin{aligned}
 x(t) &= \sum_{k=-\infty}^{\infty} \delta \left(t + \frac{T_{in}}{4} - kT_{in} \right) \delta \left(t - \frac{T_{in}}{4} - kT_{in} \right) \\
 p'(t) \longleftrightarrow p_n &= \frac{1}{T_{in}} \left[e^{jn\left(\frac{2\pi}{T_{in}}\right)\left(\frac{T_{in}}{4}\right)} - e^{jn\left(\frac{2\pi}{T_{in}}\right)\left(-\frac{T_{in}}{4}\right)} \right] \\
 p_n &= \frac{2j \sin\left(\frac{n\pi}{2}\right)}{T_{in}} \\
 p(t) \longleftrightarrow &\frac{p_n}{j n \left(\frac{2\pi}{T_{in}}\right)} \\
 p(t) &= \frac{\sin\left(\frac{n\pi}{2}\right)}{n\pi} \\
 P(\omega) &= \frac{1}{2} 2\pi \delta(\omega) + \sum_{k=-\infty}^{\infty} 2\pi \frac{\sin\left(\frac{n\pi}{2}\right)}{n\pi} \delta(\omega - k\omega_{in}) \\
 P(f) &= \frac{\delta(f)}{2} + \sum_{k=-\infty}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)}{n\pi} \delta(f - kf_{in})
 \end{aligned}$$

Fourier Transform of the function $p(t)$ is:

$$P(f) = \frac{\delta(f)}{2} + \sum_{k=-\infty}^{\infty} \frac{(-1)^{\left(\frac{n-1}{2}\right)}}{n\pi} \delta(f - kf_{in}) \quad (3.3)$$

For $q(t)$:

$$q(t) \approx T_m \cos(\omega_m t) \sum_{k=-\infty}^{k=\infty} \delta(t - kT_{in}) \quad (3.4)$$

Let $x(t)$ be the function which represents the delta function. The Fourier Transform of $x(t)$ is:

$$\begin{aligned} \sum_{k=-\infty}^{\infty} \delta(t - kT_{in}) &\longleftrightarrow \frac{2\pi}{T_{in}} \sum_{k=-\infty}^{\infty} \delta\left(\omega - k\frac{2\pi}{T_{in}}\right) = X(\omega) \\ q(t) &= T_m \cos(\omega_m t) \cdot x(t) \\ q(t) &= T_m \left(\frac{e^{j\omega_m t} + e^{-j\omega_m t}}{2} \right) \cdot x(t) \\ e^{j\omega_m t} x(t) &\longleftrightarrow X(\omega - \omega_m) \end{aligned}$$

The Fourier Transform of $q(t)$ is given as:

$$\begin{aligned} Q(\omega) &= \frac{T_m}{2} [X(\omega - \omega_m) + X(\omega + \omega_m)] \\ Q(\omega) &= \frac{T_m}{2} \left[\sum_{k=-\infty}^{\infty} \delta\left(\omega - \omega_m - \frac{k2\pi}{T_{in}}\right) + \delta\left(\omega + \omega_m - \frac{k2\pi}{T_{in}}\right) \right] \frac{2\pi}{T_{in}} \\ Q(\omega) &= \frac{\pi T_m}{2 T_{in}} \left[\sum_{k=-\infty}^{\infty} \delta\left(\omega - \omega_m - k\frac{2\pi}{T_{in}}\right) + \delta\left(\omega + \omega_m - k\frac{2\pi}{T_{in}}\right) \right] \\ Q(f) &= \frac{T_m}{2 T_{in}} \left[\sum_{k=-\infty}^{\infty} \delta\left(f - f_m - \frac{k}{T_{in}}\right) + \delta\left(f + f_m + \frac{k}{T_{in}}\right) \right] \\ Q(f) &= \frac{T_m}{2 T_{in}} \left[\sum_{k=-\infty}^{\infty} \delta(f - f_m - kf_{in}) + \delta(f + f_m - kf_{in}) \right] \quad (3.5) \end{aligned}$$

From equation 3.3 and 3.5 we can observe that jitter of width $T_m/2T_{in}$ surrounds $p(t)$ around f_{in} generating phase modulation. As we have considered only the rising edges it causes disturbance in phase with value of $(\pi/T_{in})(T_m/2)$ is observed. In a single tone modulation the message signal is sinusoidal(either sine or cosine) as sinusoidal signal has single frequency. In other cases the message signal $m(t)$ is non-sinusoidal and carrier frequency is sinusoidal then it is multitone modulation. In multitone modulation upper side band and lower side band has multiple frequency whereas single tone modulation has only one frequency.

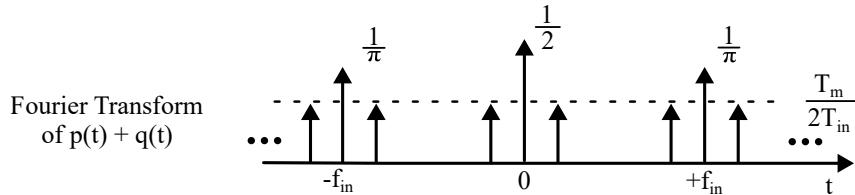


Figure 3.4: Fourier Transform of $p(t)$ and $q(t)$

If signal $x(t)$ is deterministic then power can be obtained by calculating Fourier transform and then squaring to get the power of the signal. The noise sources we deal with are WSS (Wide Sense Stationary). If the noise sources are uncorrelated they are added in power.

$$E[(x_1 + x_2)^2] = E(x_1^2) + E(x_2^2) + 2E(x_1 x_2) \quad (3.6)$$

If they are uncorrelated then $E(x_1 x_2)$ is zero. As we calculate power in 1 Hz bandwidth. Power Spectral Density (PSD) is equal to Fourier Transform of $R_X(\tau)$.

For analysis of random processes in frequency domain we evaluate its Power Spectral Density (PSD) where we can determine the distribution of power of random processes over the frequency axis. A flat PSD means that all the frequency component are present and it is mainly for the thermal noise. Since jitter is random we generalize the observation to random jitter, which modulates only the rising edges of the pulse then it is given as:

$$q(t) \approx \sigma(t) \sum_{k=-\infty}^{\infty} \delta(t - k T_{in}). \quad (3.7)$$

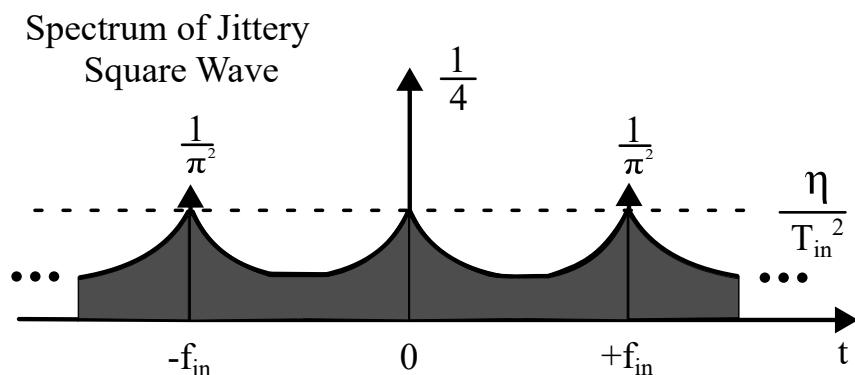


Figure 3.5: Spectrum of jittery square wave

For random jitter we add power spectral density of ideal square wave $p(t)$ and jitter component $q(t)$ gives the spectrum with jitter as shown in Fig. 3.5. As the pulse in rising edge

embeds jitter from PMOS while from NMOS in falling edges so they are not correlated. The phase noise, from jitter contribution of NMOS and PMOS is:

$$S_\phi(f) = \frac{\pi^2}{T_{in}^2} \sum_{m=-\infty}^{\infty} [S_{\sigma p}(f \pm m f_{in}) + S_{\sigma n}(f \pm m f_{in})]. \quad (3.8)$$

The spectral distribution of the jitter caused by the PMOS transistors are given by $S_{\sigma p}$ while that from NMOS transistors are denoted by $S_{\sigma n}$ which can be related to voltage spectral density by the factor of γ_{edge}^2 .

3.1 CMOS Inverter

Let us begin noise analysis with basic CMOS inverter and extend it to other CMOS gates. When the transistor is on, it injects thermal and flicker noise. The noise envelope of thermal noise is about half of the period and that of flicker noise is dominant at the transitions which is shown in Fig.3.6

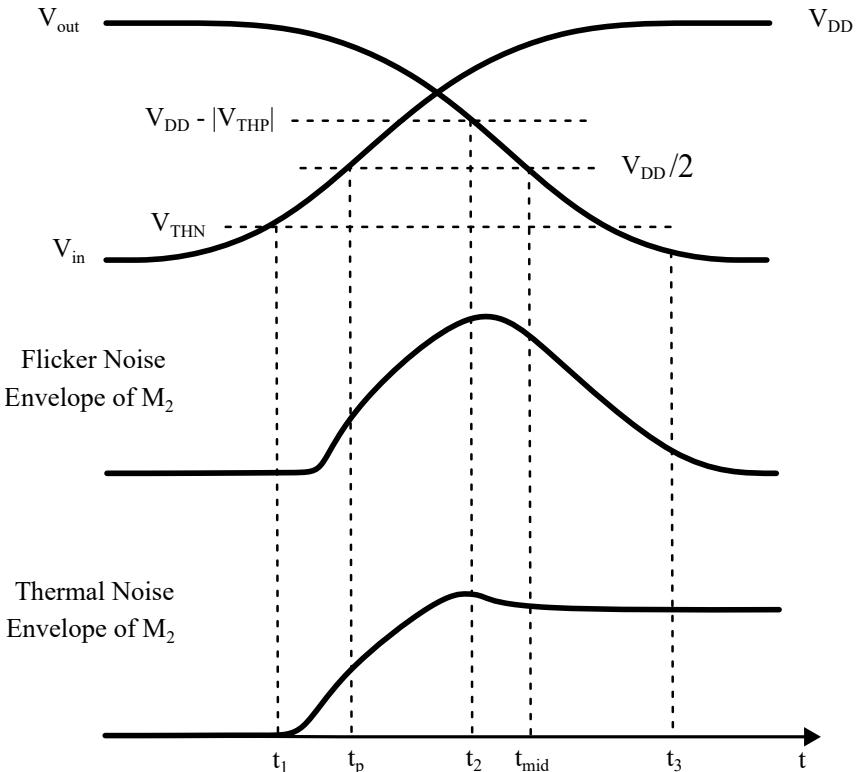


Figure 3.6: Noise envelope of thermal and flicker noise

To analyze the area under noise envelope we approximate it using rectangular waveform. From the working of CMOS inverter we can conclude that when the input reaches to peak value

only one transistor is at on state and when input is zero other transistor is at on state so the PMOS noise appears on rising edges, while the NMOS noise is present on the falling edges. In each cycle, the noise current is to load capacitance to obtain noise voltage.

Thus, the PMOS noise appears on the rising edges, while the NMOS noise is present on the falling edges. In each cycle, the noise current is multiplied by a shifted version of $w(t)$ and divided by the load capacitance to calculate the noise voltage. The noise voltage v_{n1} of the first rectangular window is given as:

$$\begin{aligned} v_{n1} &= \frac{1}{C_L} \int_0^{\Delta T} i_n(t) dt \\ &= \frac{1}{C_L} \int_{-\infty}^{+\infty} i_n(t) w(t) dt. \end{aligned} \quad (3.9)$$

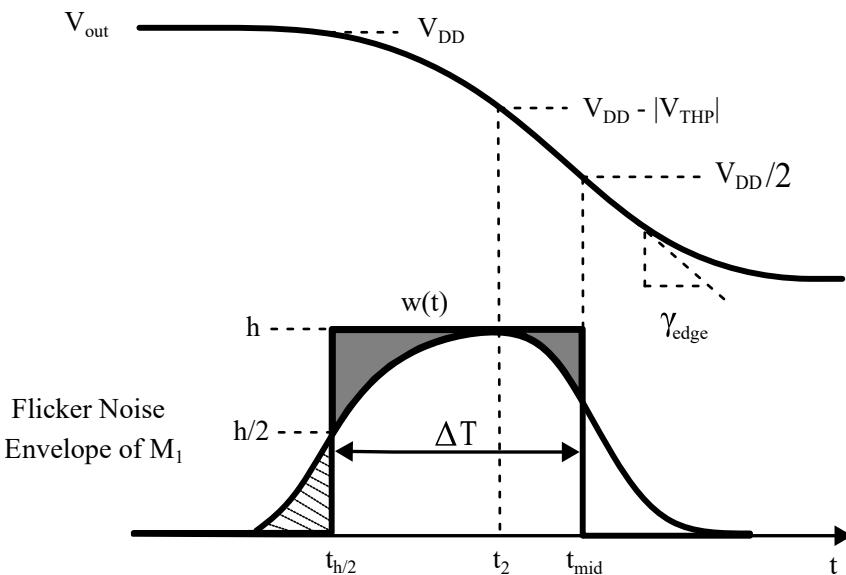


Figure 3.7: Flicker noise envelope using rectangular approximation

As rectangular window is required to frame noise after each cycle so the noise voltage equation for m cycle is given as:

$$v_{n,m} = \frac{1}{C_L} \int_{-\infty}^{+\infty} i_n(t) w(t - m T_{in}) dt. \quad (3.10)$$

Using convolution integral, the spectrum of noise voltage can be formulated as:

$$S_{Vn}(f) = \frac{1}{C_L^2} |W(f)|^2 S_{In}(f) \quad (3.11)$$

where $W(f)$ stands for Fourier Transform of $w(t)$ and spectrum of $i_n(t)$ is given by $S_{In}(f)$. We are using a rectangular window to outline the phase noise of the inverter which consists of contribution from flicker noise as well as thermal noise. Considering NMOS transistor, the phase noise is injected on the falling edges whose spectrum is given by:

$$S_\phi(f) = \frac{\pi^2}{\gamma_{\text{edge}} T_{in}^2} \sum_{m=-\infty}^{\infty} S_{Vn} \left(f - \frac{m}{T_{in}} \right). \quad (3.12)$$

Rectangular window $w(t)$ in the frequency domain is represented as:

$$W(f) = \frac{\Delta T \sin(\pi f \Delta T)}{\pi f \Delta T} \quad (3.13)$$

When we assume that the current spectral density $S_{In}(f)$, behaves as white noise, the voltage spectral density, $S_{Vn}(f)$ takes sinc^2 function which is centered at mf_{in} . Let us consider a sinc^2 shape whose Inverse Fourier Transform is a triangle. Let us begin our analysis with triangular function $g(t)$, taking inverse Fourier transform gives $G(f)^2$. Therefore, Inverse Fourier Transform of $\Delta T^2 \text{sinc}^2(\pi f \Delta T)$ is a triangle, $g(t)$ which has a width duration extending from $-\Delta$ to $+\Delta$ and to the height of ΔT . From equation of $S_{Vn}(f)$ we can observe that sinc^2 has a shift by mf_{in} in frequency domain, meaning that in the time domain $g(t)$ is multiplied with $e^{j2\pi mf_{in}t}$.

$$g(t) \sum_{m=-\infty}^{\infty} e^{j2\pi mf_{in}t} \longleftrightarrow \sum_{m=-\infty}^{\infty} \Delta T^2 \frac{\sin^2 [\pi \Delta T (f - mf_{in})]}{[\pi \Delta T (f - mf_{in})]^2} \quad (3.14)$$

Relation between exponential and delta in time domain:

$$\sum_{m=-\infty}^{m=\infty} e^{j2\pi mf_{in}t} = \frac{1}{f_{in}} \sum_{m=-\infty}^{m=\infty} \delta(t - mT_{in}) \quad (3.15)$$

When $g(t)$ is multiplied with train of impulse and period is taken so small that it encloses only one impulse at $t = 0$ then,

$$g(t) \sum_{m=-\infty}^{\infty} e^{j2\pi mf_{in}t} = \frac{\Delta T}{f_{in}} \delta(t) \quad (3.16)$$

It's Fourier Transform is equal to:

$$\sum_{m=-\infty}^{\infty} \Delta T^2 \frac{\sin^2 [\pi \Delta T (f - mf_{in})]}{[\pi \Delta T (f - mf_{in})]^2} = \frac{\Delta T}{f_{in}} \quad (3.17)$$

A process having a flat PSD is also called white as every frequency component has contributed to the total process. From equation 3.11 and 3.12 phase noise spectral density $S_\phi(f)$ due to white noise is equal to:

$$\begin{aligned} S_\phi(f) &= \frac{\pi^2}{\gamma_{\text{edge}}^2 T_{\text{in}}^2} \frac{1}{C_L^2} \frac{\Delta T}{f_{\text{in}}} S_I(f) \\ &= \frac{\pi^2}{\gamma_{\text{edge}}^2 C_L^2} \frac{\Delta T}{T_{\text{in}}} S_I(f). \end{aligned} \quad (3.18)$$

If input frequency f_{in} is greater than corner frequency then there is no aliasing and choosing $m = 0$ equation 3.12 can be deduced as:

$$S_\phi(f) = \frac{\pi^2}{\gamma_{\text{edge}}^2 T_{\text{in}}^2} S_{Vn}(f). \quad (3.19)$$

Since ΔT is much smaller than the corner frequency, from Fourier transform of $w(t)$

$W(f) = \Delta T^2 \text{sinc}^2(\pi f \Delta T)$ is constant then it reduces to ΔT^2 . Then, equation for phase noise contribution from flicker noise is given as:

$$= \frac{\pi^2}{\gamma_{\text{edge}}^2 C_L^2} \frac{\Delta T^2}{T_{\text{in}}^2} S_{1/f}(f), \quad (3.20)$$

When the transistor is in triode region it acts as resistance and combination of resistance and node capacitance injects kT/C noise. kT/C phase noise contribution of PMOS transistor and NMOS transistor is given as:

$$S_\phi(f) = \frac{2\pi^2}{T_{\text{in}}^2} \frac{1}{\gamma_{\text{edge}}^2} \frac{kT}{C_L f_{\text{in}}}. \quad (3.21)$$

Total Phase Noise:

$$\begin{aligned} S_\phi(f) &= \frac{\pi^2}{\gamma_{\text{edge}}^2 C_L^2} \left[\frac{\Delta T}{T_{\text{in}} S_I(f)} + \frac{\Delta T^2}{T_{\text{in}}^2} S_{1/f}(f) \right]_{\text{PMOS}} \\ &\quad + \frac{\pi^2}{\gamma_{\text{edge}}^2 C_L^2} \left[\frac{\Delta T}{T_{\text{in}} S_I(f)} + \frac{\Delta T^2}{T_{\text{in}}^2} S_{1/f}(f) \right]_{\text{NMOS}} \\ &\quad + \frac{2\pi^2 f_{\text{in}} kT}{\gamma_{\text{edge}}^2 C_L}. \end{aligned} \quad (3.22)$$

The phase noise analysis developed for CMOS inverter is now expanded to study the phase noise of other CMOS gates with transition behaviour modeled similarly to that of inverter.

3.2 Nand PFD

Conventional Type PFD can be realised using different logic gate topology like NAND or NOR. In this work NAND based topology is chosen over NOR based due to its faster switching. We know in CMOS logic implementation every gate is realized using series or parallel combination of NMOS and PMOS transistor. In NOR gate PMOS transistor is in series combination and NMOS in parallel which increases delay due to slower switching of PMOS. In PFD, speed of reset is very crucial for high speed operation. When we are using NAND based PFD, pull-down transistor is NMOS which inhererit the fast switching while in NOR-based PFD reset occurs on PMOS transistor pulling up the output high and it is slower than NMOS pull-down. So, NAND based PFD is faster and used for high speed application.

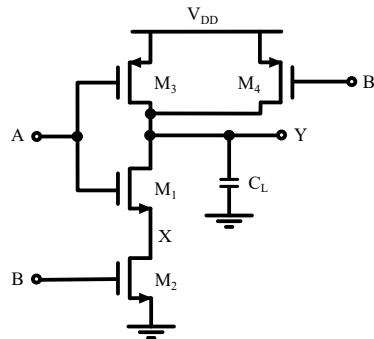


Figure 3.8: NAND gate

The phase noise analysis technique developed for inverter is used for NAND PFD where the switching of the signal through gates should be like that of inverter. So we design a PFD which works as inverter and sizing of series NMOS is done is such a way that it can replaced by single transistor with twice their length. As we have developed understanding through CMOS inverter that the falling edge of pulse takes place through NMOS transistor and rising edge of pulse takes place through PMOS transistor by which the pulse inherit jitter from the respective transistor as shown in Fig. 3.9. If the slew rate is lower then rise time and fall time of CMOS gate is longer which increases the phase noise. So, PFD should be designed in such a way that it has sharp rise and fall time. So we look into the propagation of pulse through the gates of PFD circuits and modulation of jitter on Up and Down pulse from respective gates. We omit the common jitters which is shown in Fig. 3.12.

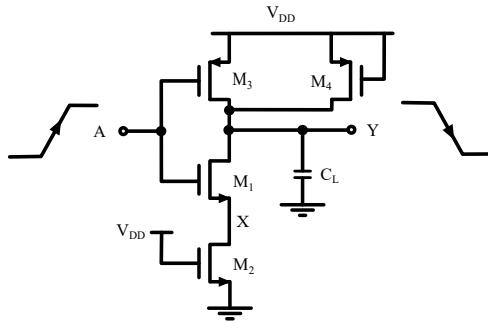


Figure 3.9: NAND gate working as inverter

When we apply falling edge of pulse A at NAND 1 it adds jitter to its falling edge which outputs rising edge of \overline{Up} . As the edge at output is rising PMOS transistor of NAND1 deposits jitter on it. \overline{Up} experiences additional jitter when it passes through NAND 2 to produce output Up. Similarly, Down pulse also experiences jitter from NAND 5 and NAND 6 when falling edge of pulse is applied in B.

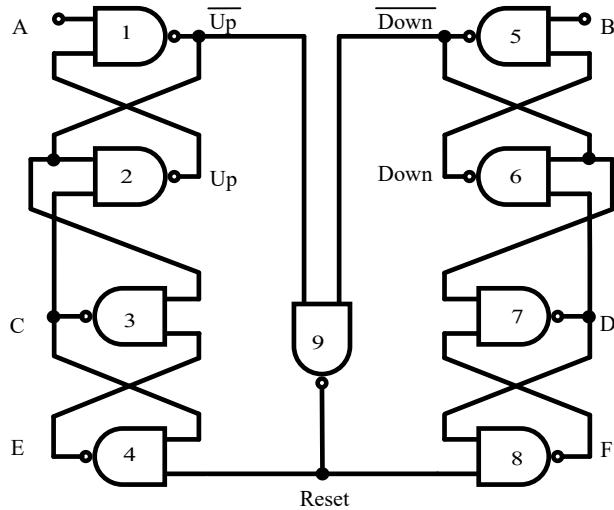


Figure 3.10: NAND based PFD

When we apply falling edge of pulse A at NAND 1 jitter is added to its falling edge which outputs rising edge of \overline{Up} with jitter contribution from NAND 1. As the edge at output is rising PMOS transistor of NAND 1 deposits jitter on it. \overline{Up} experiences additional jitter when it passes through NAND 2 to produce output Up. Similarly, Down pulse also experiences jitter from NAND 5 and NAND 6 when falling edge of pulse is applied in B.

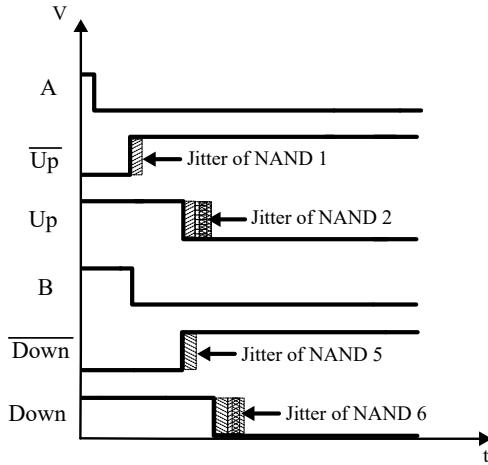


Figure 3.11: Jitter contribution on falling edges

When $\overline{\text{Up}}$ and $\overline{\text{Down}}$ goes Up Reset signal activates which inherits jitter from NAND 5 and NAND 9. As Reset is low output at nodes E and F rises where additional jitter of two gates NAND 4 and NAND 8 are added respectively.

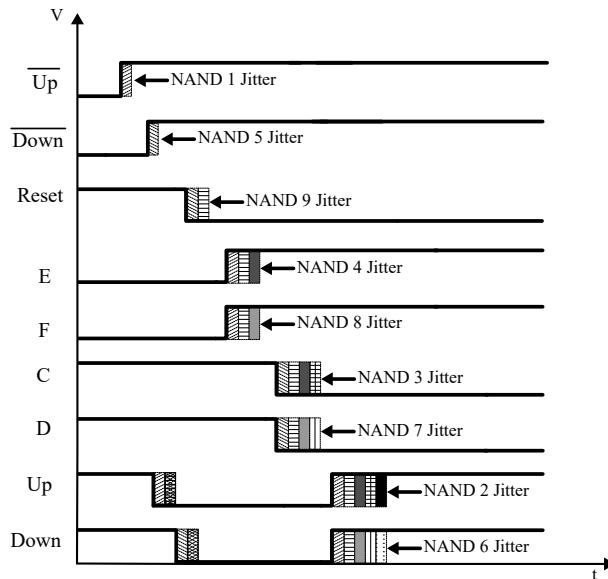


Figure 3.12: Jitter contribution on rising edges

The falling edge at C and D are affected by the jitter contribution of NAND 3 and NAND 7. In this NAND based PFD, NAND 2 contributes jitter to both the rising and falling edges of the Up signal which are uncorrelated meaning that jitter sources contribute separately to the overall timing noise. These two transitions are due to different transistor of NAND gate, rising edge jitter comes from PMOS transistor whereas falling edge jitter comes from an NMOS transistor in series configuration. NAND 6 affects the Down signal in a similar way. The jitter introduced

by NAND 9 is present on the rising edges of both the Up and Down pulses, which cancels the differential effect, making it negligible. PSD of each jitter is summed to obtain total phase noise contribution from PFD. The output from PFD is given at the charge pump which generates error current ΔI . As the jitter is random and not common between the transistors total error current considering jitter from each transistor is given by:

$$\Delta \bar{I}^2 = \frac{I_p^2}{T_{in}^2} \sum_{m=1}^{10} T_m^2. \quad (3.23)$$

$$S_{\phi,PLL}(f) = \frac{4\pi^2}{T_{in}^2} M^2 \sum_{m=1}^{10} S_{Tm}(f), \quad (3.24)$$

where $S_{Tm}(f)$ is spectral density of jitter component. Considering similar rise and fall time of each gate in-band phase noise of PLL is given by:

$$S_{\phi,PLL} \equiv 10M^2 \left[\frac{4\pi^2 \Delta T}{\gamma_{edge}^2 C_L^2 T_{in}} S_I(f) + \frac{4\pi^2 \Delta T^2}{\gamma_{edge}^2 C_L^2 T_{in}^2} S_{1/f}(f) + \frac{4\pi^2 f_{in} kT}{\gamma_{edge}^2 C_L} \right]. \quad (3.25)$$

The equation 3.25 represents the in-band phase noise of PFD where jitter from 10 transistors in NAND based PFD is accumulated to obtain phase noise of PLL.

3.3 TSPC PFD

Deploying the analysis of Phase Noise of inverter in TSPC PFD topology. We perform phase noise analysis of a TSPC PFD which has high importance in high speed applications. When a rising edge is given at A it turns on transistor M_5 and when M_6 turns on, Up output is discharged. Similarly when there is rising edge at B and M_{12} turns on, Down output is discharged. Once Up and Down signal are low then reset rises which turns on NMOS transistor M_3 and M_9 discharging nodes C and D. Low value at node C and D forces Up and Down to go high.

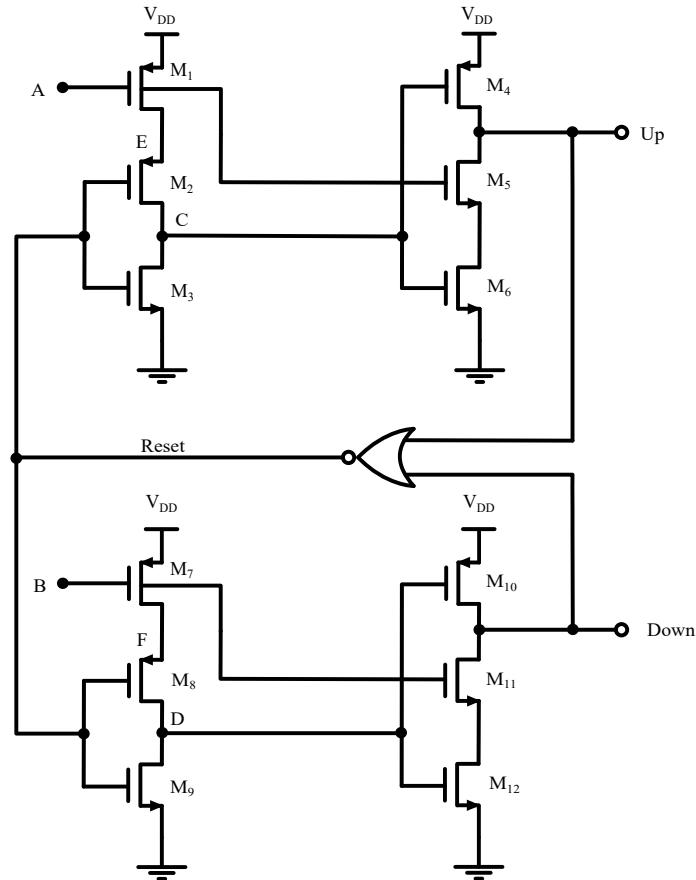


Figure 3.13: TSPC PFD

We can follow the signal's path and its transitions (high-to-low or low-to-high) through the circuit to analyze the jitter contributions from each transistor. As mentioned earlier, when the Up and Down signals fall, they are influenced by jitter introduced by transistors $M_5 - M_6$ in series and $M_{11} - M_{12}$. The reset pulse also encounters jitter due to the action of transistors $M_5 - M_6$ and the NOR gate. Then, the falling edges at C and D inherit both the jitter from the reset pulse and the jitter caused by transistors M_3 and M_9 . Finally, as the signals reach their final Up and Down states through transistors M_4 and M_{10} , the jitter from these transistors also impacts the overall jitter of the signals. As we observe the Up and Down signal, jitter from NOR gate modulates both of them equally and hence we can conclude that it can be ignored as symmetrical jitter does not produce any impact on pulse width difference of Up and Down signals resulting no change at Charge Pump output. For example: Let t_{delay} be the time difference between Up and Down Signal ($t_{\text{delay}} = t_{\text{Up}} - t_{\text{Down}}$). If both Up and Down pulses are widened by jitter of NOR gate Δt then relative time difference between them remains constant.

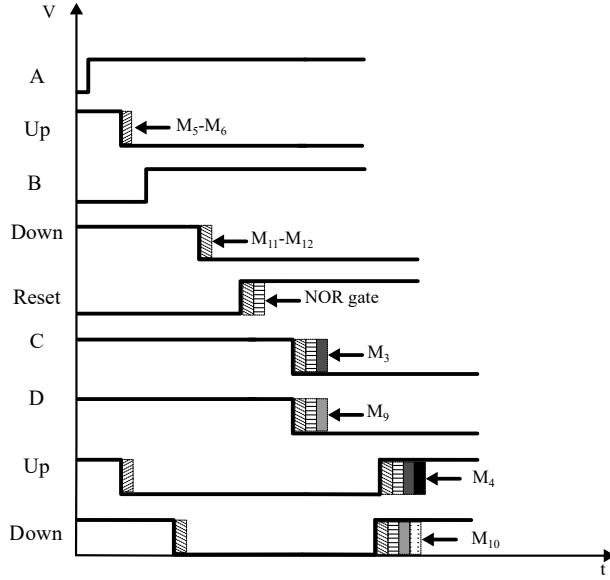


Figure 3.14: Jitter contribution of each transistor in TSPC PFD

Therefore the overall phase noise of TSPC PFD arises from six transistors and is less than that of NAND PFD. In this TSPC PFD configuration the noise injection is similar to that of inverter and NAND gates where the operating transistor injects flicker and thermal noise and transistor turning off deposits kT/C noise. In this PFD architecture there are less number of transistor which contribute jitter to the signal. Thus, the equation describing the spectra of phase noise is expressed as:

$$S_{\phi,PLL} \equiv 6M^2 \left[\frac{4\pi^2\Delta T}{\gamma_{edge}^2 C_L^2 T_{in}} S_I(f) + \frac{4\pi^2\Delta T^2}{\gamma_{edge}^2 C_L^2 T_{in}^2} S_{1/f}(f) + \frac{4\pi^2 f_{in} kT}{\gamma_{edge}^2 C_L} \right]. \quad (3.26)$$

Similarly, in TSPC based PFD the jitter from 6 transistor is injected in Up and Down signal which accumulates and result in phase noise of PFD. So, in equation 3.25 10 can be replaced by 6 to obtain in-band phase noise of PLL which is given in equation 3.26 above. For the simulation of these PFD with same power and frequency we follow the optimization technique.

3.4 Design Optimization

Increasing the width of the transistor can enhance phase noise performance, but this comes at the cost of higher power consumption. So considering this tradeoff sizing of the transistor should be done to minimize the phase noise. Approximations for this optimization technique are, The node capacitance is directly related to the sizes of both the driver and driven transistors

$(C_L \propto \eta W_a + W_b)$. Flicker noise drain current spectrum is given by $S_{1/f}(f) = g_m^2 K_f / W_a L_a C_{ox} f$. When the gate-to-source voltage increases to the supply voltage, the drain current becomes directly proportional to the width of the driving transistor, which in turn influences the slew rate, $\gamma_{edge} \propto I_D / C_L \propto W_a / C_L$. Then the equation of phase noise can be written as:

$$S_\phi(f) \propto \frac{f_{in}^2 V_{DD}^2 C_L^2}{W_a^3} \frac{1}{f}. \quad (3.27)$$

For given values of f_{in}, V_{DD} , and f ,

$$S_\phi(f) \propto \frac{(\eta W_a + W_b)^2}{W_a^3}. \quad (3.28)$$

Power Consumption by the CMOS inverter in one cycle is given as $P = f_{in} C_L V_{DD}^2$.

NAND PFD Optimization

In the NAND PFD section, we stated that phase noise was contributed by 10 transistors now, let us analyze the path of signal from input A to the output Up and the jitter contributions from each transistor. At Up signal , the phase noise arises from PMOS transistor of NAND1, NMOS transistor from NAND 2, PMOS transistor from NAND 4, NMOS transistor from NAND 3 and PMOS transistor from NAND 2. The phase noise

$$P \propto f_{in} V_{DD}^2 \left[2 \sum_{j=1}^4 (W_{Pj} + W_{Nj}) + W_{P9} + W_{N9} \right] \quad (3.29)$$

TSPC PFD Optimization

In the discussion above we have concluded that six transistors contribute noise to the TSPC based PFD design so the total power consumption is derived as:

$$P \propto f_{in} V_{DD}^2 \left[2 \sum_{j=1}^6 W_j + W_{P,NOR} + W_{N,NOR} \right] \quad (3.30)$$

This optimization technique assigns maximum width to the transistor carrying the signal, while the transistor not carrying the signal is assigned minimum width. After the size is obtained from the optimization the sizing of gates are changed manually to ensure fast transitions of signal.

Chapter 4

Results

The PFD circuit was simulated in 65-nm CMOS technology. We obtained the result from simulation and compared it with the result of the analytical conclusions. For hand calculations various terminologies are obtained from ac and transient simulation of the circuits. Understanding of jitter and phase noise was initially developed using a CMOS inverter and subsequently extended to analyze NAND-based PFD and TSPC PFD architectures.. So lets us begin our simulation with CMOS inverter. A chain of eight inverter was simulated with and without additional capacitance of 20fF at each node. Comparing the results using Cadence pnoise simulations we observed that with increase in capacitance there is degradation in phase noise. The hand calculation of NAND and TSPC based PFD is done. The parameters are taken from transient simulation in cadence virtuoso. Calculation of thermal noise and flicker noise is given as:

$$S_\phi(f) = \frac{\pi^2}{\gamma_{edge}^2 C_L^2} \frac{\Delta T}{T_{in}} S_I(f), S_I(f) = 4kT\gamma g_m, g_m = \frac{2I_D}{V_{GS} - V_{th}}$$

$$k = 1.38 \times 10^{-23} \text{ J/K}, I_D = 6.34 \times 10^{-7} \text{ A}, \gamma = 2/3, \Delta T = 9 \times 10^{-12} \text{ s}, f_{in} = 1 \text{ GHz}$$

Substituting the values in equation of thermal noise we get,

$$S_\phi(f) = \frac{\pi^2}{\gamma_{edge}^2 C_L^2} \frac{\Delta T^2}{T_{in}^2} S_{1/f}(f), S_{1/f}(f) = \frac{g_m^2 K_f}{W_a L_a C_{ox} f}, \gamma_{edge} = I_D / C_L$$

$$K_f = 10^{-25}, \quad W = 600 \text{ nm}, \quad L = 65 \text{ nm}, \quad C_{ox} = 1.11 \times 10^{-4} \text{ F/m}^2$$

Phase Noise(in dBc/Hz):

$$\mathcal{L}(f) = 10 \log_{10} \left(\frac{\text{Noise Power}}{\text{Carrier Power}} \right) \quad (4.1)$$

For NAND PFD:

Flicker Noise at 1 MHz offset with an operating frequency of 1GHz is, -154dBc/Hz and similarly for other offset frequency f should be replaced by f_{offset} .

For an operating frequency of 2 GHz,-148dBc/Hz.

Thermal Noise is frequency-independent and equal to -156 dBc/Hz for operating frequency of 1 GHz and equal to -153 dBc/Hz for operating frequency of 2 GHz.

For TSPC PFD:

Flicker Noise at 1 MHz offset with an operating frequency of 1GHz is, -161dBc/Hz and similarly for value of flicker noise at other offset frequencies f should be replaced by f_{offset} .

For an operating frequency of 2 GHz, -155 dBc/Hz.

Thermal Noise is frequency-independent and equal to -161 dBc/Hz at 1GHz operating frequency and -158 dBc/Hz at 2GHz operating frequency.

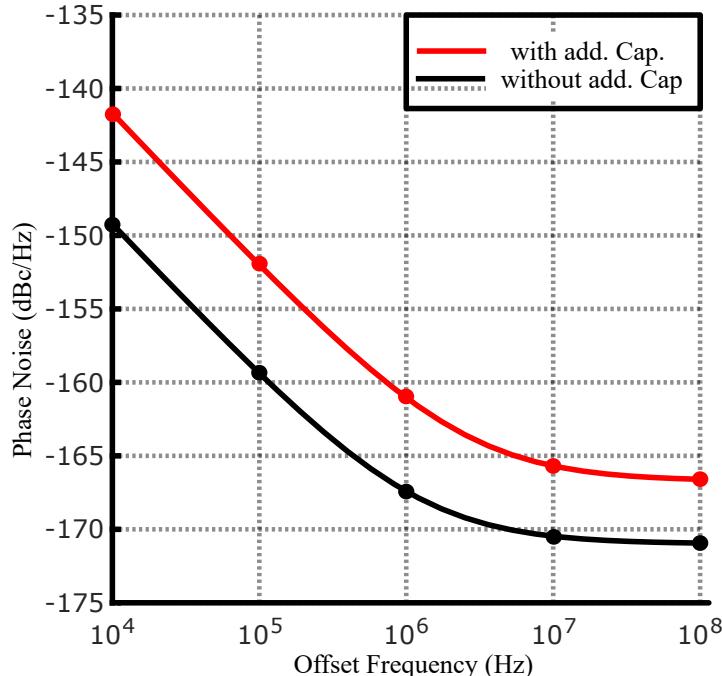


Figure 4.1: Phase noise of inverter chain

PFD Simulations

Both NAND and TSPC PFD are simulated with given sizing after design optimization.

Table 4.1: Gate sizing of TSPC PFD

Transistor	Size (μm)
W_1, W_7	6
W_2, W_8	6
W_3, W_9	12
W_4, W_{10}	30
W_5, W_{11}	10
W_6, W_{12}	10
$W_{P,NOR}$	10
$W_{N,NOR}$	2

Table 4.2: Gate sizing of NAND PFD

Transistor	Size (μm)
W_{P1}, W_{P5}	11
W_{N1}, W_{N5}	0.6
W_{P2}, W_{P6}	8.5
W_{N2}, W_{N6}	6
W_{P3}, W_{P7}	10
W_{N3}, W_{N7}	2
W_{P4}, W_{P8}	7.5
W_{N4}, W_{N8}	0.6
W_{P9}	2
W_{N9}	0.6

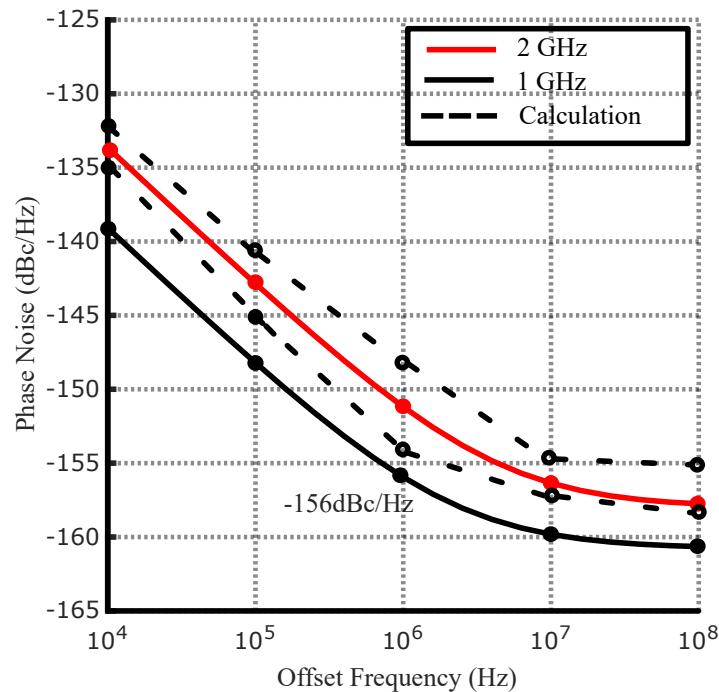


Figure 4.2: Phase noise characteristics of a NAND PFD across varying input frequencies.

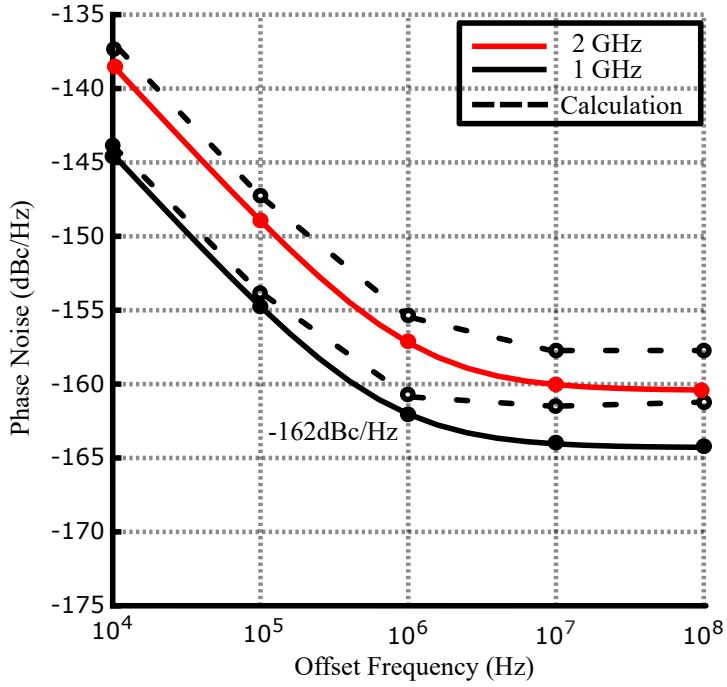


Figure 4.3: Phase noise characteristics of a TSPC PFD across varying input frequencies.

The power consumption and operating frequency is kept constant and phase noise of each PFD is calculated and result was obtained that phase noise of TSPC PFD is better than NAND based PFD. Second observation is that increase in operating frequency degrades phase noise by 3dB in thermal noise and 6dB in flicker noise. By using the design optimization technique where the transistor passing signal is provided with maximum width and other transistor are given minimum width for a fixed power consumption we obtain the improvement in phase noise of PFD when compared with [11] and [12]. The hand calculation is varied 3 to 4 dB from simulation result.

Table 4.3: Comparison table of phase noise of different PFD architectures

Parameter	Unit	Conv.	TSPC-based	[11]	[12]
Architecture	-	NAND	TSPC	Symmetrical	Resetless
Process	μm	0.65	0.65	0.18	0.18
Supply	V	1	1	1.8	1.8
Phase Noise	dBc/Hz	-156	-162	-150	-147
Power	mW	0.4	0.4	0.47	0.05

Chapter 5

Conclusion and Future Work

5.1 Conclusion

In conclusion, phase noise can be determined by accounting for the jitter contributions of individual transistors, which collectively influence the overall phase noise of the PFD. A strong correlation between phase noise and operating frequency is evident. The findings reveal that doubling the operating frequency leads to a 3 dB degradation in thermal noise and a 6 dB degradation in flicker noise. Furthermore, this study demonstrates that an increase in the number of transistors contributes to higher jitter, ultimately causing a degradation in overall phase noise performance.

5.2 Future Work

Analysis of phase noise done in PFD circuit is based on basic CMOS inveter and later extended to other CMOS gates which are building blocks of PFD. This method can be further extended to other blocks of PLL like VCO and frequency divider.

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