Code: 15A05402 **R15**

B.Tech II Year II Semester (R15) Supplementary Examinations December 2018

COMPUTER ORGANIZATION

(Common to CSE and IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Registers R_1 and R_2 contain data values 1800 and 3800 respectively in decimal and the word length of the processor is 4 bytes. What is the effective address of the memory operand for the instruction ADD 100(R_2), R_6?

(b) What is the use of buffer register?

(c) State the principle of operation of a carry look-ahead adder.

(d) Write the Add/subtract rule for floating point numbers.

(e) What will be the width of address and data buses for a 512K* 8 memory chip?

(f) Differentiate static RAM and dynamic RAM.

(g) Why does DMA have priority over the CPU when both request a memory transfer?

(h) What is bus arbitration?

(i) Is register renaming is done in pipelined processor to handle certain kinds of hazard? Justify your answer.

(j) How an array processor helps to improve the performance in arithmetic operations?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) List the steps needed to execute the machine instruction add LOC, R0 in terms of transfers between memory and processor and some simple control commands. Assume that the instruction itself is stored in the memory at location INSTR and that this address is initially in register PC.

(b) How the addresses can be assigned across the words by using the big-endian and the little-endian representations?

OR

3 Exemplify different functional units of a digital computer. Mention the functions of different processor registers such as IR, MAR and PC.

UNIT – II

4 Compare the restoring and non-restoring division algorithm. Perform the division using the restoring division algorithm. Dividend = 1000, Divisor = 11.

OR

5 With a neat block diagram, explain about the micro programmed control unit and its operations in detail?

UNIT – III

6 A computer system has a main memory consisting of 16 M words. It also has a 32K word cache organized in the block-set-associative manner, with 4 blocks per set and 128 words per block.

(a) Calculate the number of bits in each of the TAG, SET and WORD fields of the main memory address format.

(b) How will the main memory address look like for a fully associative mapped cache?

OR

7 Discuss the operation of memory hierarchy with a neat sketch.

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UNIT – IV

8 Identify and explain the various methods available to handle multiple devices using interrupts.

OR

9 With a neat sketch, discuss various standard I/O interfaces in detail?

UNIT – V

10 Why the data hazards occur in the pipelining process? Explain the methods for dealing with data hazard using your own example.

OR

11 Categorize and discuss various forms of parallel processing based on Flynn's taxonomy with a neat sketch.

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Code: 15A05402

R15

B.Tech II Year II Semester (R15) Regular Examinations May/June 2017

COMPUTER ORGANIZATION

(Common to CSE and IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What are the two possibilities of increasing the clock rate?

(b) Define register mode with example.

(c) Describe the configuration of n-bit ripple-carry adder.

(d) Define control word.

(e) List the advantages of using cache memory.

(f) Define access time.

(g) What are vectored interrupts?

(h) List two key objectives of universal serial bus.

(i) What is the use of pipelining?

(j) Draw an example 3-dimentional hypercube network.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) What is system software? What are the various functions performed by system software?

(b) Describe indirect addressing mode with suitable examples.

OR

3 Draw the basic functional unit of computer and explain each unit in detail.

UNIT – II

4 (a) Assuming 6-bit 2's-complement number representation, multiply the multiplicand A = 110101 by the multiplier B = 011011 using the normal Booth algorithm.

(b) Draw the basic structure for data processing unit and discuss in detail about it.

OR

5 Illustrate Bit-Pair recoding of multipliers derived form Booth recoding with example.

UNIT – III

6 (a) Suppose that a computer has a processor with two L1 caches, one for instructions and one for data and an L2 cache. Let τ be the access time for the two L1 caches. The miss penalties are approximately 15τ for transferring a block from L2 to L1, and 100τ for transferring a block from the main memory to L2. For the purpose of this problem, assume that the hit rates are the same for instructions and data and that the hit rates in the L1 and L2 caches are 0.96 and 0.80, respectively.

(i) Suppose that the L2 cache has an ideal hit rate of 1. By what factor would this reduce the average memory access time as seen by the processor?

(ii) Consider the following change to the memory hierarchy. The L2 cache is removed and the size of the L1 caches is increased so that their miss rate is cut in half. What is the average memory access time as seen by the processor in this case?

(b) What are the advantages and applications of flash memories?

OR

7 Describe virtual-memory address-translation method based on the concept of fixed-length Pages with a neat block diagram.

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UNIT – IV

8 Describe the use of DMA controllers in a computer system with a neat block diagram.

OR

9 Define interrupt? Illustrate the transfer of control through the use of interrupts.

UNIT – V

10 (a) Define hazard? Explain in detail about data hazards.

(b) Describe the general classification of parallel processing systems.

OR

11 Illustrate three possible ways of implementing a multiprocessor system with neat diagrams.

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B.Tech II Year II Semester (R15) Regular & Supplementary Examinations May/June 2018

COMPUTER ORGANIZATION

(Common to CSE & IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Compare and contrast RISC & CISC.
(b) What are the basic functional units of a computer?
(c) Perform the subtraction operation for the following numbers: $(63)_{10}$ and $(-17)_{10}$.
(d) What is meant by bit pair recoding? Give an example.
(e) Differentiate static and dynamic memory.
(f) Compare hit rate and miss rate.
(g) How does the processor handle an interrupt request?
(h) Differentiate synchronous bus and asynchronous bus.
(i) What is meant by RAW hazard and WAW hazard?
(j) Mention few interconnection networks that are commonly used in multiprocessors.

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Give a short sequence of machine instructions for the task: "Add the contents of memory location A to those of location B, and place the answer in location C." Instructions load LOC, R_i and store R_i LOC are the only instructions available to transfer data between the memory and general purpose register R_i. Do not destroy the contents of either location A or B.

OR

3 Discuss about the various types of addressing modes with examples in detail.

UNIT – II

4 Multiply the following unsigned numbers using Booth's algorithm: Multiplicand = 1000, multiplier = 0011.

OR

5 Draw the organization of the typical hardwired control unit and explain the various functions performed by the various blocks.

UNIT – III

6 A digital computer has a memory unit of 64K*16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block and word fields of the address format? How many blocks can the caches accommodate?

OR

7 Discuss how the virtual address is converted into real address in a paged virtual memory system with a neat sketch.

UNIT – IV

8 Exemplify the use of vectored interrupts in processes. Why priority handling is desired in interrupt controllers? How does the different priority scheme work?

OR

9 Draw the typical block diagram of a DMA controller and explain how it is used for direct data transfer between memory and peripherals.

UNIT – V

10 Exemplify how pipeline helps to speed up the processor. Discuss the types of hazard that have to be taken care of in a pipelined processor.

OR

11 What is the purpose of parallel processing? Categorize and discuss the various forms of parallel processing with a neat sketch.

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Code: 15A05402 **R15**

B.Tech II Year II Semester (R15) Supplementary Examinations December 2017

COMPUTER ORGANIZATION

(Common to CSE and IT)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What is the use of compiler?
(b) Define absolute mode with example.
(c) Draw the IEEE standard floating point format for double precision.
(d) What are the actions required for executing an instruction?
(e) Compare SRAM and DRAM.
(f) Describe virtual memory.
(g) What is program-controlled I/O?
(h) What are the functions carried out by DMA controller?
(i) Define structural hazard.
(j) What are the advantages of array processors?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 (a) List and explain the four general categories of modern computers.
(b) What are the two key characteristics of RISC instructions set? Explain RISC instruction set with suitable examples.

OR

3 (a) What are the two classes of storage? Explain the two classes in detail.
(b) Illustrate assembly language notation with suitable examples.

UNIT – II

4 Perform multiplication of signed numbers (+13)*(-6) by using Booth's algorithm.

OR

5 Draw and explain the three-bus structure used to connect registers and ALU of a processor.

UNIT – III

6 (a) Suppose that a computer has a processor with two L_1 caches, one for instructions and one for data and an L_2 cache. Let τ be the access time for the two L_1 caches. The miss penalties are approximately 15τ for transferring a block from L_2 to L_1 and 100τ for transferring a block from the main memory to L_2. For the purpose of this problem, assume that the hit rates are the same for instructions and data and that the hit rates in the L_1 and L_2 caches are 0.96 and 0.80 respectively.
(i) What fraction of accesses miss in both the L_1 and L_2 caches, thus requiring access to the main memory. (ii) What is the average access time as seen by the processor?
(b) Discuss about the various memory management requirements in detail.

OR

7 Describe the different mapping procedures in organization of cache memory

UNIT – IV

8 (a) What is the use of interrupts in operating systems? Discuss.
(b) Draw and explain the detailed timing diagram for input transfer on a synchronous bus.

OR

9 Draw and explain the implementation of Input interface circuit.

UNIT – V

10 (a) Describe the reasons for instruction hazards in detail.
(b) Give a brief note crossbar networks.

OR

11 What is pipelining? Illustrate the hardware organization of four stage pipeline with a neat block diagram.

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