STEPS FOR STANDARD CELL DESIGN

STEP 1 : Layout XL ⇒ New File ⇒ Cell name ⇒ "OK"

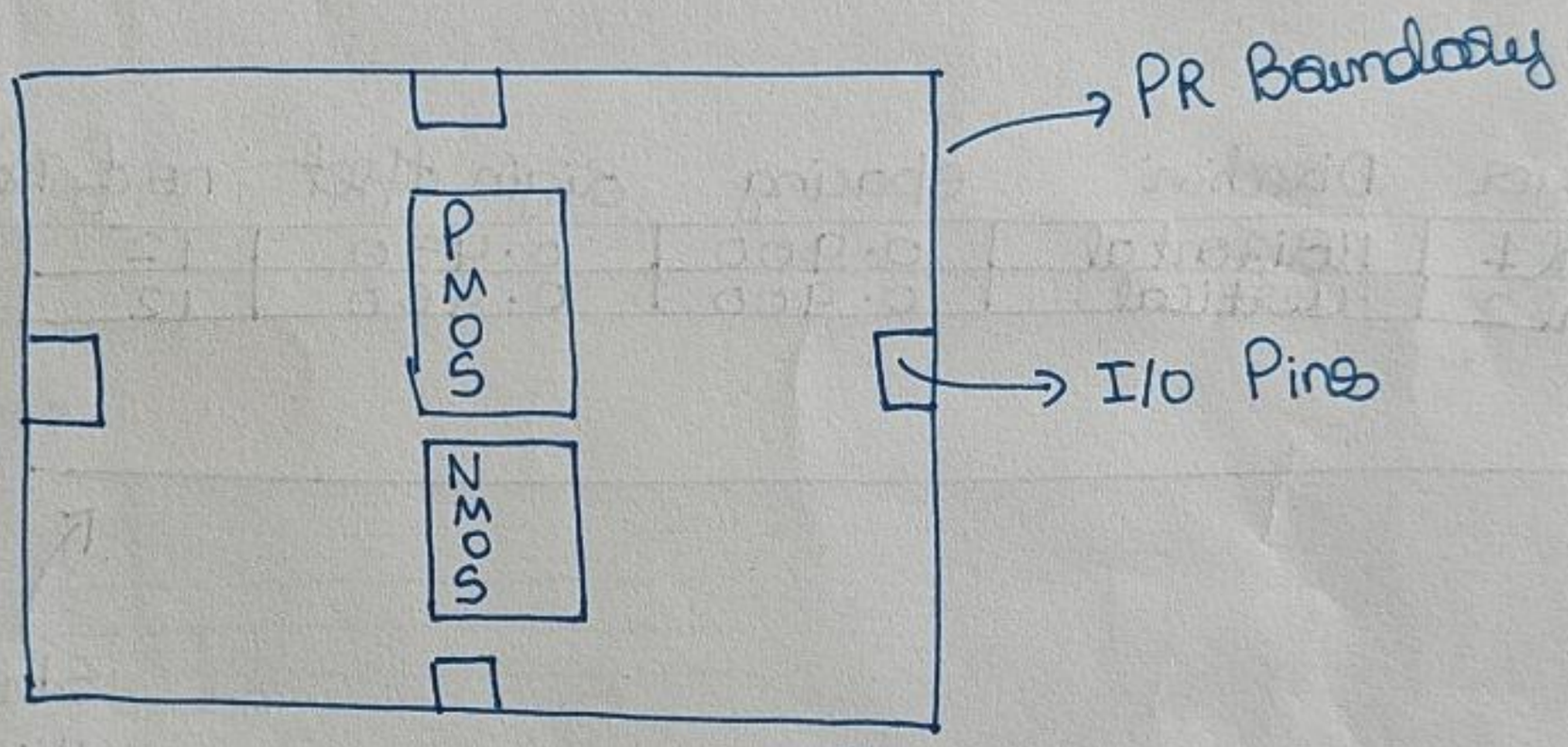
STEP 2 : Connectivity ⇒ All From Source

⇓ Generate Layout

Ensure I/O Pins mode to Metal

⇓

"OK"



NOTE: Press "SHIFT + F" to Show

STEP 3: Delete the PR boundary and Generate Track Pattern

Create ⇒ P&R object ⇒ Track Patterns

Layer : Metal 1

Direction: Horizontal

Spacing: 0.900

Origin Offset : 0.450

no of Tracks : 12

"click update"

do the Same again

Layer : Metal 2

Direction : Vertical

Spacing : 0.90

Origin Offset : 0.450

no of Tracks : 12

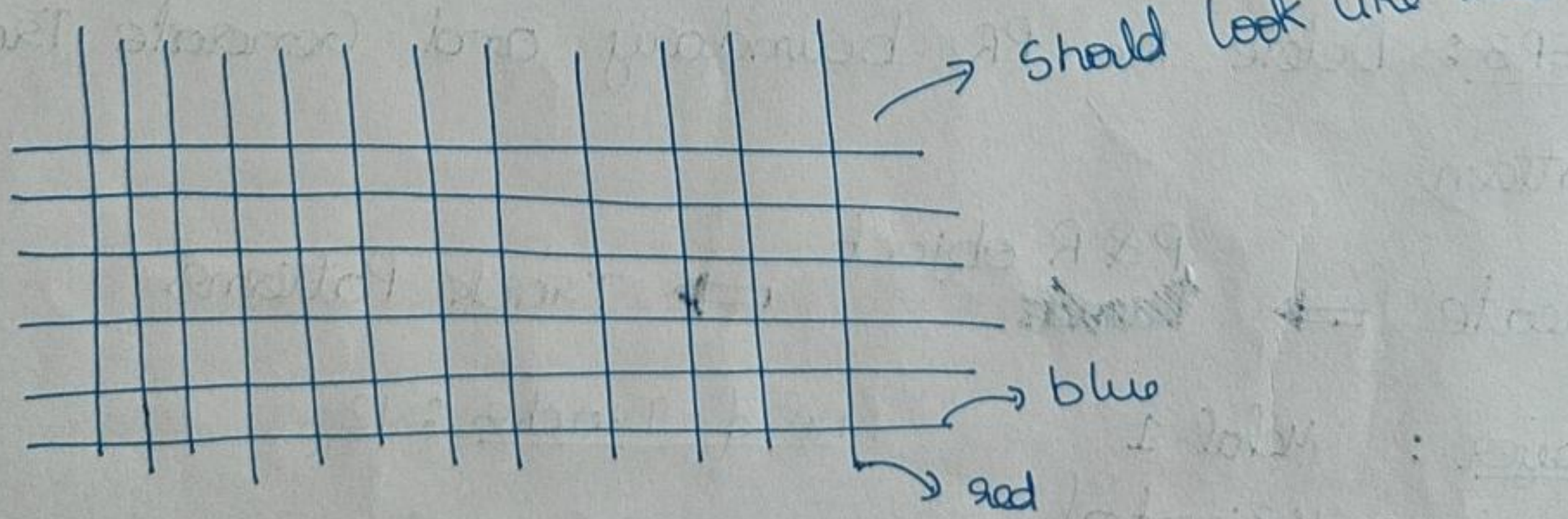
" click update "

" close "

Layer	Direction	Spacing	Origin Offset	no of Tracks
Metal 1	Horizontal	0.900	0.450	12
Metal 2	Vertical	0.900	0.450	12

↖ Should look like this

⇒ Grids ⇒ Tracks



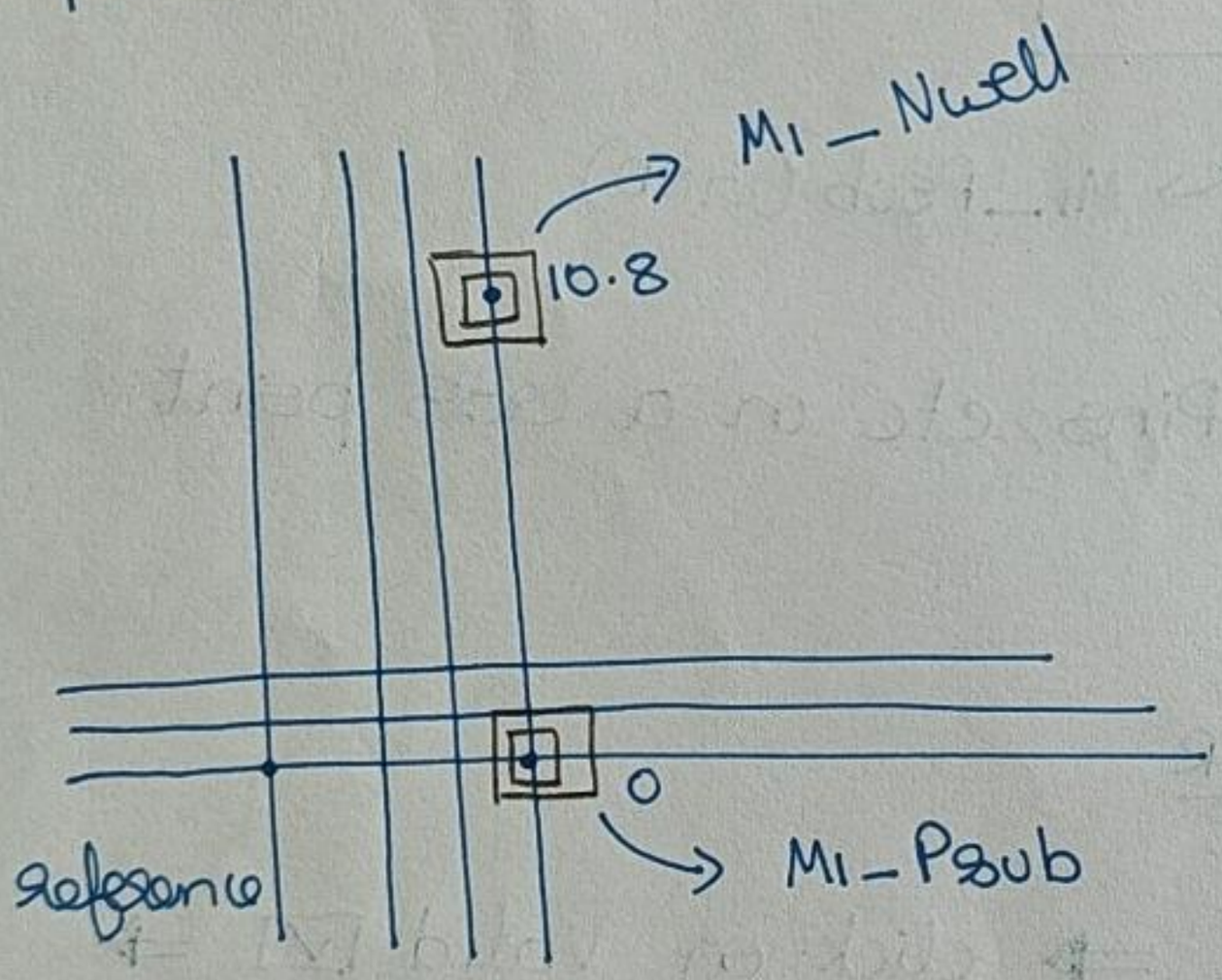
STEP4: LABELS

Click L ⟹ Label (Pattern) { A Z VDD GND }

click on the appropriate Pins to label them.

STEP5: Place Via

use k for Scale ⟹ Start Origin ⟹ measure 10.8 and press

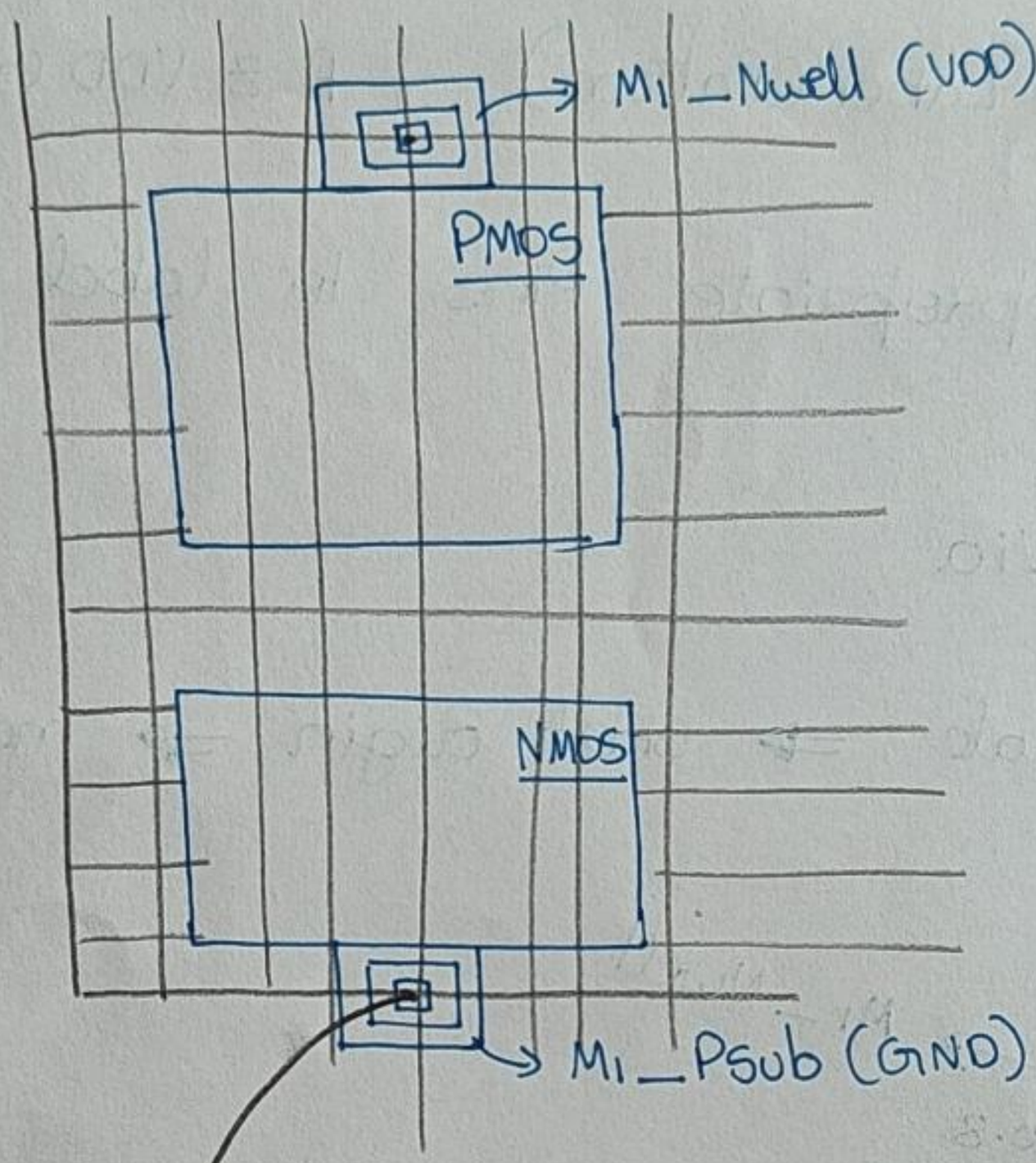


" Press 0" ⟹ VDD → use M1 – Nwell
GND → use M1 – Psub

STEP6: ALIGN NMOS and PMOS

" click A" ⟹ Select the object ⟹ click where to align

ensure we place the nMOS / PMOS as shown



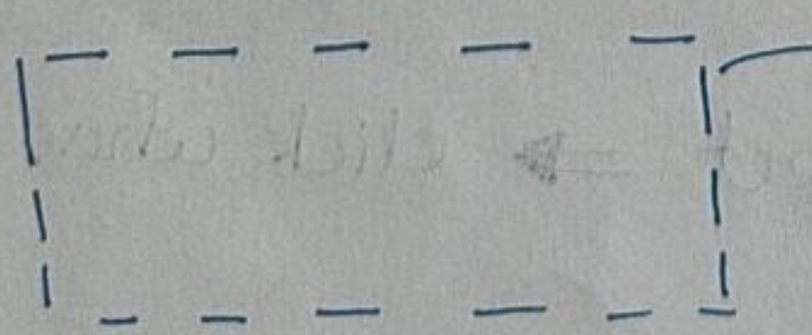
[always place Via, Pins, etc on a cross point and not alone.]

STEP 7: FIXING METAL LAYER

⇒ check left-bottom side ⇒ click on Valid ☑ ⇒

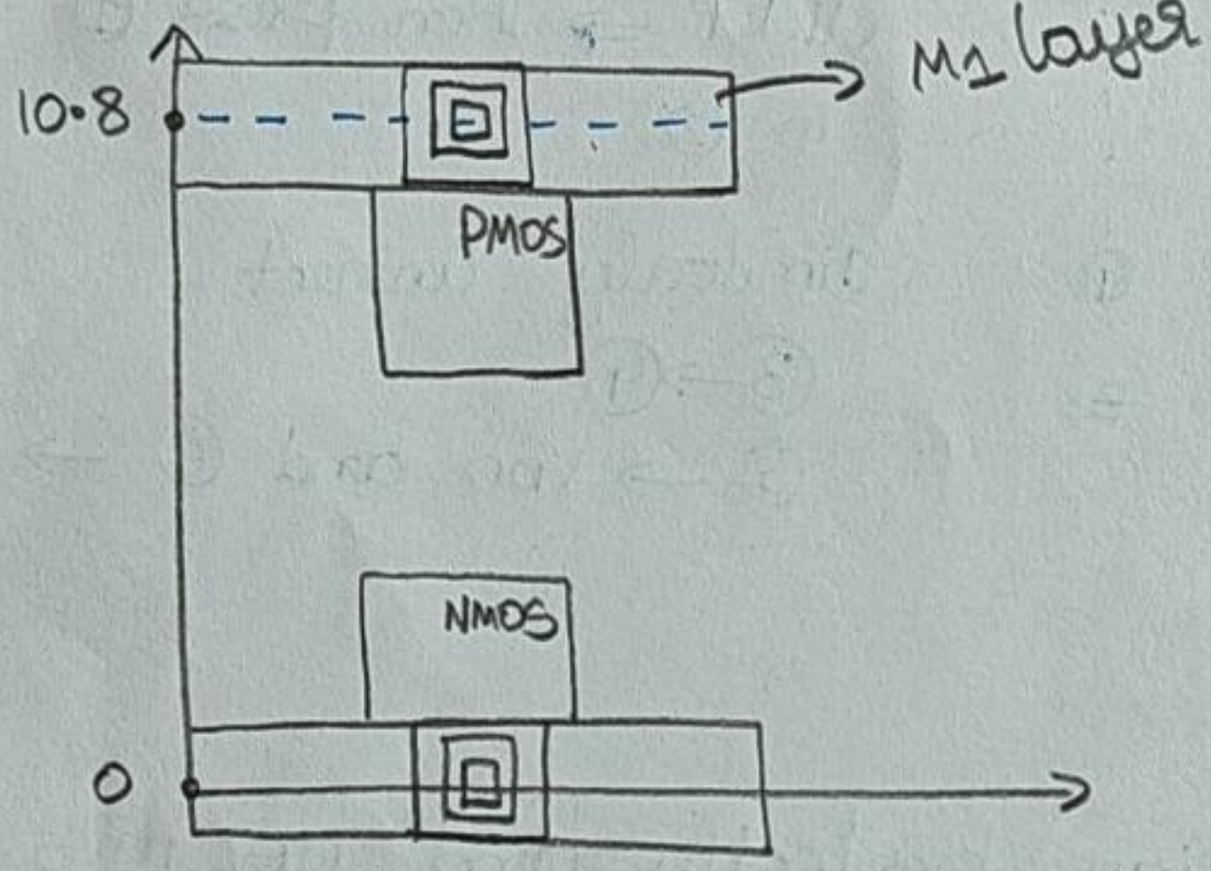
choose Metal 1

"click R" ⇒ Drag and draw a rectangle

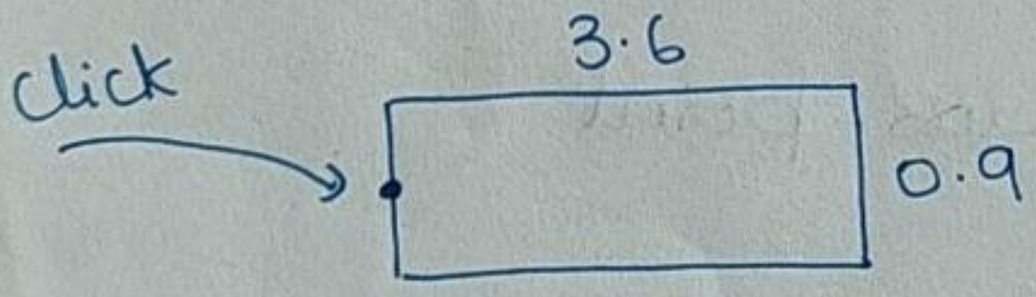


choose height = 0.9
width = 3.6

⇒ now we need to align it



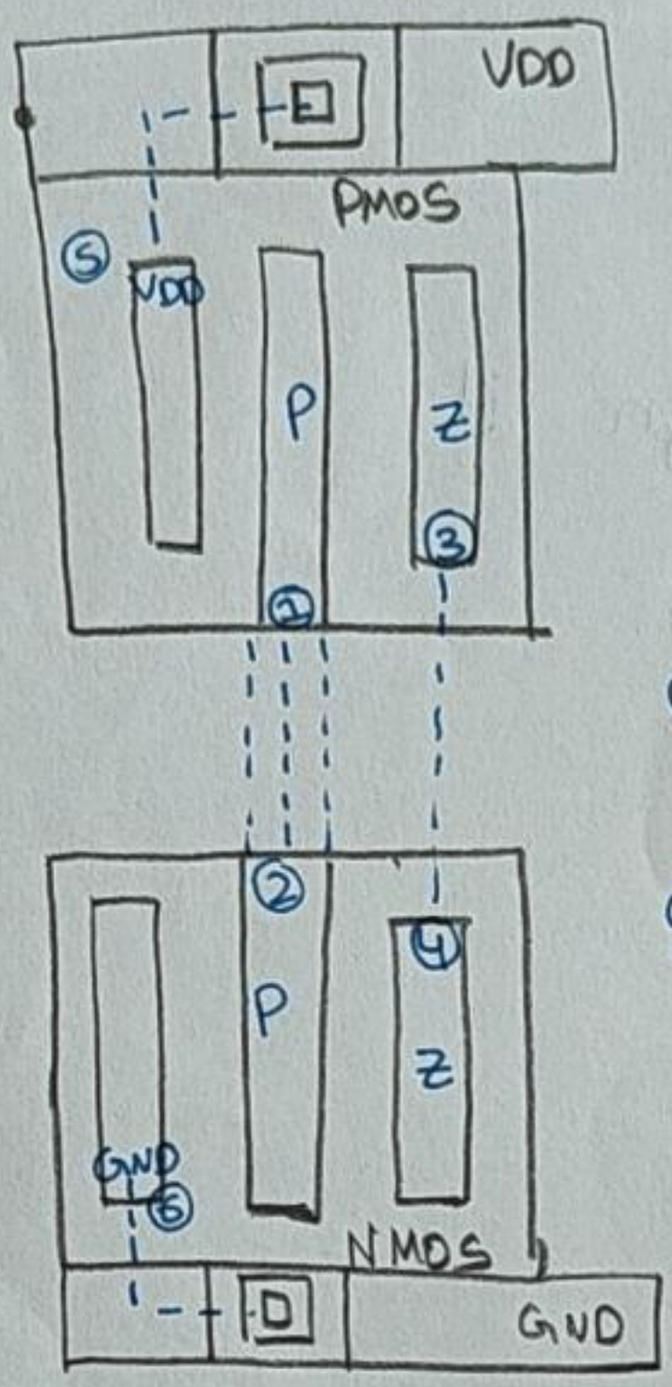
ensure we keep the alignment by Pressing A



then place it as shown at 10.8 and 0 respectively.

STEP8: Connect Poly, VDD, GND, and Z

we need to connect the respective layers by "clicking p" and then connecting



Click P ⇒ then press ① ⇒ connect to ②

Similarly connect

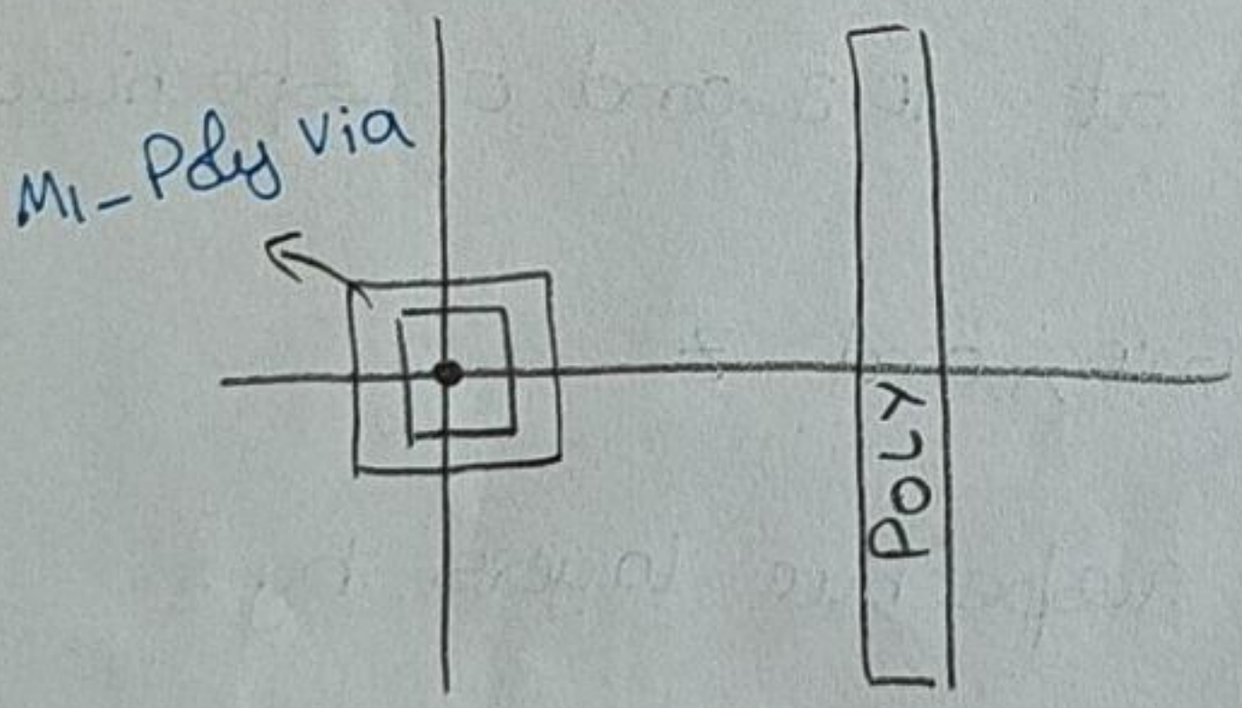
③ → ④

⑤ → VDD and ⑥ → GND

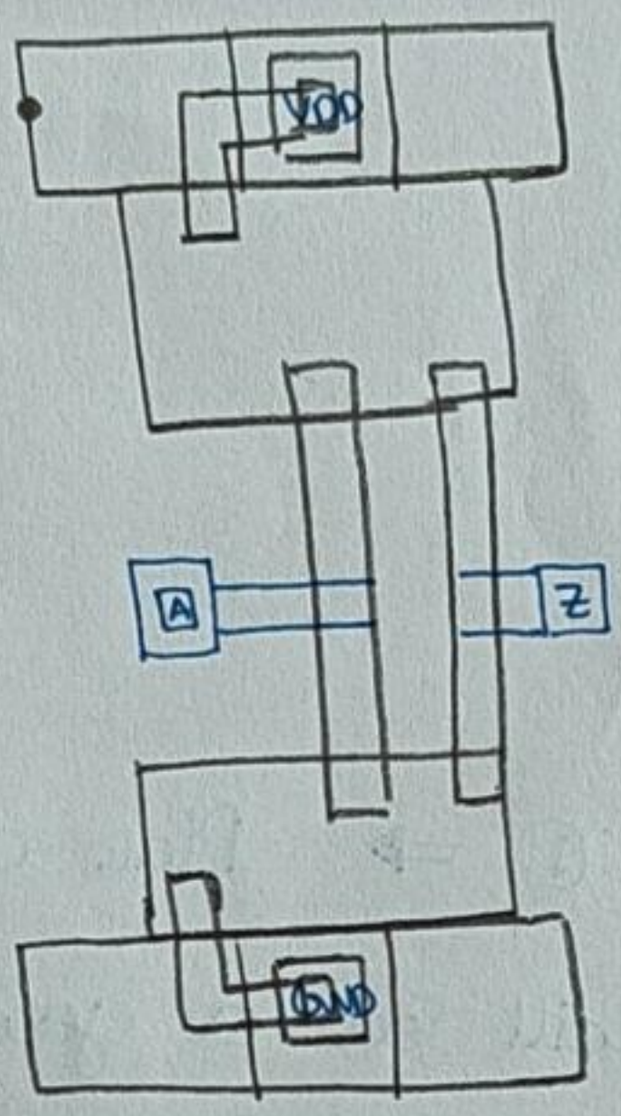
Ensure that they align perfectly and no mis-match

STEP 9: Place Pins

when placing, ensure at a cross-point



" click A" ⇒ click at center of Pin ⇒ Palace right at the center of via



Assist

we can use this assistant to check for unconnected pins.

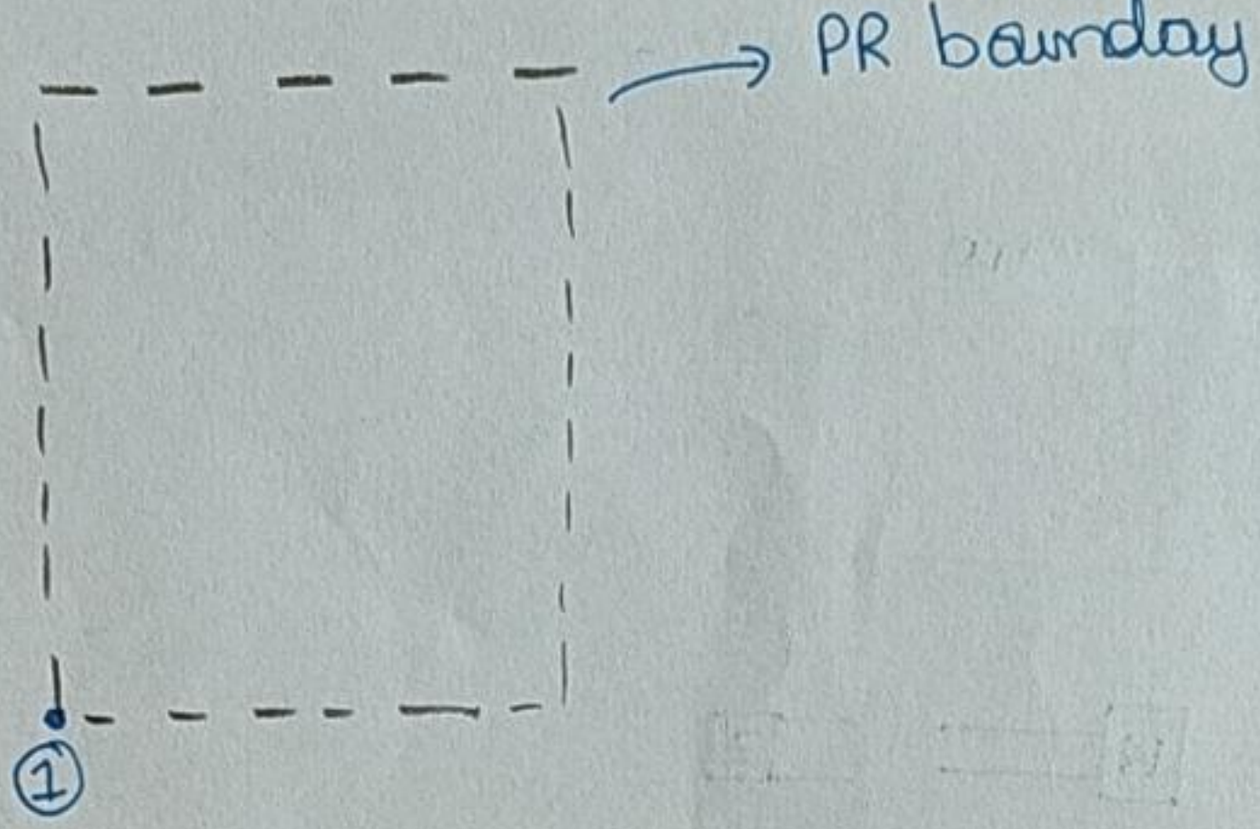
do ensure VDD, GND, A, Z are all placed at cross-points which also Includes aligning via.

STEP 10: Creating PR boundary

In the search box ⟹ Pr boundary ⟹ click and draw using R ⟹ select & press O

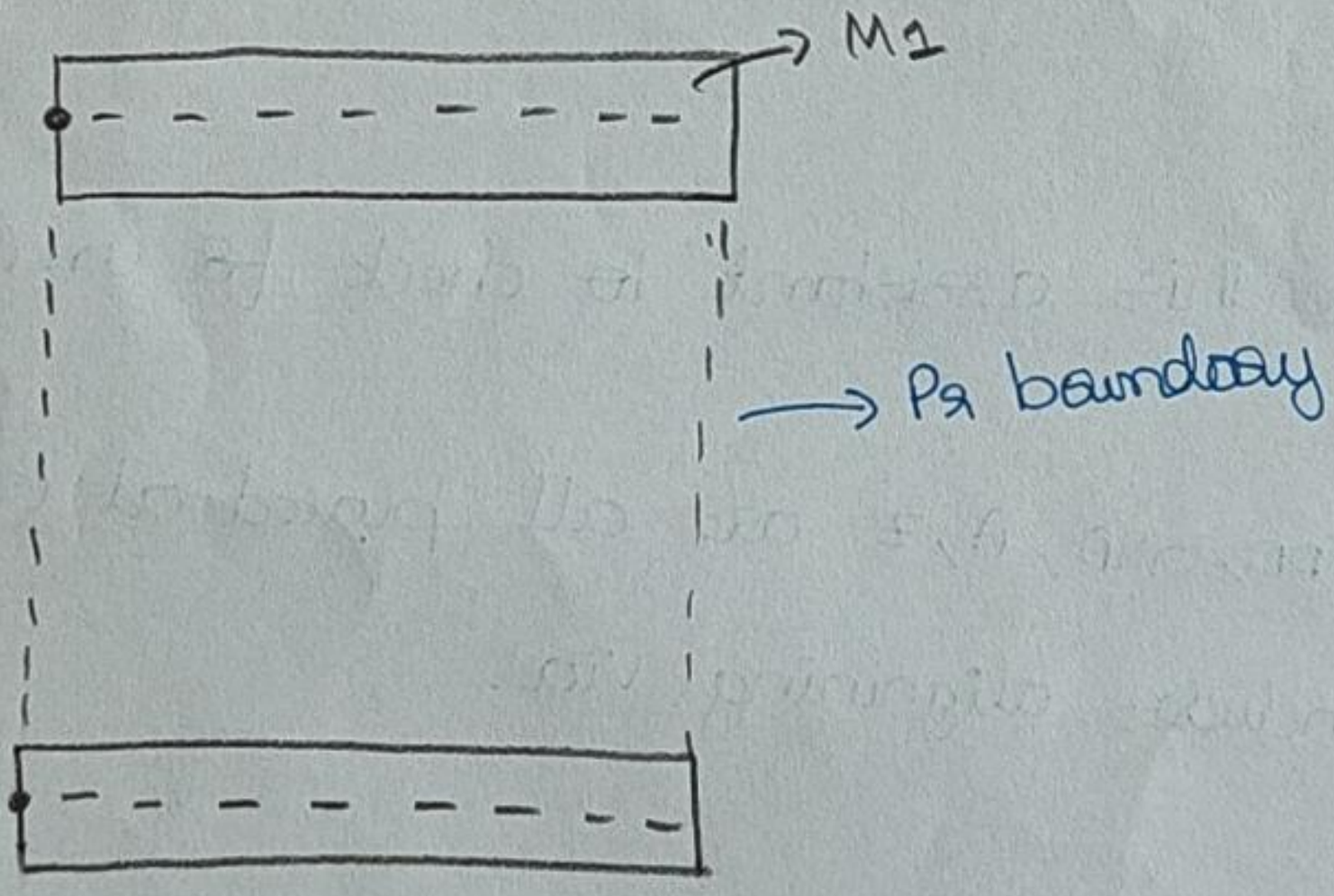
height = 10.8 [

width = 3.6



"Press A" ⇒ click here at ① ⇒ Place at the origin

⇒ If placed correctly we will see a good overlap.



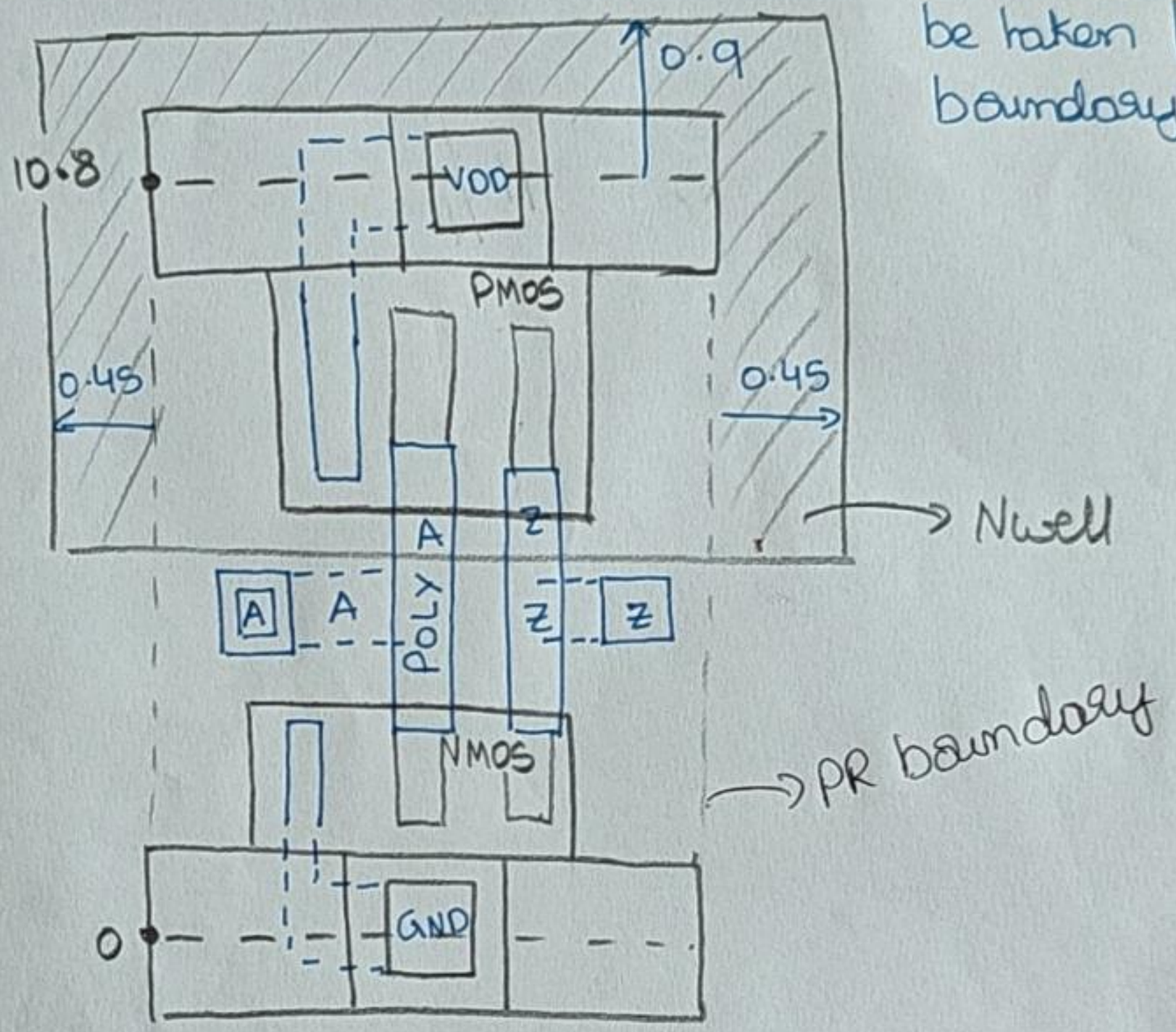
STEP 11: Create Nwell

Similarly search for Nwell (choose draw one) and draw using R.

height =	7.2
width =	4.5

⟶ for Nwell

The 0.9, 0.45 should be taken from PR boundary



Align the nwell as shown to complete the whole layout.

RUN DRC, LVS and Assura to get the Av extracted file.