


# SCK-KR-05101

## Robotics Starter Kit Carrier Card

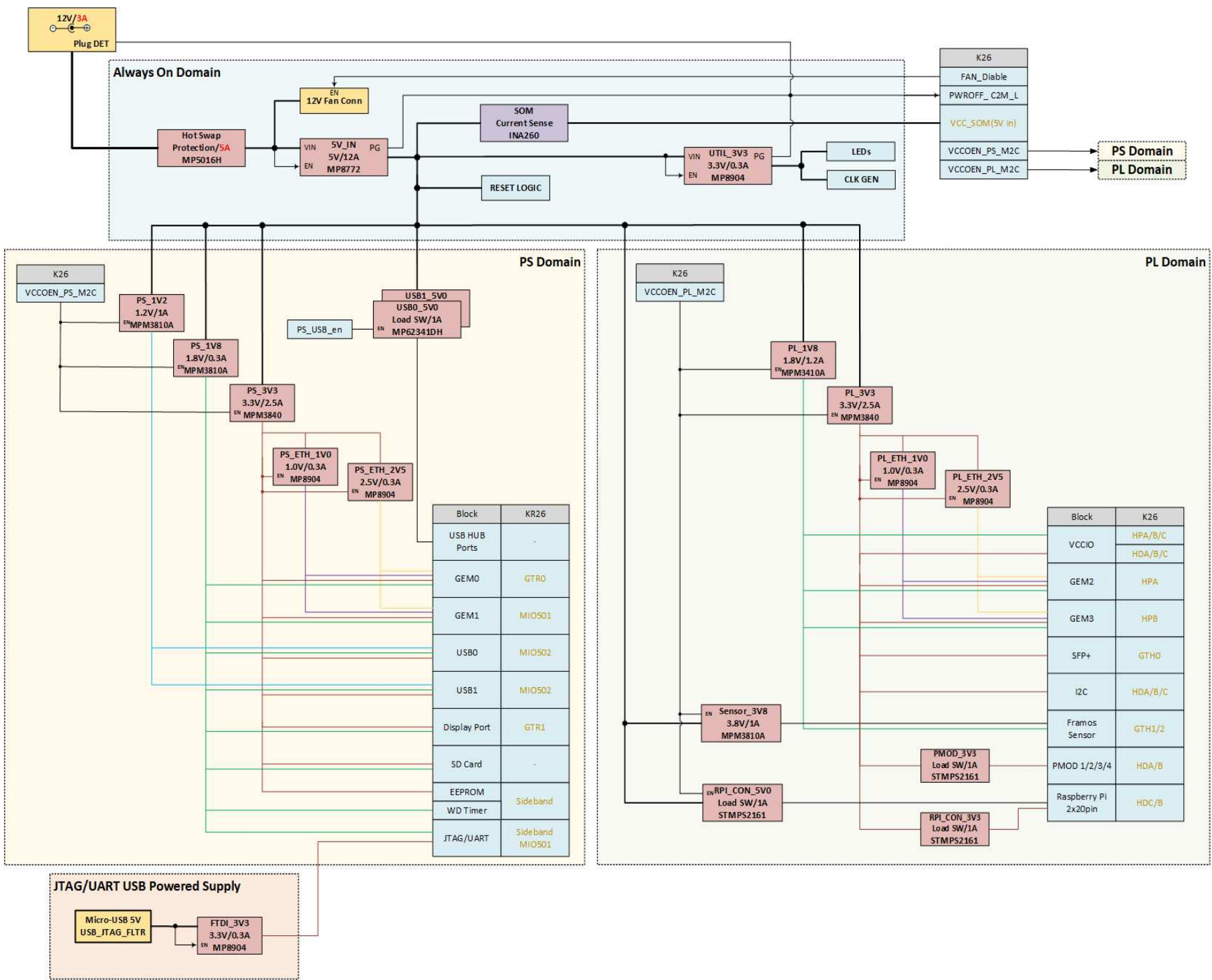
**NOTICE:** These schematics are made available for users who are working with this specific Xilinx board and should not be considered an optimal board design reference. This board was designed for evaluation purposes with components that are potentially more complex and costly than would be used in an end customer system. Users are encouraged to leverage the Xilinx design guidelines as the optimal starting point for new board designs.

© Copyright 2020 Xilinx, Inc. Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. [If applicable, insert relevant third-party sentence.] All other trademarks are the property of their respective owners.

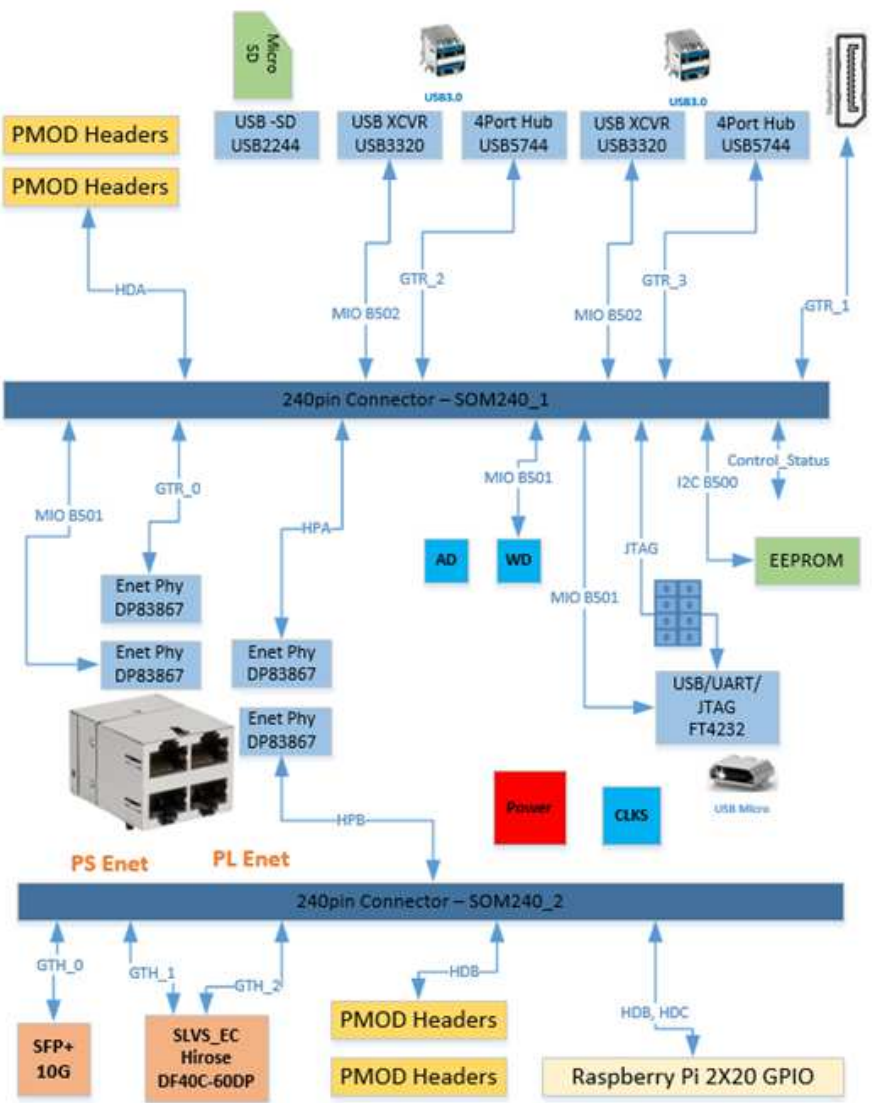
**DISCLAIMER** The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at <http://www.xilinx.com/legal.htm#tos>; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at <http://www.xilinx.com/legal.htm#tos>.

 <b>XILINX</b> 2100 LOGIC DRIVE SAN JOSE CA		SKIT	
Title: SCK-KR 01 - Title Page			
Size <b>B</b>	Date Modified: Friday, October 15, 2021	Document Number: <b>038-05101-01</b>	Rev <b>A02</b>
Engineer: RH/JW			Sheet 1 of 25

# POWER BLOCK DIAGRAM

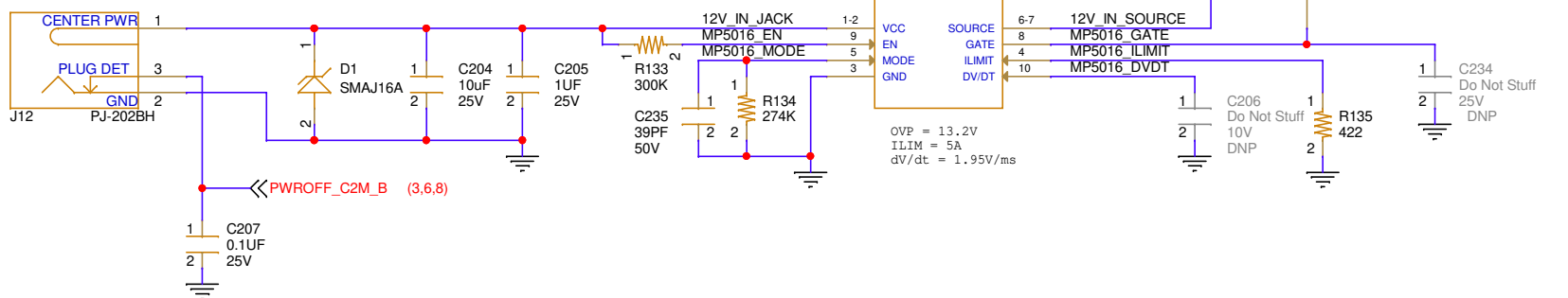


# PERIPHERAL BLOCK DIAGRAM

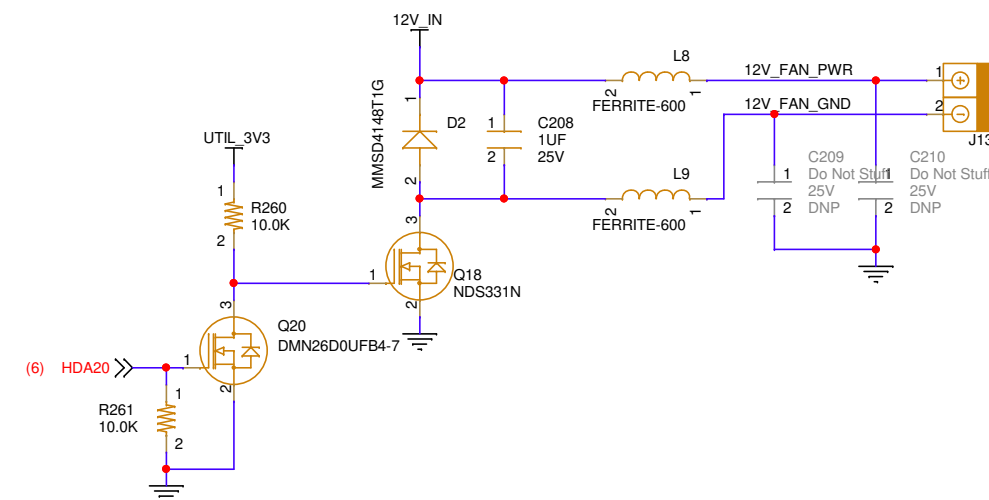


## 12V DC JACK

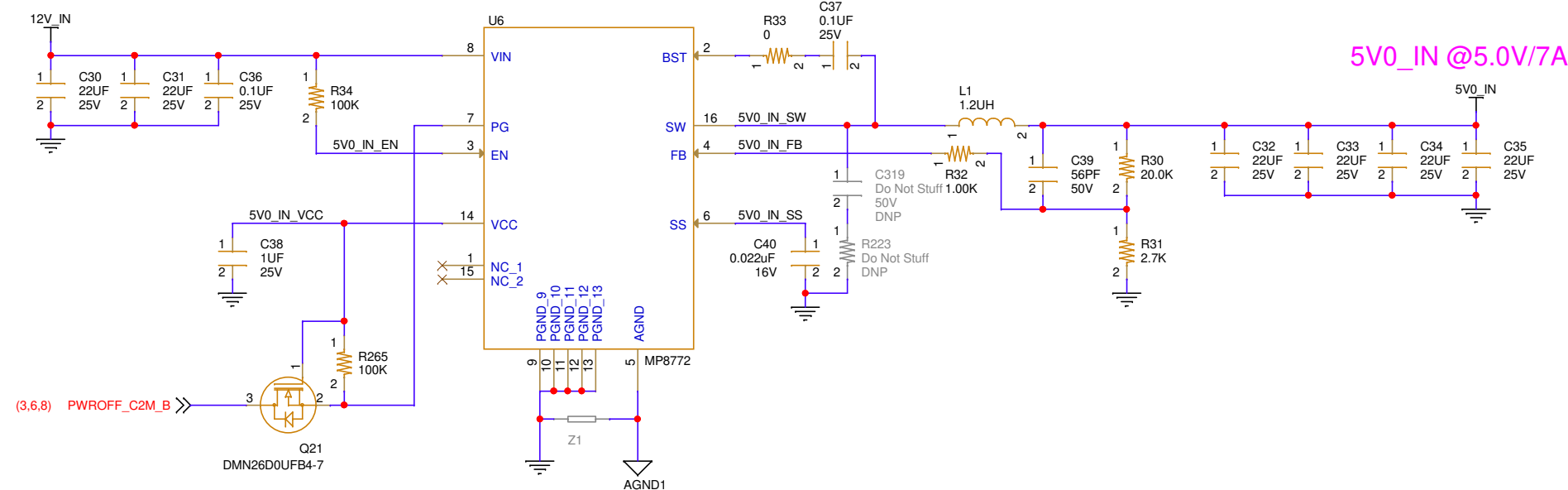
ID: 2.5mm  
OD: 5.5mm  
Depth: 9.0mm



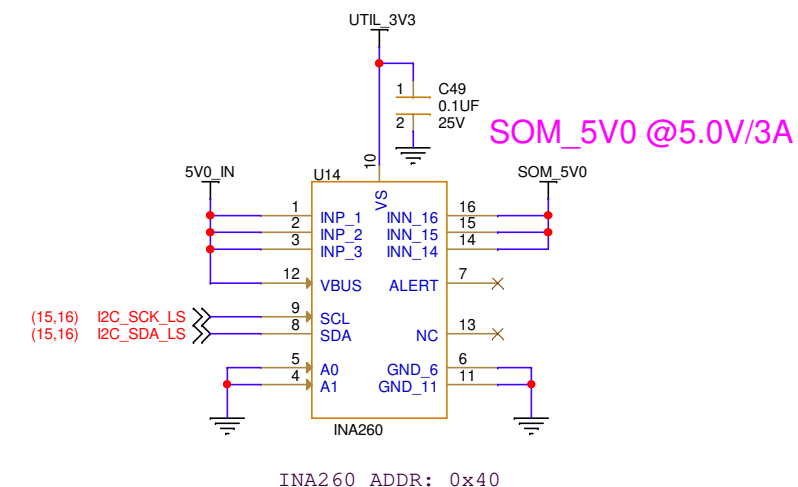
## 12V FAN HEADER



## 5V0\_IN ALWAYS ON REGULATOR

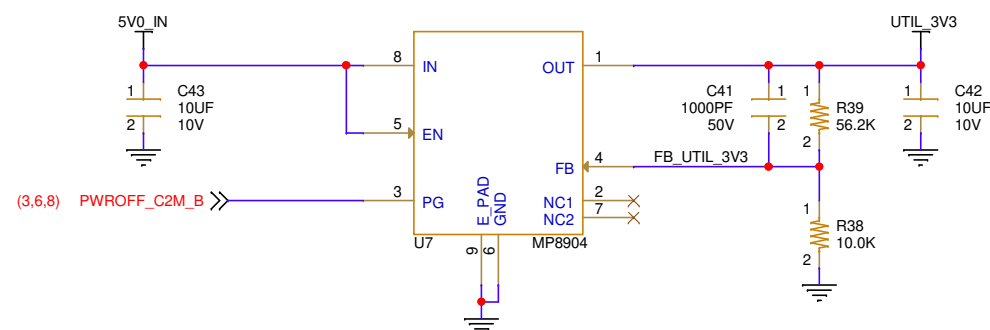


## SOM\_5V0 CURRENT MONITOR

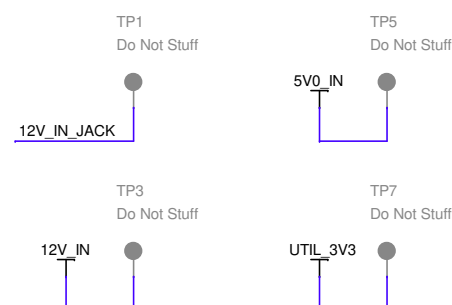


## UTIL\_3V3 ALWAYS ON REGULATOR

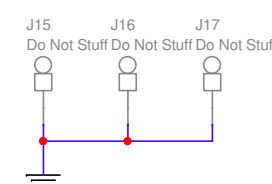
UTIL\_3V3@3.3V/0.3A



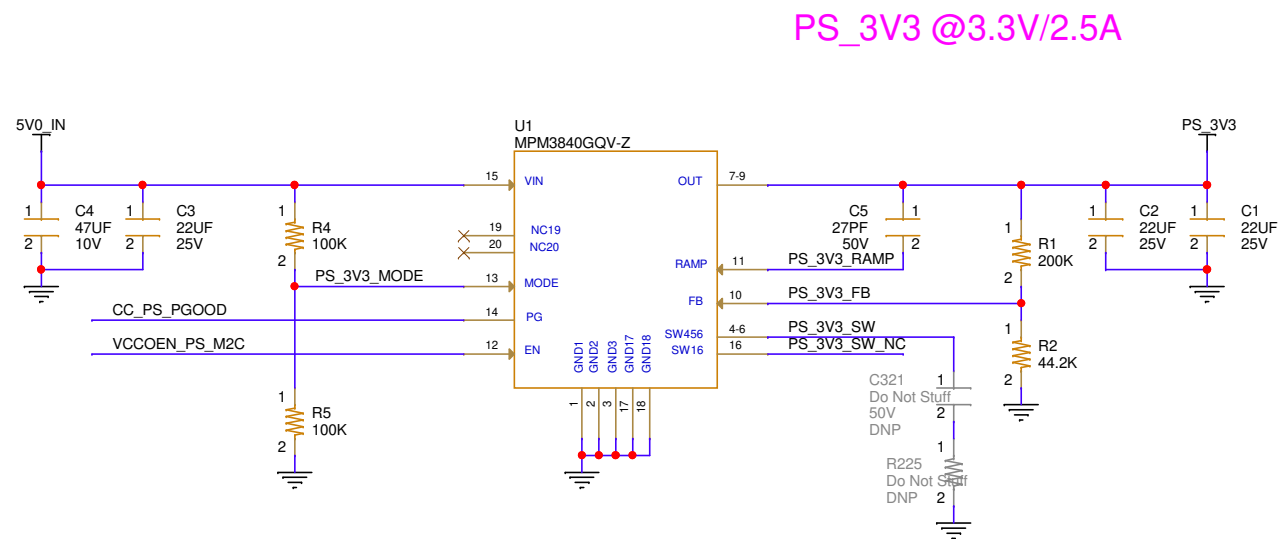
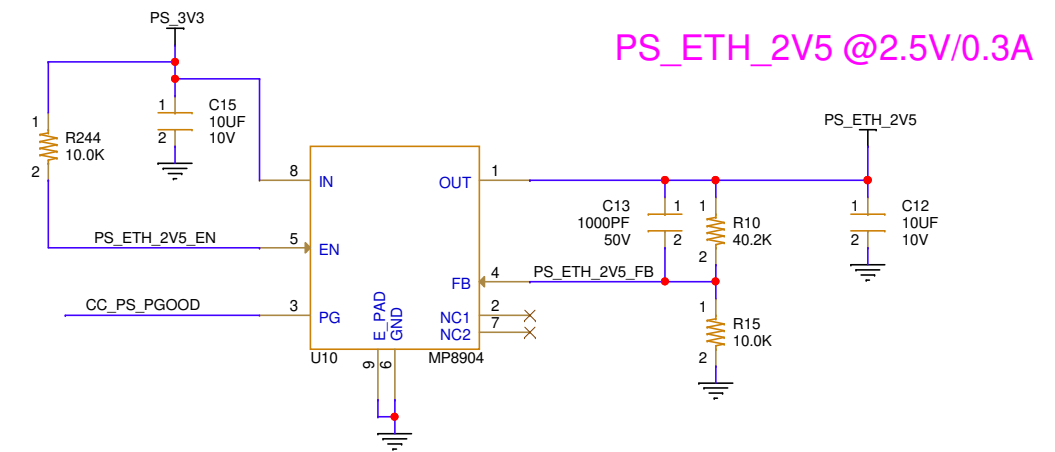
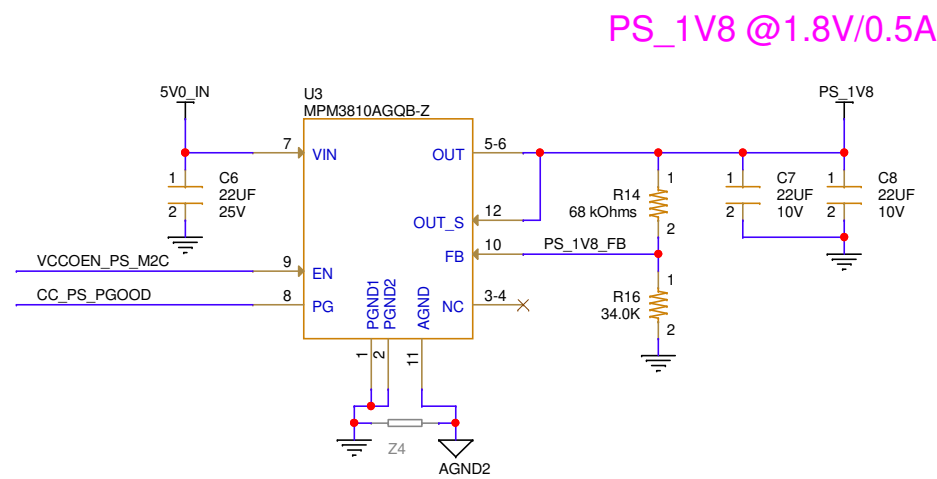
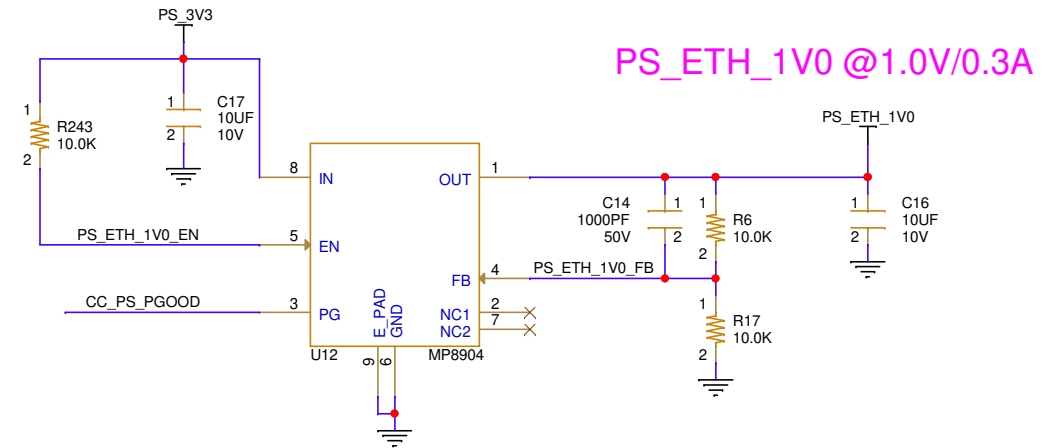
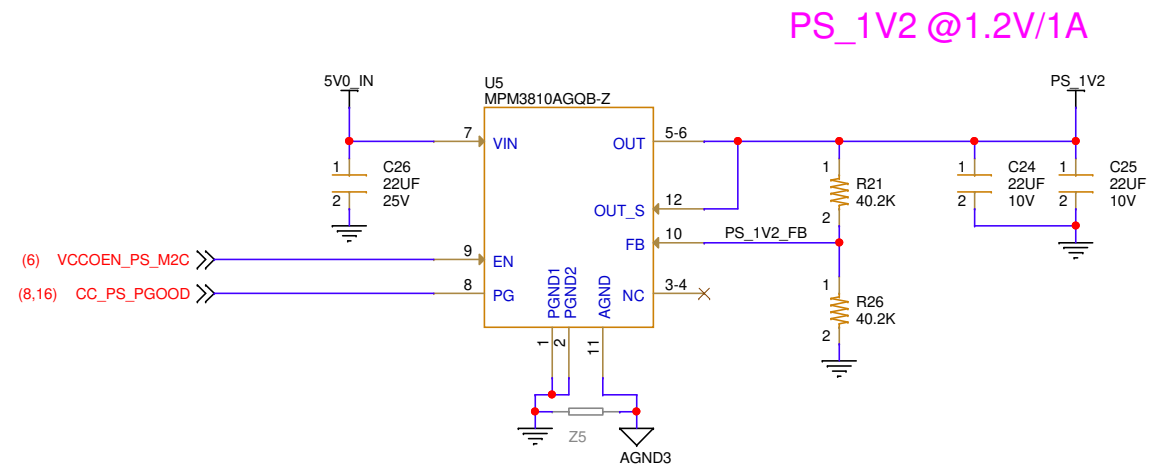
## POWER TEST POINTS



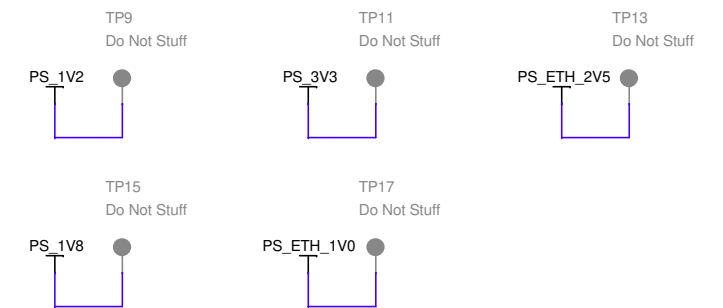
## GROUND LOOPS




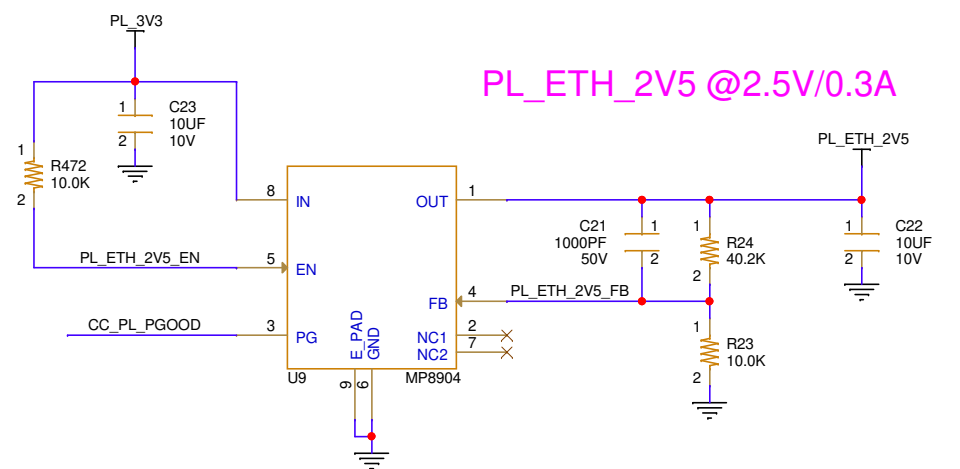
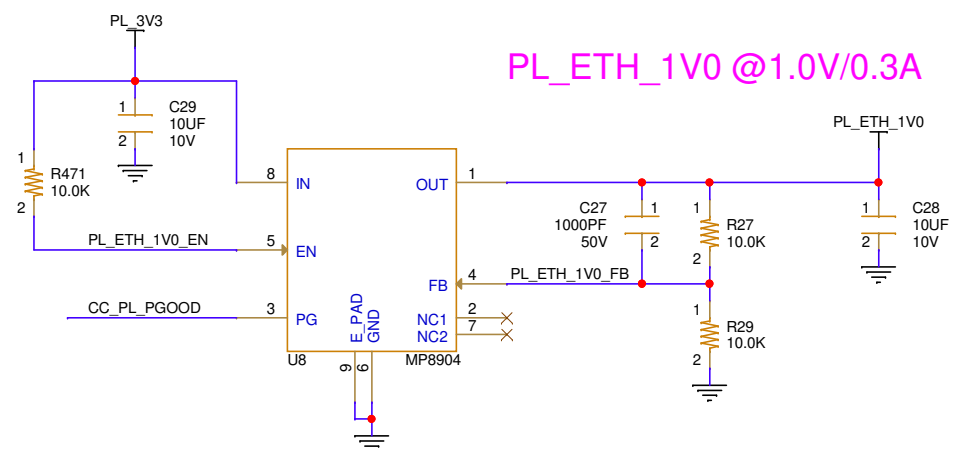
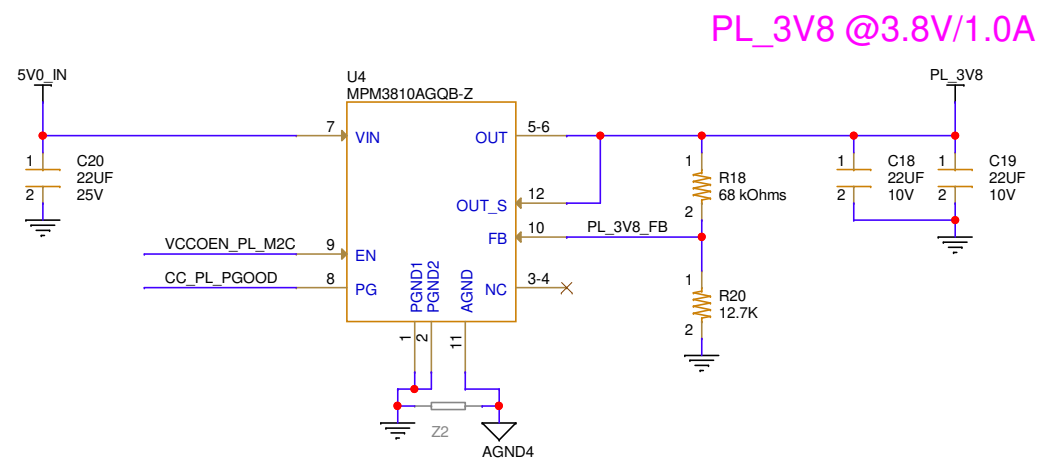
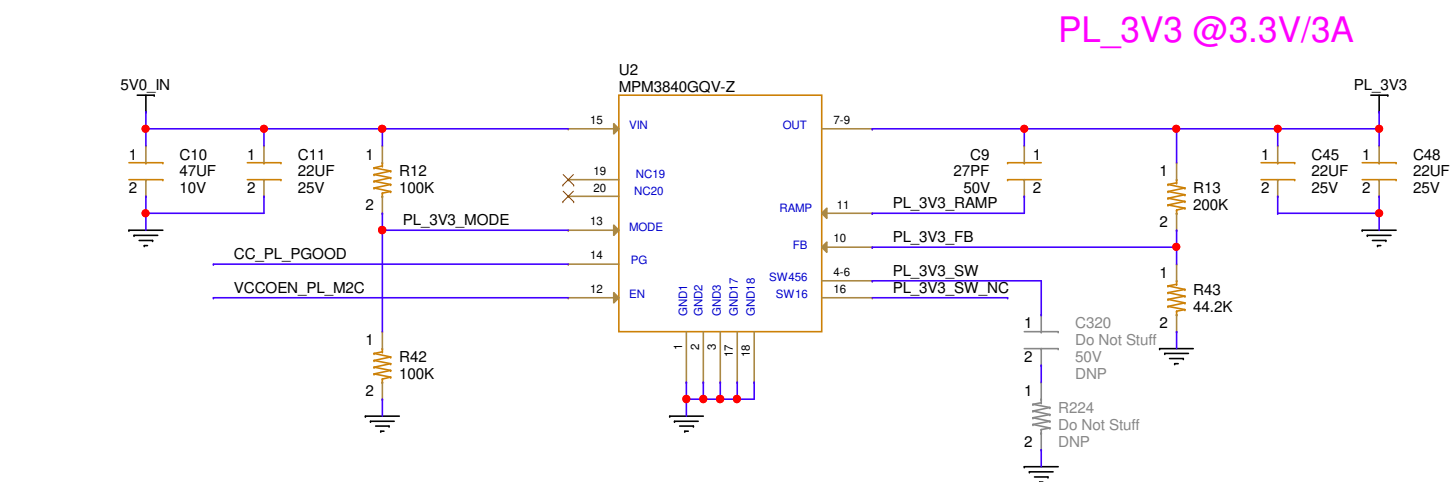
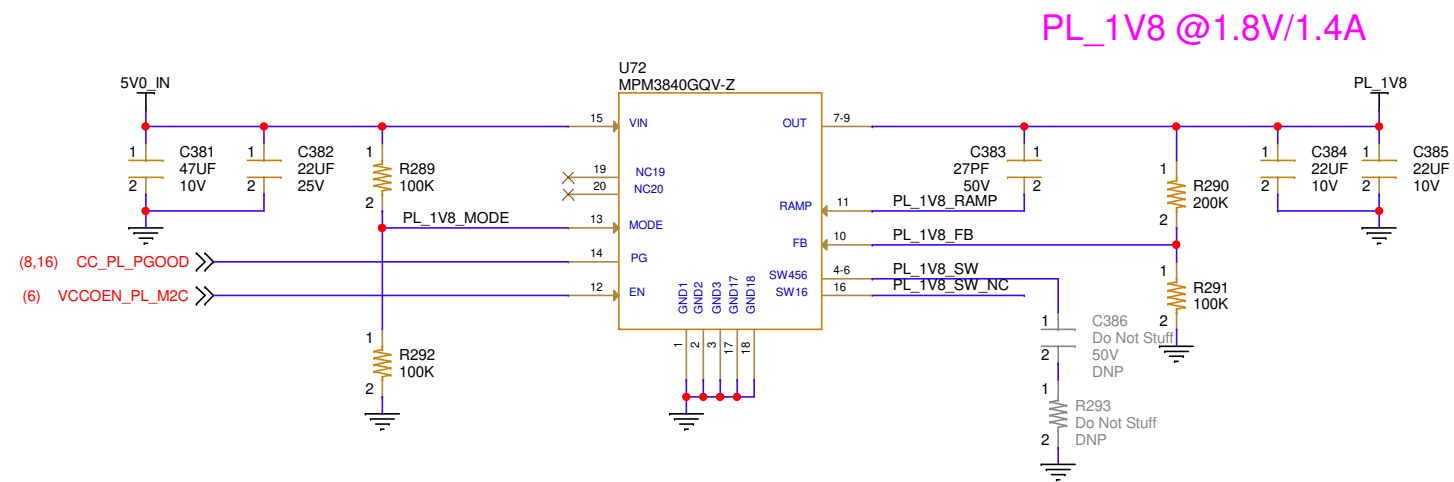
<b>XILINX</b> 2100 LOGIC DRIVE SAN JOSE CA			SKIT
Title: <b>SCK-KR</b> <b>03 - Always On Pwr, Fan Header</b>			
Size <b>B</b>	Date Modified: Friday, October 15, 2021	Document Number: <b>038-05101-01</b>	Rev <b>A02</b>
Engineer: RH/JW			Sheet 3 of 25



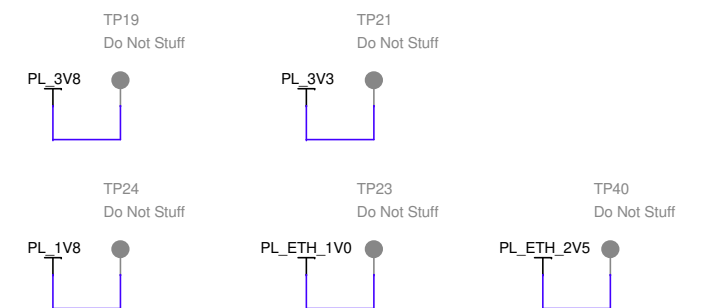
## POWER TEST POINTS




 <b>XILINX</b> 2100 LOGIC DRIVE SAN JOSE CA		SKIT
Title: <b>SCK-KR</b> <b>04 - PS Power</b>		
Size <b>B</b>	Date Modified: Friday, October 15, 2021	Document Number: <b>038-05101-01</b> Rev <b>A02</b>
Engineer: RH/JW		Sheet 4 of 25



## POWER TEST POINTS

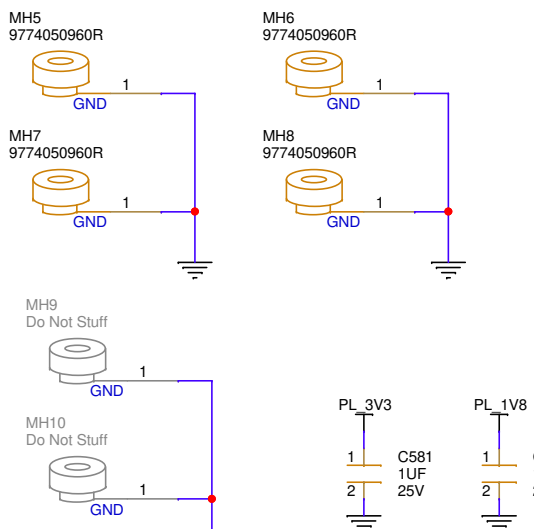
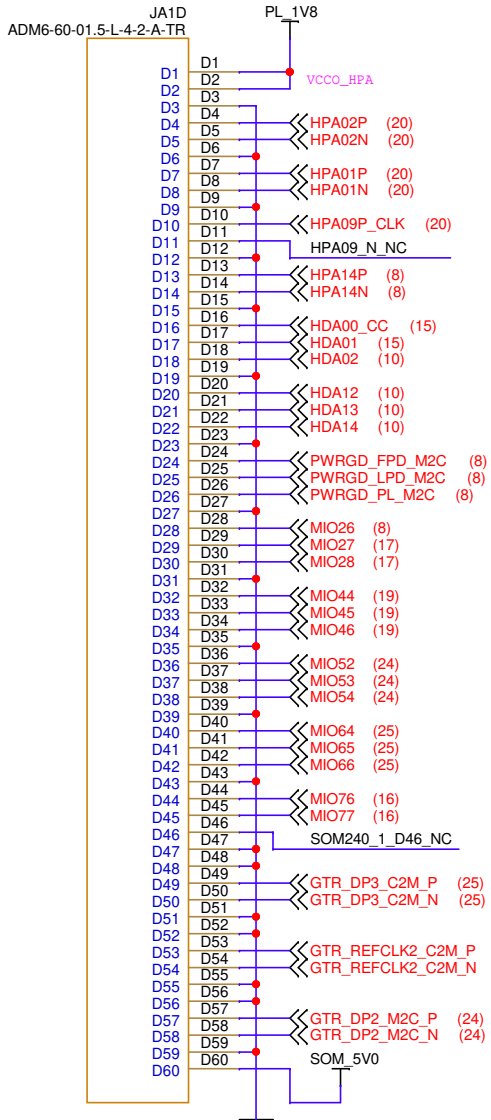
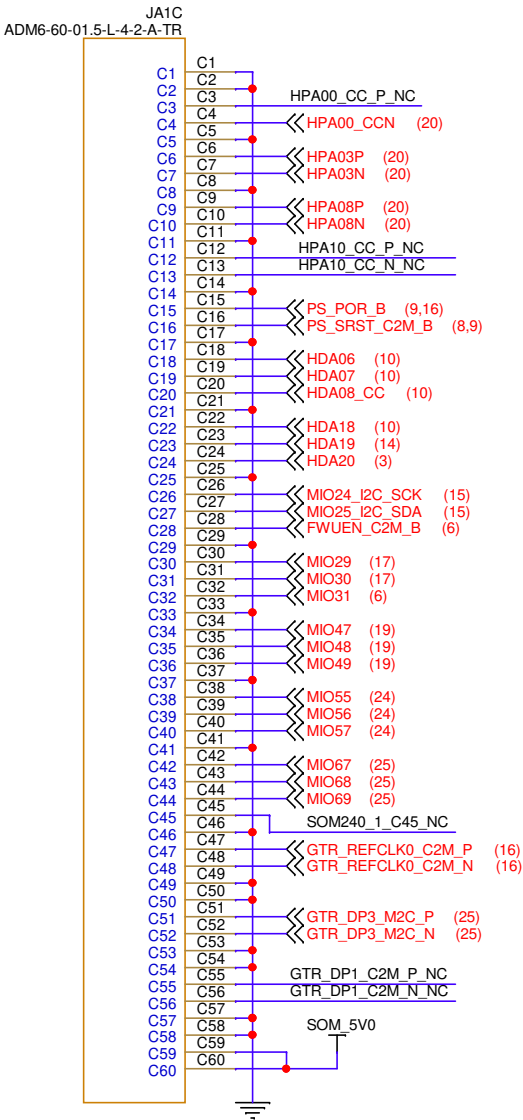
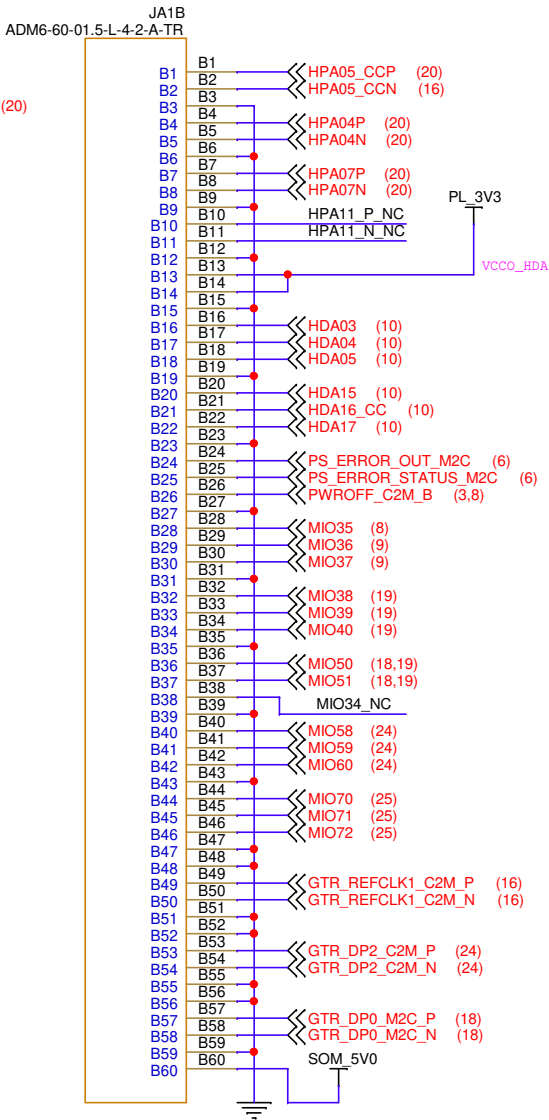
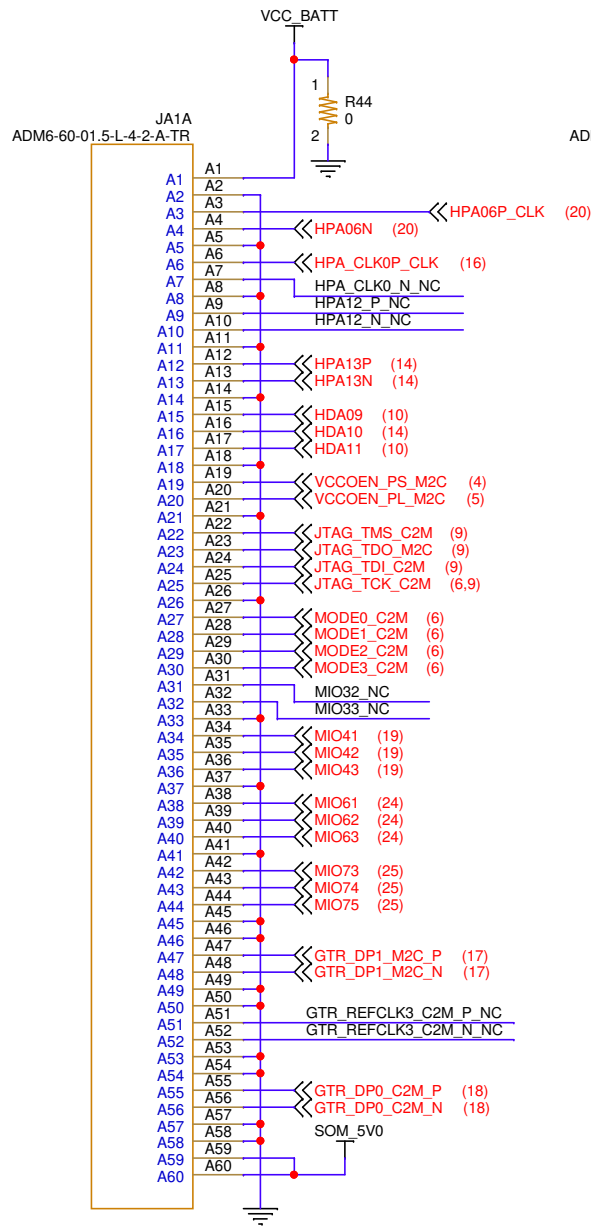


 <b>XILINX</b> 2100 LOGIC DRIVE SAN JOSE CA		SKIT
Title: <b>SCK-KR</b> <b>05 - PL Power</b>		
Size <b>B</b>	Date Modified: Friday, October 15, 2021	Document Number: <b>038-05101-01</b>
Engineer: RH/JW		Rev <b>A02</b>
Sheet 5		of 25

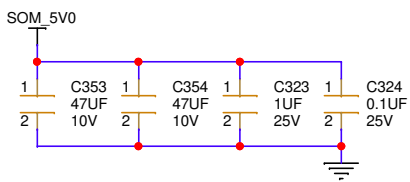


SOM240\_1 CONNECTOR

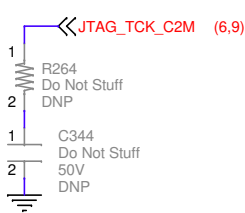
SOM STANDOFFS



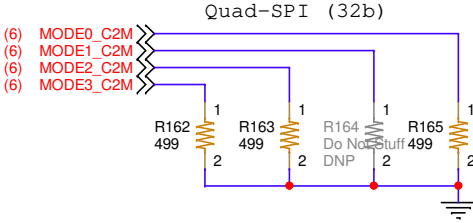
SOM\_5V0 Connector Decoupling



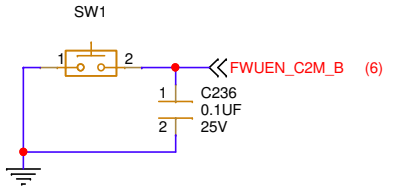
TCK TERM



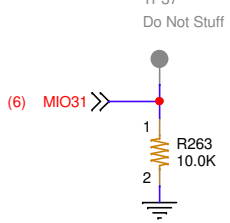
MODE PINS



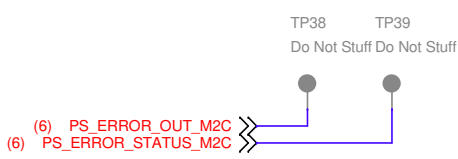
FWUEN BUTTON




SHUTDOWN

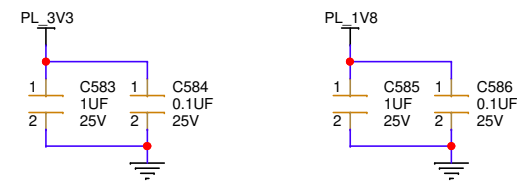
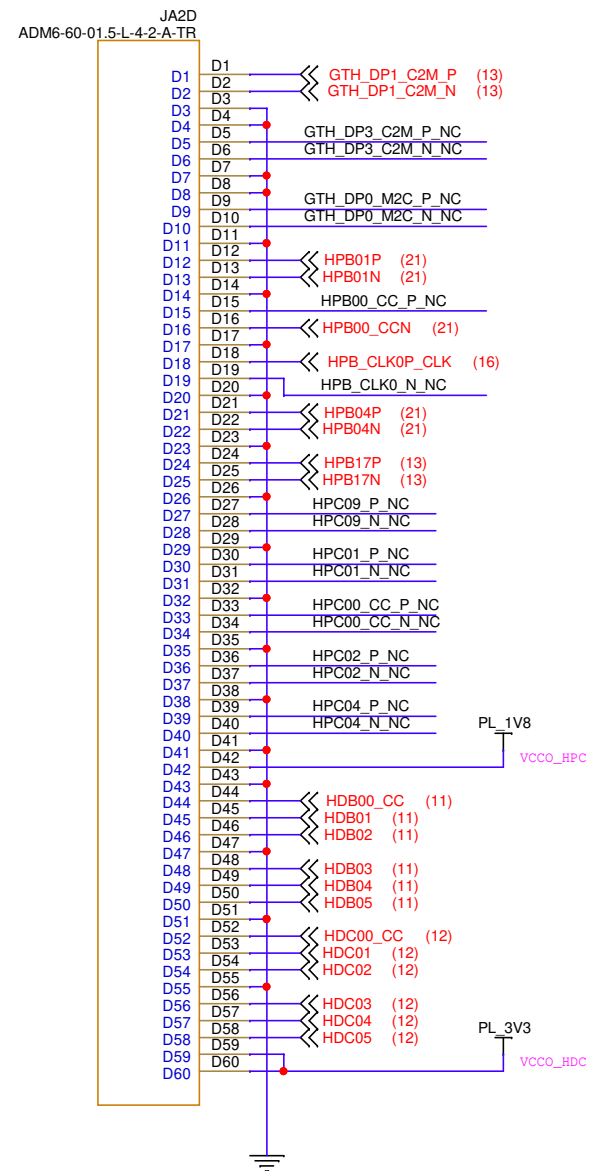
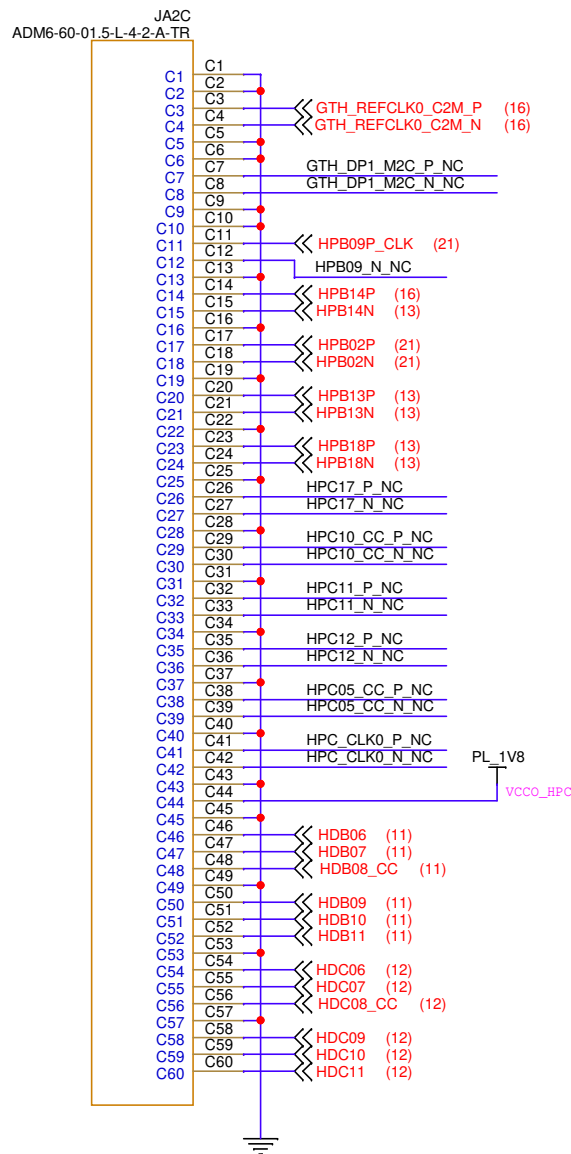
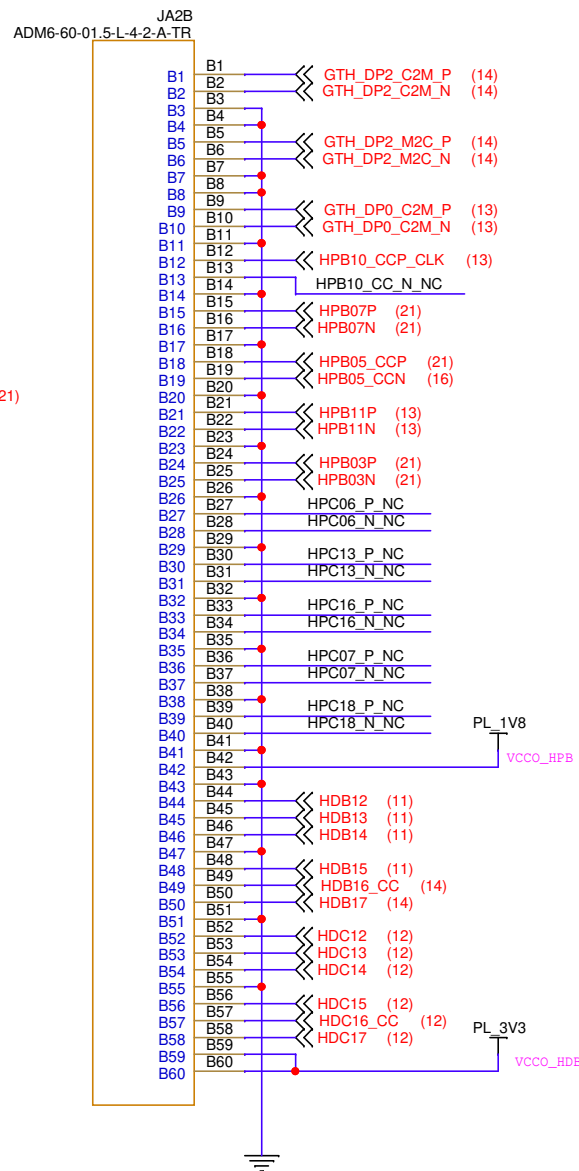
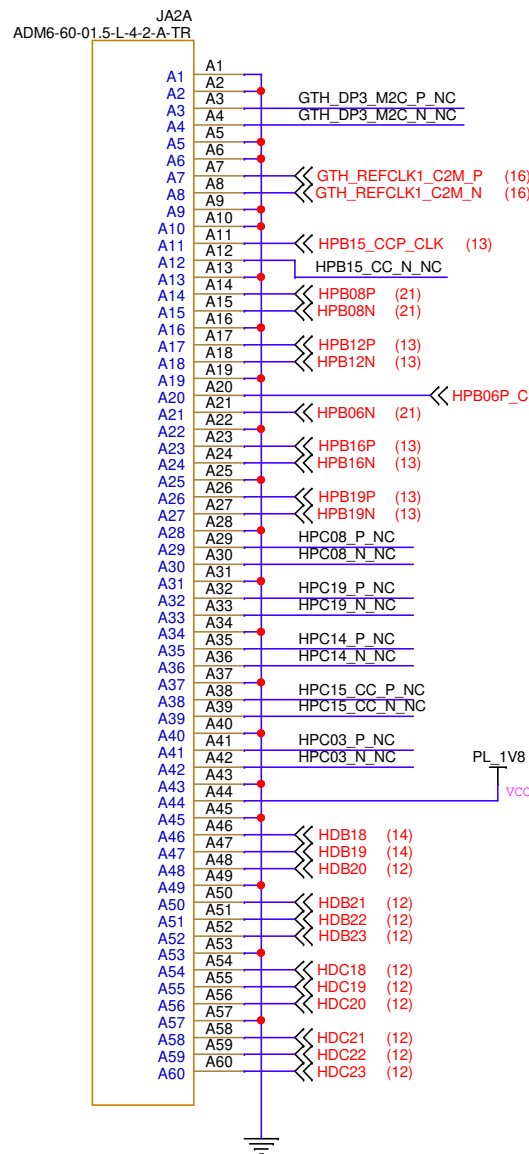


PS\_ERROR\_OUT/STATUS TEST POINTS

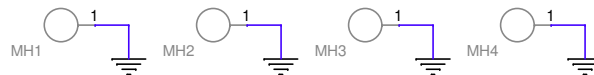



 2100 LOGIC DRIVE SAN JOSE CA		SKIT	
Title: SCK-KR 06 - SOM240_1 Connector			
Size B	Date Modified: Friday, October 15, 2021	Document Number: 038-05101-01	Rev A02
Engineer: RH/JW		Sheet 6 of 25	

# SOM240\_2 CONNECTOR

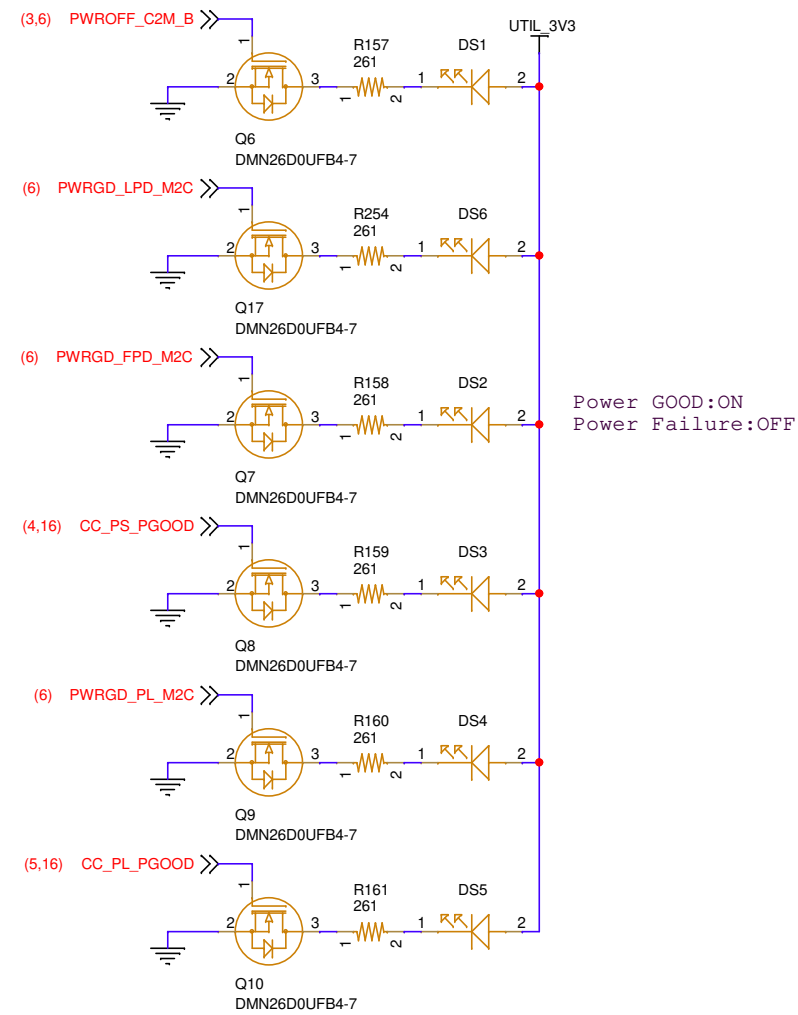


FOUR CORNER MOUNTING HOLES

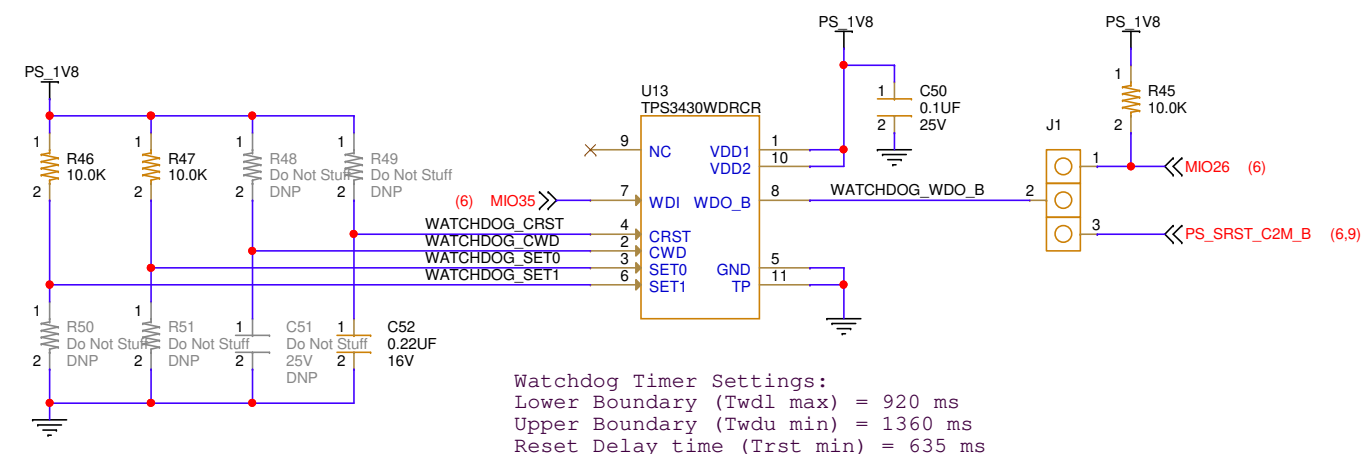


 <b>XILINX</b> 2100 LOGIC DRIVE SAN JOSE CA		SKIT	
Title: <b>SCK-KR</b> <b>07 - SOM240_2 Connector</b>			
Size <b>B</b>	Date Modified: Friday, October 15, 2021	Document Number: <b>038-05101-01</b>	Rev <b>A02</b>
Engineer: RH/JW		Sheet 7 of 25	

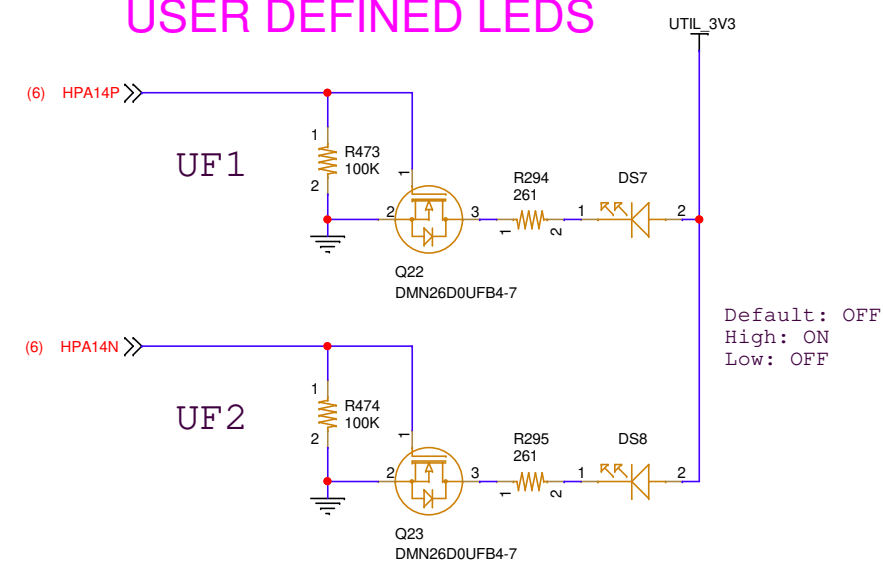
POWER STATUS LEDs




WATCHDOG TIMER



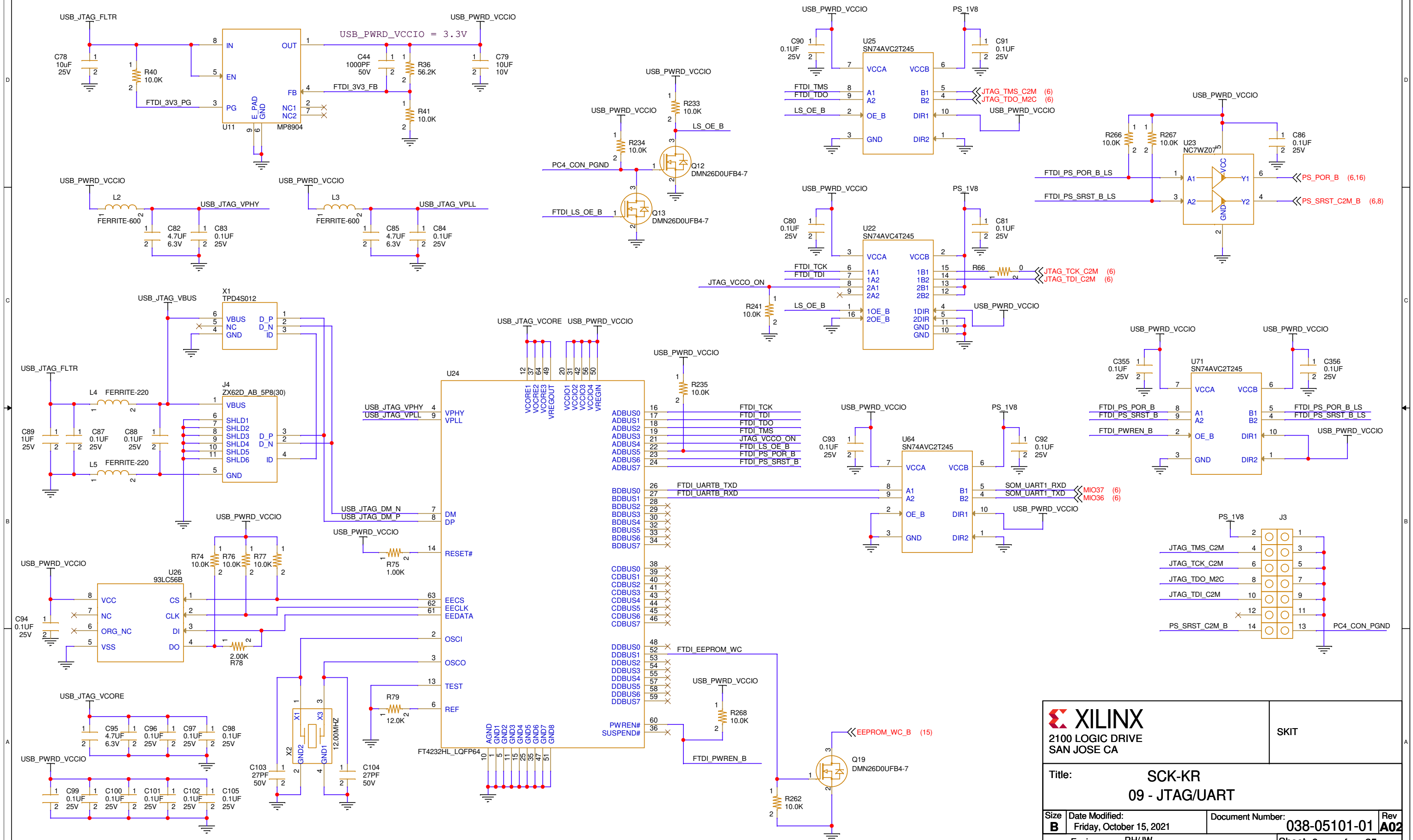
USER DEFINED LEDs




 XILINX 2100 LOGIC DRIVE SAN JOSE CA		SKIT
Title: SCK-KR 08 - WD, LEDs		
Size B	Date Modified: Friday, October 15, 2021	Document Number: 038-05101-01 Rev A02
Engineer: RH/JW		Sheet 8 of 25

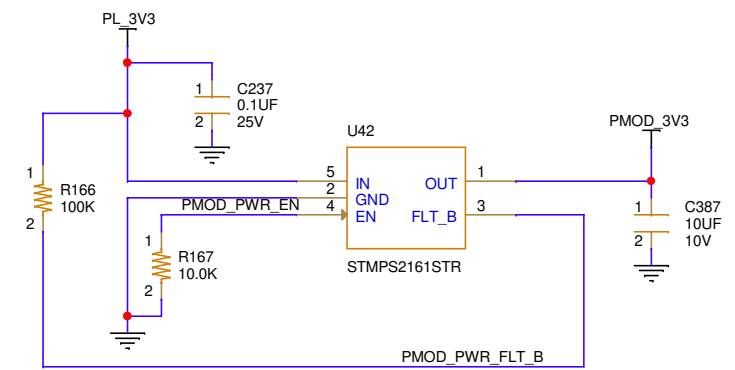
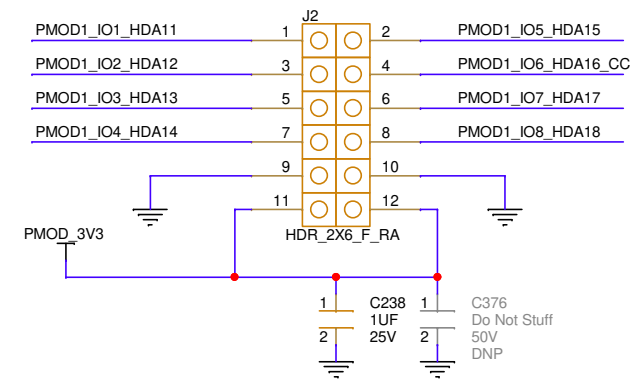
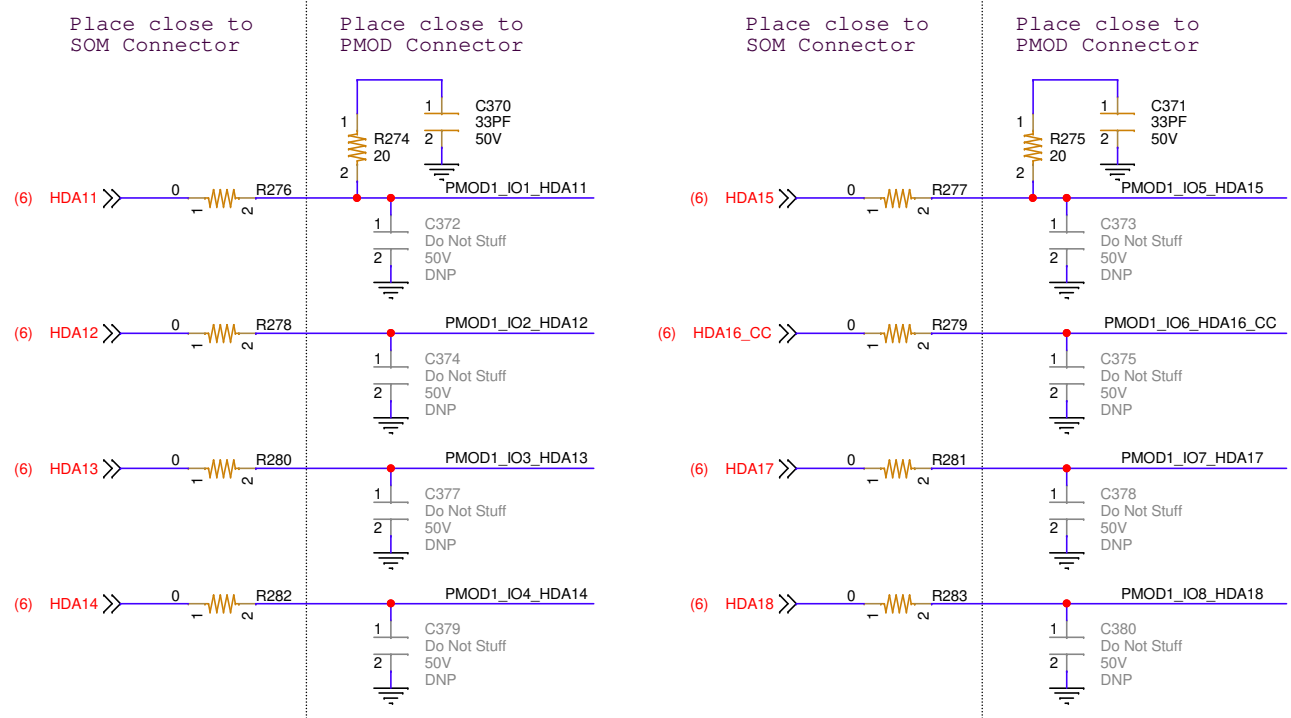


## FTDI JTAG/UART

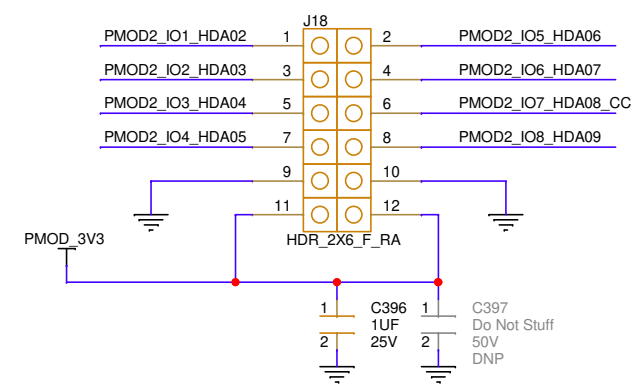
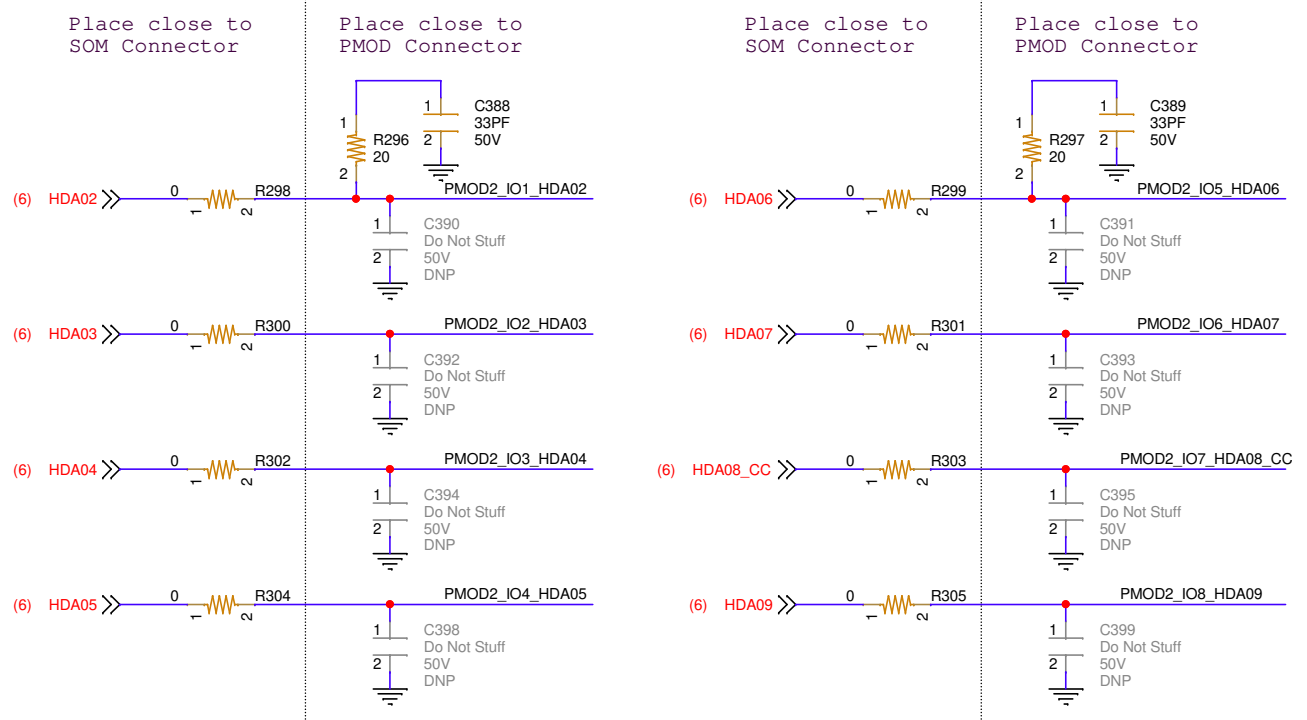


 <b>XILINX</b> 2100 LOGIC DRIVE SAN JOSE CA		SKIT
Title: <b>SCK-KR</b> <b>09 - JTAG/UART</b>		
Size <b>B</b>	Date Modified: Friday, October 15, 2021	Document Number: <b>038-05101-01</b>
Engineer: RH/JW		Rev <b>A02</b>
Sheet 9 of 25		

PMOD #1

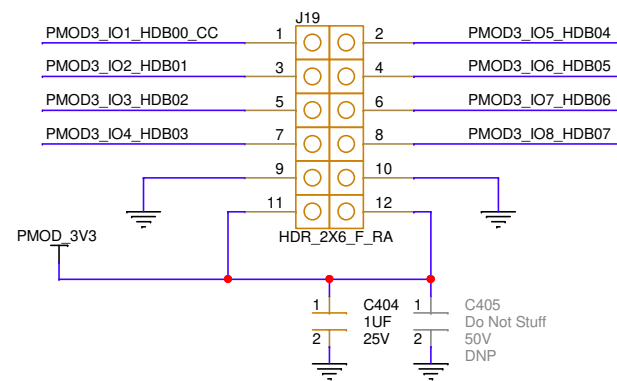
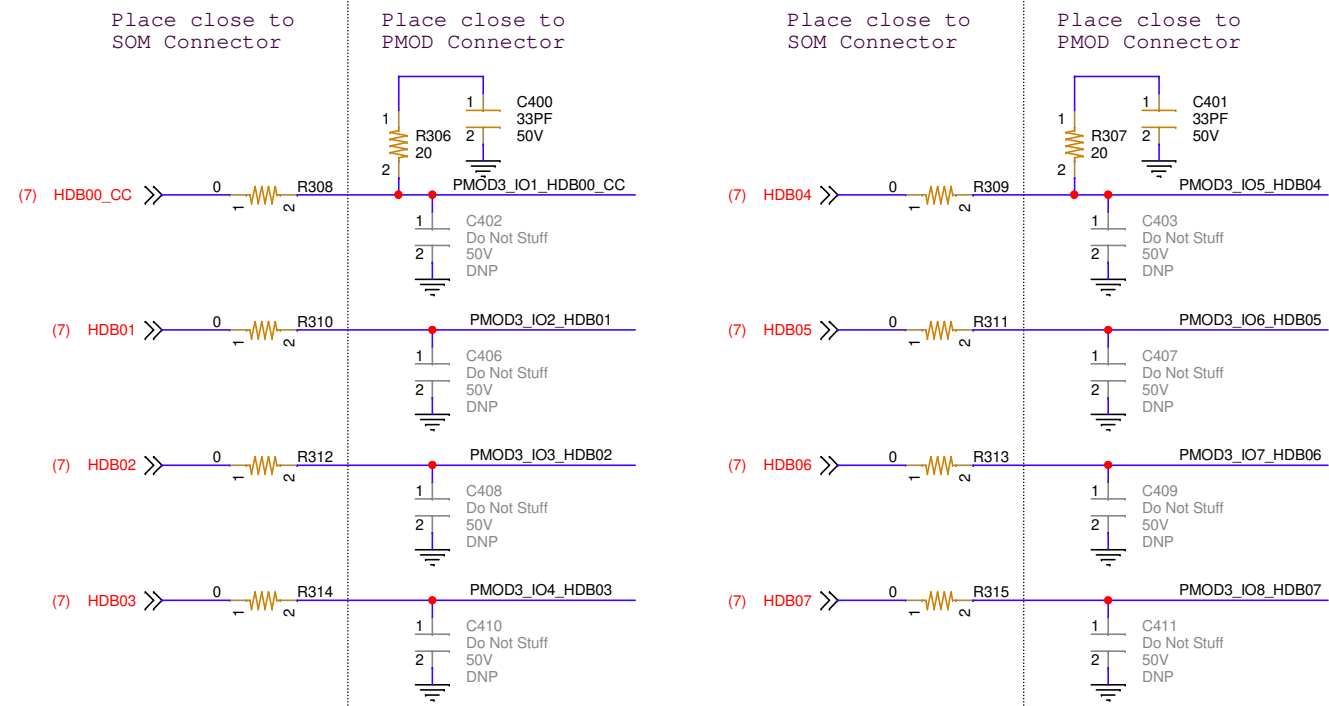


PMOD #2

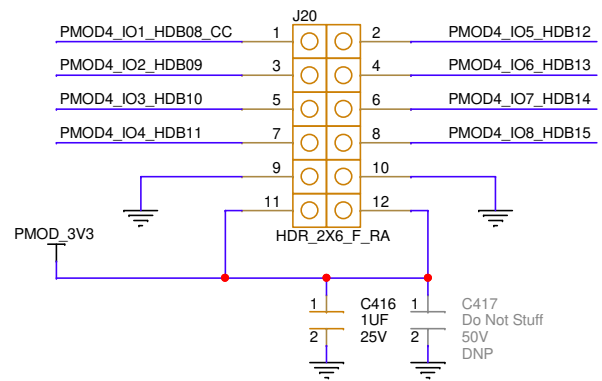
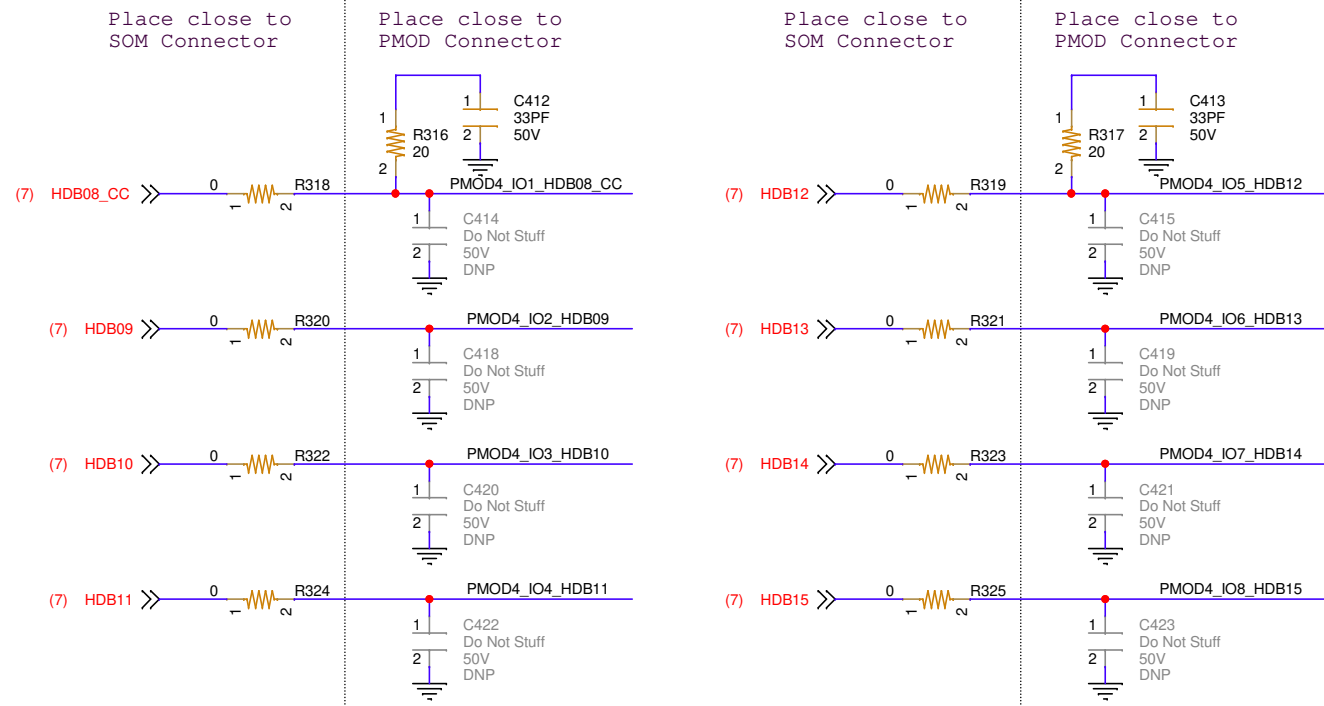



		SKIT	
Title: SCK-KR 10 - PMOD1&2			
Size B	Date Modified: Friday, October 15, 2021	Document Number: 038-05101-01	Rev A02
Engineer: RH/JW			Sheet 10 of 25

PMOD #3

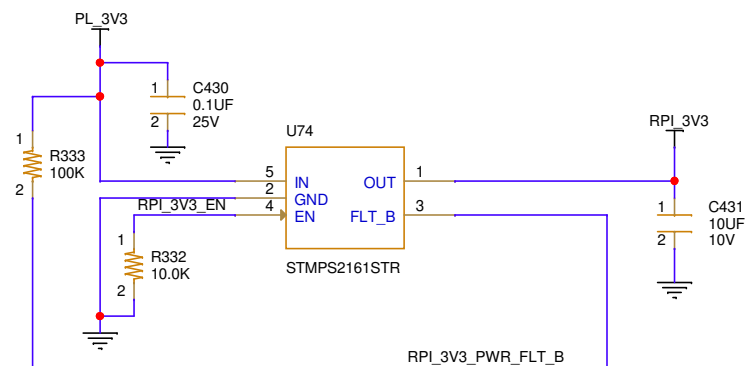
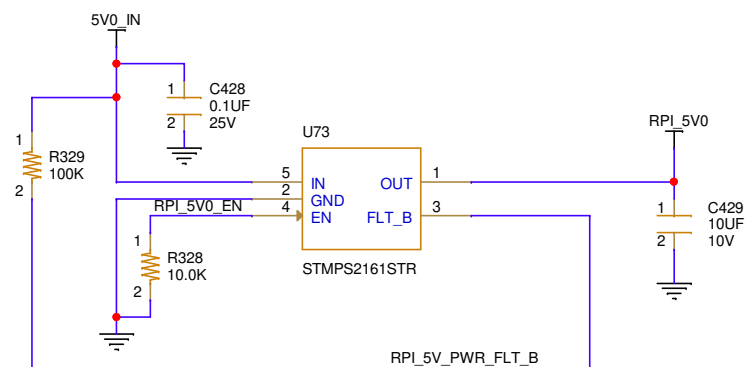
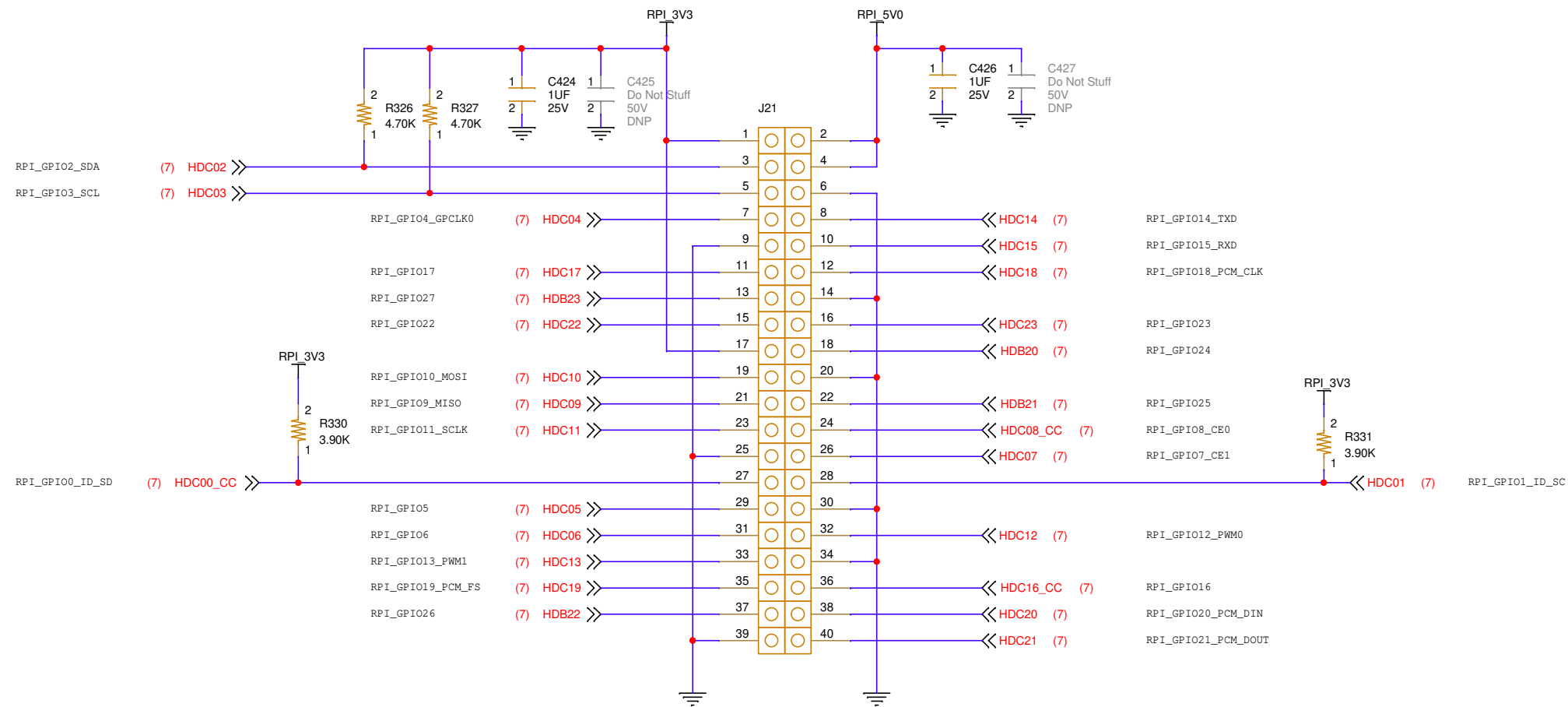



PMOD #4



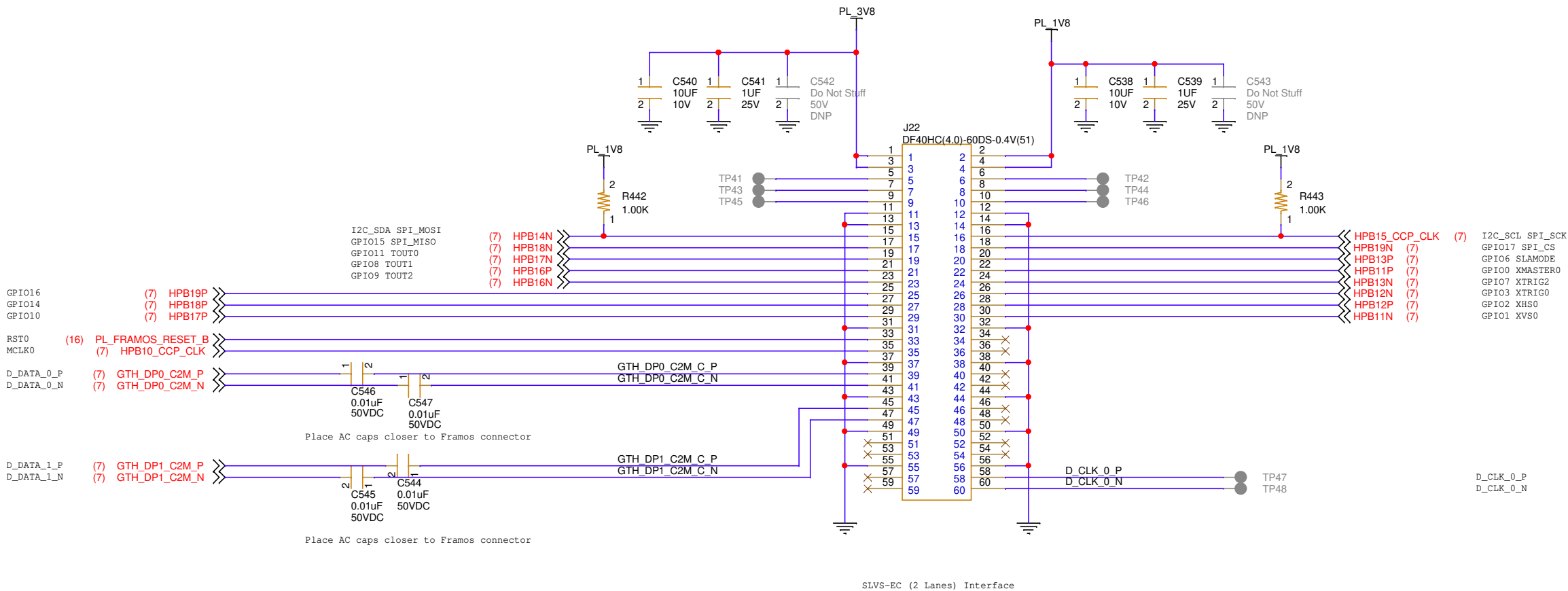
 XILINX 2100 LOGIC DRIVE SAN JOSE CA		SKIT
Title: SCK-KR 11 - PMOD3&4		
Size B	Date Modified: Friday, October 15, 2021	Document Number: 038-05101-01 Rev A02
Engineer: RH/JW		Sheet 11 of 25


# Raspberry Pi Expansion Header



 <b>XILINX</b> 2100 LOGIC DRIVE SAN JOSE CA		SKIT
Title: SCK-KR 12 - RPI Expansion CONN		
Size <b>B</b>	Date Modified: Friday, October 15, 2021	Document Number: 038-05101-01 <b>A02</b>
Engineer: RH/JW		Sheet 12 of 25

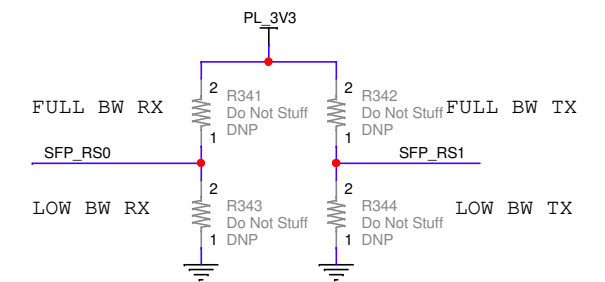
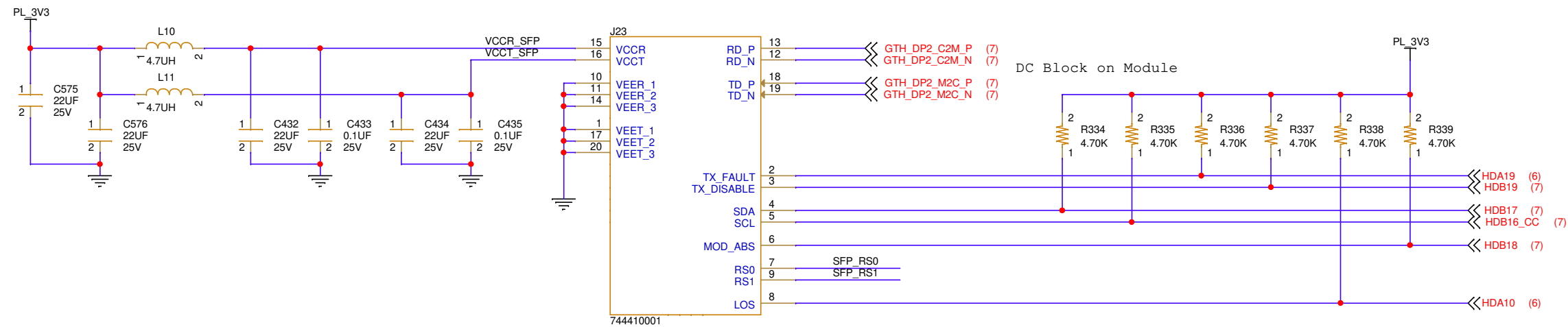
Framos FPA SLVS-EC



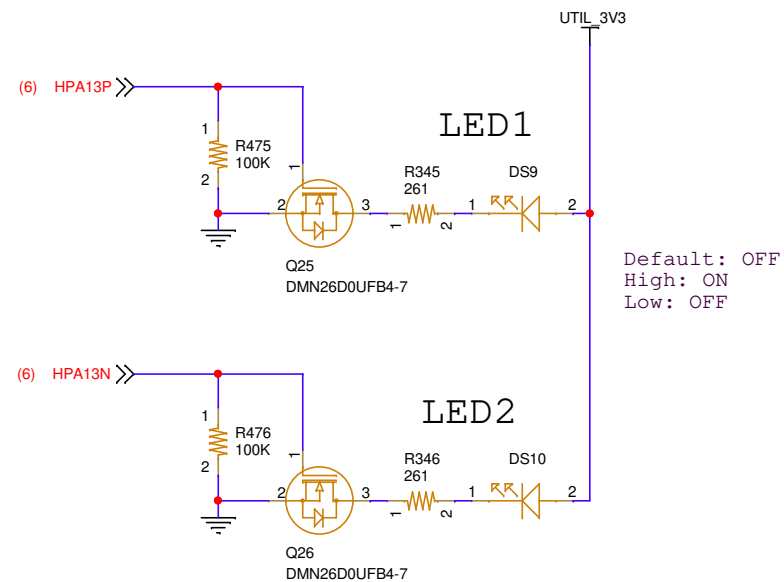
 2100 LOGIC DRIVE SAN JOSE CA		SKIT	
Title: SCK-KR 13 - Framos CONN			
Size B	Date Modified: Friday, October 15, 2021	Document Number: 038-05101-01	Rev A02
Engineer: RH/JW		Sheet 13 of 25	



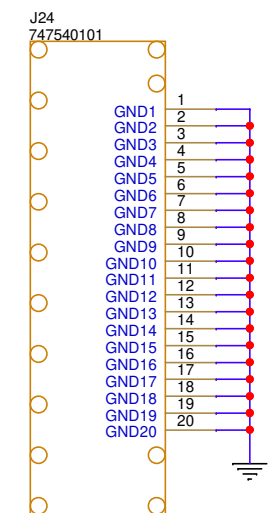
## SFP+ Connector




## SFP+ LEDs

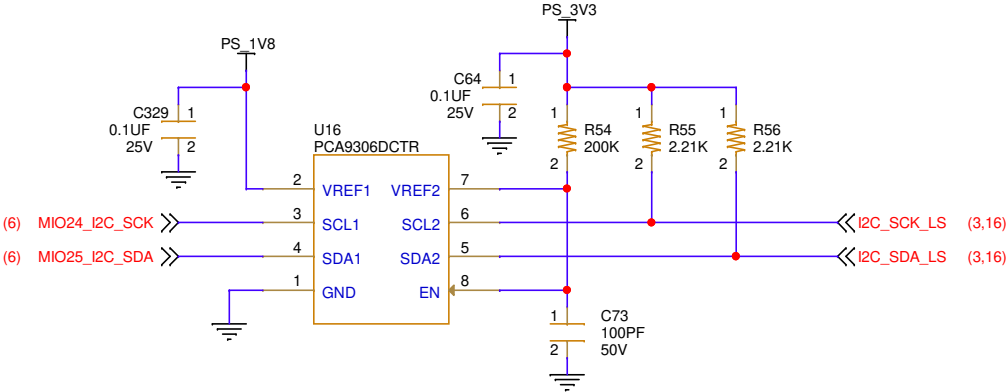


## SFP+ Cage

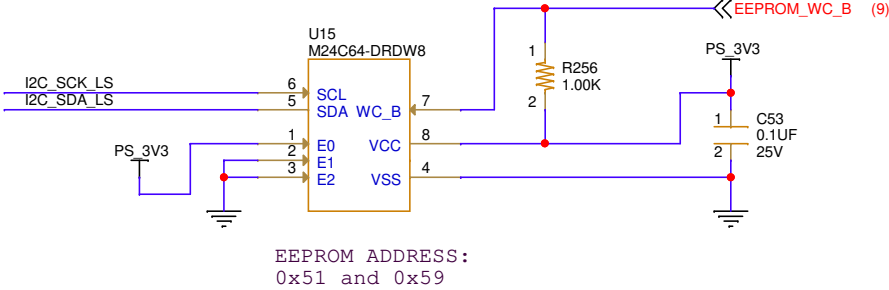


 <b>XILINX</b> 2100 LOGIC DRIVE SAN JOSE CA		SKIT
Title: <b>SCK-KR</b> <b>14 - SFP+</b>		
Size <b>B</b>	Date Modified: Friday, October 15, 2021	Document Number: <b>038-05101-01</b> Rev <b>A02</b>
Engineer: RH/JW		Sheet 14 of 25

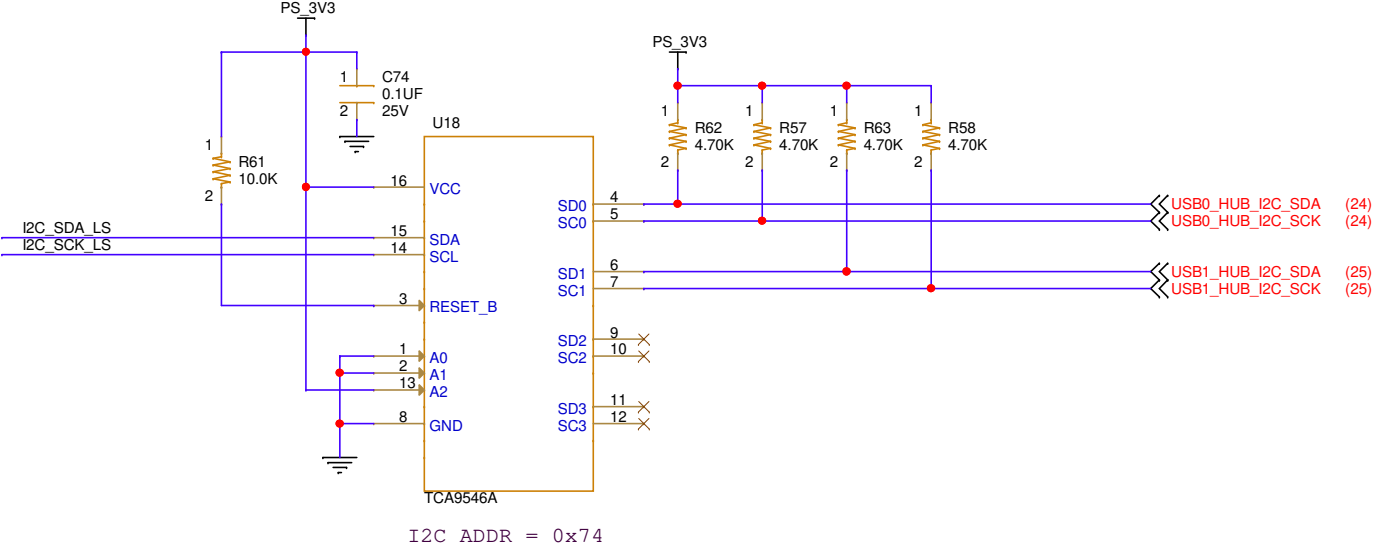
MIO I2C LEVEL SHIFTER



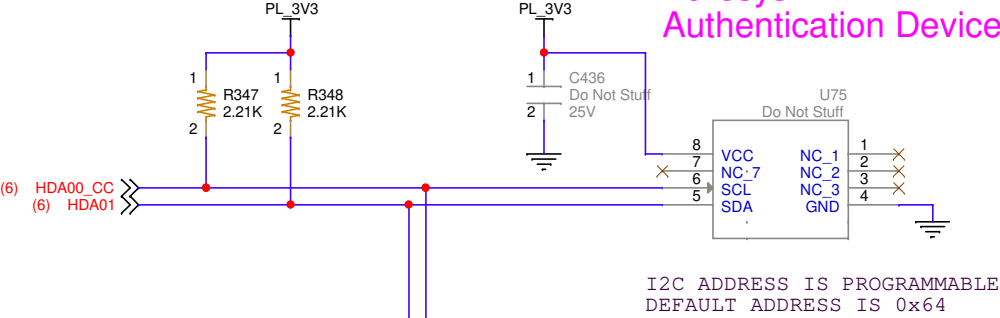
SYSTEM EEPROM



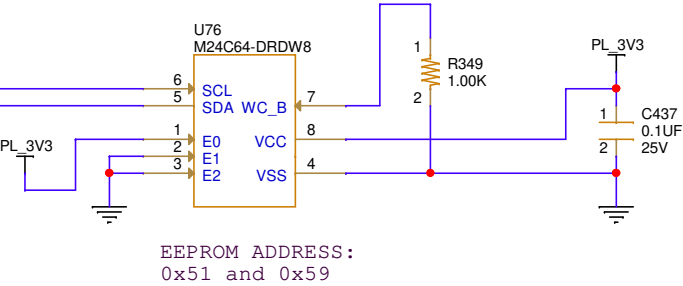
MIO I2C SWITCH



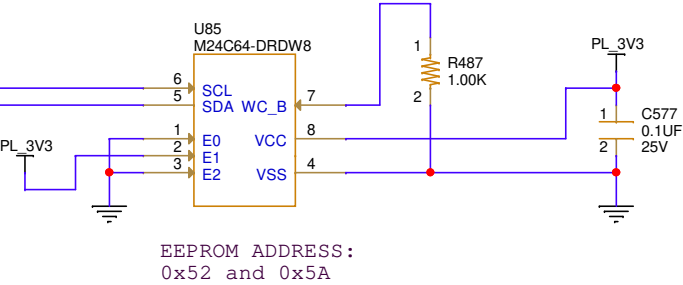
Euresys IP Authentication Device




Euresys IP EEPROM

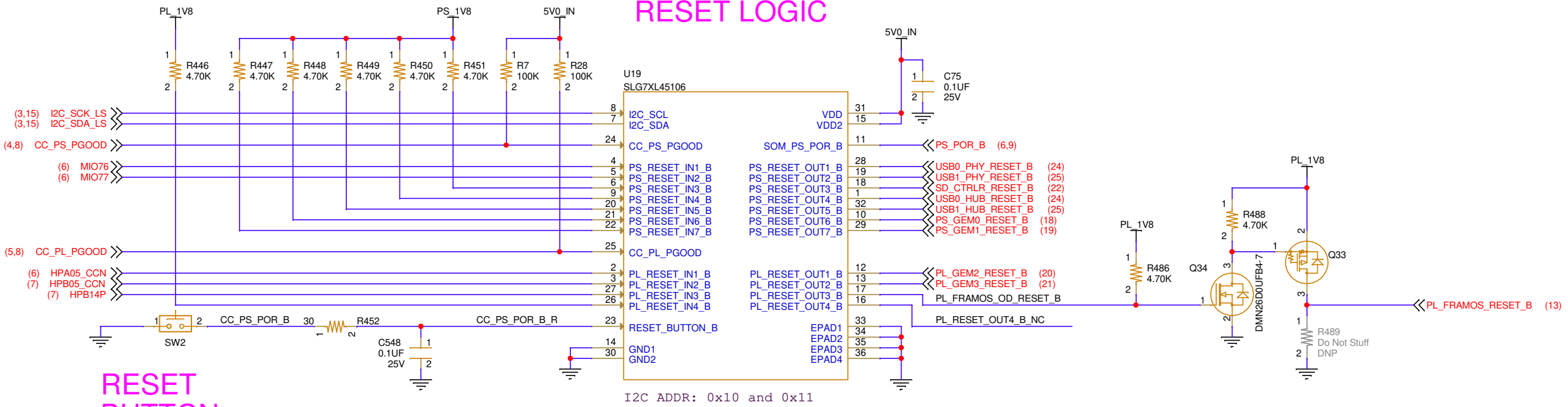


EtherCAT IP EEPROM

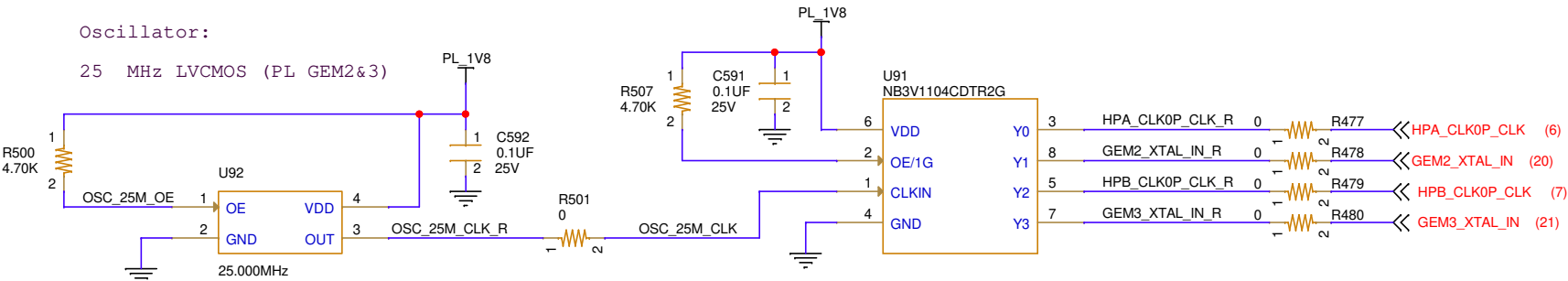
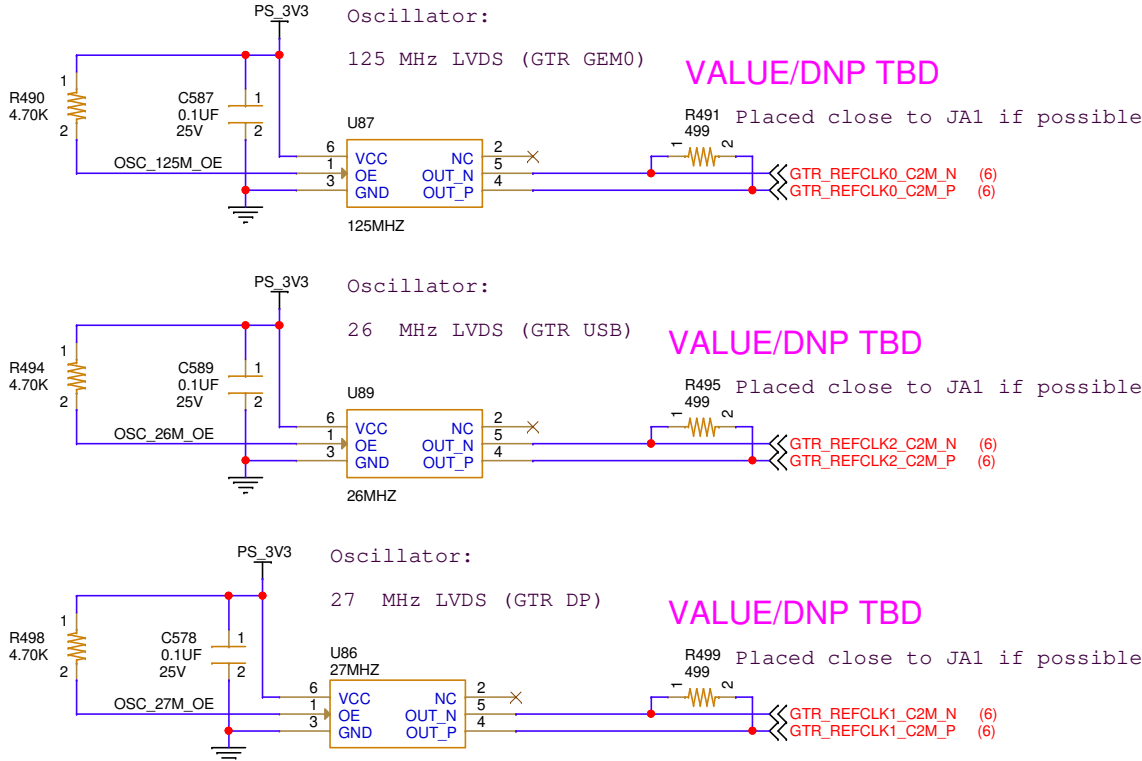
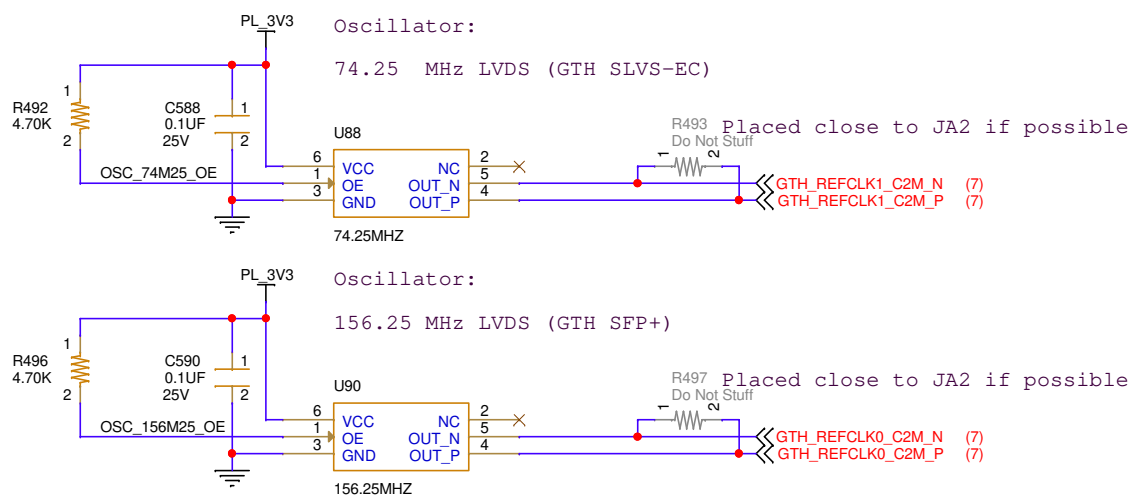



 XILINX 2100 LOGIC DRIVE SAN JOSE CA		SKIT	
Title: SCK-KR 15 - I2C, EEPROM			
Size B	Date Modified: Friday, October 15, 2021	Document Number: 038-05101-01	Rev A02
Engineer: RH/JW		Sheet 15 of 25	

# RESET LOGIC

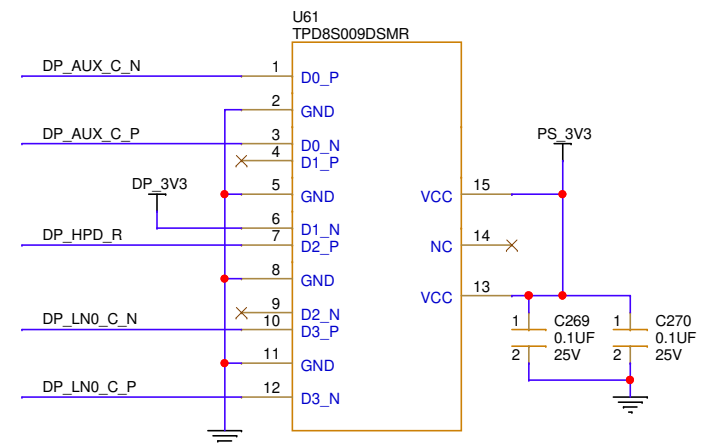
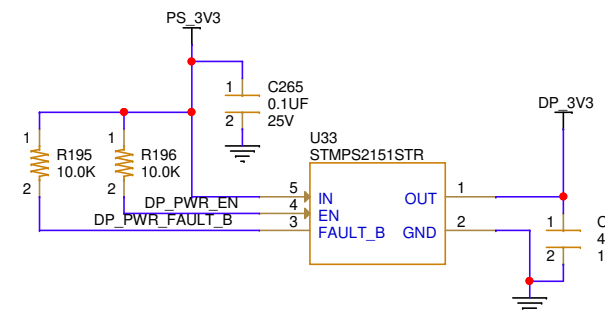
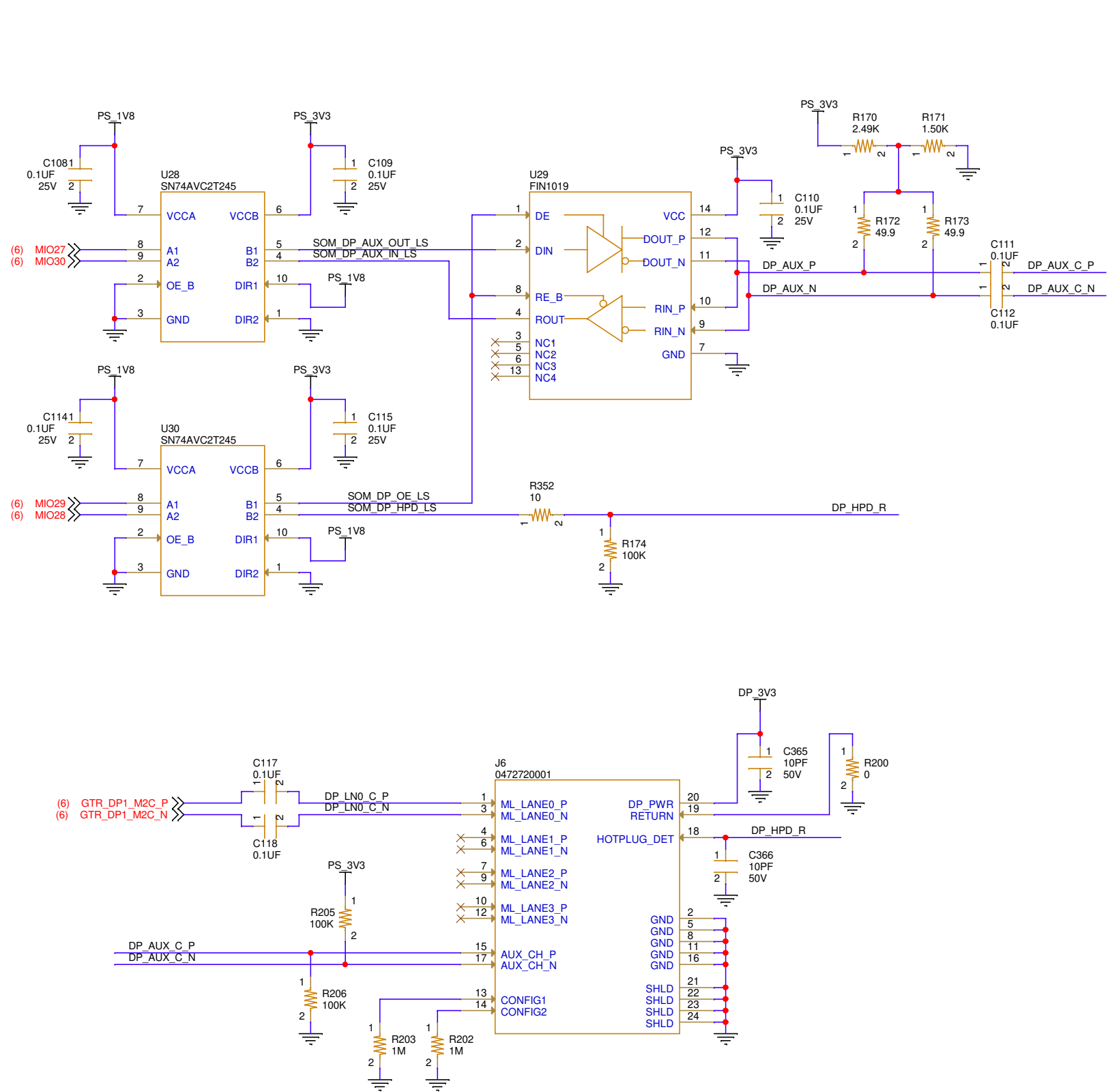



## RESET BUTTON



 2100 LOGIC DRIVE SAN JOSE CA		SKIT	
Title: SCK-KR 16_Clock Gen, Reset			
Size B	Date Modified: Friday, October 15, 2021	Document Number: 038-05101-01	Rev A02
Engineer: RH/JW		Sheet 16 of 25	

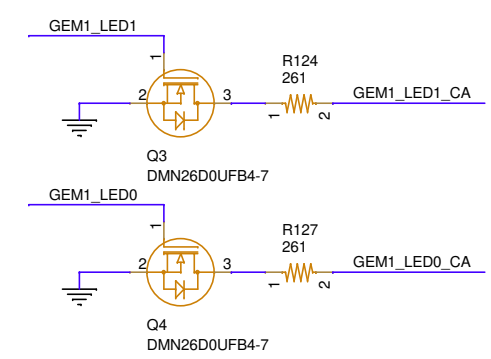
DISPLAY PORT



 <b>XILINX</b> 2100 LOGIC DRIVE SAN JOSE CA		SKIT	
Title: <b>SCK-KR</b> <b>17_DisplayPort</b>			
Size <b>B</b>	Date Modified: Friday, October 15, 2021	Document Number: <b>038-05101-01</b>	Rev <b>A02</b>
Engineer: <b>RH/JW</b>		Sheet 17 of 25	

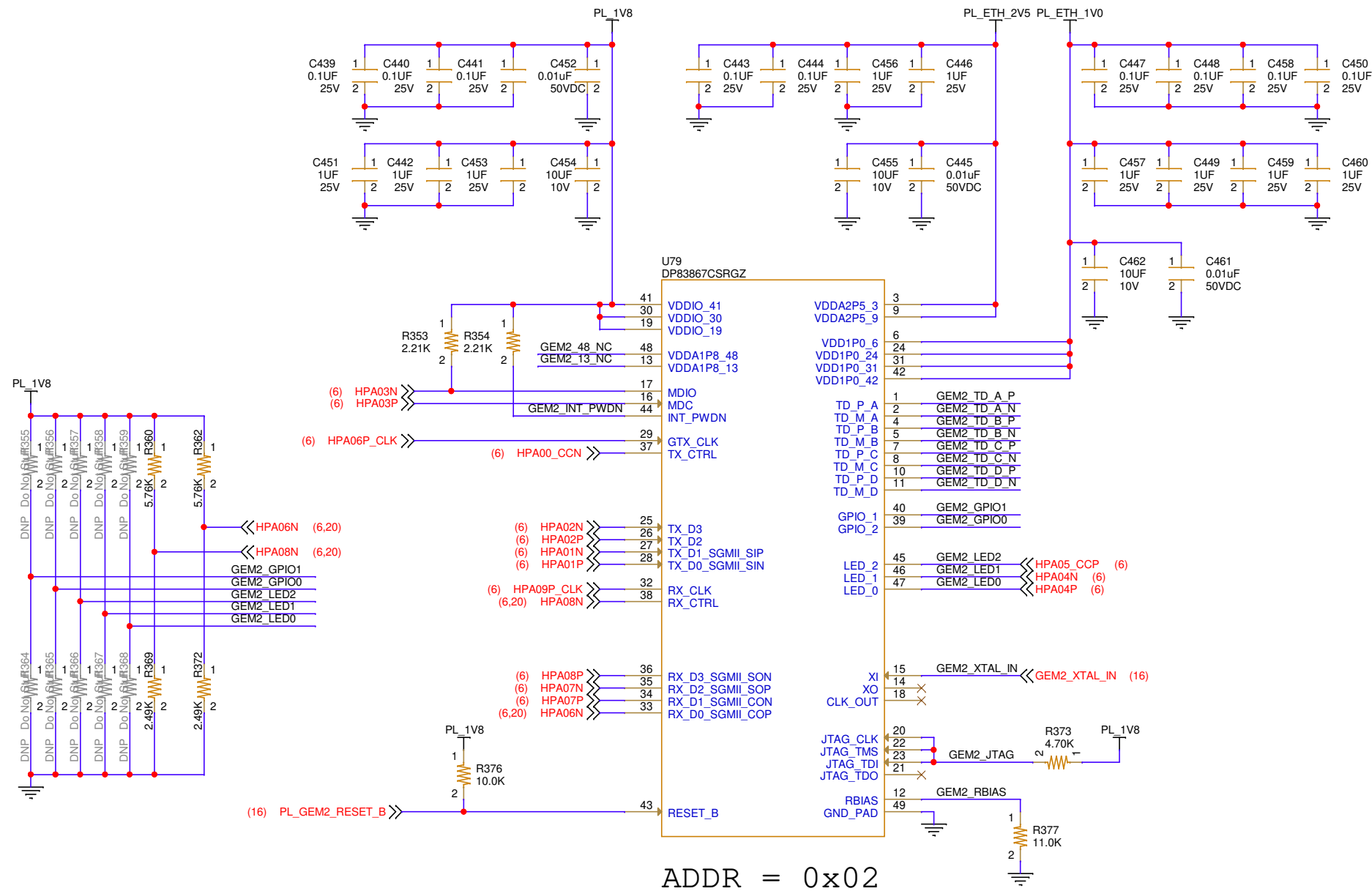
5	4	3	2	1
---	---	---	---	---



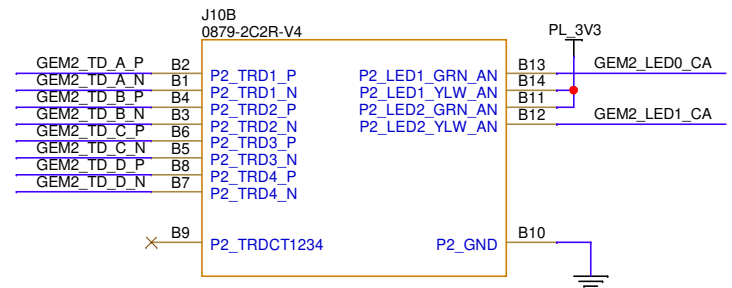


5	4	3	2	1
---	---	---	---	---

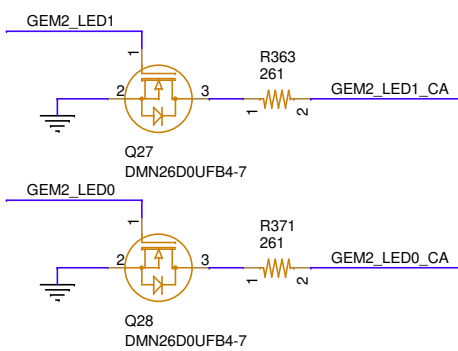
# PL GEM2 RGMII ETHERNET




ADDR = 0x02

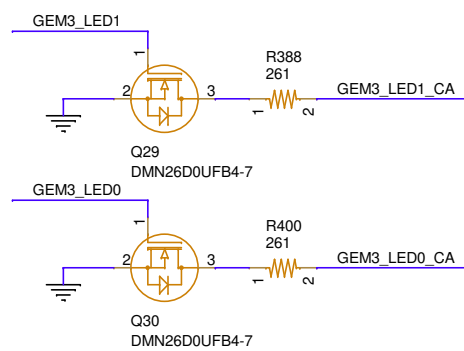
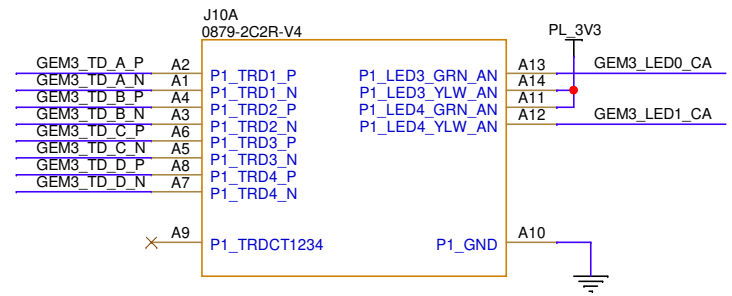
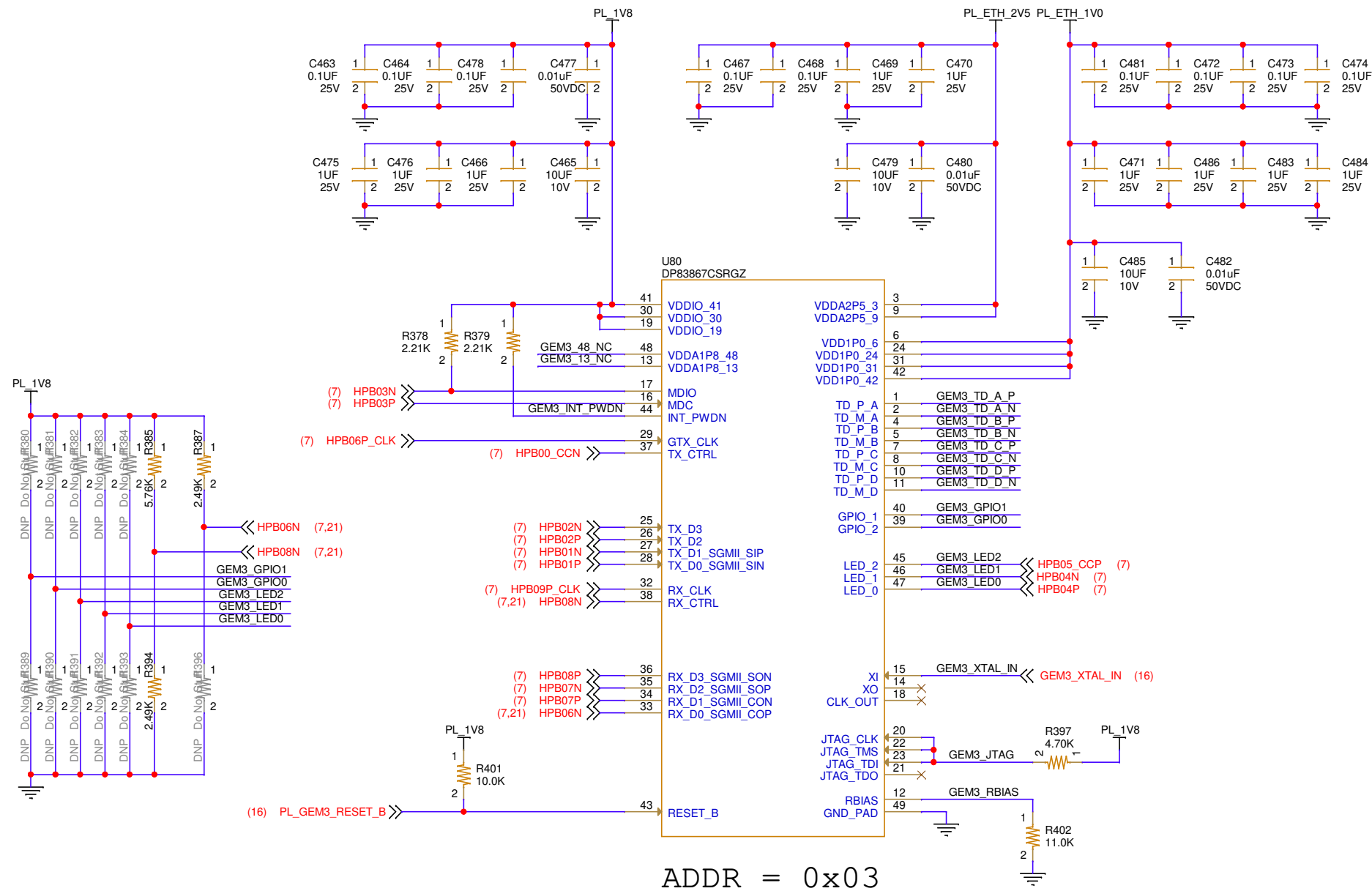



TOP LEFT



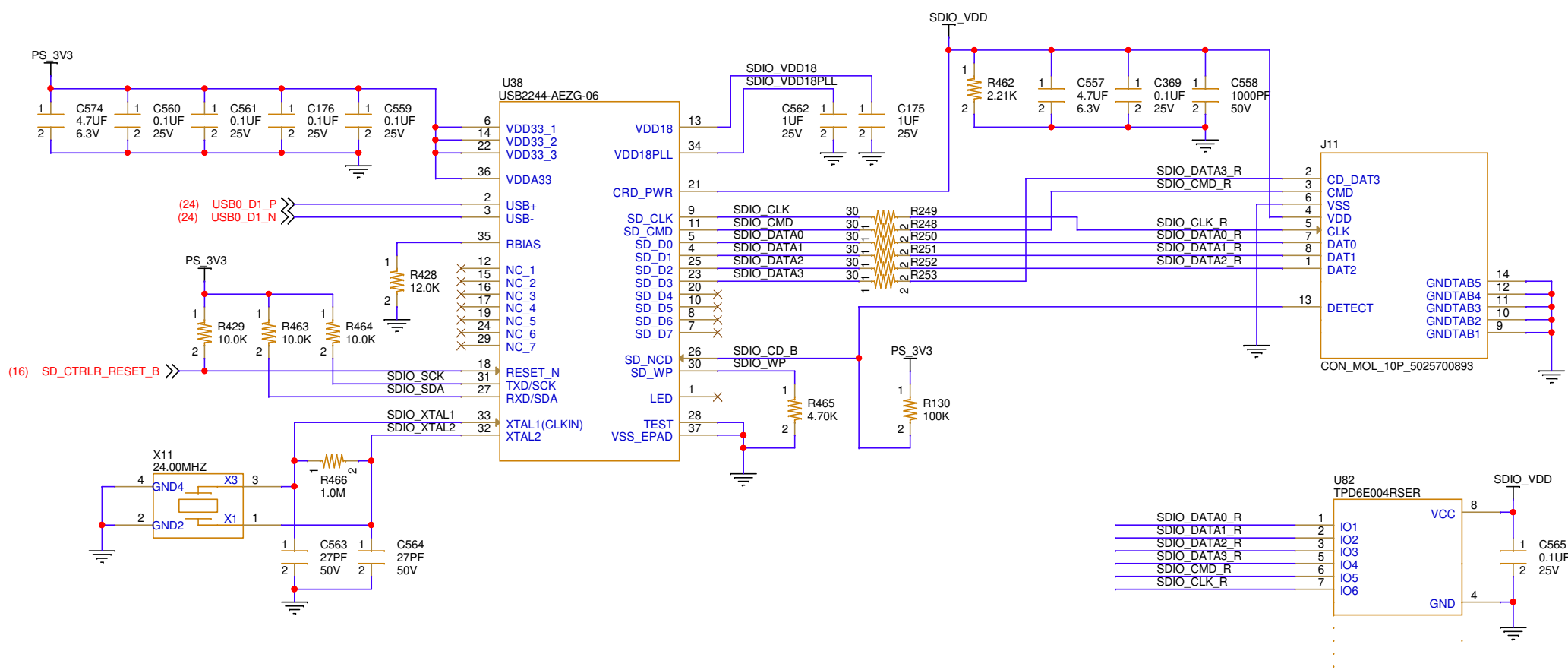
 XILINX 2100 LOGIC DRIVE SAN JOSE CA		SKIT	
Title: SCK-KR 20_PL_GEM2			
Size B	Date Modified: Friday, October 15, 2021	Document Number: 038-05101-01	Rev A02
Engineer: RH/JW		Sheet 20 of 25	

PL GEM3 RGMII ETHERNET

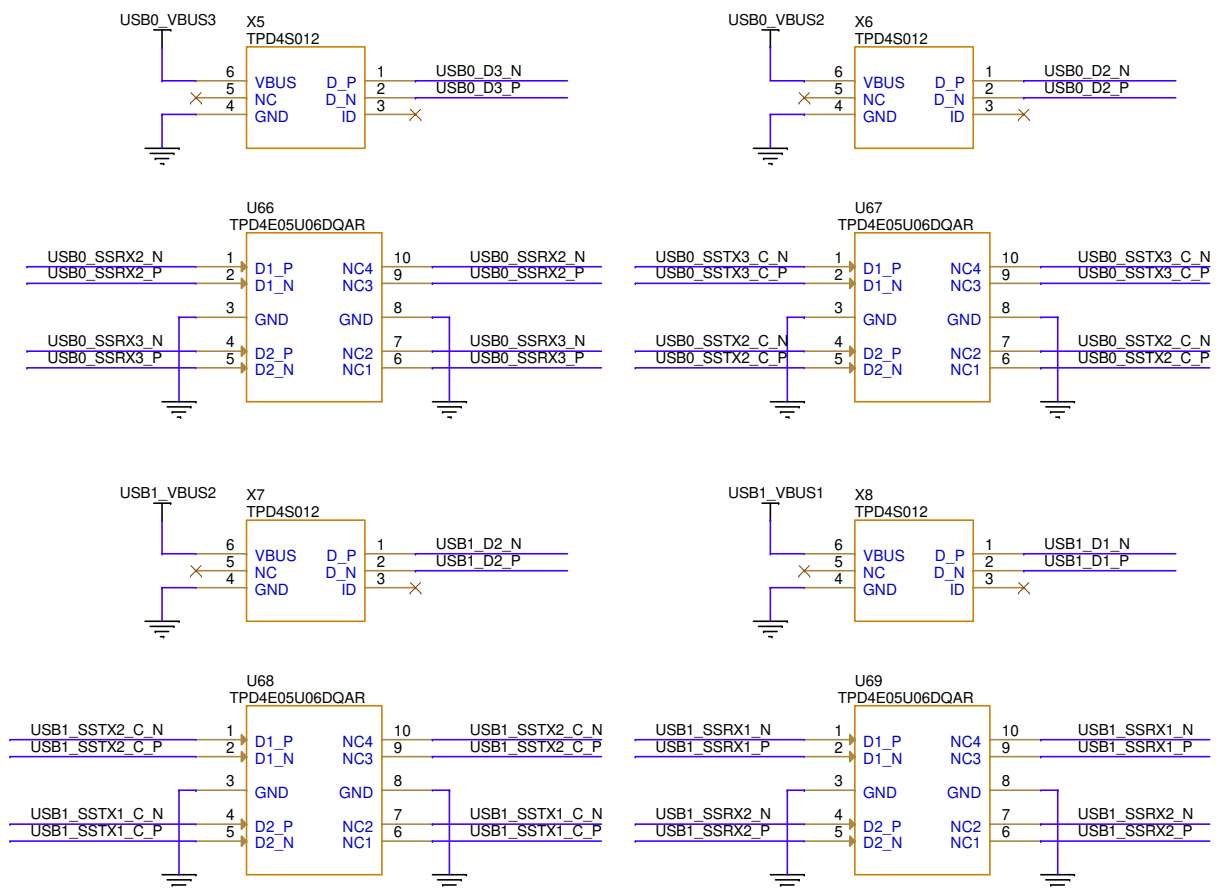
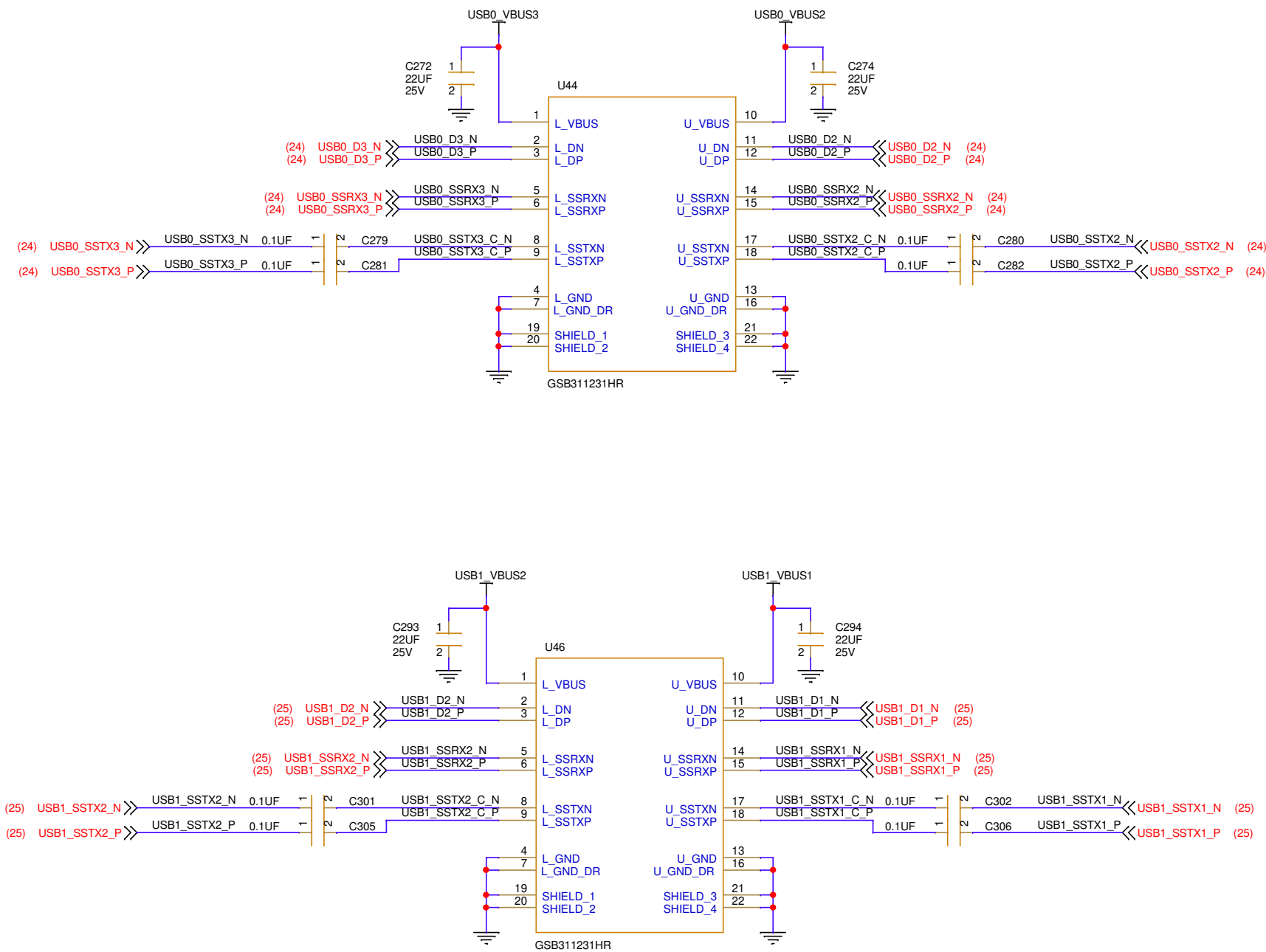



 2100 LOGIC DRIVE SAN JOSE CA		SKIT	
Title: SCK-KR 21_PL_GEM3			
Size B	Date Modified: Friday, October 15, 2021	Document Number: 038-05101-01	Rev A02
Engineer: RH/JW		Sheet 21 of 25	

SD 2.0



# USB CONNECTORS



 <b>XILINX</b> 2100 LOGIC DRIVE SAN JOSE CA		SKIT	
Title: <b>SCK-KR</b> <b>23_USB Connectors</b>			
Size <b>B</b>	Date Modified: Friday, October 15, 2021	Document Number: <b>038-05101-01</b>	Rev <b>A02</b>
Engineer: <b>RH/JW</b>		Sheet 23 of 25	

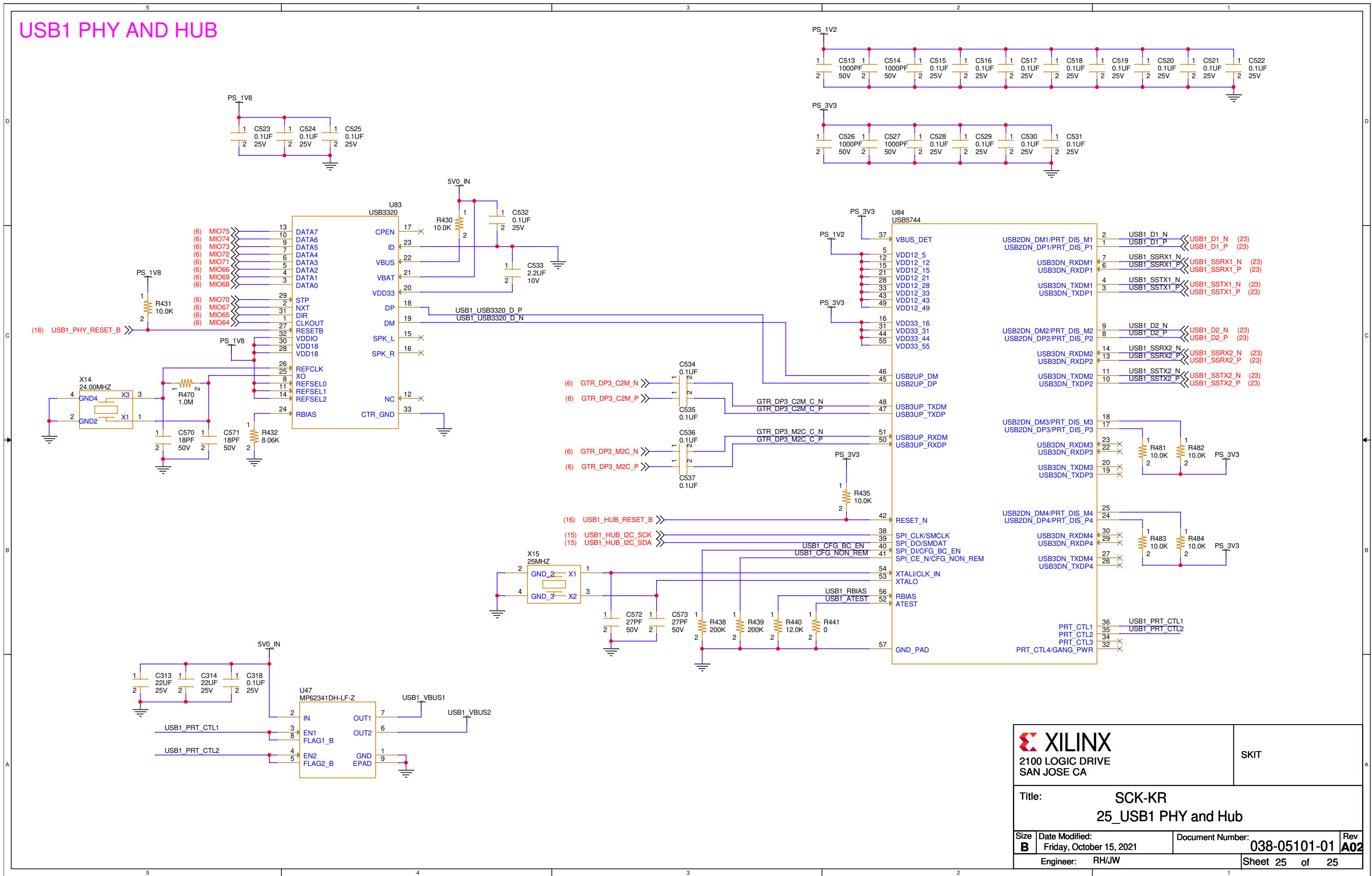



The diagram illustrates the PCB layout for the USB0 PHY and HUB. It includes the following components and connections:

- Power Supply and Decoupling:** PS\_1V8 and PS\_3V3 are connected to various decoupling capacitors (C275, C276, C277, C278, C295, C296, C283, C284, C285, C286, C289, C290, C291, C292, C297, C298, C303, C299, C304, C300).
- USB3320 (U37):** This IC is connected to PS\_1V8, PS\_3V3, and various data lines (DATA0-DATA7, STP, NXT, DIR, CLKOUT, RESETB, VDDIO, VDD18, VDD18, REFCLK, XO, REFSEL0, REFSEL1, REFSEL2, RBIAS, CTR\_GND).
- USB5744 (U43):** This IC is connected to PS\_1V2, PS\_3V3, and various data lines (USB0\_D1\_N, USB0\_D1\_P, USB0\_D2\_N, USB0\_D2\_P, USB0\_D3\_N, USB0\_D3\_P, USB0\_D4\_N, USB0\_D4\_P, USB0\_PRT\_CTL1, USB0\_PRT\_CTL2, USB0\_PRT\_CTL3, USB0\_PRT\_CTL4).
- MP62341DH-LF-Z (U45):** This IC is connected to PS\_3V3 and various data lines (USB0\_PRT\_CTL1, USB0\_PRT\_CTL2, USB0\_PRT\_CTL3, USB0\_PRT\_CTL4).
- Resistors:** R210, R209, R213, R218, R219, R220, R221, R222, R467, R468, R469.
- Capacitors:** C309, C310, C315, C316, C566, C567, C568, C569.
- Crystal Oscillators:** X12 (24.00MHz), X13 (25MHz).
- Reset and Control:** USB0\_PHY\_RESET\_B, USB0\_HUB\_RESET\_B, USB0\_HUB\_I2C\_SCK, USB0\_HUB\_I2C\_SDA.

The layout shows the physical placement of these components on the PCB, with labels for each pin and connection point.

# USB1 PHY AND HUB



 2100 LOGIC DRIVE SAN JOSE CA		SKIT	
Title: SCK-KR 25_USB1 PHY and Hub			
Size B	Date Modified: Friday, October 15, 2021	Document Number: 038-05101-01	Rev A02
Engineer: RH/JW		Sheet 25 of 25	