A. ECAD Design Information

This appendix contains information that supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
R7F701371EABG	292	FBGA	PRBG0292GC-A
R7F701372AEABG	292	FBGA	PRBG0292GC-A
R7F701372EABG	292	FBGA	PRBG0292GC-A

A.2 Symbol Pin Information

A.2.1 292-FBGA

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
A1	VSS	Power	-
A10	P3_1	I/O	GTM0I7/GTMAT0O7/ETH0LINKSTA/SENT4SPCO/CSIH0CSS6
A11	P2_15	I/O	GTM1I7/GTMAT0O3/EXTCLK0O
A12	P2_13	I/O	GTM1I2/GTMAT1O1/CSIH2CSS6/CSIH0DCS/CSIH0SO1
A13	P2_11	I/O	GTM1I4/GTMAT1O3/CSIH2CSS4/CSIH0SI1
A14	P2_9	I/O	GTM1I4/GTMAT0O1N/CSIH0CSS4/RLIN30RX/HSURT1SDIR
A15	P2_7	I/O	GTM1I2/RLIN30TX/INTP5/CSIH0CSS2/MTTCAN0TX/HSURT1SCKI/HSURT1SCKO
A16	P2_5	I/O	GTM0I6/GTMAT0O2/CSIH2CSS2/RLIN31TX/HSURT1SDIO2I/HSURT1SDIO2O
A17	P2_3	I/O	GTM1I1/GTMAT0O1/GTM0I5/GTMAT0O5/CSIH2SI0/CSIH0CSS0/HSURT1SDIO0I/HSURT1SDIO0O
A18	P2_1	I/O	GTM1I0/GTMAT0O0/CSIH1CSS2/CSIH2DCS/CSIH2SO0/HSURT0CSI/HSURT0CSO
A19	VSS	Power	-
A2	VSS	Power	-
A20	VSS	Power	-
A3	ERROROUTZ	Output	-
A4	VSS	Power	-
A5	P3_12	I/O	GTM0I4/GTMAT0O0/ETH0TXD2/CSIH1CSS2/SENT2RX
A6	P3_9	I/O	GTM0I7/GTMAT1O0/ETH0TXD0/CSIH1CSS4/SENT1SPCO
A7	P3_7	I/O	GTM0I4/GTMAT0O4/ETH0CRS/RLIN30TX/CSIH0CSS2/FLX0TXDA
A8	P3_5	I/O	GTM1I5/GTMAT1O2N/ETH0COL/GTMAT0O7/INTP6/FLX0TXENA
A9	P3_3	I/O	GTM1I1/GTMAT1O3N/ETH0MDI/ETH0MDO/SENT1RX/CSIH3CSS2/FLX0RXDB
B1	VSS	Power	-
B10	P3_0	I/O	GTM1I2/GTMAT0O6/SENT3SPCO/CSIH0CSS5
B11	P2_14	I/O	GTM1I4/GTMAT1O3N/CSIH2CSS7/CSIH0CSS0/CSIH0CSS7
B12	P2_12	I/O	GTM0I4/GTMAT1O3N/CSIH2CSS5/CSIH0SCI1/CSIH0SCO1
B13	P2_10	I/O	GTM1I7/GTMAT1O3/CSIH2RYI/CSIH2RYO/RLIN30TX/CSIH3CSS3
B14	P2_8	I/O	GTM1I1/GTMAT0O1N/CSIH0CSS3/EXTCLK0O/HSURT1CSI/HSURT1CSO
B15	P2_6	I/O	GTM1I6/GTMAT0O2/RLIN30RX/CSIH2CSS3/MTTCAN0RX/CSIH1CSS1/HSURT1/HSURT1SDIO3I/SDIO3O
B16	P2_4	I/O	GTM0I3/GTMAT0O3/ESO0Z/CSIH2CSS1/RLIN31RX/SENT0SPCO/HSURT1/HSURT1SDIO1I/SDIO1O
B17	P2_2	I/O	GTM0I2/GTMAT0O2N/GTM0I4/CSIH2CSS1/CSIH1SCI1/CSIH1SCO1/HSURT0SDIR
B18	P2_0	I/O	GTM0I1/GTMAT0O1N/GTM0I0/CSIH1CSS0/CSIH2SCI0/CSIH2SCO0/HSURT0SCKI/HSURT0SCKO
B19	P1_6	I/O	GTM1I3/GTMAT1O4/CSIH3CSS2/ESO2Z/CSIH1CSS7
B2	P3_14	I/O	GTM0I1/GTMAT0O1/RLIN30RX/ETH0TXEN/MCAN0RX/FLX0RXDA/INTP10
B20	VSS	Power	-
B3	VSS	Power	-
B4	P3_13	I/O	GTM0I0/GTMAT0O0/ETH0REF50CK/ETH0TXD3/CSIH1CSS3/SENT3RX/SENT1SPCO
B5	P3_10	I/O	GTM0I5/GTMAT0O1/ETH0TXD1/CSIH1CSS5

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
B6	P3_8	I/O	GTM1I6/GTMAT0O3N/ETH0TXER/INTP7/CSIH1CSS1/FLX0TXENB
B7	P3_6	I/O	GTM0I6/GTMAT0O3N/ETH0MDC/CSIH0CSS1/FLX0TXDB
B8	P3_4	I/O	GTM1I5/GTMAT1O2/GTMAT0O6/CSIH1CSS3/FLX0STPWT/SENT2SPCO
B9	P3_2	I/O	GTM1I0/GTMAT1O3/RLIN30RX/SENT0RX/CSIH3CSS1/FLX0RXDA
C1	P4_0	I/O	GTM1I0/GTMAT0O0/ETH0RXER/MCAN0TX/FLX0RXDB/RLIN30TX
C19	P1_5	I/O	GTM1I6/GTMAT2O4/CSIH3CSS1
C2	P4_1	I/O	GTM0I2/GTMAT0O2/ETH0TXCLK/CSIH1SSIZ/CSIH1CSS0/FLX0STPWT
C20	P1_4	I/O	GTM0I0/GTMAT1O3/CSIH3DCS/CSIH3SO0/HSURT0SDIO3I/HSURT0SDIO3O
D1	MODE0	Input	P4_2/GTM1I1/GTMAT0O1/ETH0RXCLK/CSIH1DCS/CSIH1SO0/FLX0TXENA
D10	P8_2	I/O	GTM0I0/GTMAT2O3/ETH1CRS/FLXNTUOUT/MEMC0A3/CSIH3SSIZ/CSIH3CSS0
D11	P8_4	I/O	GTM0I1/GTMAT2O4/ETH1RXD1/MEMC0A5
D12	P8_5	I/O	GTM1I4/GTMAT1O4/ETH1RXD0/MEMC0A6
D13	P8_6	I/O	GTM1I5/GTMAT1O5/ETH1RXCLK/MEMC0A7
D14	P8_8	I/O	GTM0I7/GTMAT1O7/ETH1REF50CK/MEMC0D0I/MEMC0D0O/MTTCAN0
D15	P8_9	I/O	GTM1I3/GTMAT2O0/ETH1TXD0/MEMC0D1I/MEMC0D1O/MTTCAN0EVT
D16	P1_7	I/O	GTM1I4/GTMAT1O5/CSIH3CSS3/CSIH1CSS6
D17	VSS	Power	-
D19	P1_3	I/O	GTM0I4/GTMAT0O3/CSIH3SI0/HSURT0SDIO2I/HSURT0SDIO2O
D2	MODE1	Input	P4_3/GTM0I3/GTMAT0O0N/ETH0RXD0/CSIH1SCI0/CSIH1SCO0/FLX0TXDB
D20	P1_2	I/O	GTM0I5/GTMAT0O2/CSIH3SCI0/CSIH3SCO0/CSIH1DCS/CSIH1SO1/HSURT0SDIO1I/HSURT0SDIO1O
D4	VSS	Power	-
D5	P7_4	Output	GTM1I6/GTMAT1O7/ETH1RXDV/CSIH3CSS7/RLIN32RX
D6	P7_3	Output	GTM0I3/GTMAT2O0/FLX1TXDB/ETH1LINKSTA/MEMC0WRZ
D7	P7_2	Output	GTM0I7/GTMAT2O0N/FLX1RXDB/ETH1COL/MEMC0RDZ
D8	P7_1	Output	GTM1I2/GTMAT2O1/FLX1TXENB/SENT6RX/ETH1MDC
D9	P7_0	Output	GTM0I6/GTMAT2O1N/SENT7RX/MEMC0A0/CSIH3RYI/CSIH3RYO
E1	P4_4	I/O	GTM0I6/GTMAT0O2/ETH0RXD1/RLIN30TX/CSIH1SI0/FLX0TXDA
E10	P8_1	I/O	GTM0I2/GTMAT2O2N/ETH1RXD2/MEMC0A2/CSIH3SI2
E11	P8_3	I/O	GTM0I4/GTMAT2O3N/ETH1RXER/MEMC0A4/CSIH3SCI2/CSIH3SCO2
E12	E1VCC	Power	-
E13	E1VSS	Power	-
E14	P8_7	I/O	GTM1I2/GTMAT1O6/ETH1TXCLK/MEMC0A8
E15	VDD	Power	-
E16	VSS	Power	-
E17	P8_10	I/O	GTM1I7/GTMAT2O0N/ETH1TXEN/MEMC0D2I/MEMC0D2O/MTTCAN0SOC
E19	P1_1	I/O	GTM0I1/GTMAT0O5/INTP4/CSIH3CSS0/CSIH1SI1/HSURT0SDIO0I/HSURT0SDIO0O
E2	FLMD1	Input	P4_5/GTM1I4/GTMAT0O0/ETH0RXD2/MTTCAN0RX/RLIN30RX/FLX0TXENB
E20	X1	Input	-
E4	P7_5	Output	GTM1I7/GTMAT1O6/FLX1TXDA/CSIH3CSS6/RLIN32TX
E5	VSS	Power	-
E6	VCC	Power	-
E7	E1VSS	Power	-
E8	E1VCC	Power	-
E9	P8_0	I/O	GTM0I5/GTMAT2O2/ETH1RXD3/INTP8/MEMC0A1/CSIH3DCS/CSIH3SO2
F1	P4_6	I/O	GTM1I5/GTMAT0O5/ETH0RXD3/RLIN30TX/MTTCAN0TX
F16	SYSVCC	Power	-
F17	P8_11	I/O	GTM0I6/GTMAT2O1/ETH1TXD1/MEMC0D3I/MEMC0D3O/MTTCAN0TMP
F19	OSCVSS	Power	-
F2	P4_7	I/O	GTM1I1/GTMAT0O5/ETH0RXDV/INTP0/EXTCLK0O/SENT0RX/BHPDGRCLK0
F20	X2	Output	-
F4	P7_6	Output	GTM1I1/GTMAT1O5/FLX1TXENA/CSIH3CSS5/MEMC0CS0Z
F5	VSS	Power	-
G1	P4_8	I/O	GTM1I0/GTMAT0O0N/ETH0WOL/RLIN30RX/SENT1RX/BHPDGRCLK1
G10	VDD	Power	-
G11	VDD	Power	-
G12	VDD	Power	-
G13	VDD	Power	-
G16	E1VSS	Power	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
G17	P8_12	I/O	GTM0I3/GTMAT2O1N/ETH1TXD2/MEMC0D4I/MEMC0D4O/MTTCAN0RTP
G19	OSCVSS	Power	-
G2	P4_9	I/O	GTM1I4/GTMAT0O4/EXTCLK1O/CSIH2SSIZ/CSIH2CSS0/RLIN30TX
G20	RESETZ	Input	-
G4	P7_7	Output	GTM1I0/GTMAT1O4/FLX1RXDA/INTP11/CSIH3CSS4/MEMC0CS1Z
G5	VCC	Power	-
G8	VSS	Power	-
G9	VDD	Power	-
H1	P4_10	I/O	GTM0I3/GTMAT1O1N/MCAN1RX/CSIH2DCS/CSIH2SO2/CSIH0CSS3
H10	VSS	Power	-
H11	VSS	Power	-
H12	VSS	Power	-
H14	VSS	Power	-
H16	E1VCC	Power	-
H17	P8_13	I/O	GTM0I1/GTMAT2O2/ETH1TXD3/MEMC0D5I/MEMC0D5O
H19	JP0_4	Input	TRSTZ
H2	P4_11	I/O	GTM0I2/GTMAT1O2N/MCAN1TX/CSIH2SCI2/CSIH2SCO2/CSIH1CSS4
H20	JP0_0	I/O	FLSCI3RXD/FLSCI3TXD/TDI
H4	P7_8	Output	CSIH3CSS1/ETH1WOL/MEMC0CS2Z
H5	E1VSS	Power	-
H7	VSS	Power	-
H9	VSS	Power	-
J1	P4_12	I/O	GTM0I1/GTMAT1O3N/INTP1/FLXNTUOUT/CSIH2SI2/ADC1TRG/CSIH1CSS5
J10	VSS	Power	-
J11	VSS	Power	-
J13	VSS	Power	-
J14	VDD	Power	-
J16	SYSVCC	Power	-
J17	P8_14	I/O	GTM1I5/GTMAT2O2N/ETH1TXER/MEMC0D6I/MEMC0D6O
J19	JP0_1	I/O	FLSCI3TXD/TDO
J2	P4_13	I/O	GTM1I7/GTMAT1O0/CSIH0CSS5/SENT2RX/ESO1Z/CSIH2CSS7
J20	JP0_2	I/O	FLSCI3SCKI/TCK
J4	P7_9	Output	CSIH3CSS2/FLX1STPWT/MEMC0CS3Z
J5	E1VCC	Power	-
J7	VDD	Power	-
J8	VSS	Power	-
K1	P4_14	I/O	GTM1I7/GTMAT1O0N/CSIH0CSS6/SENT3RX/EXTCLK1O
K10	VSS	Power	-
K11	VSS	Power	-
K12	VSS	Power	-
K13	VSS	Power	-
K14	VDD	Power	-
K16	P8_15	I/O	GTM1I0/GTMAT2O3/ETH1MDI/ETH1MDO/MEMC0D7I/MEMC0D7O
K17	P9_8	I/O	GTMAT1O0/MCAN2RX
K19	JP0_3	I/O	TMS
K2	P6_0	Output	GTM1I6/GTMAT1O1/SENT4RX/CSIH1CSS6/ICUMGPIO0
K20	JP0_5	I/O	RDYZ
K4	ADC1I12	I/O	-
K5	VDD	Power	-
K7	VDD	Power	-
K8	VSS	Power	-
K9	VSS	Power	-
L1	P6_1	Output	GTM1I6/GTMAT1O1N/SENT5RX/CSIH0CSS7/ICUMGPIO1
L10	VSS	Power	-
L11	VSS	Power	-
L12	VSS	Power	-
L13	VSS	Power	-
L14	VDD	Power	-
L16	P9_7	I/O	GTMAT1O0N/MCAN2TX

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
L17	P9_6	I/O	GTMAT1O1/CSIH1CSS4
L19	P0_14	I/O	GTM0I2/GTMAT0O4/EXTCLK1O/SENT0RX/MCAN0TX/BHPDGREN
L2	ADC1I0	I/O	-
L20	P0_13	I/O	GTM1I3/GTMAT1O1N/CSIH1RYI/CSIH1RYO/SENT4RX/MCAN0RX
L4	ADC1I13	I/O	-
L5	VCC	Power	-
L7	VDD	Power	-
L8	VSS	Power	-
L9	VSS	Power	-
M1	ADC1I1	I/O	-
M10	VSS	Power	-
M11	VSS	Power	-
M13	VSS	Power	-
M14	VDD	Power	-
M16	E0VCC	Power	-
M17	P9_5	I/O	GTMAT1O1N/CSIH1CSS5
M19	RESETOUTZ	Output	P0_10
M2	ADC1I2	I/O	-
M20	CVMOUTZ	Output	-
M4	ADC1I14	I/O	-
M5	VCC	Power	-
M7	VDD	Power	-
M8	VSS	Power	-
N1	ADC1I3	I/O	-
N10	VSS	Power	-
N11	VSS	Power	-
N12	VSS	Power	-
N14	VSS	Power	-
N16	E0VSS	Power	-
N17	P9_4	I/O	GTMAT1O2
N19	FLMD0	Input	-
N2	ADC1I4	I/O	-
N20	P0_9	I/O	GTM1I4/GTMAT1O0N/EXTCLK1O/CSIH0DCS/CSIH0SO2/CSIH1SI2
N4	ADC1I15	I/O	-
N5	VSS	Power	-
N7	VSS	Power	-
N9	VSS	Power	-
P1	ADC1I5	I/O	-
P10	VDD	Power	-
P11	VDD	Power	-
P12	VDD	Power	-
P13	VSS	Power	-
P16	P9_3	I/O	GTMAT1O2N
P17	P9_2	I/O	GTMAT1O3/RLIN33RX
P19	P0_8	I/O	GTM0I5/GTMAT1O3/MCAN1TX/CSIH0SCI2/CSIH0SCO2/CSIH1SCI2/CSIH1SCO2
P2	ADC1I6	I/O	-
P20	P0_7	I/O	GTM0I4/GTMAT1O2/MCAN1RX/CSIH0SI2/CSIH1DCS/CSIH1SO2
P4	ADC1I16	I/O	-
P5	ADC1I17	I/O	-
P8	VSS	Power	-
P9	VDD	Power	-
R1	ADC1I7	I/O	-
R16	VSS	Power	-
R17	P9_1	I/O	GTMAT1O3N/RLIN33TX
R19	P0_6	I/O	GTM0I0/GTMAT0O6/CSIH2CSS7/CSIH1CSS0
R2	ADC1I8	I/O	-
R20	P0_5	I/O	GTM1I3/GTMAT1O0/INTP3/CSIH2CSS6/CSIH1CSS1
R4	ADC1I18	I/O	-
R5	A0VSS	Power	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
T1	ADC1I9	I/O	-
T10	E0VCC	Power	-
T11	E0VSS	Power	-
T12	P6_7	Output	GTM0I5/GTMAT2O2/HSURT2SDIO1I/HSURT2SDIO1O/SENT7SPCO
T13	P6_9	Output	GTM1I2/GTMAT2O1/HSURT3SDIR
T14	P6_11	Output	GTM0I3/GTMAT2O0/CSIH3CSS0/HSURT3SCKI/HSURT3SCKO
T15	VSS	Power	-
T16	VSS	Power	-
T17	P9_0	I/O	GTMAT0O4
T19	P0_4	I/O	GTM0I1/GTMAT1O2/CSIH2CSS5/CSIH1CSS2
T2	ADC1I10	I/O	-
T20	P0_3	I/O	GTM1I0/GTMAT0O0/CSIH2CSS4/CSIH0CSS3
T4	ADC1I19	I/O	-
T5	A0VSS	Power	-
T6	A0VSS	Power	-
T7	ADC0I17	I/O	-
T8	ADC0I15	I/O	-
T9	ADC0I13	I/O	-
U1	A1VCC	Power	-
U10	P6_4	Output	GTM0I4/GTMAT2O3N/HSURT2SCKI/HSURT2SCKO/SENT6RX/INTP9
U11	P6_5	Output	GTM0I0/GTMAT2O3/HSURT2SDIO3I/HSURT2SDIO3O/SENT7RX
U12	P6_6	Output	GTM0I2/GTMAT2O2N/HSURT2SDIO2I/HSURT2SDIO2O/SENT6SPCO
U13	P6_8	Output	GTM0I6/GTMAT2O1N/HSURT2SDIO0I/HSURT2SDIO0O
U14	P6_10	Output	GTM0I7/GTMAT2O0N/CSIH3SCI1/CSIH3SCO1/HSURT3CSI/HSURT3CSO
U15	P6_12	Output	GTM1I6/GTMAT1O7/CSIH3SI1/HSURT3SDIO3I/HSURT3SDIO3O
U16	P6_13	Output	GTM1I7/GTMAT1O6/CSIH3DCS/CSIH3SO1/HSURT3SDIO2I/HSURT3SDIO2O
U17	VSS	Power	-
U19	P6_14	Output	GTM1I1/GTMAT1O5/HSURT3SDIO1I/HSURT3SDIO1O
U2	ADC1I11	I/O	-
U20	P0_2	I/O	GTM0I2/GTMAT1O1/CSIH2CSS2/CSIH0CSS4
U4	A0VSS	Power	-
U5	ADC0I19	I/O	-
U6	ADC0I18	I/O	-
U7	ADC0I16	I/O	-
U8	ADC0I14	I/O	-
U9	ADC0I12	I/O	-
V1	A1VREFH	Power	-
V19	P6_15	Output	GTM1I0/GTMAT1O4/HSURT3SDIO0I/HSURT3SDIO0O
V2	A1VSS	Power	-
V20	P3_11	I/O	GTM1I1/GTMAT0O1/CSIH1CSS7/CSIH0CSS7
W1	A1VSS	Power	-
W10	P6_2	Output	GTM0I6/GTMAT0O6/HSURT2SDIR/SENT4RX/CSIH1CSS7
W11	P5_0	I/O	GTM0I0/GTMAT0O3/MCAN0RX/CSIH2CSS2
W12	P5_4	I/O	GTM1I5/GTMAT0O1/CSIH0SSIZ/CSIH0CSS0/ADC0TRG/ADC1CNV/RLIN31RX
W13	P5_6	I/O	GTM0I3/GTMAT1O0/CSIH0SCI0/CSIH0SCO0/SENT4SPCO/CSIH2DCS/CSIH2SO1
W14	P5_8	I/O	GTM0I7/GTMAT0O3/RLIN30TX/EXTCLK1O/CSIH0RYI/CSIH0RYO
W15	P5_10	I/O	GTM0I6/GTMAT1O1/EXTCLK0O/MCAN1RX/CSIH2SI1
W16	P5_12	I/O	GTM1I1/GTMAT1O2/EXTCLK0O/CSIH2CSS3/SENT3RX
W17	P5_14	I/O	GTM1I2/GTMAT0O2/MTTCAN0TX/RLIN30TX/CSIH2CSS0
W18	P0_0	I/O	GTM0I6/GTMAT0O2/SENT0RX/CSIH0CSS1/CSIH0CSS5
W19	P0_1	I/O	GTM0I3/GTMAT0O3N/SENT1RX/CSIH1CSS6/CSIH0CSS6
W2	A1VSS	Power	-
W20	VSS	Power	-
W3	A0VSS	Power	-
W4	ADC0I11	I/O	-
W5	ADC0I9	I/O	-
W6	ADC0I7	I/O	-
W7	ADC0I5	I/O	-
W8	ADC0I3	I/O	-

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
W9	ADC0I1	I/O	-
Y1	A1VSS	Power	-
Y10	ADC0I0	I/O	-
Y11	P6_3	Output	GTM0I3/GTMAT0O7/HSURT2CSI/HSURT2CSO/SENT5RX/MCAN0TX
Y12	P5_1	I/O	GTM1I3/GTMAT0O0N/CSIH0CSS1/MCAN0TX/CSIH2CSS3
Y13	P5_5	I/O	GTM1I0/GTMAT0O4/CSIH0DCS/CSIH0SO0/ADC0CNV/RLIN31TX
Y14	P5_7	I/O	GTM0I7/GTMAT1O0N/CSIH0SI0/NMI/SENT5SPCO/CSIH2SCI1/CSIH2SCO1
Y15	P5_9	I/O	GTM1I3/GTMAT0O3N/RLIN30RX/MCAN1TX/CSIH1CSS3
Y16	P5_11	I/O	GTM0I6/GTMAT1O1N
Y17	P5_13	I/O	GTM1I2/GTMAT1O2N/SENT2RX/INTP2/CSIH0CSS2/RLIN30RX
Y18	P5_15	I/O	GTM1I5/GTMAT0O2N/MTTCAN0RX/RLIN30RX/CSIH0CSS4
Y19	VSS	Power	-
Y2	A0VSS	Power	-
Y20	VSS	Power	-
Y3	A0VREFH	Power	-
Y4	A0VCC	Power	-
Y5	ADC0I10	I/O	-
Y6	ADC0I8	I/O	-
Y7	ADC0I6	I/O	-
Y8	ADC0I4	I/O	-
Y9	ADC0I2	I/O	-

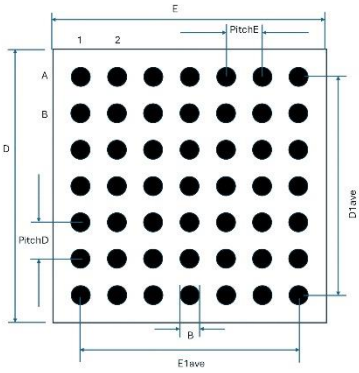
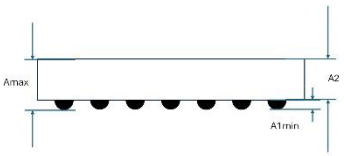
A.3 Symbol Parameters

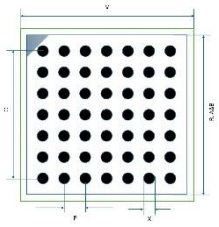
Orderable Part Number	Min Input Voltage	Max Input Voltage	Max Output Frequency	Min Operating Temperature	Max Operating Temperature	RAM Size	Memory Size	Interface	Number of ADC Channels	Number of I2C Channels	Number of SPI Channels	Number of UART Channels	Number of Timers/Counters
R7F701371EABG	1.2 V	1.35 V	240 MHz	-40 °C	+150 °C	1088 KB	8 MB	LIN, SPI, UART	12-bit X 40-Ch	0	4	4	64-bit X 2-Ch
R7F701372AEABG	1.2 V	1.35 V	240 MHz	-40 °C	+150 °C	1088 KB	4 MB	LIN, SPI, UART	12-bit X 32-Ch	0	4	4	64-bit X 2-Ch
R7F701372EABG	1.2 V	1.35 V	240 MHz	-40 °C	+150 °C	1088 KB	4 MB	LIN, SPI, UART	12-bit X 32-Ch	0	4	4	64-bit X 2-Ch

A.4 **Footprint Design Information**

A.4.1 292-FBGA

IPC Footprint Type	Package Code/ POD number	Number of Pins
BGA	PRBG0292GC-A	292

Description	Dimension	Value (mm)	Diagram
Minimum body span (vertical side)	Dmin	17	
Maximum body span (vertical side)	Dmax	17	
Average length of grid (vertical side)	D1ave	15.2	
Minimum body span (horizontal side)	Emin	17	
Maximum body span (horizontal side)	Emax	17	
Average length of grid (horizontal side)	E1ave	15.2	
Minimum Standoff Height	A1min	0.3	
Maximum Height	Amax	17	
Average ball diameter	Bnom	1.9	
Distance between the center of any two adjacent balls (vertical side)	PitchD	0.55	
Distance between the center of any two adjacent balls (horizontal side)	PitchE	0.8	
P = Plain Grid, S = Staggered Grid	GridType	0.8	
F = Full Matrix, P = Perimeter, SD = Selectively Depopulated, TE = Thermally Enhanced	MatrixType	P	
Number of balls (vertical side)	Rows	P	
Number of balls (horizontal side)	Columns	20	
Maximum number of ball positions (Rows x Columns)	Nmax	20	
Number of actual balls present	PinCount	20	
Ball positions removed from matrix. Example: C5-H10,B6-B9,A1	DepopulateBalls	-	
Ball positions added back into depopulated matrix. Example: C8,D6-F9	RepopulateBalls	-	

Recommended Land Pattern (NSMD Design)			
Description	**Dimension**	**Value (mm)**	**Diagram**
Diameter of pad. If specified this overrides the calculated value. This can be used to specify a manufacturer's recommended pad size.	X	-	
Solder Mask Expansion	S	-	