A. ECAD Design Information

This appendix contains information that supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
R5F212C7SDFP#V2	80	LFQFP	PLQP0080KB-A
R5F212C7SNFP#V2	80	LFQFP	PLQP0080KB-A
R5F212C8SNFP#V2	80	LFQFP	PLQP0080KB-A
R5F212CASNFP#V2	80	LFQFP	PLQP0080KB-A
R5F212CCSDFP#V2	80	LFQFP	PLQP0080KB-A
R5F212CCSNFP#V2	80	LFQFP	PLQP0080KB-A
R5F212D7SNFP#V2	80	LFQFP	PLQP0080KB-A
R5F212D8SDFP#V2	80	LFQFP	PLQP0080KB-A
R5F212D8SNFP#V2	80	LFQFP	PLQP0080KB-A
R5F212DASDFP#V2	80	LFQFP	PLQP0080KB-A
R5F212DASNFP#V2	80	LFQFP	PLQP0080KB-A
R5F212DCSNFP#V2	80	LFQFP	PLQP0080KB-A

A.2 Symbol Pin Information

A.2.1 80-LFQFP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	P3_3	I/O	SSI
2	P3_4	I/O	SCS#/SDA
3	P5_7	I/O	-
4	P5_6	I/O	-
5	P5_5	I/O	-
6	MODE	Input	-
7	XCIN	Input	P4_3
8	XCOUT	Output	P4_4
9	\RESET	Input	-
10	XOUT	Output	P4_7
11	VSS	Power	AVSS
12	XIN	Input	P4_6
13	VCC	Power	AVCC
14	P5_4	I/O	TRCIOD
15	P5_3	I/O	TRCIOC
16	P5_2	I/O	TRCIOB
17	P5_1	I/O	TRCIOA/TRCTRG
18	P5_0	I/O	TRCCLK
19	P9_3	I/O	-
20	P9_2	I/O	-
21	P9_1	I/O	-
22	P9_0	I/O	-
23	P2_7	I/O	TRDIOD1
24	P2_6	I/O	TRDIOC1
25	P2_5	I/O	TRDIOB1
26	P2_4	I/O	TRDIOA1
27	P2_3	I/O	TRDIOD0
28	P2_2	I/O	TRDIOC0
29	P2_1	I/O	TRDIOB0
30	P2_0	I/O	TRDIOA0/ TRDCLK
31	P1_7	I/O	INT1#/TRAIO
32	P1_6	I/O	CLK0
33	P1_5	I/O	(INT1#)/(TRAIO)/RXD0

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
34	P1_4	I/O	TXD0
35	P8_7	I/O	-
36	P8_6	I/O	-
37	P8_5	I/O	TRFO12
38	P8_4	I/O	TRFO11
39	P8_3	I/O	TRFO10/TRFI
40	P8_2	I/O	TRFO02
41	P8_1	I/O	TRFO01
42	P8_0	I/O	TRFO00
43	P6_0	I/O	TREO
44	P4_5	I/O	INT0#
45	P6_6	I/O	INT2#/TXD1
46	P6_7	I/O	INT3#/RXD1
47	P6_5	I/O	(CLK1)/CLK2
48	P6_4	I/O	RXD2
49	P6_3	I/O	TXD2
50	P3_1	I/O	TRBO
51	P3_0	I/O	TRAO
52	P3_6	I/O	(INT1#)
53	P3_2	I/O	(INT2#)
54	P1_3	I/O	KI3#/AN11
55	P1_2	I/O	KI2#/AN10
56	P1_1	I/O	KI1#/AN9
57	P1_0	I/O	KI0#/AN8
58	P7_7	I/O	AN19
59	P7_6	I/O	AN18
60	P7_5	I/O	AN17
61	P7_4	I/O	AN16
62	P7_3	I/O	AN15
63	P7_2	I/O	AN14
64	P7_1	I/O	AN13
65	P7_0	I/O	AN12
66	P0_0	I/O	AN7
67	P0_1	I/O	AN6
68	P0_2	I/O	AN5
69	P0_3	I/O	AN4
70	P0_4	I/O	AN3
71	P6_2	I/O	-
72	P6_1	I/O	-
73	P0_5	I/O	CLK1/AN2
74	P0_6	I/O	AN1/DA0
75	VSS	Power	AVSS
76	P0_7	I/O	AN0/DA1
77	VREF	Input	-
78	VCC	Power	AVCC
79	P3_7	I/O	SSO
80	P3_5	I/O	SSCK/SCL

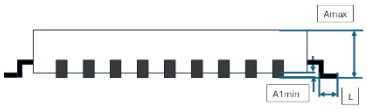
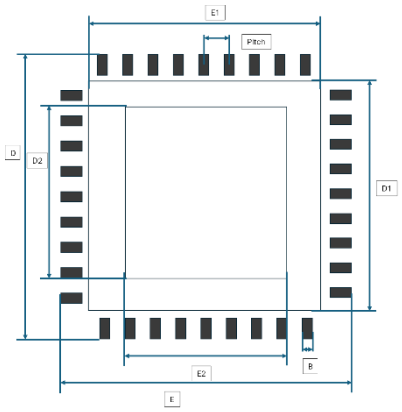
A.3 Symbol Parameters

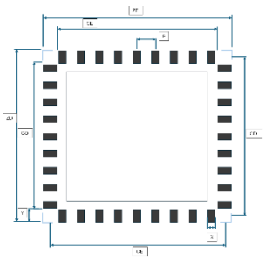
Orderable Part Number	Min Input Voltage	Max Input Voltage	Max Output Frequency	Min Operating Temperature	Max Operating Temperature	RAM Size	Memory Size	Interface	Number of ADC Channels	Number of I2C Channels	Number of SPI Channels	Number of UART Channels	Number of Timers/Counters
R5F212C7SDFP#V2	2.2 V	5.5 V	20 MHz	-40 °C	+85 °C	2.5 KB	48 KB	UART,I2C,LIN	10 bit x 20-Ch	2	0	3	8-bit X 3-Ch, 16-bit X 4-Ch
R5F212C7SNFP#V2	2.2 V	5.5 V	20 MHz	-20 °C	+85 °C	2.5 KB	48 KB	UART,I2C,LIN	10 bit x 20-Ch	2	0	3	8-bit X 3-Ch, 16-bit X 4-Ch
R5F212C8SNFP#V2	2.2 V	5.5 V	20 MHz	-20 °C	+85 °C	3 KB	64 KB	UART,I2C,LIN	10 bit x 20-Ch	2	0	3	8-bit X 3-Ch, 16-bit X 4-Ch
R5F212CASNFP#V2	2.2 V	5.5 V	20 MHz	-20 °C	+85 °C	7 KB	96 KB	UART,I2C,LIN	10 bit x 20-Ch	2	0	3	8-bit X 3-Ch, 16-bit X 4-Ch
R5F212CCSDFP#V2	2.2 V	5.5 V	20 MHz	-40 °C	+85 °C	7.5 KB	128 KB	UART,I2C,LIN	10 bit x 20-Ch	2	0	3	8-bit X 3-Ch, 16-bit X 4-Ch
R5F212CCSNFP#V2	2.2 V	5.5 V	20 MHz	-20 °C	+85 °C	7.5 KB	128 KB	UART,I2C,LIN	10 bit x 20-Ch	2	0	3	8-bit X 3-Ch, 16-bit X 4-Ch
R5F212D7SNFP#V2	2.2 V	5.5 V	20 MHz	-20 °C	+85 °C	2.5 KB	48 KB	UART,I2C,LIN	10-bit X 20-Ch	2	0	3	8-bit X 3-Ch, 16-bit X 4-Ch
R5F212D8SDFP#V2	2.2 V	5.5 V	20 MHz	-40 °C	+85 °C	3 KB	64 KB	UART,I2C,LIN	10-bit X 20-Ch	2	0	3	8-bit X 3-Ch, 16-bit X 4-Ch
R5F212D8SNFP#V2	2.2 V	5.5 V	20 MHz	-20 °C	+85 °C	3 KB	64 KB	UART,I2C,LIN	10-bit X 20-Ch	2	0	3	8-bit X 3-Ch, 16-bit X 4-Ch
R5F212DASDFP#V2	2.2 V	5.5 V	20 MHz	-40 °C	+85 °C	7 KB	96 KB	UART,I2C,LIN	10-bit X 20-Ch	2	0	3	8-bit X 3-Ch, 16-bit X 4-Ch
R5F212DASNFP#V2	2.2 V	5.5 V	20 MHz	-20 °C	+85 °C	7 KB	96 KB	UART,I2C,LIN	10-bit X 20-Ch	2	0	3	8-bit X 3-Ch, 16-bit X 4-Ch
R5F212DCSNFP#V2	2.2 V	5.5 V	20 MHz	-20 °C	+85 °C	7.5 KB	128 KB	UART,I2C,LIN	10-bit X 20-Ch	2	0	3	8-bit X 3-Ch, 16-bit X 4-Ch

A.4 Footprint Design Information

A.4.1 80-LFQFP

IPC Footprint Type	Package Code/ POD number	Number of Pins
QFP	PLQP0080KB-A	80

Description	Dimension	Value (mm)	Diagram
Minimum lead span (vertical side)	Dmin	14.2	
Maximum lead span (vertical side)	Dmax	14.2	
Minimum lead span (horizontal side)	Emin	14.2	
Maximum lead span (horizontal side)	Emax	14.2	
Minimum body span (vertical side)	D1min	12.1	
Maximum body span (vertical side)	D1max	12.1	
Minimum body span (horizontal side)	E1min	12.1	
Maximum body span (horizontal side)	E1max	12.1	
Minimum Lead Width	Bmin	0.15	
Maximum Lead Width	Bmax	0.25	
Minimum Lead Length	Lmin	0.3	
Maximum Lead Length	Lmax	0.7	
Maximum Height	Amax	1.7	
Minimum Standoff Height	A1min	0	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.2	
Number of pins (vertical side)	PinCountD	20	
Number of pins (horizontal side)	PinCountE	20	
Distance between the center of any two adjacent pins	Pitch	0.5	
Location of pin 1; S2 = corner of D side, C1 = center of E side	Pin1	S2	
Minimum thermal pad size (vertical side)	D2min	-	
Maximum thermal pad size (vertical side)	D2max	-	
Minimum thermal pad size (horizontal side)	E2min	-	
Maximum thermal pad size (horizontal side)	E2max	-	

Recommended Land Pattern (NSMD Design)			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	-	
Distance between top pad toe to bottom pad toe (vertical side)	ZD	-	
Distance between left pad heel to right pad heel (horizontal side)	GE	-	
Distance between top pad heel to bottom pad heel (vertical side)	GD	-	
Pad Width	X	-	
Pad Length	Y	-	