A. ECAD Design Information

This appendix contains information that supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
R5F21368ZJFP	64	LFQFP	PLQP0064KB-A
R5F21368ZKFP	64	LFQFP	PLQP0064KB-A
R5F2136AZJFP	64	LFQFP	PLQP0064KB-A
R5F2136AZKFP	64	LFQFP	PLQP0064KB-A
R5F2136CZJFP	64	LFQFP	PLQP0064KB-A
R5F2136CZKFP	64	LFQFP	PLQP0064KB-A

A.2 Symbol Pin Information

A.2.1 64-LFQFP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	P3_0	I/O	(TRAO0) /TRGCLKA
2	P4_2	Input	VREF
3	MODE	Input	-
4	P4_3	I/O	-
5	P4_4	I/O	-
6	\RESET	Input	-
7	XOUT	I/O	P4_7
8	VSS	Power	AVSS
9	XIN	Input	P4_6
10	VCC	Power	AVCC
11	P5_4	I/O	TRCIOD
12	P5_3	I/O	TRCIOC
13	P5_2	I/O	TRCIOB
14	P5_1	I/O	TRCIOA/TRCTRG
15	P5_0	I/O	TRCCLK
16	P3_7	I/O	TRAO0/(TXD2)/(SDA2)/(RXD2)/(SCL2) /SSO
17	P3_5	I/O	(CLK2) /SSCK
18	P3_4	I/O	(TXD2)/(SDA2)/(RXD2)/(SCL2) /(SCS#) /SSI
19	P3_3	I/O	INT3#/CTS2#/RTS2#/SCS#/(SSI)
20	P2_7	I/O	TRDIOD1
21	P2_6	I/O	TRDIOC1
22	P2_5	I/O	TRDIOB1
23	P2_4	I/O	TRDIOA1
24	P2_3	I/O	TRDIOD0
25	P2_2	I/O	TRDIOC0
26	P2_1	I/O	TRDIOB0
27	P2_0	I/O	TRDIOA0/TRDCLK
28	P3_6	I/O	(INT1#)
29	P3_1	I/O	(TRBO)
30	P8_6	I/O	-
31	P8_5	I/O	TRFO12
32	P8_4	I/O	TRFO11
33	P8_3	I/O	TRFO10/TRFI
34	P8_2	I/O	TRFO02
35	P8_1	I/O	TRFO01
36	P8_0	I/O	TRFO00
37	P6_7	I/O	(INT3#)/(RXD2)/(SCL2)
38	P6_6	I/O	INT2#/(TXD2)/(SDA2)
39	P6_5	I/O	INT4#/(CLK2) /(CLK1)

40	P4_5	I/O	INT0#/ADTRG
41	P1_7	I/O	INT1#/(TRAIO0) /ANEX3
42	P1_6	I/O	CLK0/ANEX2
43	P1_5	I/O	(INT1#)/(TRAIO0) (1)/RXD0/ANEX1
44	P1_4	I/O	TXD0/ANEX0
45	P1_3	I/O	KI3#/TRBO/AN11
46	P1_2	I/O	KI2#/AN10
47	P1_1	I/O	KI1#/AN9
48	P1_0	I/O	KI0#/AN8
49	P0_7	I/O	AN0
50	P0_6	I/O	AN1
51	P0_5	I/O	AN2
52	P0_4	I/O	TREO/AN3
53	P0_3	I/O	(CLK1) /AN4
54	P0_2	I/O	(RXD1) /AN5
55	P0_1	I/O	(TXD1) /AN6
56	P0_0	I/O	AN7
57	P6_4	I/O	(INT2#) /TRAIO1/(RXD1)
58	P6_3	I/O	(TRAO1) /(TXD1)
59	P6_2	I/O	-
60	P6_1	I/O	-
61	P6_0	I/O	(TREO)
62	P5_7	I/O	TRGIOB
63	P5_6	I/O	TRGIOA
64	P3_2	I/O	(INT1#)/(INT2#) /TRGCLKB

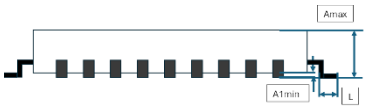
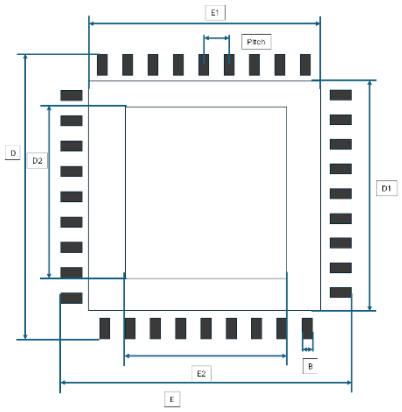
A.3 Symbol Parameters

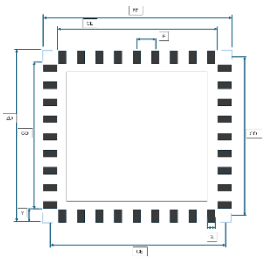
Orderable Part Number	Min Input Voltage	Max Input Voltage	Max Output Frequency	Min Operating Temperature	Max Operating Temperature	RAM Size	Memory Size	Interface	Number of ADC Channels	Number of I2C Channels	Number of SPI Channels	Number of UART Channels	Number of Timers/Counters
R5F21368ZJFP	2.7 V	5.5 V	20 MHz	-40 °C	+85 °C	6 KB	64 KB	UART, LIN, I2C, SSU	10-bit X 16-Ch	1	0	3	8-bit X 4-Ch, 16-bit X 5-Ch
R5F21368ZKFP	2.7 V	5.5 V	20 MHz	-80 °C	+125 °C	6 KB	64 KB	UART, LIN, I2C, SSU	10-bit X 16-Ch	1	0	3	8-bit X 4-Ch, 16-bit X 5-Ch
R5F2136AZJFP	2.7 V	5.5 V	20 MHz	-40 °C	+85 °C	8 KB	96 KB	UART, LIN, I2C, SSU	10-bit X 16-Ch	1	0	3	8-bit X 4-Ch, 16-bit X 5-Ch
R5F2136AZKFP	2.7 V	5.5 V	20 MHz	-80 °C	+125 °C	8 KB	96 KB	UART, LIN, I2C, SSU	10-bit X 16-Ch	1	0	3	8-bit X 4-Ch, 16-bit X 5-Ch
R5F2136CZJFP	2.7 V	5.5 V	20 MHz	-40 °C	+85 °C	10 KB	128 KB	UART, LIN, I2C, SSU	10-bit X 16-Ch	1	0	3	8-bit X 4-Ch, 16-bit X 5-Ch
R5F2136CZKFP	2.7 V	5.5 V	20 MHz	-80 °C	+125 °C	10 KB	128 KB	UART, LIN, I2C, SSU	10-bit X 16-Ch	1	0	3	8-bit X 4-Ch, 16-bit X 5-Ch

A.4 Footprint Design Information

A.4.1 64-LQFP

IPC Footprint Type	Package Code/ POD number	Number of Pins
QFP	PLQP0064KB-A	64

Description	Dimension	Value (mm)	Diagram
Minimum lead span (vertical side)	Dmin	12.2	
Maximum lead span (vertical side)	Dmax	12.2	
Minimum lead span (horizontal side)	Emin	12.2	
Maximum lead span (horizontal side)	Emax	12.2	
Minimum body span (vertical side)	D1min	10.1	
Maximum body span (vertical side)	D1max	10.1	
Minimum body span (horizontal side)	E1min	10.1	
Maximum body span (horizontal side)	E1max	10.1	
Minimum Lead Width	Bmin	0.15	
Maximum Lead Width	Bmax	0.25	
Minimum Lead Length	Lmin	0.35	
Maximum Lead Length	Lmax	0.65	
Maximum Height	Amax	1.7	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.2	
Number of pins (vertical side)	PinCountD	16	
Number of pins (horizontal side)	PinCountE	16	
Distance between the center of any two adjacent pins	Pitch	0.5	
Location of pin 1; S2 = corner of D side, C1 = center of E side	Pin1	S2	
Minimum thermal pad size (vertical side)	D2min	-	
Maximum thermal pad size (vertical side)	D2max	-	
Minimum thermal pad size (horizontal side)	E2min	-	
Maximum thermal pad size (horizontal side)	E2max	-	

Recommended Land Pattern (NSMD Design)			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe (horizontal side)	ZE	-	
Distance between top pad toe to bottom pad toe (vertical side)	ZD	-	
Distance between left pad heel to right pad heel (horizontal side)	GE	-	
Distance between top pad heel to bottom pad heel (vertical side)	GD	-	
Pad Width	X	-	
Pad Length	Y	-	