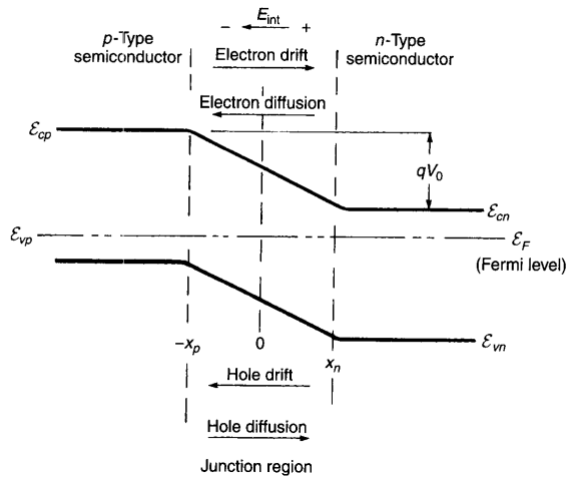
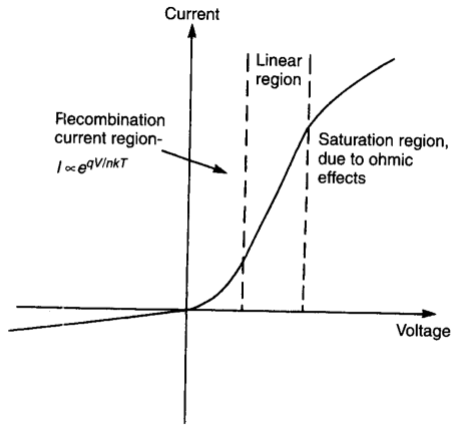
Diodes for Microwave Control Circuits

- The efficient control of electrical signals in RF circuits requires the use of nonlinear devices.
- These devices can be either active or passive.
- In hybrid circuit applications active devices (transistors or FETs) are generally used for signal generation and amplification, whereas passive devices (diodes) are often used for signal detection, frequency shifting (mixing), and control.
- Active devices are often used in place of passive devices in monolithic IC applications where, due to the fabrication process, it is not difficult to obtain large number of well-matched devices.



[Energy band diagram of pn-junction diode]



$$I = I_0(e^{qV/kT} - 1)$$

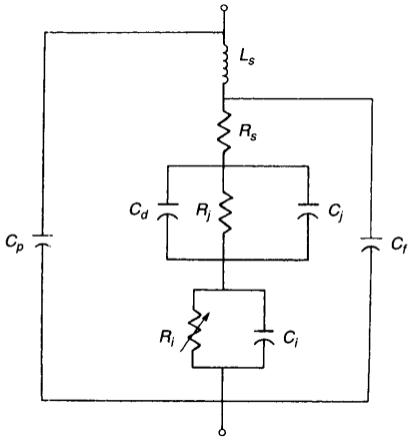
[The I-V characteristic for pn-junction showing regions of deviation from the ideal]

pin Diodes

- A *pin* diode is a *pn*-junction device that has very minimally doped or intrinsic region located between the p- and n-type contact regions.
- In reverse bias the *i*-region results in very high values for the diode breakdown voltage, whereas the device capacitance is reduced by the increased separation between the *p* and *n* regions. Therefore, the diode is very useful for high-frequency, high-power rectifier applications.
- In forward bias the conductivity of the intrinsic region is controlled or modulated by the injection of charge from the end regions. The diode is a bias-current-controlled resistor with excellent linearity and low insertion.
- The *pin* diodes are used extensively in microwave circuits for amplitude modulation, attenuation, and leveling functions. They also make excellent RF switches, phase shifters, and limiters.

The diode basically consists of two main elements in series: a diode with diffusion capacitance C_d and junction parameters R_j and C_j all in parallel and the parallel combination of the undepleted *i*-region resistance and capacitance.

$$C_d = \frac{q\tau}{kT} I_{\text{dc}} \qquad R_j = \frac{nkTA}{qI_0} \qquad C_j = A\left[\frac{q\epsilon N_d}{2(V_0 - V)}\right]^{1/2}$$

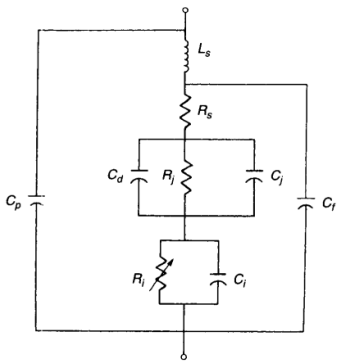


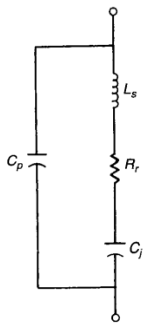
[Equivalent circuit for *pin*-diode]

$$R_i \cong \frac{3(kT)W^2}{8qI_0L_a^2} \qquad C_i = \frac{\epsilon A}{W}$$

L_s: Lead inductance
C_f : fringing capacitance from the top contact of the diode to the mounting structure
C_p: package and/or mounting structure capacitance
R_s: resistance of the bulk semiconductor region plus the resistance of the contacts
τ: Minority-carrier lifetime in the depletion region
W: i-layer thickness (typically 10 – 100 μm)
I_0: bias current
A: cross-sectional area of the device
L_a:diffusion length

Reverse bias condition:

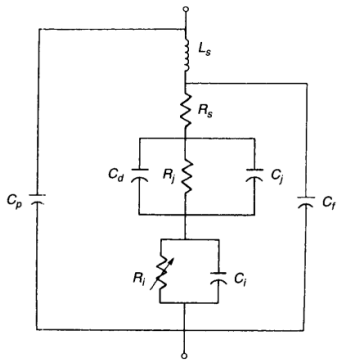


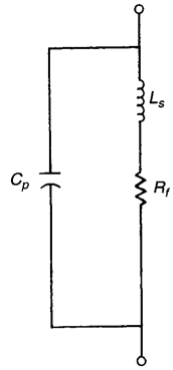


[(a) *pin*-diode under reverse bias]

The equivalent circuit shown in Fig. is modified under certain bias and high-frequency operating conditions. For example, under reverse bias the diffusion capacitance C_d vanishes and the junction resistance R_j becomes very large. Only C_j remains significant in the junction network. If the reverse bias is sufficient to completely deplete the *i* region, the R_i–C_i network will vanish. The equivalent circuit reduces to that shown in Fig. .a, where R_r is the total series resistance for the reverse-bias state.

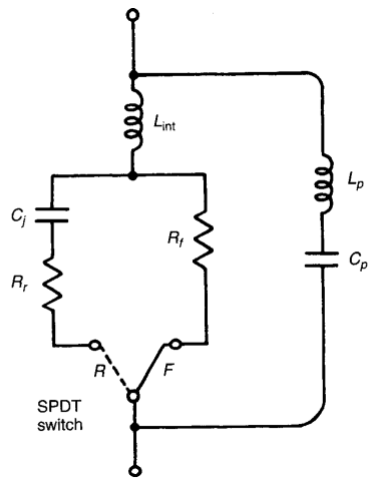
Forward bias condition:





[(b) *pin*-diode under forward bias]

Under forward-bias and high-frequency operation the diffusion capacitance C_d will be large and will short out the junction parameters. The i region will be injected with charge carriers so that the R_i–C_i network is represented by R_i only. The equivalent circuit reduces to that shown in Fig. b, where R_f is the total series resistance for the forward-bias state.



[Equivalent circuit of a packaged *pin*-diode]

- In forward bias, the single-pole double-throw (SPDT) switch is in position F, and in the reverse bias it is put in position R.
- Inductance Lp and capacitance Cp are contributed by the package.

Table Equivalent-Circuit Parameters for Two Commercially Available *pin* Diodes

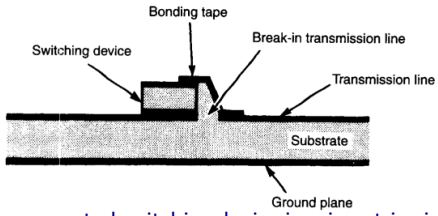
Parameters	MA47892-109	MA47899-030
C_j	1 pF	0.1 pF
R_f	0.4 Ω	1 Ω
R_r	0.5 Ω	4 Ω
L_{int}	0.3 nH	0.3 nH
C_p	0.08 pF	0.18 pF
τ	5 μs	0.5 μs
f_{cs} $[=1/(2\pi C_j\sqrt{R_r R_f})]$	350 GHz	800 GHz

Design of Switches

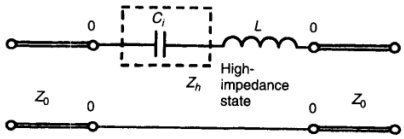
There are two basic configurations that may be used for a simple single-pole single-throw (SPST) switch designed to control the flow of microwave signals along a transmission line.

Series Mounted Switching Device

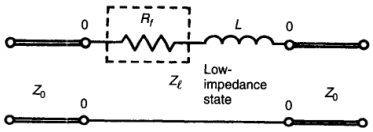
The switching device (SD) is mounted in series with one of the conductors of the transmission line (strip conductor of the microstrip line)



[Series-mounted switching device in microstrip circuit]



[Simplified eq. circuit for high impedance state]

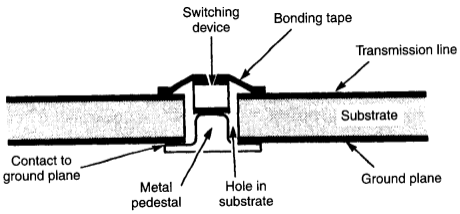


[Simplified eq. circuit for low impedance state]

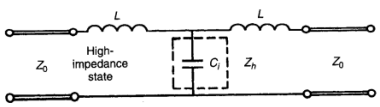
L: inductance of bonding ribbons

Shunt Mounted Switching Device

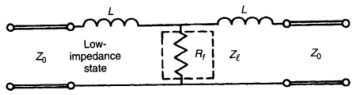
The switching device (SD) is mounted in shunt across the two conductors of the transmission line.



[Shunt-mounted switching device in microstrip circuit]



[Simplified eq. circuit for high impedance state]

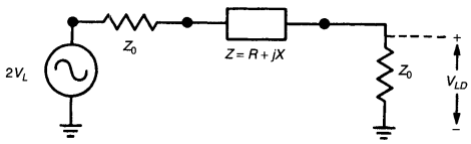


[Simplified eq. circuit for low impedance state]

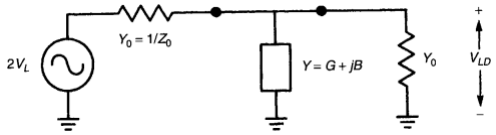
Insertion Loss and Isolation:

Because of a finite nonzero impedance of switching devices in the low-impedance state and a definite noninfinite impedance in the high-impedance state, the switching circuits are not perfect. The performance of a practical switch can be expressed by specifying its insertion loss and isolation.

Insertion loss is defined as the ratio of the power delivered to the load in the ON state of the ideal switch to the actual power delivered by the practical switch (in the ON state). It is usually expressed in decibels.



[Equivalent circuit of the series-mounted SPST switch]
Z: Impedance of the SD

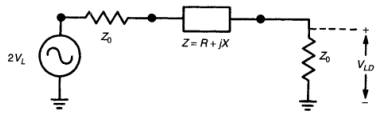


[Equivalent circuit of the shunt-mounted SPST switch]
Y: Admittance of the SD

If V_L denotes the actual voltage across the load in the ideal switch, the insertion loss (*IL*) may be written as:

$$\mathrm{IL} = \left|\frac{V_L}{V_{LD}}\right|^2$$

V_{LD}: voltage across the load in the practical switch.



For the series configuration, simple circuit analysis yields:

$$V_{LD} = \frac{2V_L}{2 + Z/Z_0}$$

$Z(R + jX)$: impedance of the switching device

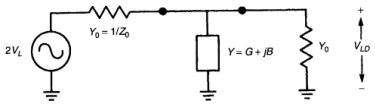
The insertion loss is given by:

$$\mathrm{IL} = \left|\frac{2 + Z/Z_0}{2}\right|^2$$

$$= 1 + \frac{R}{Z_0} + \frac{1}{4}\left(\frac{R}{Z_0}\right)^2 + \frac{1}{4}\left(\frac{X}{Z_0}\right)^2 \qquad \text{Eqn. [1]}$$

R and X are the resistance and the reactance of the switching device in the low-impedance state.

For the shunt configuration, the voltage across the load may be written as:



$$V_{LD} = \frac{2V_L Y_0}{2Y_0 + Y}$$

and the insertion loss becomes

$$\text{IL} = \left|\frac{2Y_0 + Y}{2Y_0}\right|^2 = \left|1 + \frac{G + jB}{2Y_0}\right|^2$$
$$= 1 + \frac{G}{Y_0} + \frac{1}{4}\left(\frac{G}{Y_0}\right)^2 + \frac{1}{4}\left(\frac{B}{Y_0}\right)^2$$

Eqn. [2]

$Y_0 = 1/Z_0$ and G and B are the real and imaginary parts of the admittance Y of the switching device in the high-impedance state.

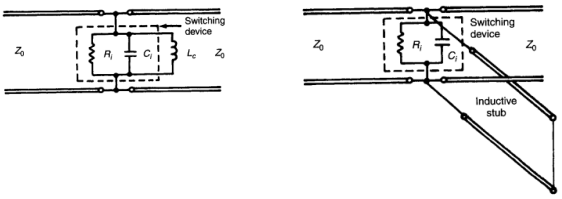
- Isolation is a measure of the performance of the switch when it is in the OFF state.
- Isolation is defined as the ratio of the power delivered to the load for an ideal switch in the ON state to the actual power delivered to the load when the switch is in the OFF state.
- For the series configuration, the OFF state exists when the device is in the high-impedance state. The isolation, in this case, is also given by eqn. [1] with R and X replaced by the corresponding values in the high-impedance state.
- Similarly, the isolation for the shunt configuration is given by eqn.[2] when we use the low-impedance-state values for G and B.

Compensation of Device Reactances:

$$IL = \left|\frac{2 + Z/Z_0}{2}\right|^2 = 1 + \frac{R}{Z_0} + \frac{1}{4}\left(\frac{R}{Z_0}\right)^2 + \frac{1}{4}\left(\frac{X}{Z_0}\right)^2$$ Eqn. [1]

$$IL = \left|\frac{2Y_0 + Y}{2Y_0}\right|^2 = \left|1 + \frac{G + jB}{2Y_0}\right|^2 = 1 + \frac{G}{Y_0} + \frac{1}{4}\left(\frac{G}{Y_0}\right)^2 + \frac{1}{4}\left(\frac{B}{Y_0}\right)^2$$ Eqn. [2]

An examination of the above equations for *IL* and isolation of series and shunt switches, indicated that the performance of switching circuits is limited by the device reactance X or the susceptance B. Compensation of device reactances, therefore, provides a mechanism for improving the switch performance.



[*a*] [*b*]

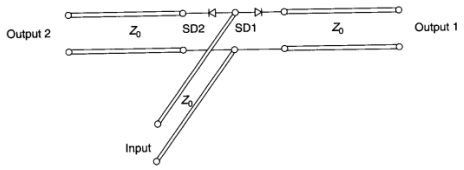
[Compensation of capacitance of switching device in high impedance state by using a (a) lumped inductance and (b) an inductive stub

$$IL = 1 + \frac{G}{Y_0} + \frac{1}{4}\left(\frac{G}{Y_0}\right)^2$$

Single-Pole Double-Throw (SPDT) Switches

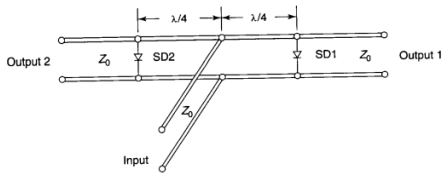
SPDT switches require a minimum of two switching devices.

SPDT Switch using series-mounted devices



In the series configuration, the input signal is routed to output 1 when the switching device SD1 is in the low-impedance state and device SD2 is in the high-impedance state.

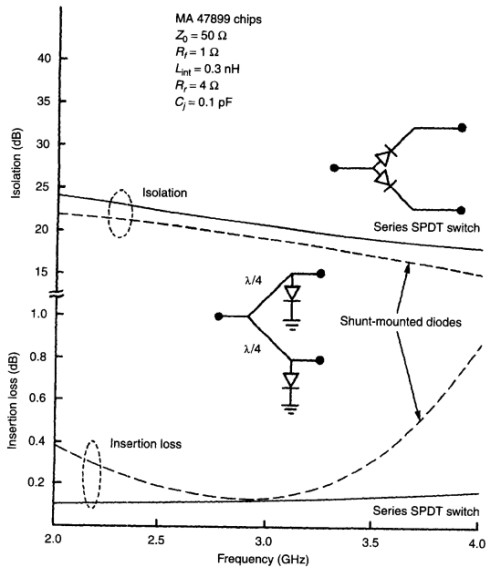
SPDT Switch using shunt-mounted devices



In the shunt configuration, the input signal is routed to output 1 when device SD1 is in the high-impedance state and device SD2 is in the low-impedance state.

Thus, in either configuration, at any time, one of the devices is in the low-impedance state while the other one is in the high-impedance state.

The bandwidth of the SPDT in shunt configuration is limited because of the $\lambda/4$ line lengths required between the transmission-line junction and the locations of the two switching devices.



The design concept of SPDT switches may also be extended to single-pole multiple-throw switches.

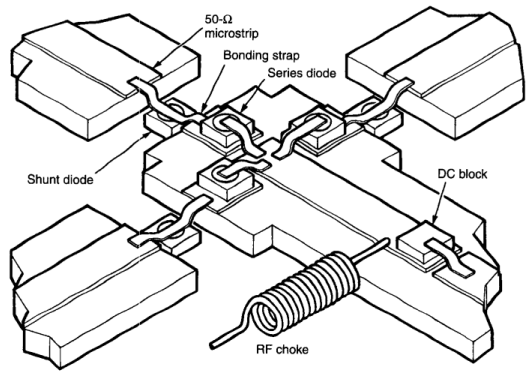
An SP3T switch will use a minimum of three switching devices.

Microstrip construction of a typical SP3T switch is shown.

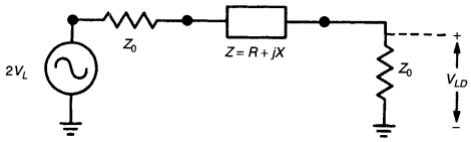
In this configuration there are six devices, two associated with each of the output ports.

Using a combination of series- and shunt-mounted diodes improves the switch's performance

The DC blocking capacitors and RF chokes are needed for DC biasing.

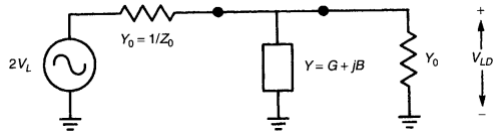


Series-Shunt Switching Configurations



[Equivalent circuit of the series-mounted SPST switch]
Z: Impedance of the SD

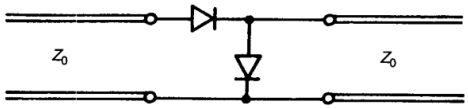
$$IL = \left|\frac{2 + Z/Z_0}{2}\right|^2$$
$$= 1 + \frac{R}{Z_0} + \frac{1}{4}\left(\frac{R}{Z_0}\right)^2 + \frac{1}{4}\left(\frac{X}{Z_0}\right)^2 \quad \text{Eqn. [1]}$$

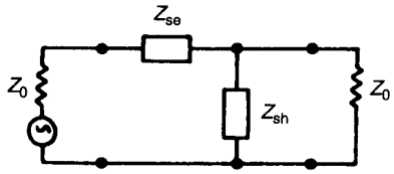


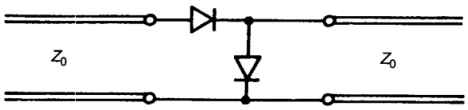
[Equivalent circuit of the shunt-mounted SPST switch]
Y: Admittance of the SD

$$IL = \left|\frac{2Y_0 + Y}{2Y_0}\right|^2 = \left|1 + \frac{G + jB}{2Y_0}\right|^2$$
$$= 1 + \frac{G}{Y_0} + \frac{1}{4}\left(\frac{G}{Y_0}\right)^2 + \frac{1}{4}\left(\frac{B}{Y_0}\right)^2 \quad \text{Eqn. [2]}$$

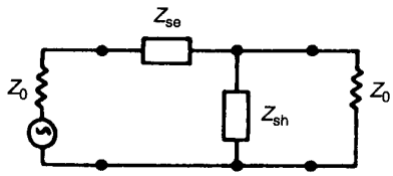
One could realize a better switching performance when both series- and shunt- mounted devices are included in a single circuit.







[Simplest series-shunt switching configuration]

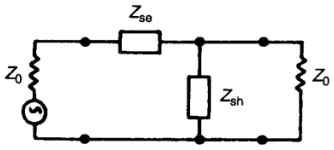


[Eq. ckt. for the series-shunt configuration]

This switch is ON when the series device is in the low-impedance state and the shunt device is in the high-impedance state.

In the OFF state of the switch, the series device is in the high-impedance state and the shunt device is in the low-impedance state.

This switching circuit may be analyzed in terms of the equivalent circuit, as shown.



Z_{se}: impedance of the series-mounted device
Z_{sh}: impedance of the shunt-mounted device

For the ON state, the device impedance Z_{se} is denoted by the low-impedance Z_l, and the device impedance Z_{sh} is denoted by the high-impedance Z_h.

From circuit analysis, the insertion loss may be written as:

$$\text{IL} = \left|\frac{1}{2} + \frac{(Z_0 + Z_h)(Z_0 + Z_l)}{2Z_0 Z_h}\right|^2 \qquad \text{Eqn. [3]}$$

Similarly,

$$\text{Isolation} = \left|\frac{1}{2} + \frac{(Z_0 + Z_l)(Z_0 + Z_h)}{2Z_0 Z_l}\right|^2$$

Eqn.[1] and eqn.[2] for series and shunt switches may be obtained as limiting cases of eqn.[3] for Z_{sh} (= Z_h)$\rightarrow\infty$ and for Z_{se} (= Z_l)$\rightarrow$0, respectively.

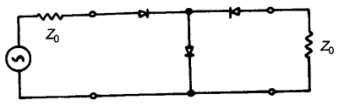
Comparison of Three Switching Configurations
(with MA-47899 Chip *pin* Diodes at 6.37 GHz)

Configuration	Insertion Loss (dB)	Isolation (dB)
Series–shunt (2 devices)	0.108	20.17
Series switch (2 device)	0.147	8.29
Shunt switch (1 device)	0.063	7.52

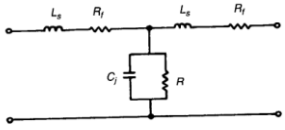
- Isolation obtained with a series-shunt configuration is much better (more than twice in decibels) than that for either the series or shunt switch.
- The insertion loss for the series-shunt configuration is worse than that for a shunt switch but better than that for a series switch.

Wide-band Series-Shunt Switch Configuration

- Use of multiple switching devices in a series-shunt configuration can lead to ultra-wide-band switches.
- The basic concept involves the use of a ladder network structure that behaves like a low-pass filter when series devices are in the low-impedance state (inductive) and shunt devices are in the high-impedance state (capacitive).
- When the bias levels on the series- and shunt-switching devices are interchanged, the network behaves as a high-pass filter providing a high insertion loss below the cutoff frequency.
- If this cutoff frequency of the high-pass filter configuration is arranged to lie slightly above the cutoff frequency of the low-pass configuration, the network behaves as a switch with the bandwidth of the low-pass filter configuration.

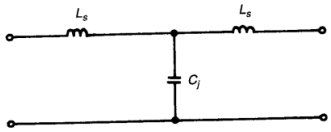


[Series-shunt switch using three switching devices]



[Eq. ckt. with series devices in low-impedance state and shunt device in high-impedance state (ON state for switch]

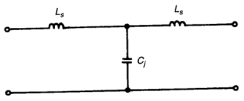
- Let us consider a three-device T-structure switch as shown.
- In the ON state of the switch, the series devices are in the low-impedance state and shunt devices are in the high-impedance state.
- Wire-bonded devices exhibit a series inductance in the low-impedance state leading to an eq. circuit of the switch as shown.



[Simplified eq. circuit (ignoring resistances) for ON state]

- If the effect of device resistances is ignored, the circuit reduces to the LPF configuration as shown.

- The cutoff frequency and the impedance level of this LPF configuration are obtained by comparing with a three-element maximally flat low-pass design.
- For a protype filter of this type, we have $L = L_s = 1\ H$ and $C = C_j = 2\ F$ (corresponding to $Z_0 = 1\ \Omega$ and cutoff frequency $\omega_c = 1\ rad/s$)



[Simplified eq. circuit (ignoring resistances) for ON state]

Transforming this prototype to have a cutoff frequency $\omega_c$and an input-output impedance level of $Z_0\ \Omega$, we have

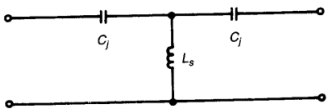
$$L = \frac{Z_0}{\omega_c}\ \text{H} \qquad C = \frac{2}{Z_0\omega_c}\ \text{F}$$

Thus for $L = L_s$ and $C = C_j$, the cutoff frequency ω_c and the impedance level Z_0 are given by

$$\omega_c = \sqrt{\frac{2}{L_s C_j}} \qquad Z_0 = \sqrt{\frac{2L_s}{C_j}}$$

Taking typical values of L_s and C_j to be 0.2 nH and 0.05 pF (typical of chip or beam-lead *pin* diodes), we get a 3-dB cutoff frequency $f_c\ (=\omega_c/2\pi) = 71.18$ GHz and an impedance level $Z_0 = 89.4\ \Omega$.

- When the series devices are in the high-impedance state and the shunt device is in the low-impedance state, the switch is in the OFF state.
- The eq. circuit for this state is shown and corresponds to a high-pass LC filter circuit.
- Low-frequency cutoff and the impedance level of this high-pass filter may be obtained by comparing it with a prototype ($\omega_c = 1\ rad/s$ and $Z_0 = 1\ \Omega$) three-element high-pass filter.
- For a protype filter circuit, $C = C_j = 1\ F$ and $L = L_s = 0.5$ H.
- Transforming the cutoff frequency to $\omega_c$and the impedance level to $Z_0\ \Omega$, we get



[Simplified eq. circuit for OFF state]

$$C = \frac{1}{\omega_c Z_0}\ \text{F} \qquad L = \frac{0.5Z_0}{\omega_c}\ \text{H}$$

In terms of L_s and C_j, we obtain

$$\omega_c = \sqrt{\frac{0.5}{L_s C_j}} \qquad Z_0 = \sqrt{\frac{2L_s}{C_j}}$$

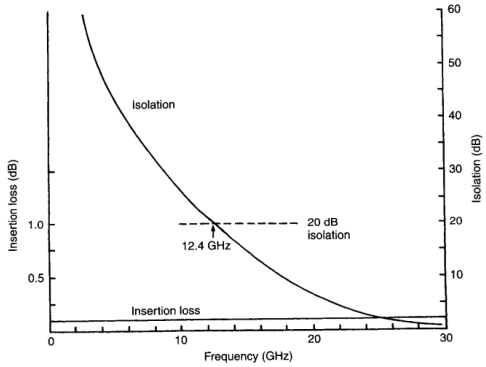
LPF $\omega_c = \sqrt{\frac{2}{L_s C_j}}$ $Z_0 = \sqrt{\frac{2L_s}{C_j}}$

HPF $\omega_c = \sqrt{\frac{0.5}{L_s C_j}}$ $Z_0 = \sqrt{\frac{2L_s}{C_j}}$

Comparing the result with the corresponding results for the ON state, we find that whereas Z_0 has the same value as for the low-pass filter the value of the cutoff frequency for the high-pass filter (OFF state) is only half that of the low-pass filter corresponding value to the ON state.

Considering an example with three identical switching devices (with $L_s = 0.2$ nH, $C_j = 0.1$ pF, and $R_f = 0.5\ \Omega$), the insertion loss and isolation of the series–shunt switch are plotted in Fig. as a function of frequency up to 30 GHz.

We note that the insertion loss is less than 0.1 dB throughout this range, but the performance is limited by the value of isolation, which decreases monotonically. An isolation better than 20 dB is obtained for frequencies up to 12.4 GHz.

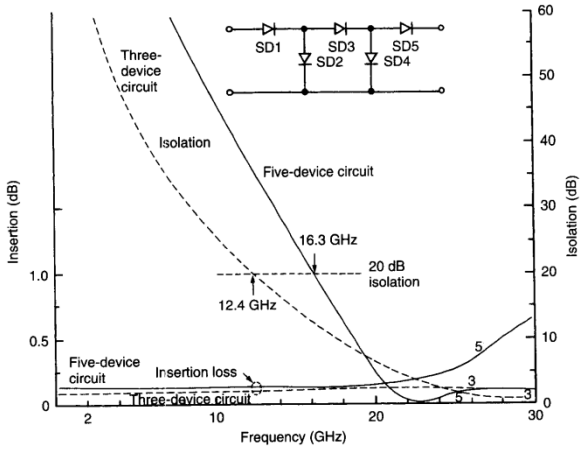


[Insertion loss and isolation performance of three-device series-shunt switch circuit]

Five-Device Series-Shunt Configuration:

When five identical devices similar to that for the three-device switch are used, the insertion loss and isolation obtained are shown in Fig.

It may be noted that the isolation is improved for frequencies below 19 GHz and is better than 20 dB for frequencies up to 16.3 GHz. In this frequency range, the insertion loss is only marginally worse (≃0.1 dB in place of ≃0.08 dB for the three-device case when $R_f = 0.5\ \Omega$).

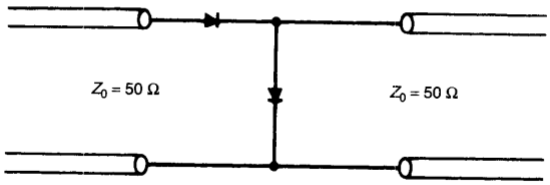


[Insertion loss and isolation performance of five-device series-shunt switching configuration and its comparison with performance of a three-device switch]

Assignments:

[Q1]

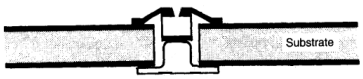
An SPST switch employs two *pin* diodes in the series–shunt configuration shown below. Calculate the insertion loss and isolation at 6 GHz when two *pin* diodes have $C_j = 0.1$ pF, $R_f = 1\ \Omega$, and $L_{\text{int}} = 0.3$ nH. Package capacitances may be ignored.



Compare the results with the switch performance when only one diode is used in (a) series configuration and (b) shunt configuration.

[Q2]

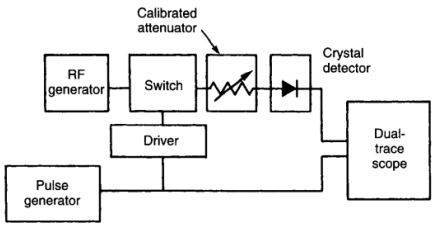
A *pin* diode chip is mounted in shunt across a 50-Ω microstrip line with two bonding tapes as shown in Fig. . The length of the bonding tapes and hence their inductance L can be adjusted. Find the value of the inductances needed to optimize the insertion loss at 6 GHz. In reverse bias the *pin* diode chip may be represented by a capacitance $C_j = 0.1$ pF.

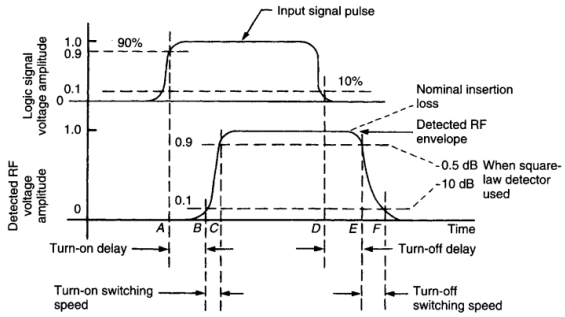


[Q3]

An SP3T switch is designed using *pin* diode chips ($C_j = 0.1$ pF, $R_f = 1\ \Omega$, $R_r = 4\ \Omega$, and $L_{\text{int}} = 0.3$ nH). The center design frequency is 3 GHz. Calculate and plot switch performance over the frequency range 2–4 GHz for (a) series configuration and (b) shunt configuration.

Switching Speed Considerations





- *Turn-on delay* is the time interval between the instants when the input signal reaches 90% of its peak value and when the detected RF envelope reaches 10% of its peak value.
- *Turn-on switching speed* is defined as the time interval between the instants when the envelope of the RF output rises from 10% of its peak value to 90% of its peak value.
- *Turn-off delay* and *turn-off switching* are defined in a similar manner.

Speed Limitations Imposed by Switching Devices

- When *pin* diodes are used for microwave switching, the main factor limiting the switching speed is the time required to remove the charge from the intrinsic region when the diode bias is switched from forward to reverse.
- This charge removal time depends on the width (thickness) of the intrinsic layer. A decrease in the width *W* of the intrinsic layer makes the charge removal faster but at the same time reduces the reverse breakdown voltage and hence the power-handling capability of the pin diode switches.
- Since the power-handling capability is proportional to the square of the breakdown voltage, it is also proportional to the square of width *W*.
- On the other hand, switching time τ is proportional to width *W*.
- So, a trade-off exists between switching time τ and the square root of the power-handling capability *P*.

$$\tau = \frac{\sqrt{P}}{25} \text{ ns}$$

P: power handling capability in Watts.

Switching Speed Limitation Imposed by Biasing Network:

- Considering the DC bias terminal as a separate port, a single-pole single-throw switching circuit may be viewed as a 3-port network.
- A LPF arrangement is needed at the bias port to ensure that the RF signal does not leak away via the bias port.
- HPFs are needed at the RF input and output ports to ensure that the DC bias (or switching pulse) does not interfere with the other parts of the circuit.
- These filters increase the rise time of the switching pulse and thereby reduce the switching speed.
- Rise time τ of a pulse (10 – 90 % levels) passing through a filter is related to the 3-dB bandwidth of the filter, as

$$\tau = \frac{0.44}{\mathrm{BW}}$$

- Thus in order to decrease the rise time, the 3-dB bandwidth of the filters should be as large as possible.
- Since we have LPF and an HPF in the path of the switching pulse, optimum filter characteristics are as shown:
- With this arrangement, the switching time contributed by the filters is given by

$$\tau = \sqrt{\tau_1^2 + \tau_2^2} = \sqrt{2}\tau_F = \frac{1.24}{f_0}$$

where τ_1 and τ_2 are rise times for the two filters (we assume $\tau_1 = \tau_2 = \tau_F$) and f_0 is the operating frequency.