



# **ECN-342: RF and Mixed Signal Circuits**

## **Module#1: Introduction to RFIC, MOSFET Operation & Passive Components**





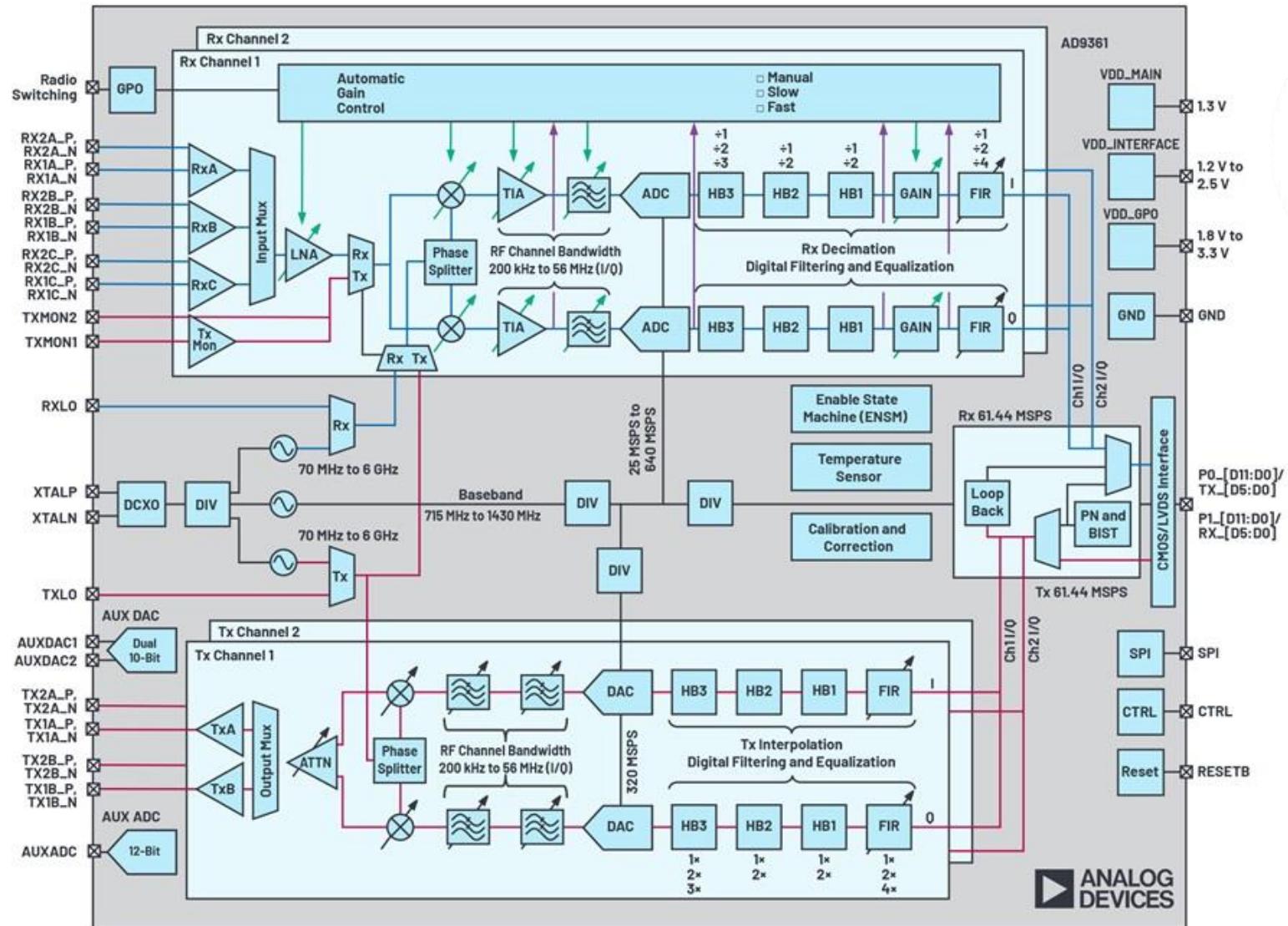
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# Part 1: Introduction to RF Transceivers & Their Requirements

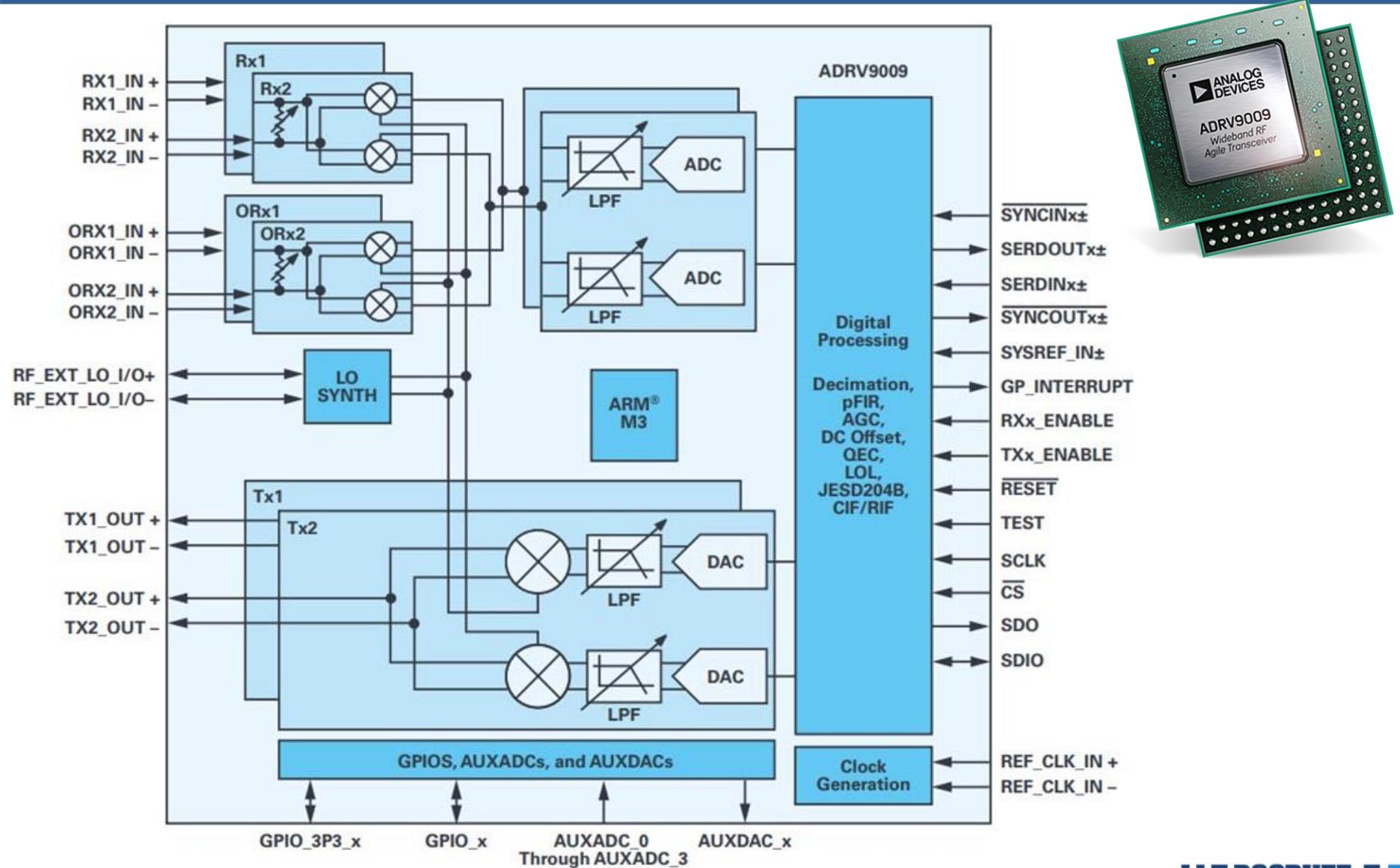
# Introduction to RF Transceiver Architecture (1/2)



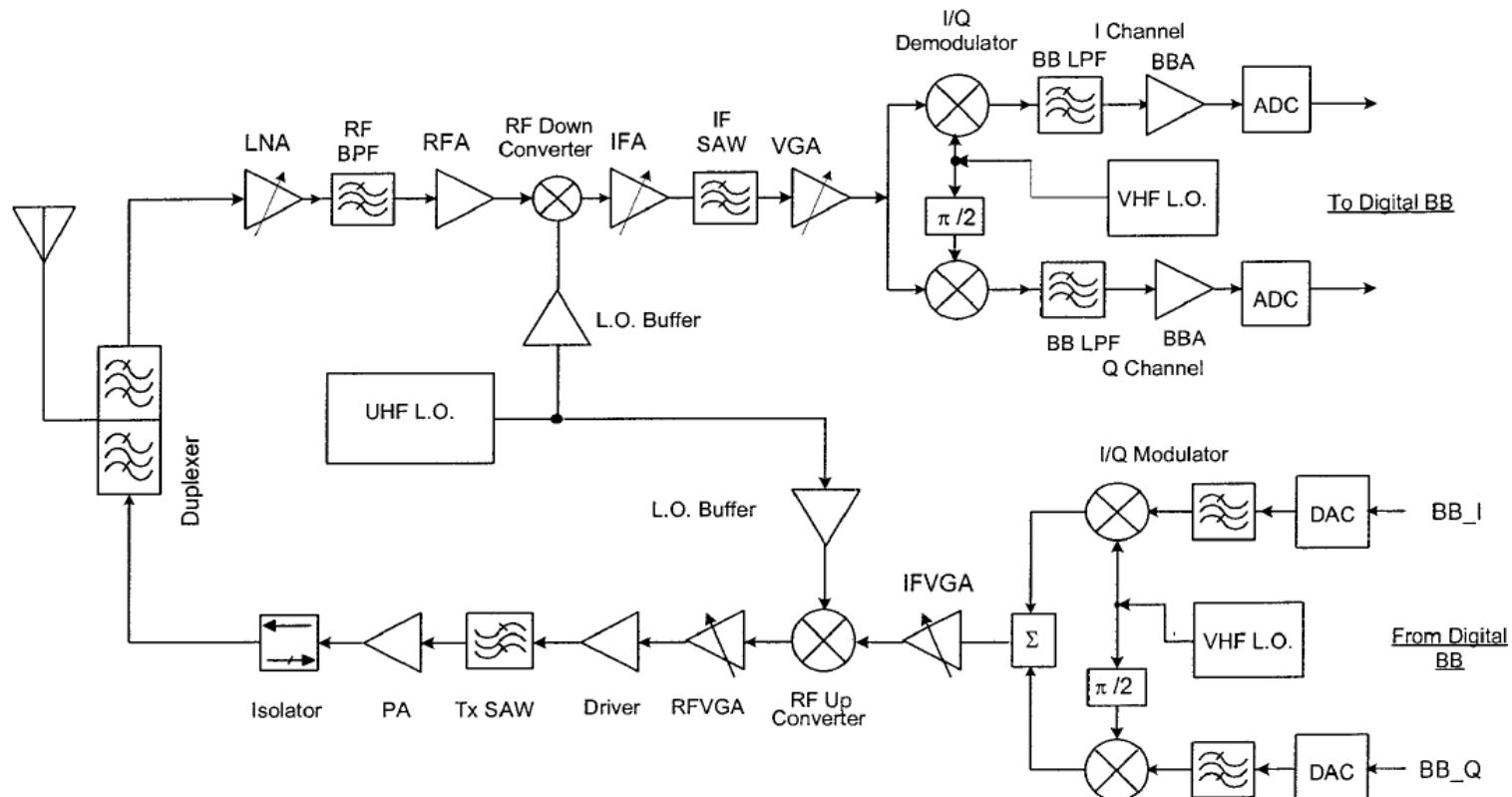
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# Introduction to RF Transceiver Architecture (2/2)



# Superheterodyne Full Duplex Transceiver



**IF:** Intermediate frequency  
**LO:** Local Oscillator  
**RF:** Radio Frequency  
**BB:** Baseband

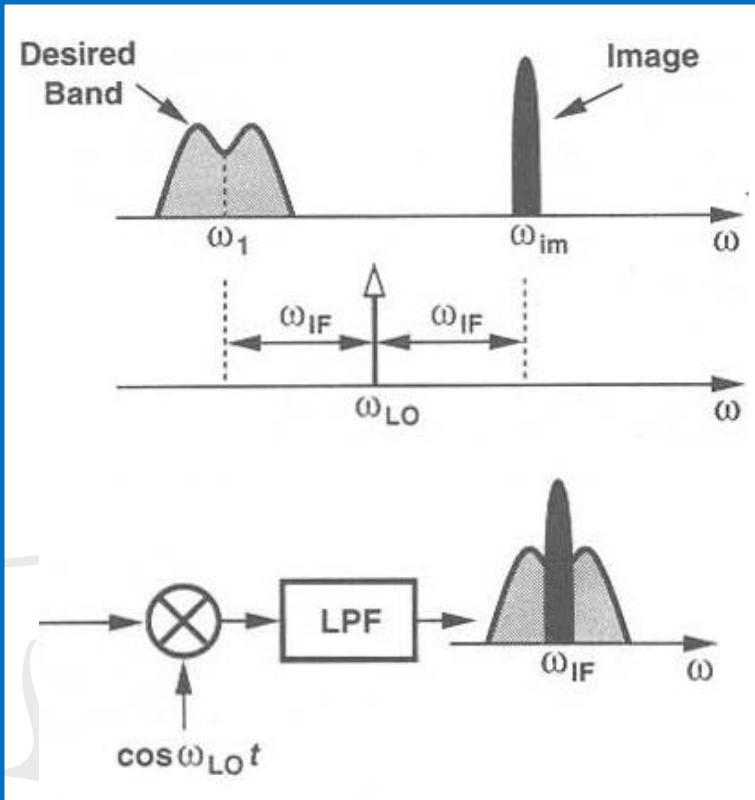
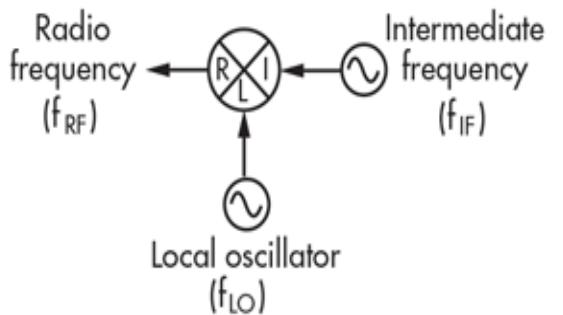
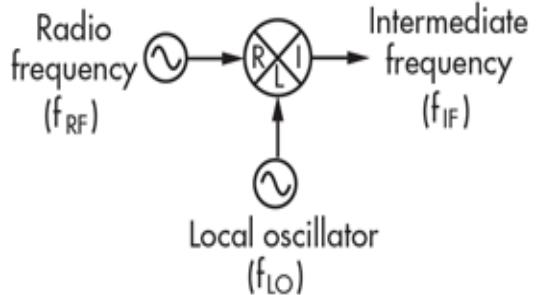
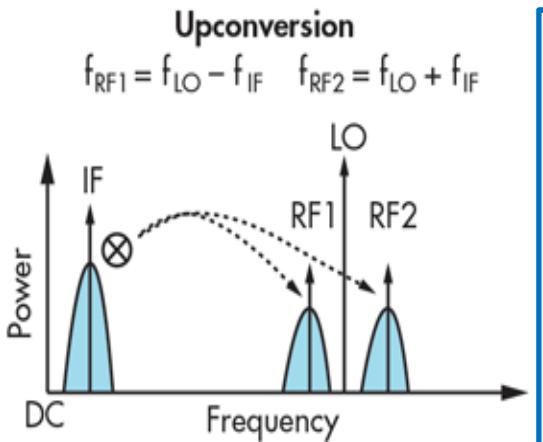
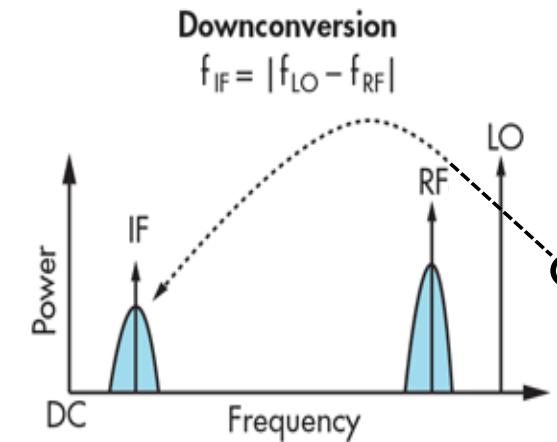
LO is Programmable Synthesizer for reception channel tuning, since IF filter is fixed

The High gain obtained at IF (low power consumption than in RF) & Fixed Channel filters suppress unwanted signals giving a good dynamic range

**Heterodyne process:** Mixing an incoming signal with an offset frequency local oscillator (LO) in a nonlinear device (Mixer) generates an intermediate frequency (IF) signal in the receiver and vice versa in the transmitter.

**Preselection Filter (RF BPF):** Suppress unwanted interferers (image); **Channel Filter: IF Saw**

# Superheterodyne Transceivers: Concept of Image Frequency



Same IF can be generated by an incoming signal with a frequency either above or below the LO. The undesired signal is an image frequency.

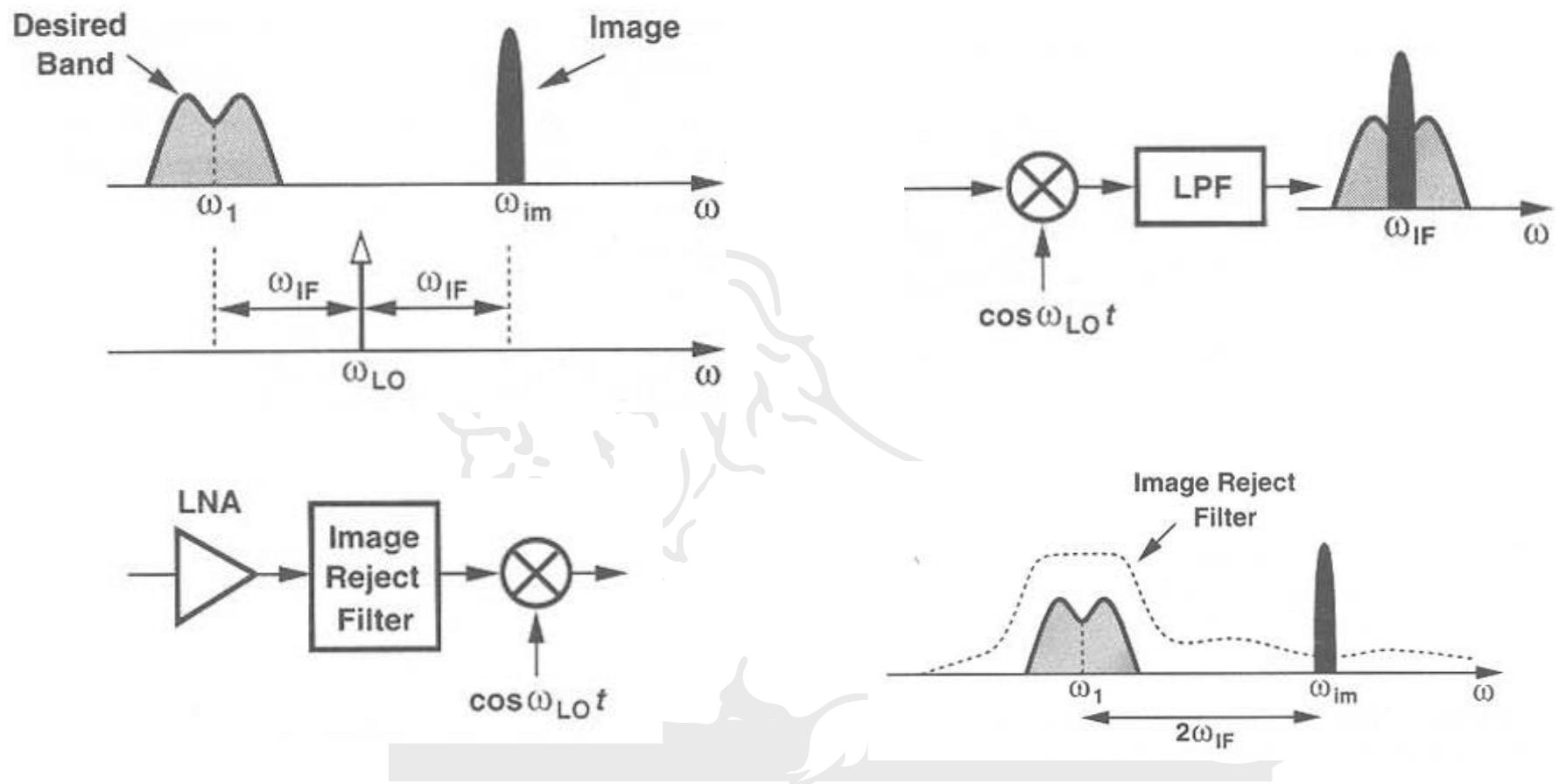
$$2\sin \omega_1 t \sin \omega_2 t = \cos(\omega_1 - \omega_2)t - \cos(\omega_1 + \omega_2)t$$

$$2\sin \omega_1 t \cos \omega_2 t = \sin(\omega_1 + \omega_2)t + \sin(\omega_1 - \omega_2)t$$

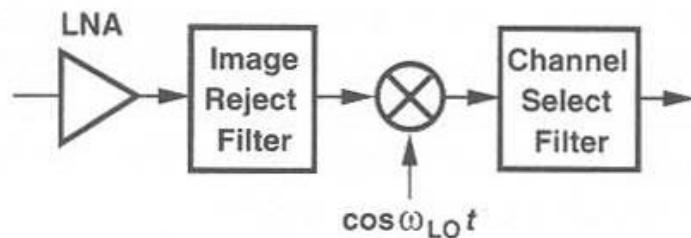
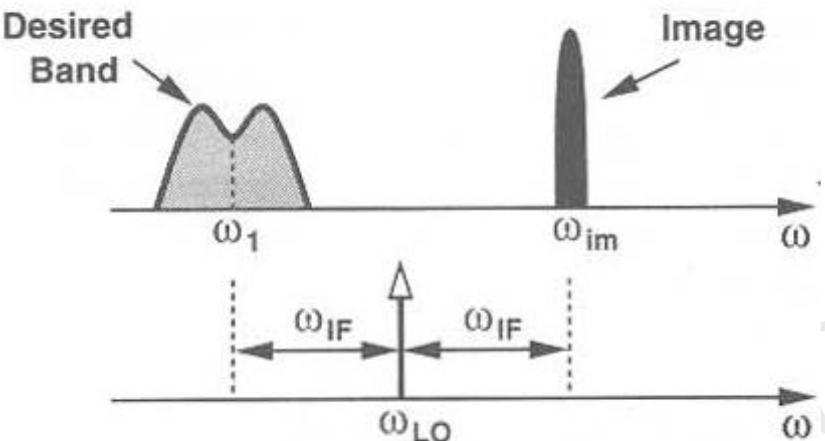
$$2\cos \omega_1 t \sin \omega_2 t = \sin(\omega_1 + \omega_2)t - \sin(\omega_1 - \omega_2)t$$

$$2\cos \omega_1 t \cos \omega_2 t = \cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t$$

# Mitigating Image: Basic Configuration

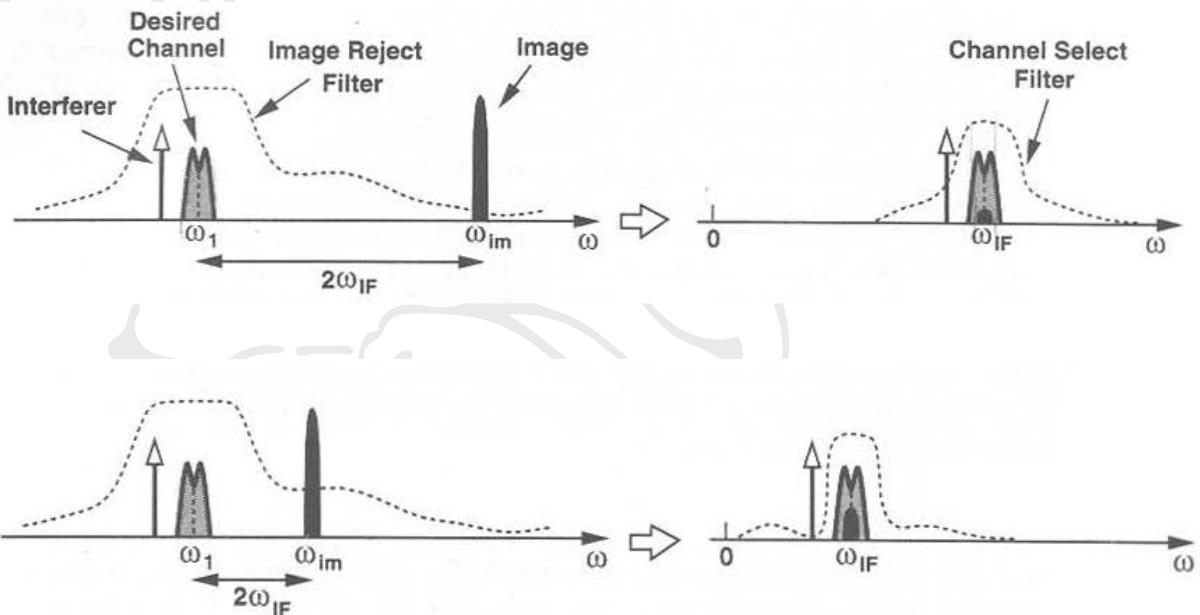


# Mitigating Image: Sensitivity vs Selectivity

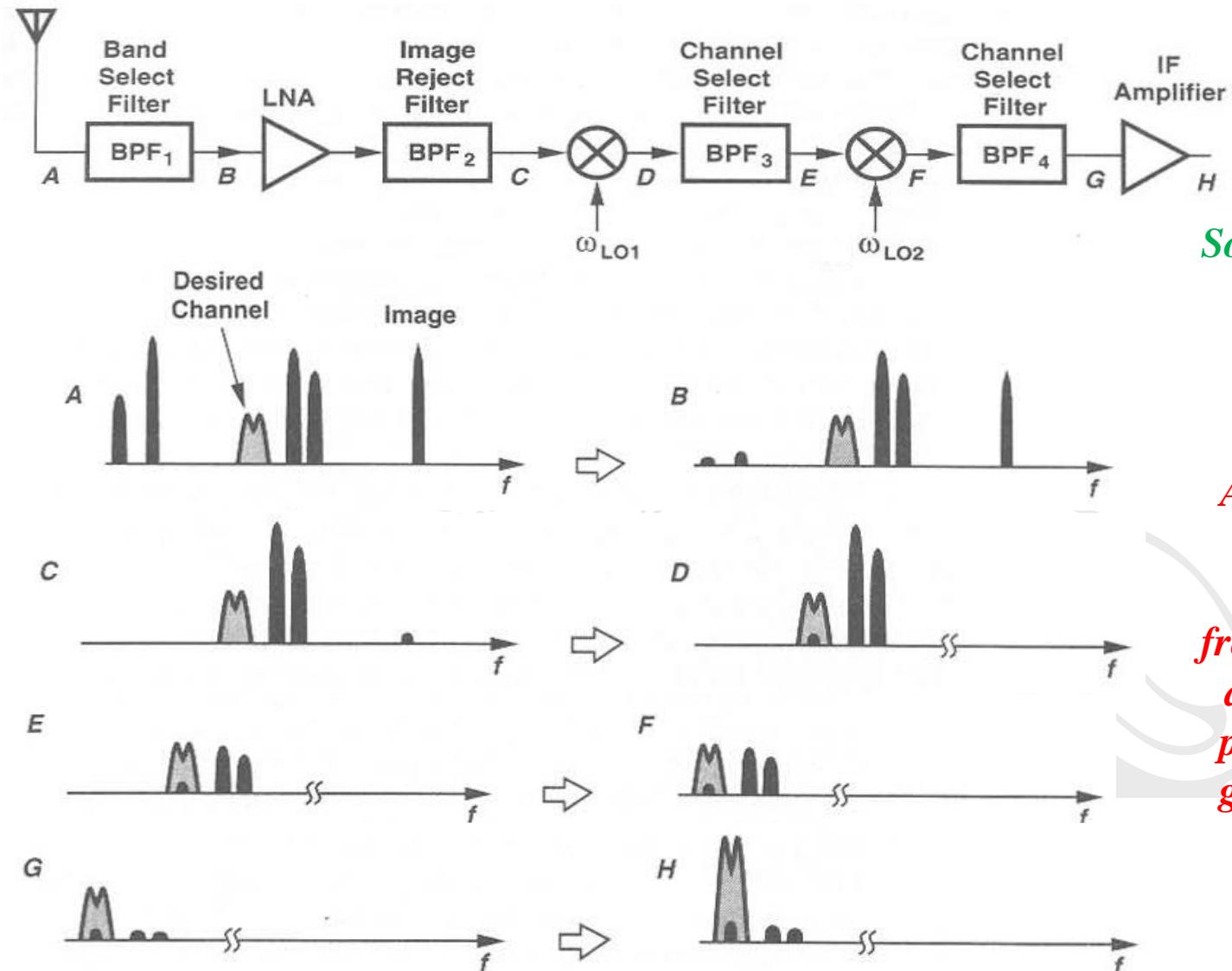


Sensitivity: Image degrades the sensitivity

- Larger  $\omega_{IF}$  put constraint over practical implementation of channel selection filter.
- As center frequency of any filter increases, the Q must be increased in order to have sharper selection.
- For higher  $\omega_{IF}$ , the channel selection is (suppression of nearby interferers) difficult.
- IF also depends on availability and physical size of filters.



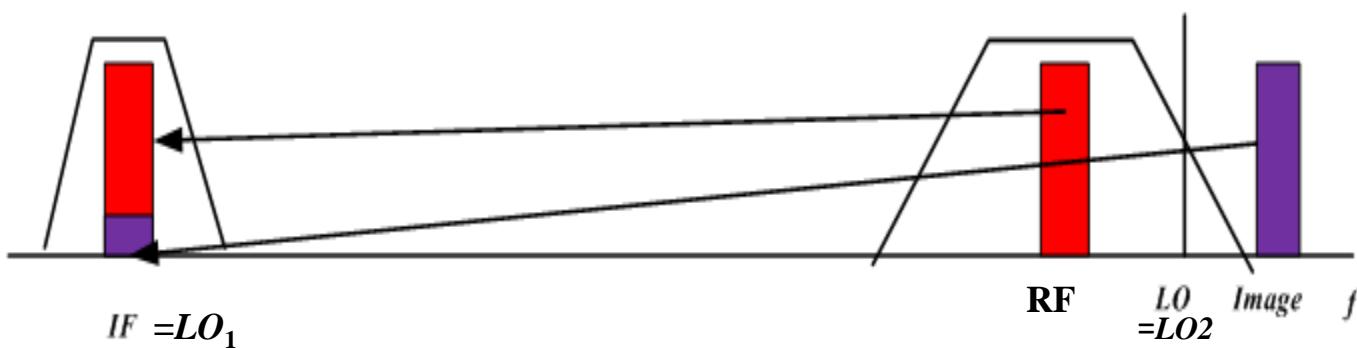
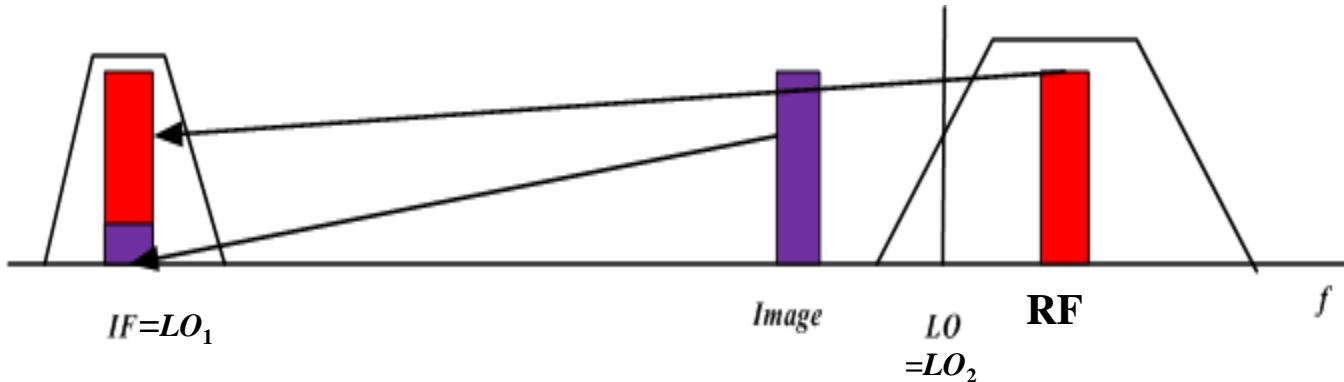
# Mitigating Image: Optimum Sensitivity vs Selectivity Using Multiple IF



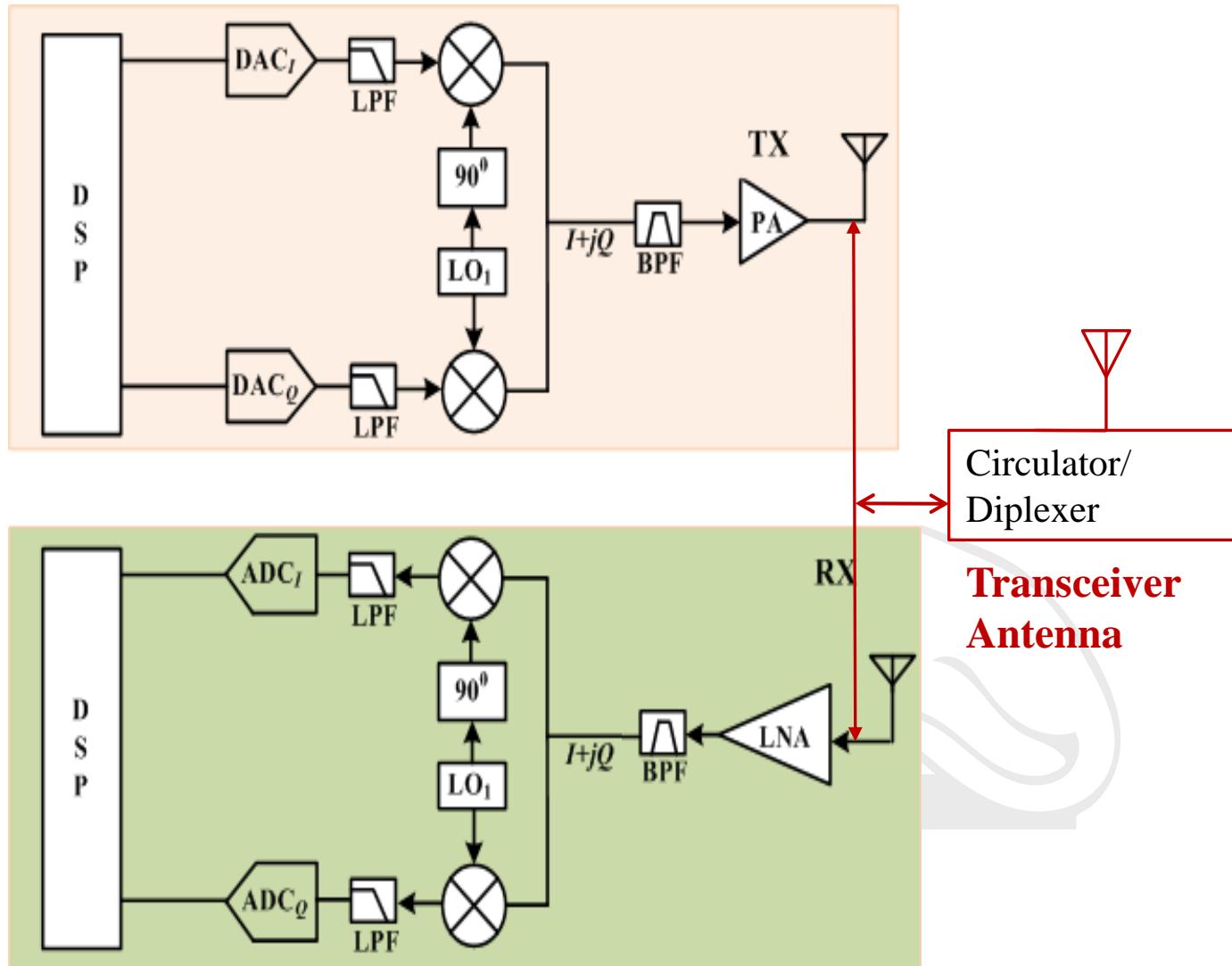
*Solution: The multiple intermediate frequencies.*

*Additional Problem: The multiple intermediate frequencies may cause a spurious response problem and require good frequency plan*

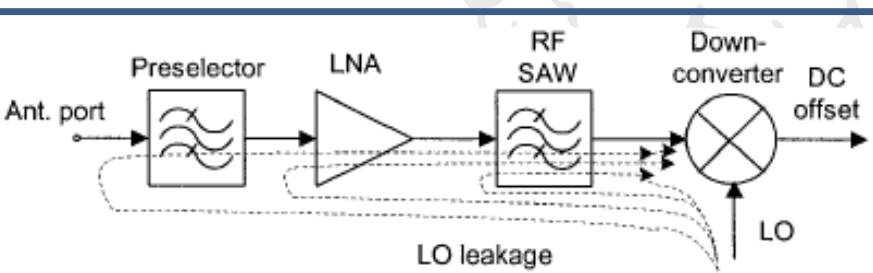
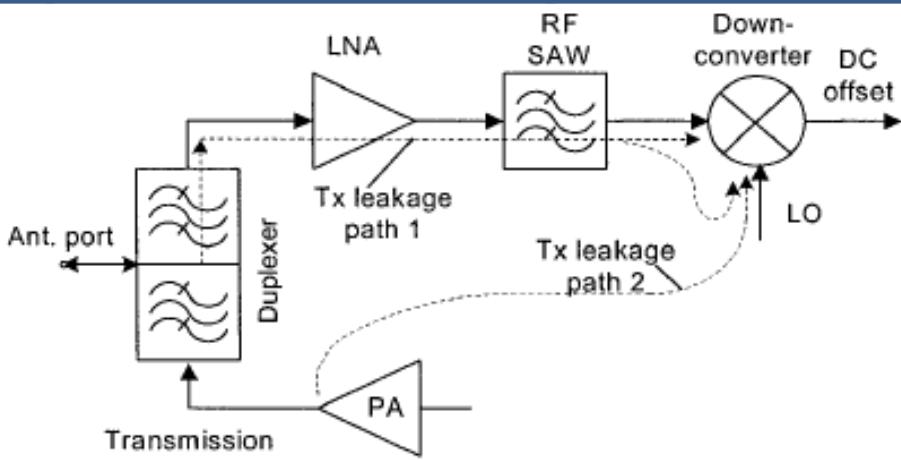
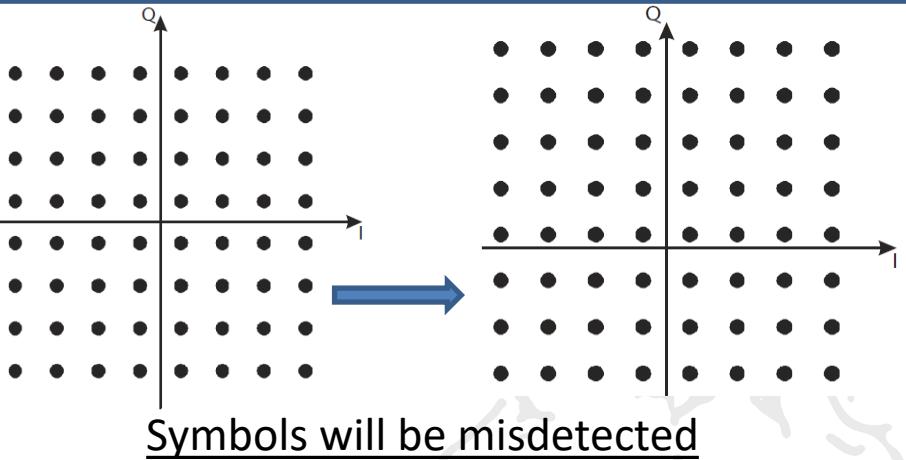
# Selection of LO2 frequency



# Homodyne Transceiver/ zero-IF transceiver



# Homodyne Transceiver/ zero-IF transceiver: Distortions (DC-OFFSET)



### *Due to LO Self Mixing*

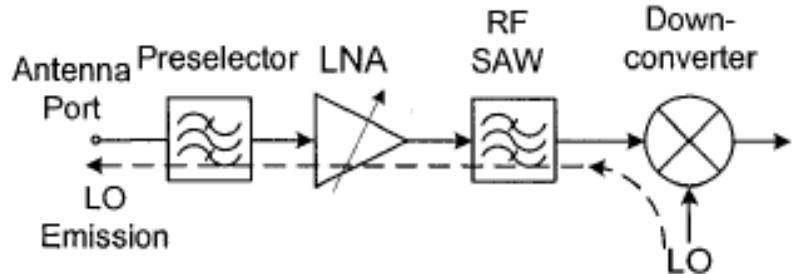
- Due to limited isolation between the LO and the RF port downconverter.
- The LO leakage is reflected at the interface between stages

### *Due to Transmission Leakage Self Mixing*

- 1<sup>st</sup> leakage path is from the duplexer through the LNA
- 2<sup>nd</sup> Leakage path is from the power amplifier of the transmitter through the substrate PCB, and/or the common power supply circuitry, and the receiver LO path to the LO port of the down-converter.
- 1<sup>st</sup> and 2<sup>nd</sup> transmission leakages self-mixing also produce the third DC offset.

The DC offset can be time-invariant or the time-variant DC offsets

# Homodyne Transceiver/ zero-IF transceiver: Distortions (DC-OFFSET)



## ***LO Leakage Emission***

The LO frequency is equal to the received carrier frequency, and this emission is in the receiver band.

Example: If the allowable level of the emission within the receiver band : -60 to -80 dBm.  
 & LO level: -5 to 0 dBm.

To be in the limit: LO to RF isolation in down-converter + LNA reverse isolation > 85 dB

## ***Second Order Distortion***

Two strong narrow-band interferers  $x(t) = A\cos 2\pi f_a t + B\cos 2\pi f_b t$  (*Can be interpreted as AM modulated signal with baseband BW=f<sub>b</sub>-f<sub>a</sub>*) when passes 2<sup>nd</sup> order nonlinearity

$$y = a_1 x(t) + a_2 x^2(t) + \dots$$

$$\text{2}^{\text{nd}} \text{ order term} = a_2 \frac{A^2 + B^2}{2} + AB \cos 2\pi(f_a - f_b)t + \text{high freq. components} \dots$$

DC Component                      Near to DC Component

- The second-order distortion interference primarily happens due to 2<sup>nd</sup> -order nonlinearity of the RF I/Q down-converter.
- The low frequency and DC products caused by such distortion of the LNA and the RFA in the front-end are blocked by the RF BPF and the AC coupling capacitor.

# Homodyne Transceiver/ zero-IF transceiver

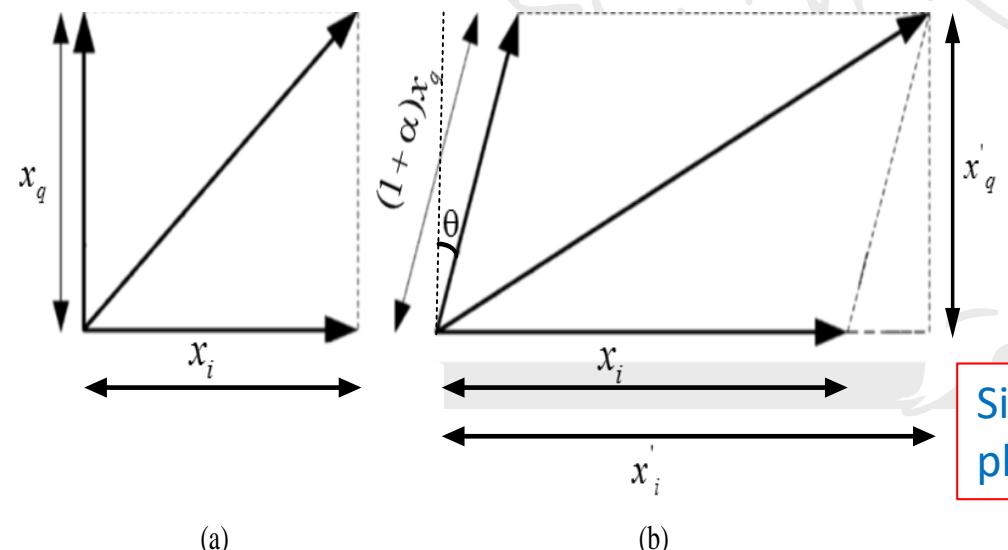
## Distortions (I/Q Imbalance) (1/3)

### I/Q imbalance in Transmitter:

Baseband signal:  $x = x_i + jx_q$

Up-converted signal:  $y = \Re\{xe^{j2\pi f_c t}\} = x_i \cos(2\pi f_c t) - x_q \sin(2\pi f_c t)$

Effect of Phase-Imbalance



The phase imbalance changes the effective values of I and Q signals:

$$x'_i = x_i + (1 + \alpha)x_q \sin(\theta)$$

$$x'_q = (1 + \alpha)x_q \cos(\theta)$$

Similarly gain imbalance will change the phase relation!



# Homodyne Transceiver/ zero-IF transceiver

## Distortions (I/Q Imbalance) (1/3)

Transmitted signal with I/Q imbalance is given as:

$$y = x_i \cos(2\pi f_c t) + x_q (1 + \alpha) \sin(2\pi f_c t + \theta)$$

The I/Q imbalance can also be shown as quadrature coefficients:

If gain is distributed as  $1 + \frac{\alpha}{2}$  and  $1 - \frac{\alpha}{2}$  between I and Q branches and

phase is also distributed as  $\frac{\theta}{2}$  deviation from both the axis.

$$y = k_1 x(t) + j k_2 x^*(t)$$

$k_1$  and  $k_2$  define the extent of gain and phase imbalance.

# Homodyne Transceiver/ zero-IF transceiver Distortions (I/Q Imbalance) (3/3)

Received data:

No I/Q imbalance

$$\hat{x}_I = \int_0^T y \cos(2\pi f_c t) dt = \frac{1}{2} [x_I]$$

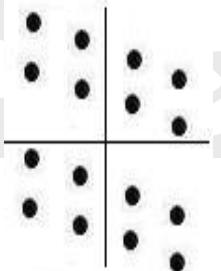
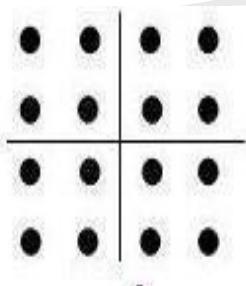
$$\hat{x}_Q = \int_0^T y \sin(2\pi f_c t) dt = \frac{1}{2} [x_Q]$$

With I/Q imbalance

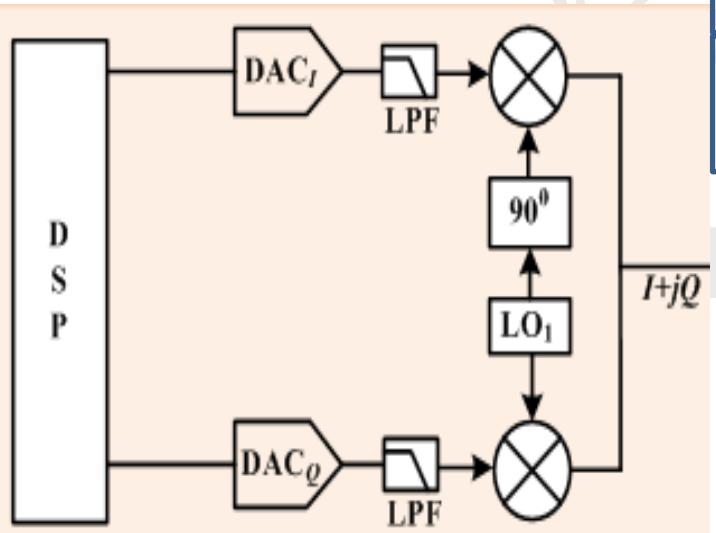
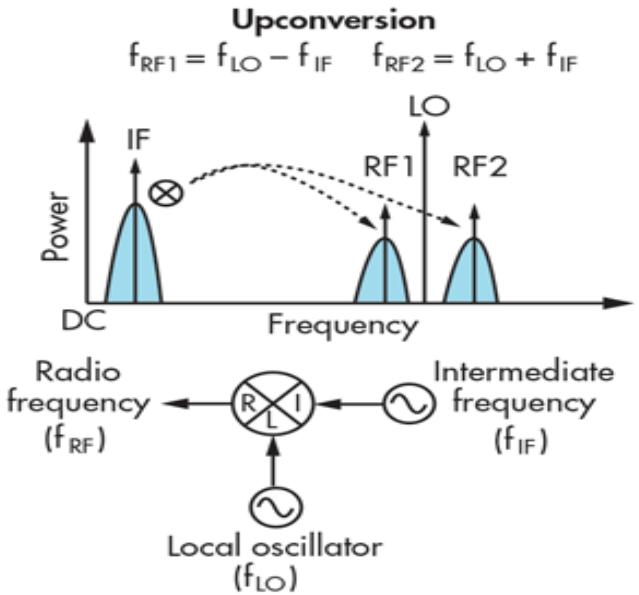
$$\hat{x}_i = \int_0^T y \cos(2\pi f_c t) dt = \frac{1}{2} [x_i + x_q (1+\alpha) \sin(\varphi)]$$

$$\hat{x}_q = \int_0^T y (-\sin(2\pi f_c t)) dt = \frac{1}{2} [x_q (1+\alpha) \cos(\varphi)]$$

Constellation Diagram for 16-QAM signal



# Low IF Transceiver: Image Rejection in Quadrature Upconverter



$$v_{out}(t) = V_0 \sin \omega_{in} t \sin \omega_{LO} t + V_0 (1+\epsilon) \cos \omega_{in} t \cos(\omega_{LO} t + \theta)$$

$$= \frac{V_0}{2} [1 + (1+\epsilon) \cos \theta] \cos(\omega_{in} - \omega_{LO}) t$$

**Image Suppression in presence of I-Q Imbalances**

$$- \frac{V_0}{2} (1+\epsilon) \sin \theta \sin(\omega_{in} - \omega_{LO}) t$$

$$+ \frac{V_0}{2} [-1 + (1+\epsilon) \cos \theta] \cos(\omega_{in} + \omega_{LO}) t$$

$$+ \frac{V_0}{2} (1+\epsilon) \sin \theta \sin(\omega_{in} + \omega_{LO}) t$$

If  $\epsilon = 0; \theta = 0 \Rightarrow V_{out} = V_0 \cos(\omega_1 - \omega_2) t$

**Image Rejection**

$$\frac{P_{im}}{P_{sig}} = IRR = \frac{(1+\epsilon)^2 - 2(1+\epsilon)\cos\theta + 1}{(1+\epsilon)^2 + 2(1+\epsilon)\cos\theta + 1}$$

If,  $I = V_0 \sin \omega_{in} t;$

$Q = V_0 \cos \omega_{in} t;$

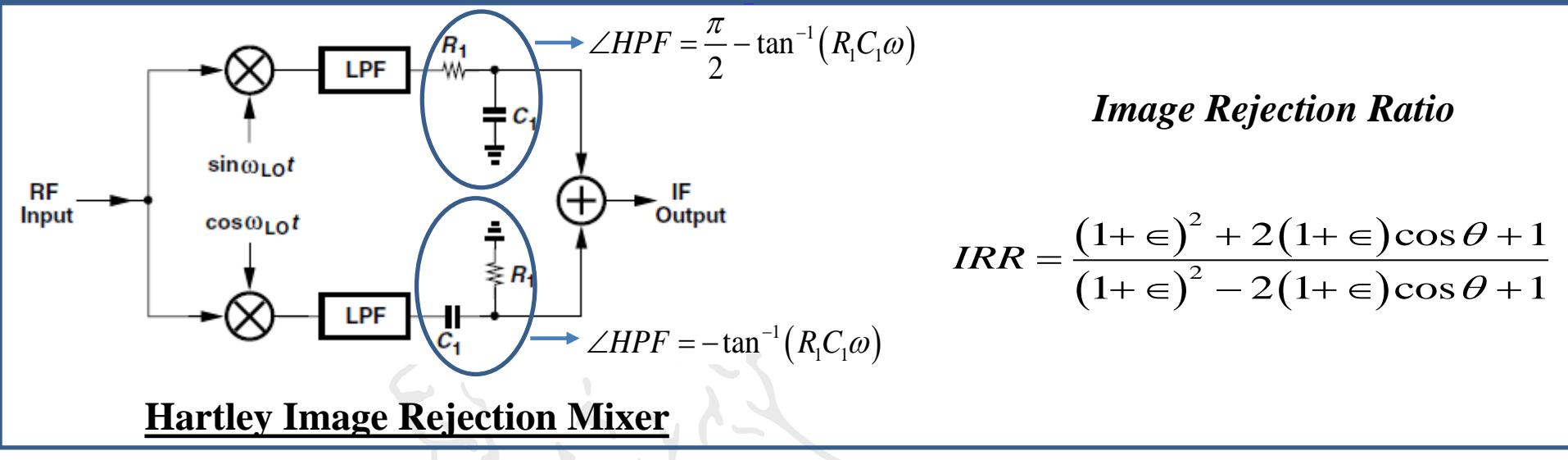
$LO = \cos \omega_{LO} t$

$$V_{out} = I \sin \omega_{LO} t + Q \cos \omega_{LO} t$$

$$V_{out} = V_0 \cos(\omega_1 - \omega_2) t$$

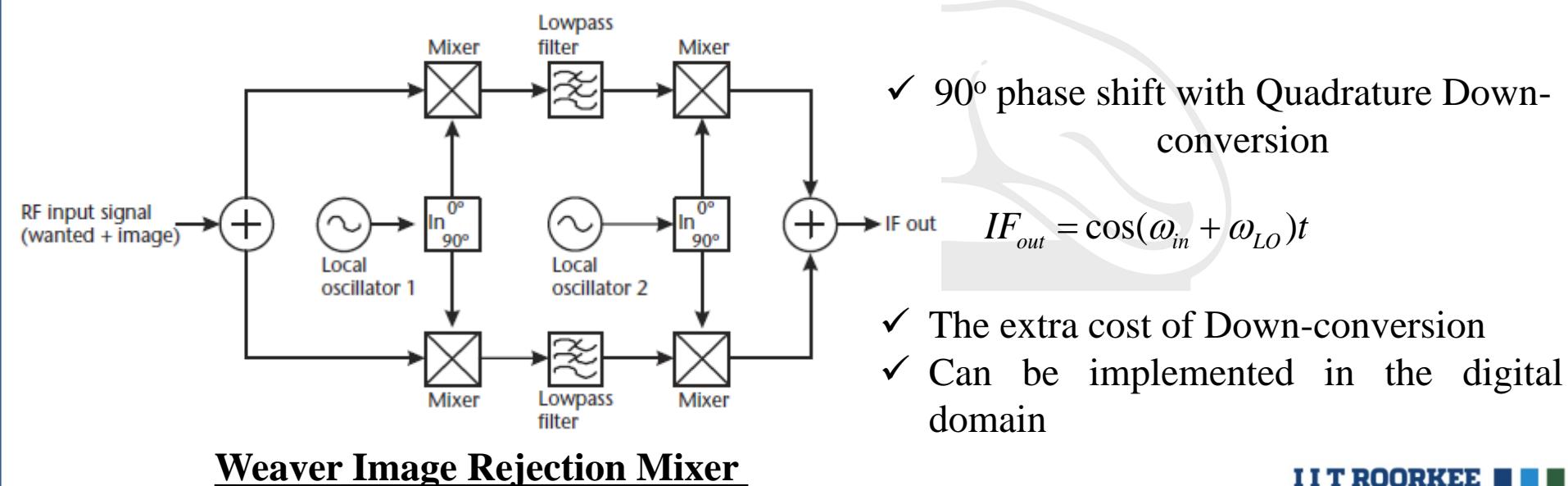
$2 \sin \omega_1 t \sin \omega_2 t = \cos(\omega_1 - \omega_2) t - \cos(\omega_1 + \omega_2) t$   
 $2 \sin \omega_1 t \cos \omega_2 t = \sin(\omega_1 + \omega_2) t + \sin(\omega_1 - \omega_2) t$   
 $2 \cos \omega_1 t \sin \omega_2 t = \sin(\omega_1 + \omega_2) t - \sin(\omega_1 - \omega_2) t$   
 $2 \cos \omega_1 t \cos \omega_2 t = \cos(\omega_1 + \omega_2) t + \cos(\omega_1 - \omega_2) t$   
 $\cos(\omega_{LO} t + \theta) = \cos \omega_{LO} t \cos \theta + \sin \omega_{LO} t \sin \theta$

# Low IF Transceiver: Image Rejection in Quadrature Upconverter



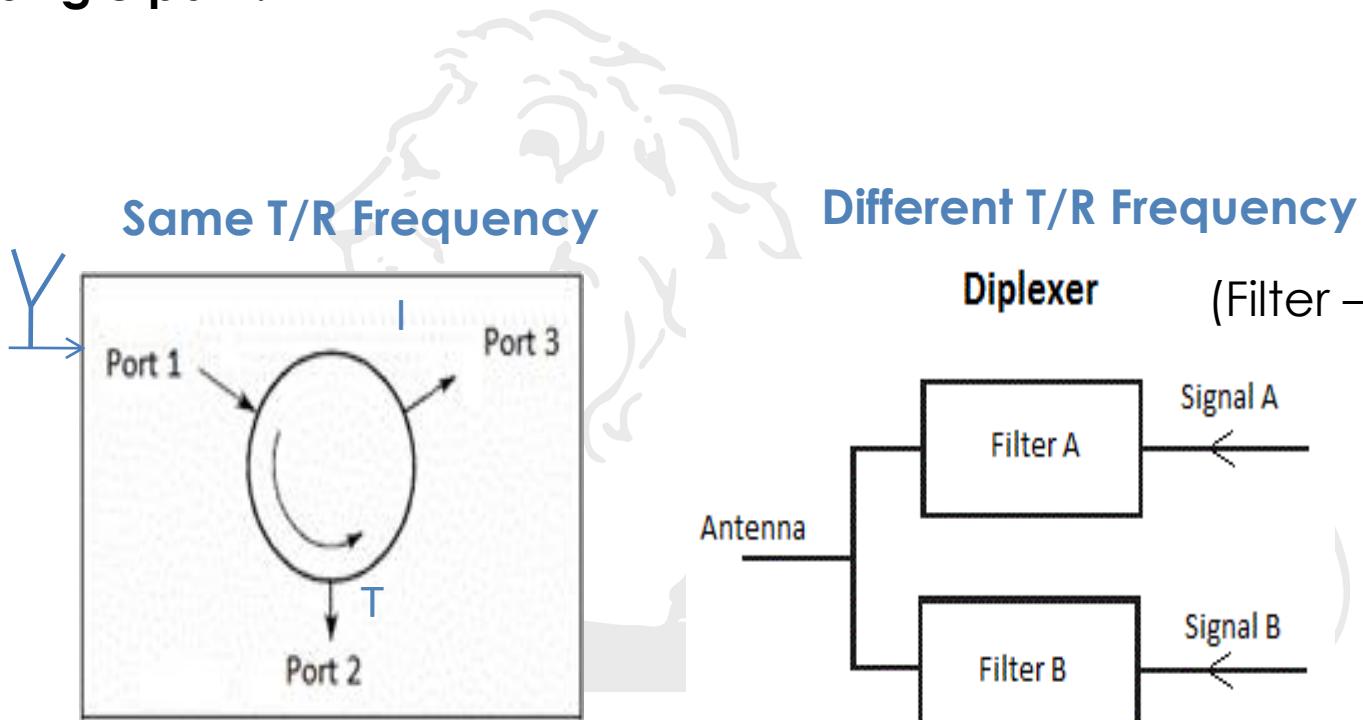
$$IRR = \frac{(1+\epsilon)^2 + 2(1+\epsilon)\cos\theta + 1}{(1+\epsilon)^2 - 2(1+\epsilon)\cos\theta + 1}$$

## Hartley Image Rejection Mixer



# Key Hardware Components (1/2)

- Power amplifiers
- Circulator/ diplexer: To allows directional communication over a single path.



# Key Hardware Components (3/3)

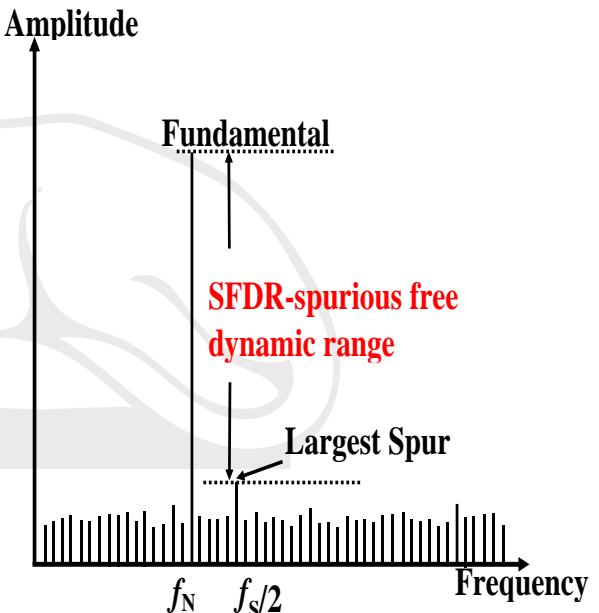
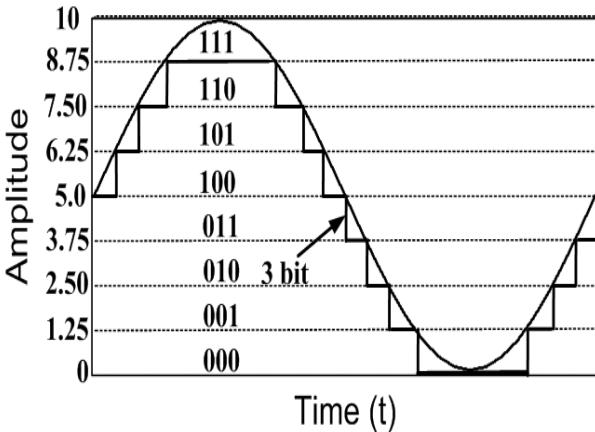
- D/A converter and A/D converter

**SNR:** Signal to noise ratio (S/N)

**SINR (SINAD, SFDR) :** Signal to noise and distortion ratio ( $S/(N+D)$ )  
 (Effective bits are calculated according to the SINR)

$$\text{SNR} = (6.02 \cdot N + 1.76) \text{ dB}$$

Where,  $N$ = Number of bits



## Superheterodyne

- More complex, difficult for chip-based implementation.
- I/Q imbalance can be avoided.
- LO leakage and Dc offset errors are not significant.
- More costly design due to extra analog components.

## Homodyne

- Candidate for chip-based design.
- I/Q imbalance image leads to in-band distortion
- LO leakage and Dc offset errors are significant.
- Simple design.

Combination of these two methods can be investigated for the best of two architectures!

## Part 2: Introduction to Basics of MOSFET & Its Model

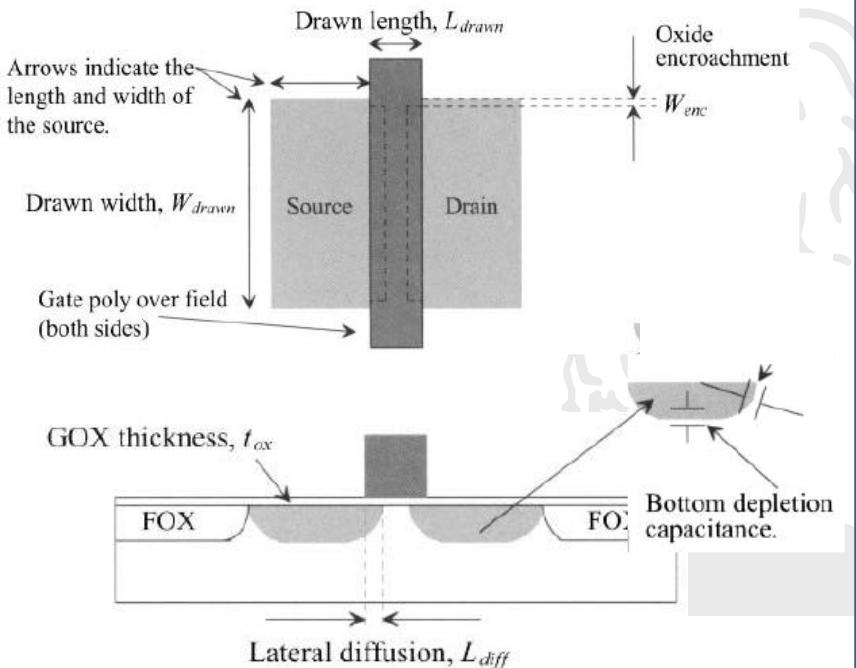


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- Introduction to MOSFET Device
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  - ❖ IV Characteristics: TRIODE and Saturation Region
  - ❖ Channel Length Modulation
  - ❖ Subthreshold Region
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- Short Channel Effect
- MOSFET Scaling
- MOS Transistor small signal Behavior
- MOS Static Transistor Modelling
- The Shichman-Hodges Model for Heavy Inversion Operation
- The SPICE Level 3 Empirical Model
- References

# Introducing MOSFET Device

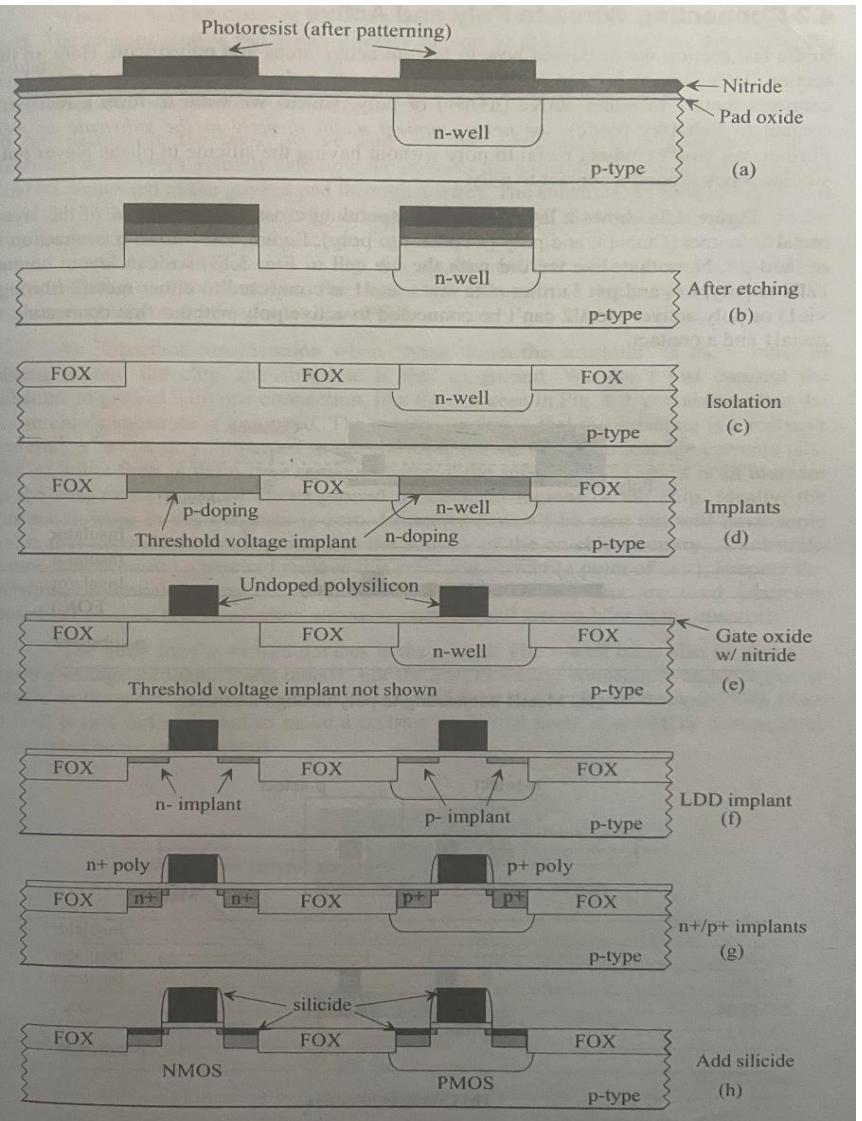
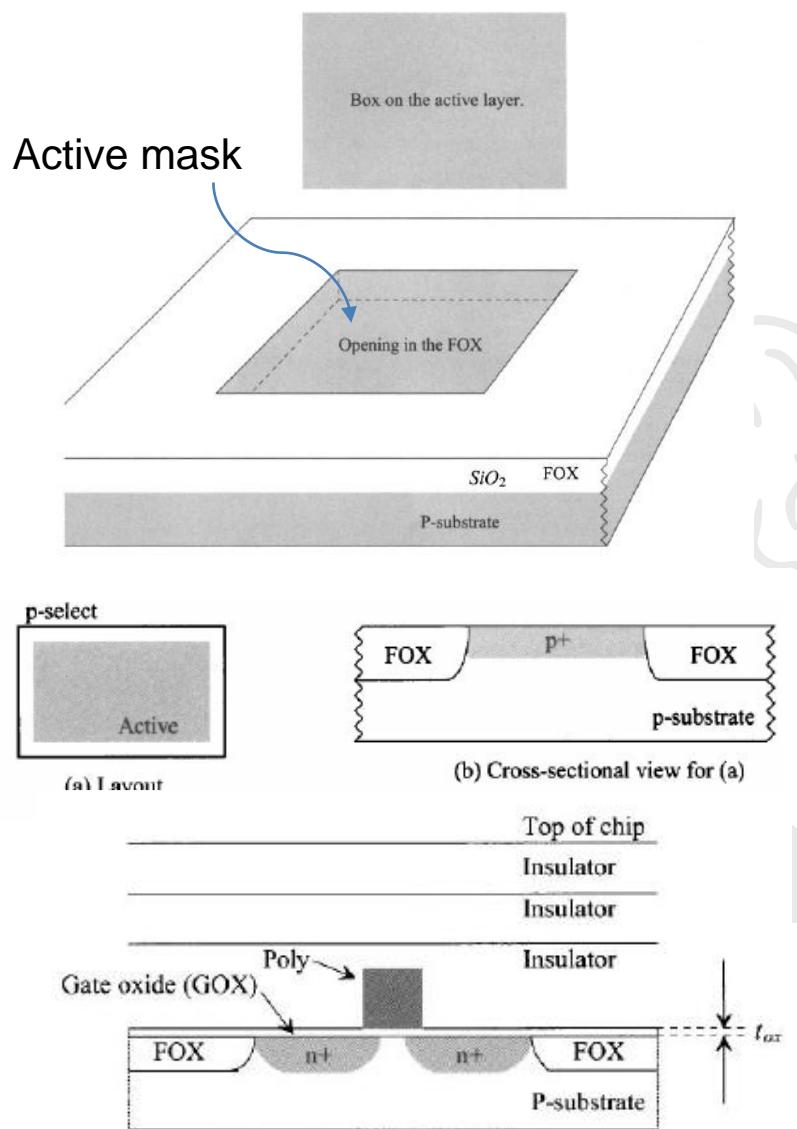
- MOSFET is a 4-terminal device: **Gate, Drain, Source and Bulk/Substrate**. The Voltage applied at the Gate will decide the channel formation between drain and source and hence drain current.
- The substrate is typically biased to maintain the reverse bias at S/D junctions for MOSFET operation.



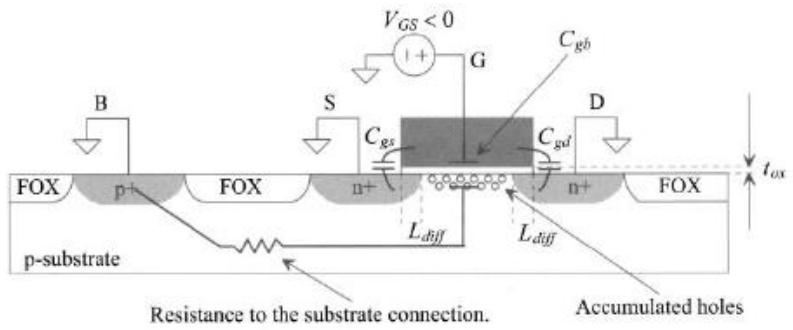
GOX: Gate Oxide (primarily present as integral part of MOSFET operation).  
 FOX: Field Oxide is used to isolate the devices from one another.

- Gate Dimension along Source-Drain path is called Length ( $L$ ).
- Gate Dimension perpendicular along Source-Drain path is called width ( $W$ ).
- Lateral diffusion: While drain and source regions are implanted, implant laterally diffuses underneath the gate.
- If  $L_{drawn}$  is the drawn length (in the layout), the effective length is  $L_{eff} = L_{drawn} - 2L_{diff}$ , where  $L_{diff}$  is the length of lateral diffusion.
- Similarly, due to limited precision in patterning FOX as specified by the active mask layer, the oxide may encroach on the active area called oxide encroachment.  $W_{eff} = W_{drawn} - 2W_{diff}$ ,
- In the remaining course we denote  $L_{eff}$  and  $W_{eff}$  as  $L$  and  $W$  respectively.

# General CMOS PROCESS flow



# Introducing MOSFET Device: Capacitances (1/3)



## 1. Accumulation: $V_{gs} < 0$

- In this case, mobile holes (in case of NMOS) from the substrate are attracted (or accumulated) under the GOX.
- The drain/source and bulk is grounded.

➤ Various Capacitances formed in such a case are:

❖  $C_{gb}$ : Capacitance between gate electrode and substrate

$$C_{gb} = \frac{\epsilon_{ox}}{t_{ox}} (L_{eff}) W_{drawn} (scale)^2 = C'_ox L_{eff} W_{drawn} (scale)^2$$

Where,  $\epsilon_{ox} = \epsilon_r \epsilon_0 = 3.97 \times (8.85 \times 10^{-18}) F/\mu m$ ,  $C'_ox = \frac{\epsilon_{ox}}{t_{ox}}$  is oxide capacitance per unit area.

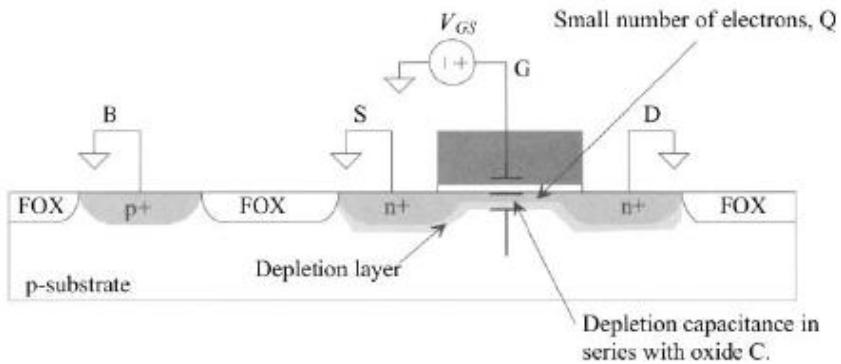
❖  $C_{gd}$ : Capacitance between gate and drain;  $C_{gs}$ : Capacitance between gate and source

$$C_{gs} = C'_ox L_{diff} W_{drawn} (scale)^2 = C_{gd}$$

❖ The total Capacitance is :  $C_{ox} = C_{gd} + C_{gs} + C_{gb} = C'_ox L_{drawn} W_{drawn} (scale)^2$

➤ There is a significant resistance in series with  $C_{gb}$  due to significant distance between the area under the gate oxide and substrate connection. However, the resistivity of n+ source and drain region in series with  $C_{gs}$  and  $C_{gd}$  can be neglected.

# Introducing MOS Device: Capacitances (2/3)

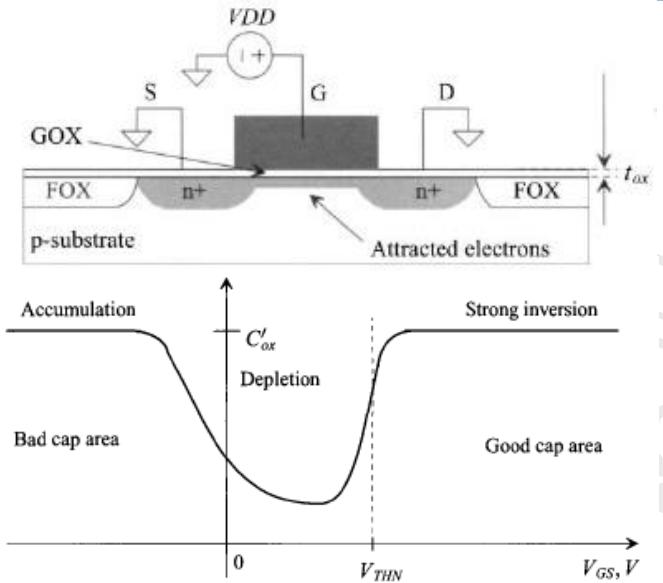


## 2. Depletion:

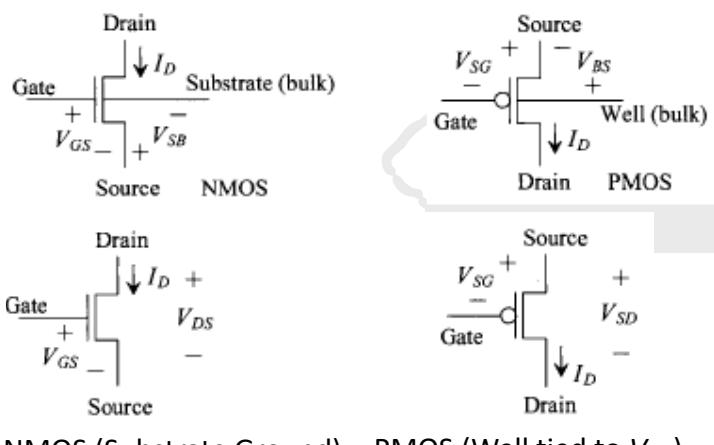
- $V_{gs}$  is neither negative enough to attract a large number of holes under the oxide and nor positive enough to attract a large number of electrons.
- In such a condition, gate is said to be nearly depleted (depleted of free electrons and holes).

- As  $V_{GS}$  is increased from some negative voltage, holes will be displaced under the gate, leaving immobile acceptor ions that contribute a negative charge.
- As we increase  $V_{gs}$  a capacitance between the gate and the induced (n) channel under the oxide exists.
- Also, a depletion capacitance between the depleted channel and the substrate is formed.
- The capacitance between the gate and the source/drain is simply the overlap capacitance, while the capacitance between the gate and the substrate is the oxide capacitance *in series* with the depletion capacitance.
- The MOSFET operated in this region is said to be in *weak inversion* or the *subthreshold region* because the surface under the oxide is not heavily n+.

# Introducing MOS Device: Capacitances (3/3)



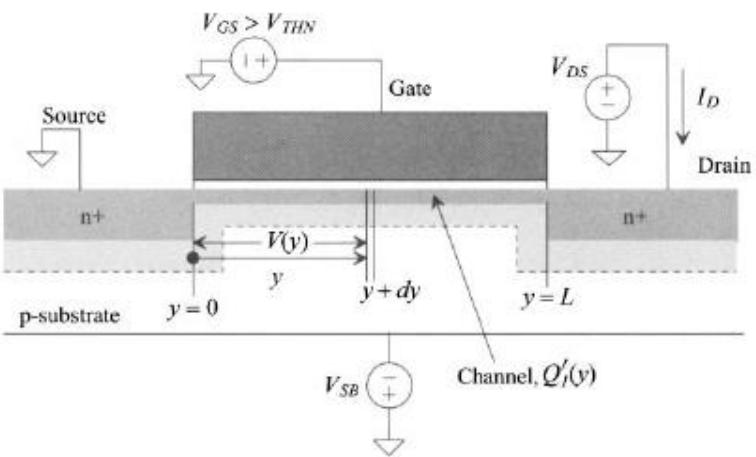
Various MOSFET Symbols



## 3. Strong Inversion:

- $V_{gs}$  is sufficiently large ( $\gg V_{THN}$ , the threshold voltage of the NMOS device)
- A large number of electrons are attracted under the gate, the surface is said to be inverted, that is, no longer p-type.
- Above figure shows the change in the capacitance at the gate as  $V_{GS}$  is varied (for an NMOS device), when the source, drain, and bulk are grounded.
- Above figure shows that the MOSFET can operate as capacitor in accumulation region. However, due to large resistance appearing in series to  $C_{gb}$  in this region, this may not provide a good capacitance.
- It is preferable to operate MOSFET in strong inversion region when a capacitor is needed. In such a case, the attracted electrons under GOX short the drain and source together forming a low resistance bottom plate for the capacitor.

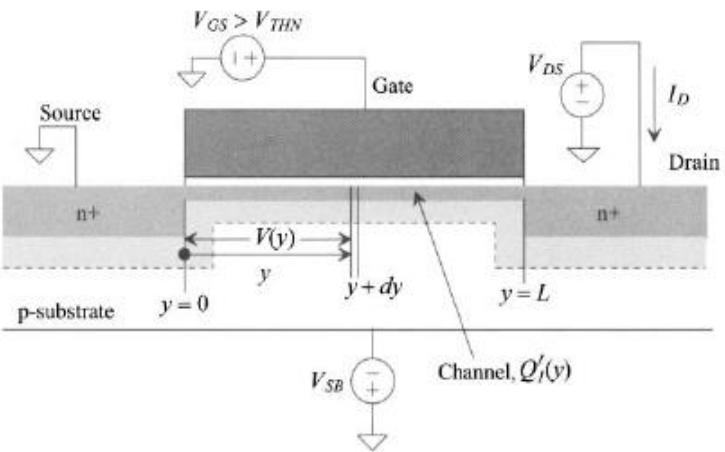
# Introducing MOS Device: IV Characteristics in TRIODE Region (1/2)



- $V_{gs}$  is sufficiently large ( $\gg V_{THN}$ , the threshold voltage of the NMOS device)
- A large number of electrons are attracted under the gate, the surface is said to be inverted, that is, no longer p-type.
- In such a case  $V_{DS}>0$  cause a drift current to flow from drain to source.

- In the analysis below, it is assumed that  $V_{DS}$  is sufficiently small such that  $V_{THN}$  and depletion layer width is approximately constant.
- The charge/unit area in the inversion layer is given by:  $Q'_{ch} = C'_{ox} \{V_{GS} - V(y)\}$  ----(1) , where, the term  $V(y)$  is the voltage w.r.t the source of MOSFET at  $y$  distance away from the source.
- A charge present in the inversion layer due to the application of  $V_{THN}$  necessary for the conduction is:  $Q'_b = C'_{ox} V_{THN}$  ----(2) .
- The total charge available in the inverted channel for the conduction of current: (1)-(2) i.e  $Q'_I = C'_{ox} \{V_{GS} - V(y) - V_{THN}\}$  ----(3)

# Introducing MOS Device: IV Characteristics in TRIODE Region (2/2)



- The differential resistance of the channel region with length  $dy$  and width  $W$  is given by:
 
$$dR = \frac{1}{\mu_n Q'_I(y)} \frac{dy}{W} \quad \text{---(4)}$$
 where,  $\mu_n$  is the mobility ( $\text{cm}^2/\text{Vsec}$ ).
- For short channel devices, the mobility decreases when the velocity of the carrier starts to saturate.
- This causes the effective sheet resistance in (4) to increase resulting into lowering of drain current. This is called velocity saturation.

- The differential voltage drop across the differential resistance is given by
- $dV(y) = I_D \cdot dR = \frac{I_D}{W \mu_n Q'_I(y)} \cdot dy \quad \text{---(5)}$ . Substituting (3) into (5) and rearranging will give:
- $I_D \cdot dy = W \mu_n C'_ox (V_{GS} - V(y) - V_{THN}) \cdot dV(y) \quad \text{---(6)}$
- The current can be obtained by integrating LHS of (6) from 0 to  $L$  and RHS from 0 to  $V_{DS}$

$$I_D = K P_n \cdot \frac{W}{L} \cdot \left[ (V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right] \text{ for } V_{GS} \geq V_{THN} \text{ and } V_{DS} \leq V_{GS} - V_{THN}$$

For PMOS

Triode Region often called Linear or Ohmic

$$I_D = K P_p \cdot \frac{W}{L} \cdot \left[ (V_{SG} - V_{THP}) V_{SD} - \frac{V_{SD}^2}{2} \right] \text{ for } V_{SG} \geq V_{THP} \text{ and } V_{SD} \leq V_{SG} - V_{THP}$$

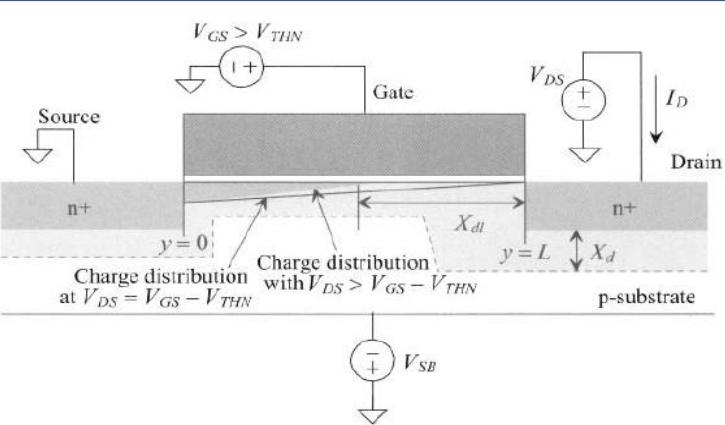
$$K P_n = \mu_n \cdot C'_ox = \mu_n \cdot \frac{\epsilon_{ox}}{t_{ox}}$$

Process Transconductance parameter

$$K P_p = \mu_p \cdot C'_ox = \mu_p \cdot \frac{\epsilon_{ox}}{t_{ox}}$$

Process Transconductance parameter

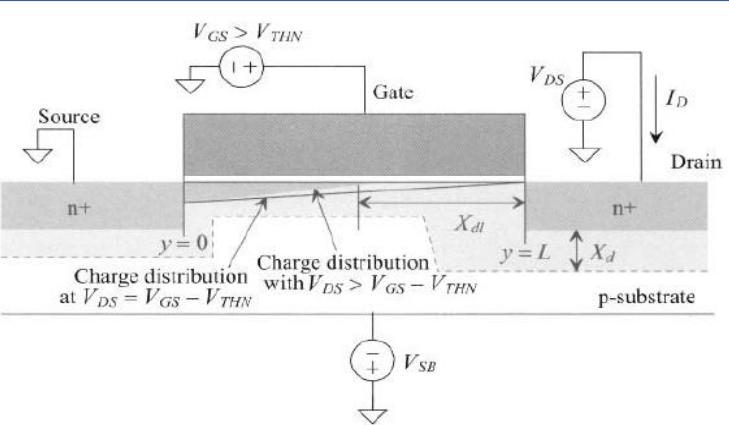
# Introducing MOS Device: IV Characteristics in SATURATION Region (1/4)



- At  $V_{DS,sat}$  the channel charge is ***pinched off*** at the drain channel interface.
- For  $V_{DS} > V_{DS,sat}$ , the fixed channel charge is attracted to the drain terminal depleting the charge in channel directly adjacent to the drain.

- Further increase in  $V_{DS}$  do not cause an increase in the drain current resulting into saturation region.
- Referring the above figure, the depletion region thickness between the drain and the channel  $X_{dl}$  increases with  $V_{DS}$ . This region eventually extend to the source side when  $V_{DS}$  is further increased resulting into ***punched through*** causing device failure.
- Max  $V_{DS}$  that can be applied: For Short Channel is set by punched through voltage, For a long channel is set by breakdown voltage of drain (n+) to substrate diode.

# Introducing MOS Device: IV Characteristics in SATURATION Region (2/4)



- Recalling Drain current equation in Triode Region:

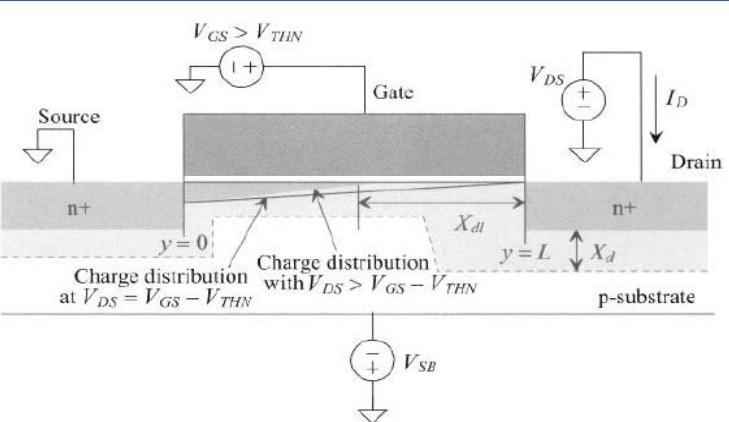
$$I_D = KP_n \cdot \frac{W}{L} \cdot \left[ (V_{GS} - V_{THN})V_{DS} - \frac{V_{DS}^2}{2} \right]$$

- When MOSFET is operating at pinch-off and beyond i.e  $V_{DS} \geq V_{GS} - V_{THN}$  and  $V_{GS} \geq V_{THN}$ , one can substitute

$$I_{D,sat} = \frac{KP_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN})^2 \quad \text{for } V_{DS} \geq V_{GS} - V_{THN} \text{ and}$$

- If,  $V_{DS} = V_{DS,sat}$  in the above equation  $V_{GS} \geq V_{THN}$
- The electrical channel length in such a case is  $L_{elec}$  which is the difference between the channel length  $L$  (neglecting lateral diffusion) and depletion layer width i.e.  $L_{elec} = L - X_{dl}$ .
- $I_D = \frac{KP_n}{2} \cdot \frac{W}{L_{elec}} \cdot (V_{GS} - V_{THN})^2$  implying the current still increases with increasing  $V_{DS}$  since the depletion layer width increases effectively reducing  $L_{elec}$ . This is called **Channel length modulation (CLM)**. Also, the effect of CLM is negligible if  $L$  increases (long channel).
- The effect of CLM can be obtained as change in  $I_D$  with  $V_{DS}$  when  $L \approx L_{elec}$ , around  $V_{DS} = V_{DS,sat}$ .

# Introducing MOS Device: IV Characteristics in SATURATION Region (3/4)



➤ The effect of CLM can be obtained as change in  $I_D$  with  $V_{DS}$  when  $L \approx L_{elec}$ , around  $V_{DS} = V_{DS,sat}$ .

➤ Derivative of  $I_D$  w.r.t  $V_{DS}$  around  $V_{DS,sat}$ :

$$\frac{\partial I_D}{\partial V_{DS}} = -\frac{KP_n}{2} \cdot \frac{W}{L_{elec}^2} \cdot (V_{GS} - V_{THN})^2 \cdot \frac{dL_{elec}}{dV_{DS}} = I_D \cdot \left[ \frac{1}{L_{elec}} \frac{dX_{dl}}{dV_{DS}} \right]$$

➤ The factor in [ ] in the above equation is called channel length modulation parameter:  $\lambda = \frac{1}{L_{elec}} \cdot \frac{dX_{dl}}{dV_{DS}}$

➤ Typical values for  $\lambda$  range from greater than  $0.1 \text{ V}^{-1}$  to less than  $0.01 \text{ V}^{-1}$  (ideally  $\lambda = 0$ ).

➤ The drain current equation considering CLM is given by:

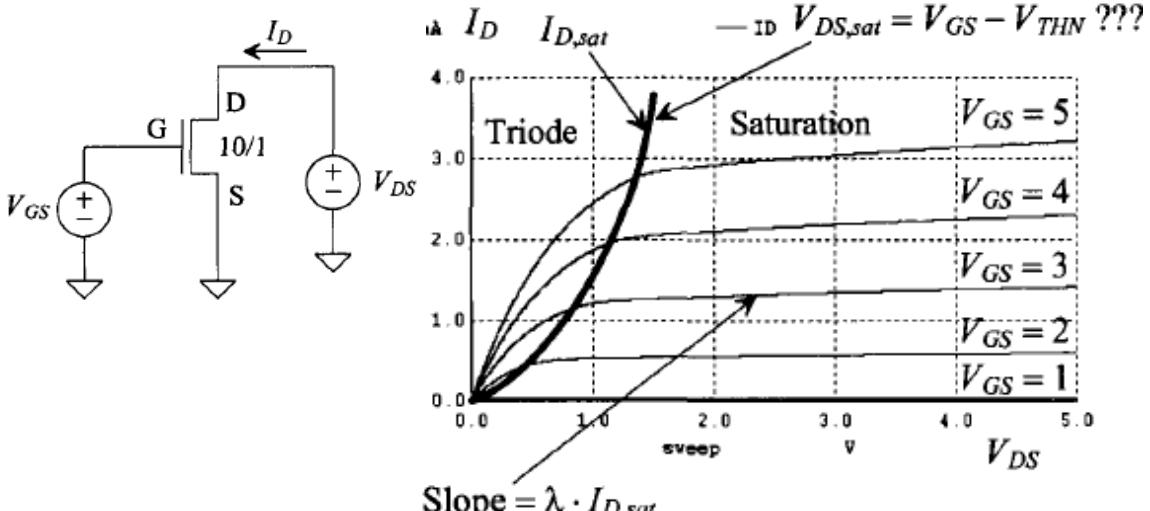
$$\therefore \partial I_D = I_D \lambda \partial V_{DS}$$

$$I_D = \frac{KP_n}{2} \cdot \frac{W}{L} (V_{GS} - V_{THN})^2 \left[ 1 + \lambda (V_{DS} - V_{DS,sat}) \right] = I_{D,sat} \cdot \left[ 1 + \lambda (V_{DS} - V_{DS,sat}) \right]$$

for  $V_{DS} > V_{DS,sat} = V_{GS} - V_{THN}$  and  $V_{GS} > V_{THN}$

➤ The above equation are assumed that the mobility does not vary with  $V_{DS}$ .

# Introducing MOS Device: IV Characteristics in SATURATION Region (4/4)



Drain Current in Triode Region:

$$I_D = K P_n \cdot \frac{W}{L} \cdot \left[ (V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

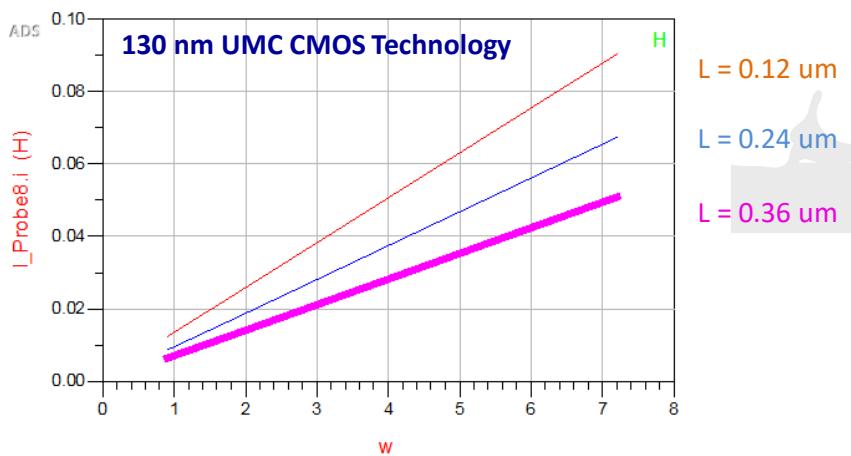
Drain Current in Saturation Region:

$$I_D = \frac{K P_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN})^2 \left[ 1 + \lambda (V_{DS} - V_{DS,sat}) \right]$$

Gate to Source Capacitance ( $C_{gs}$ ):

$$C_{gs} = \frac{\partial Q_1}{\partial V_{GS}} = \frac{2}{3} \cdot W \cdot L \cdot C'_{ox}$$

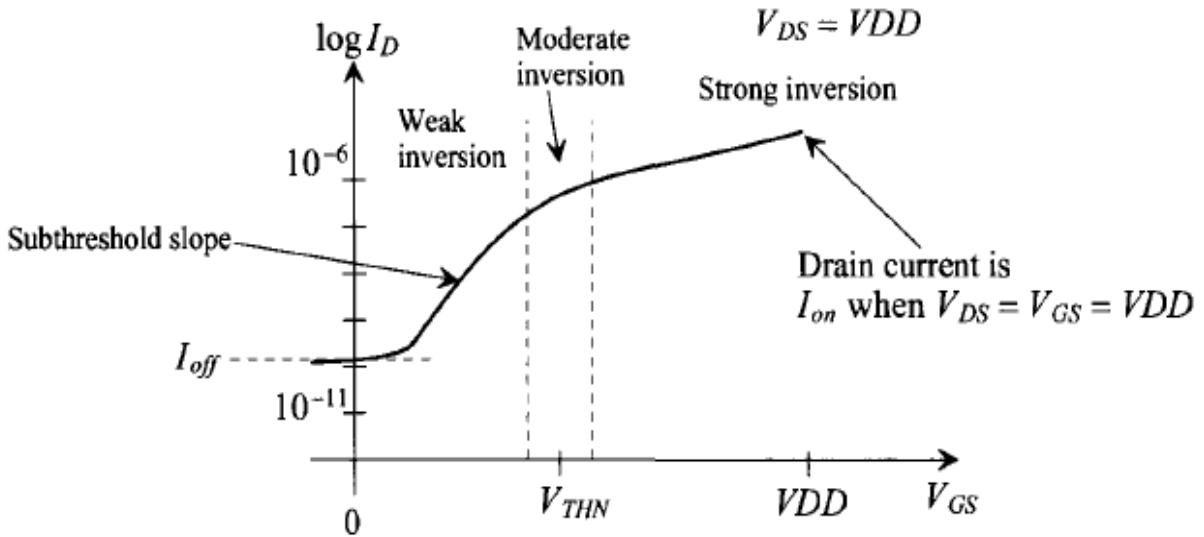
**Note :** In designing we use W/L aspect ratio to vary the current.



W: channel width ; L: channel length

- Drain current increases with increasing **channel width** and decreases by increasing the **channel length**.

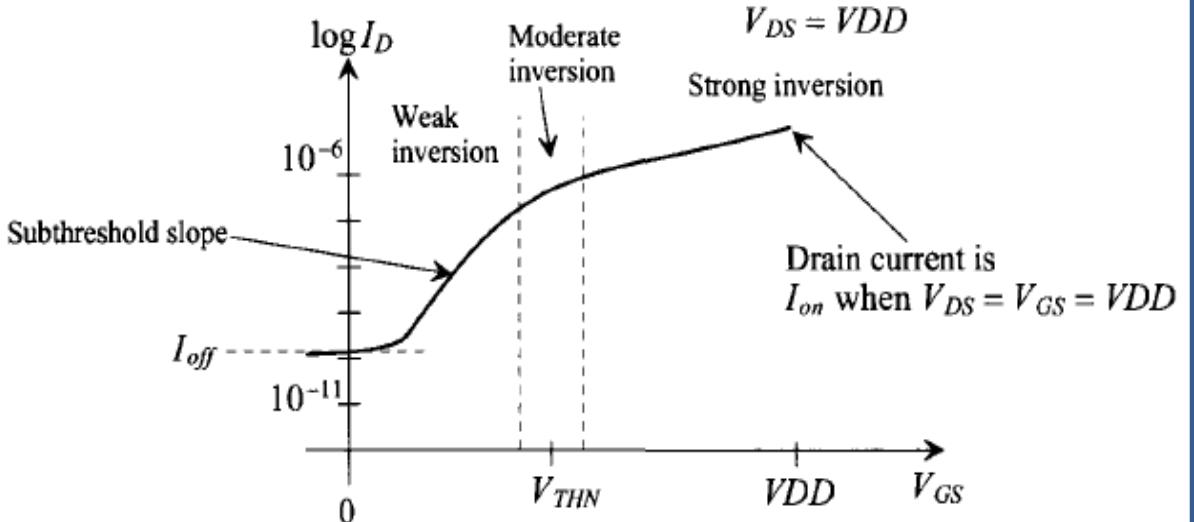
# Introducing MOS Device: The Subthreshold Region (1/2)



- Subthreshold operation can be very useful for low-power operation e.g. devices in Solar-powered calculators, battery-operated watches etc.
- Main challenge is exponential drain current characteristics resulting into problems related to matching, noise and bandwidth.

- Remember the MOSFET operating in depletion mode when:
  - ✓  $V_{gs}$  is not negative enough to attract a large number of holes under the oxide and not positive enough to attract a large number of electrons.
- In such a condition, gate is said to be nearly depleted (depleted of free electrons and holes).
- The MOSFET can still conduct (drain current can exist) in this weak inversion region.
- However, the current exist due to carrier diffusion (rather than drift in strong inversion region) similar to the carrier movement in the BJT.
- Similar to the BJT, where, carriers emitted from the emitter diffuse across base and collected by the collector, In MOSFET operating in subthreshold region, the carriers are emitted by source, diffuse across the body of the device (under GOX) and are collected by the drain.

# Introducing MOS Device: The Subthreshold Region (2/2)



- The drain Current of the MOSFET in the subthreshold region:

$$I_D = I_{D0} \cdot \frac{W}{L} \cdot e^{q(V_{GS} - V_{THN})/(n \cdot kT)}$$

Where,  $V_T = kT/q$  (thermal voltage)

- Taking the log of both the sides in the above equation:

$$\log I_D = \log \frac{W}{L} + \log I_{D0} + \underbrace{\frac{V_{THN}}{nV_T} \cdot \log e}_{\text{subthreshold slope}} + \left[ \frac{1}{V_T \cdot n} \cdot \log e \right] \cdot V_{GS}$$

- The reciprocal of the subthreshold slope is

$$\text{Subthreshold slope}^{-1} = \frac{V_T \cdot n}{\log e} (\text{mV / decade})$$

- At room temperature ( $KT/q$  is 26 mV) and  $n$  (slope parameter)=1, the slope is 60 mV/decade.
- For bulk CMOS,  $n=1.6$  this becomes 100 mV/decade

- The subthreshold slope can be a very important MOSFET design parameter in many applications.

- In Ideal MOSFET,  $I_D=0$ , when  $V_{GS} < V_{THN}$ , resulting into infinite slope.
- The drain current that flows with  $V_{GS} = 0$  and  $V_{DS} = V_{DD}$  is called  $I_{off}$ .
- The drain current that flows when  $V_{GS} = V_{DS} = V_{DD}$  (in the strong inversion region) is called  $I_{on}$ .

# The Threshold Voltage & Body Effect

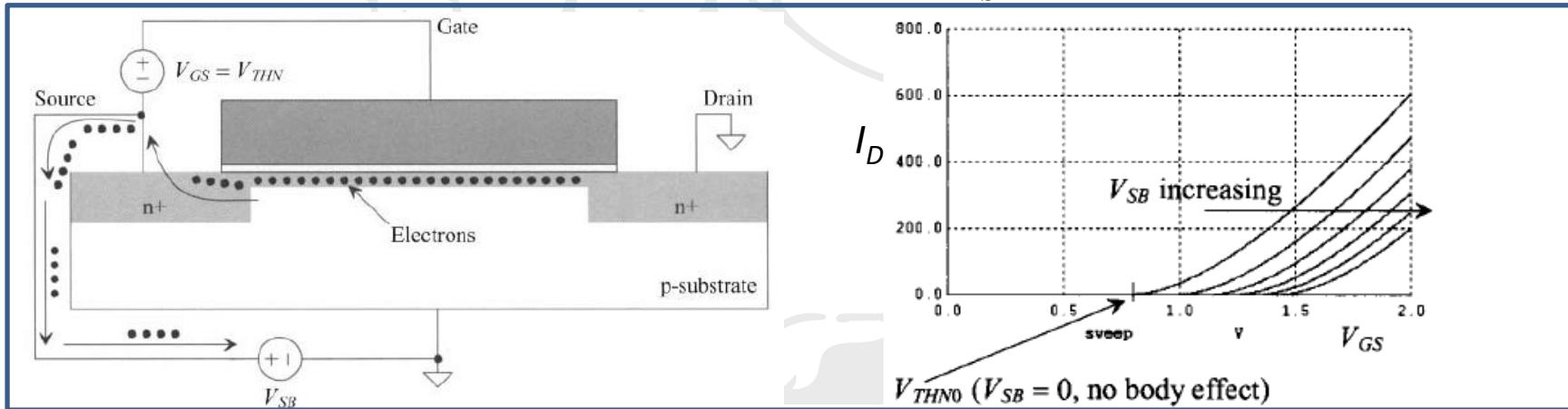
**Threshold Voltage ( $V_{th}$ ):** It is the Potential difference which is applied to the gate oxide to form a channel (**inversion layer**) between the Drain and Source.

$$V_{THN} = V_{THN0} + \gamma \left( \sqrt{2V_{fp}} + V_{SB} - \sqrt{2V_{fp}} \right)$$

$$V_{fp} = -\frac{kT}{q} \ln \frac{N_A}{n_i}; \quad \gamma = \frac{\sqrt{2q\epsilon N_A}}{C'_o}$$

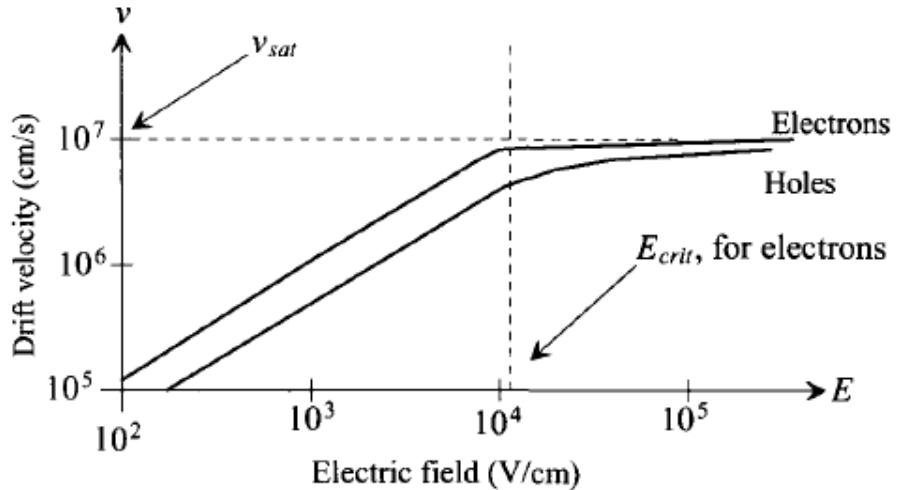
Where,  $V_{THN0}$  is the zero bias threshold voltage;  $V_{fp}$  is the electrostatic potential of *p*-type substrate.  $\gamma$  is the body effect coefficient or body factor

- It depends upon **gate material, insulating material,  $V_{BS}$  and channel doping.**



- As the source potential rises above the bulk (substrate) potential i.e ( $V_{SB}$  increasing), electrons are attracted towards the positive terminal of  $V_{SB}$  from the MOSFET's channel.
- To keep the surface inverted, a larger  $V_{gs}$  must be applied to the MOSFET.
- Thus the effect of the body stealing charge from the channel raises the threshold voltage

# The Short Channel MOSFETs

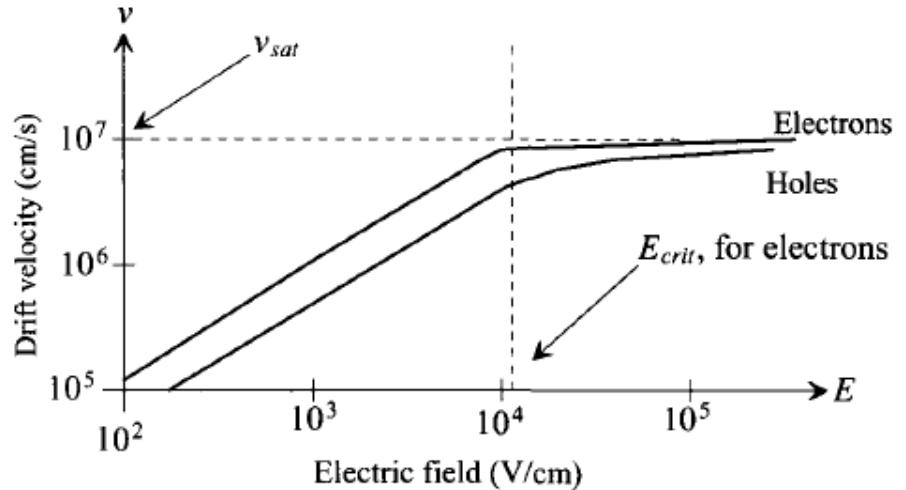


The slope of the above curve represents mobility ( $\mu=v/E$ )

- The  $I_D$  derived in previous section (for saturation region) holds for long channel CMOS process
- The modern CMOS process are well below  $<<1$  um and characterized as short channel.
- For short channel: The electric field under the gate oxide can no longer be treated in a single dimension.
- The velocity of the carriers drifting between the channel and the drain of the MOSFET can saturate. ***Carrier Velocity Saturation.***

- The above graph shows that when the electric field reaches a critical value, labeled  $E_{crit}$ , the velocity saturates at a value  $v_{sat}$ .
  - Since,  $\mu_n=v/E$ , For  $E < E_{crit}$   $\mu_n$  is constant, whereas, as  $E > E_{crit}$   $\mu_n$  starts decreasing and approximately given by
- $$\mu_n = \frac{v_{sat}}{E} = \frac{v_{sat}}{dV(y)/dy}$$
- The carrier velocity saturation results into reduction in electron or hole mobility ( $\mu_n$  or  $\mu_p$ ) and resulting into increase in the channel's effective sheet resistance.
  - The mobility of the electron also decreases with increase in the temperature and termed as **hot carrier effect.**

# The Short Channel Effect



- The drain current in Short channel vs Long channel

## Short Channel

$$I_D = W \cdot v_{sat} \cdot C'_{ox} \left( V_{GS} - V_{THN} - V_{DS,sat} \right)$$

$$I_{on} = I_{drive} = v_{sat} \cdot C'_{ox} \left( V_{GS} - V_{THN} - V_{DS,sat} \right)$$

$$I_D = I_{on} \cdot W = I_{drive} \cdot W \text{ with } V_{GS} = V_{DS} = V_{DD}$$

## Long Channel

### Drain Current in Triode Region:

$$\text{Since, } I_D = K P_n \cdot \frac{W}{L} \cdot \left[ (V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

### Drain Current in Saturation Region:

$$I_D = \frac{K P_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN})^2 \left[ 1 + \lambda (V_{DS} - V_{DS,sat}) \right]$$

# MOSFET Scaling

- A scaling parameter  $S$  ( $S < 1$ ) is used to scale the dimension of the MOSFET.
- The typical value of  $S$  in the neighborhood of 0.7 from one CMOS technology generation to the next. e.g. if a process uses a  $V_{DD}$  of 2 V, a next generation process would use a  $V_{DD}$  of 1.4 V.

$$VDD' = VDD \cdot S$$

$$L' = L \cdot S \quad W' = W \cdot S$$

Parameter	Scaling
Supply voltage ( $VDD$ )	$S$
Channel length ( $L_{min}$ )	$S$
Channel width ( $W_{min}$ )	$S$
Gate-oxide thickness ( $t_{ox}$ )	$S$
Substrate doping ( $N_A$ )	$S^{-1}$
On current ( $I_{on}$ )	$S$
Gate capacitance ( $C_{ox}$ )	$S$
Gate delay	$S$
Active power	$S^3$

- The main benefits of scaling are:
  - ❖ Smaller device sizes and thus reduced chip size (increased yield and more parts per wafer),
  - ❖ Lower gate delays, allowing higher frequency operation, and
  - ❖ Reduction in power dissipation.
- The above benefits comes in expense of several short-channel effects.

# Modeling MOSFET for Analog Design: Basics

- Mathematical Models for MOSFET are being discussed considering:
  - ❖ Long Channel MOSFETs: Following the square-law equation for the current
  - ❖ Short Channel MOSFET: Short Channel lengths (<1um)

Short Channel

Drain Current in Saturation Region:

$$I_D = W \cdot v_{sat} \cdot C'_{ox} \left( V_{GS} - V_{THN} - V_{DS,sat} \right)$$

Vary Linearly with  $V_{GS}$

Long Channel

Drain Current in Triode Region:

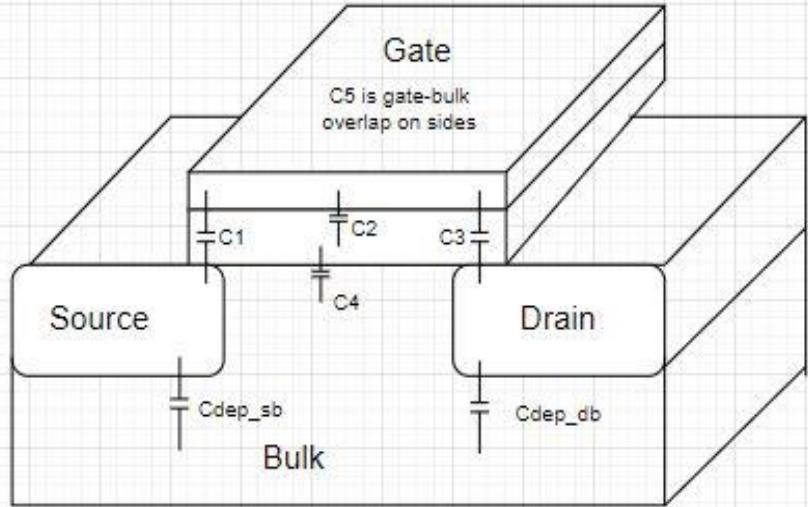
$$I_D = KP_n \cdot \frac{W}{L} \cdot \left[ (V_{GS} - V_{THN})V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Drain Current in Saturation Region:

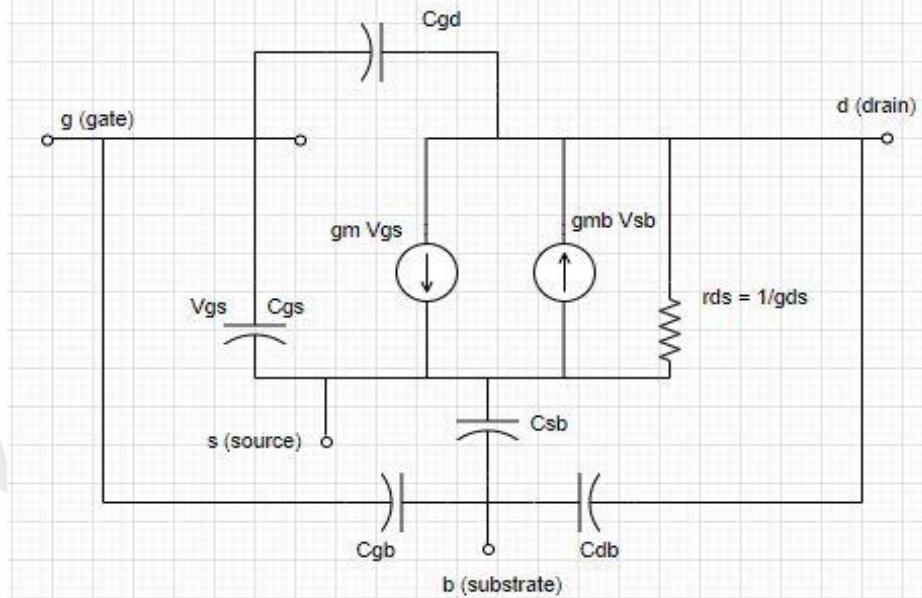
$$I_D = \frac{KP_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN})^2 \left[ 1 + \lambda (V_{DS} - V_{DS,sat}) \right]$$

Variation with  $V_{GS}$   
follows square law

# Modeling MOSFET for Analog Design: Capacitances (1/3)



$$L_{eff} = L_{drawn} - 2L_{diff} \quad W_{eff} = W_{drawn} - 2W_{diff}$$



- Each of the capacitances is a function of bias conditions (bias dependent). Hence changes with region of operation of MOSFET.
- Some of the capacitances are familiar from previous discussion:
  - **Accumulation region (When Device OFF)**  $C_1 = C_{gs}$ ,  $C_3 = C_{gd}$ ,  $C_{gb} = C_2 + 2C_5 = C_2 + CGBO * L$  where,  $CGBO$  (Capacitance due to oxide encroachment) &  $L$  is  $L_{drawn}$ .
    - ✓  $CGBO = C'_ox 2W_{enc}$ , Remember,  $C'_ox = \epsilon_{ox} / t_{ox}$ .
    - ✓  $CGDO$  is capacitance due to gate drain overlap,  $CGSO$  is capacitance due to **gate source overlap**. They are often used as SPICE parameters.
    - ✓  $CGDO = C'_ox L_{diff}$     $CGSO = C'_ox L_{diff}$     $\therefore C_1 = C_{gs} = CGSO * W_{eff}$ ,  $C_3 = C_{gd} = CGDO * W_{eff}$   
 $C_2 = C'_ox WL_{eff}$

# Modeling MOSFET for Analog Design: Capacitances (2/3)

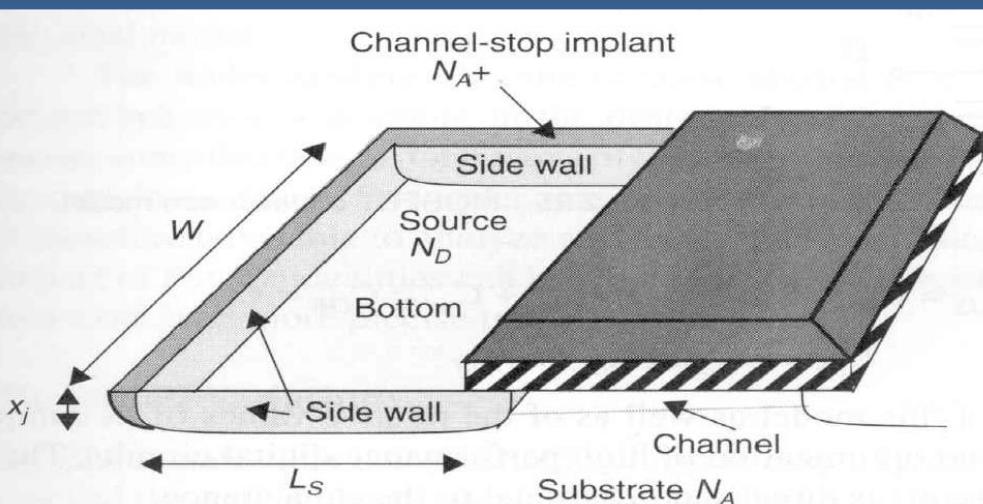
- The capacitance between source/drain and bulk (e.g.  $C_{sb}$  and  $C_{db}$ ) are simply depletion capacitance (formed due to depletion region in p-n junction under reverse bias).

$$C_j = \frac{A}{2} \sqrt{\frac{2q\epsilon}{V_0 - V} \frac{N_d N_a}{N_d + N_a}}$$

$$C_{j0} / \text{unit area} = C_j \Big|_{V=0} = \sqrt{\frac{q\epsilon}{2V_0} \frac{N_d N_a}{N_d + N_a}}$$

Where,  $C_{j0}$  is the depletion capacitance at 0 bias,  $\epsilon$  is permittivity ,  $V$  is voltage applied,  $V_0$  is the built-in potential or contact potential (a barrier potential at 0 bias). The m=0.5 for abrupt junction and 0.3 for graded junction.

$$C_j / \text{unit area} = \frac{C_{j0}}{(1 - V/V_0)^m}; V_0 = \frac{kT}{q} \ln \left( \frac{N_a N_d}{n_i^2} \right)$$



- Junction formed with substrate:
    - ✓ Bottom area =  $W * L_s$ ,  $L_s$  is length of the drain/source.
    - ✓ The capacitance  $C_{JA} = C_j * W * L_s$ .
  - Junction formed with sidewalls:
    - ✓ Perimeter ( $P$ ) =  $2L_s + W$
    - ✓ Area =  $P * x_j$ ,  $x_j$  is junction depth
    - ✓ The capacitance  $C_{JSW} = C_j * P * x_j$
  - Total Capacitance  $C = C_{JA} + C_{JSW}$
- Same in OFF, TRIODE & Saturation**

# Modeling MOSFET for Analog Design: Capacitances (2/3)

## ➤ Saturation region:

$$C_{gs} = \frac{2}{3}W * L * C_{ox}' + CGSO * W = \frac{2}{3}C_2 + C_1$$

$$C_{gb} = CGBO * L; C_{gd} = CGDO * W$$

*As given in slide 35 and calculated from charge stored in inversion region with an addition of Gate source overlap*

## ➤ Triode region: Channel spans from source to drain

$$C_{gs} = \frac{1}{2}W * L * C_{ox}' + CGSO * W = \frac{C_2}{2} + C_1$$

$$C_{gd} = \frac{1}{2}W * L * C_{ox}' + CGDO * W = \frac{C_2}{2} + C_1$$

$$C_{gb} = CGBO * L;$$

*Channel capacitance splits equally between source and drain. However overlap capacitances are added to them*

Summary of Capacitances

Name	Off	Triode	Saturation
$C_{gd}$	$CGDO \cdot W$	$\frac{1}{2} \cdot W \cdot L \cdot C_{ox}'$	$CGDO \cdot W$
$C_{db}$	$C_{jd}$	$C_{jd}$	$C_{jd}$
$C_{gb}$	$C_{ox}'WL_{eff} + CGBO \cdot L$	$CGBO \cdot L$	$CGBO \cdot L$
$C_{gs}$	$CGSO \cdot W$	$\frac{1}{2} \cdot W \cdot L \cdot C_{ox}'$	$\frac{2}{3} \cdot W \cdot L \cdot C_{ox}'$
$C_{sb}$	$C_{js}$	$C_{js}$	$C_{js}$

➤ The capacitances listed in table is same as above discussion where:

- ✓  $C_{js} = C_{JA} + C_{JSW}$  (Slide 44)
- ✓  $L_{eff} = L_{drawn} - 2L_{diff}$ ,  $L = L_{drawn}$
- ✓  $W_{eff} = W_{drawn} - 2W_{enc}$



# MOS Static Transistor Modelling

- The **computer-aided modelling** process for the MOS transistor.
- Most challenging problems with **modern process modelling** is to predict the behavior of transistors of **varying geometry** that are fabricated using a **small-feature size technology**.
- The **SPICE** program has formed the basis for modeling by a large number of universities and companies.
- It has too expensive for most companies to have their own fabrication facilities.

- There are **six** main **MOS models** that are worthy of attention:
  - The **Shichman-Hodges Model** (known as level 1 in SPICE).
  - The **SPICE Level 3 (semi empirical) model** – not used for deep submicron devices. i.e. below 350nm.
  - The **Berkeley BSIM 3/4 models** (released in 1997/2000, and updated every year)
  - The **HSPICE Models**
  - The **Phillips MOS 11 model**.
  - A New Model Developed for Analog Circuit Modelling called the **EKV(for Enz-Krummenacher-Vittoz) Model**

# The Shichman-Hodges Model for Heavy Inversion Operation

- Typically used for **long-channel devices** fabricated in larger feature size processes (for channel lengths and widths greater than, say **1 micrometer**).

$$I_D = \frac{KP_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN})^2 \left[ 1 + \lambda (V_{DS} - V_{DS,sat}) \right] \quad V_{DS} \geq V_{GS} - V_T$$

$$I_D = KP_n \cdot \frac{W}{L} \cdot \left[ (V_{GS} - V_{THN})V_{DS} - \frac{V_{DS}^2}{2} \right] \left[ 1 + \lambda (V_{DS} - V_{DS,sat}) \right] \quad V_{DS} < V_{GS} - V_T$$

Where

- $KP_n = \mu C_{OX} / 2$
- $V_{TH} = V_{TO} = \gamma (\sqrt{V_{SB}} + 0.6) - \sqrt{0.6}$
- $g_m \propto W \cdot V_{od} / L$
- $g_m / g_{ds} \propto \sqrt{I_D}$

- **$KP_n$**  and  $\gamma$  parameter are related to **fabrication process**. The **lambda** parameter is used to model the finite output conductance in the saturation region.
- It models, the **increase** in drain current with increasing drain-source voltage in saturation.



# The SPICE Level 3 Empirical Model

- Developed for **short and narrow channel** transistors with **channel widths and/or lengths down to 0.35 micrometers**.
- The **Level 3 model** account for:
  - **Substrate bias and short/narrow channel effects** on threshold voltage, including static feedback from the drain to the gate.
  - **Saturation** due to scattering limited drift velocity of carriers and finite voltage-dependent output conductance.
  - **Surface field-dependent** mobility
  - **Subthreshold** conduction
  - **Optional charge** conservation
  - **Optical impact ionization** modelling

Typical values shown are for a 0.5 micron CMOS Process

KEYWORD	Description	Units	Default	Typical
LEVEL	Model Level		3	3
DELTA	Width Effect on Threshold	-	0.0	0.691
ETA	Static Feedback	-	0.0	0.037
GAMMA	Bulk Threshold Parameter	V <sup>1/2</sup>	0.0	0.5976
KAPPA	Saturation Field Factor	-	0.2	0.029
KP	Transconductance Parameter	uA/V <sup>2</sup>	UO*COX	196
LD	Lateral Diffusion Along Length	m	0.0	0.047u
NSUB	Substrate Doping	1/cm <sup>3</sup>	0.0	1.39e17
PHI	Surface Potential	V	0.6	0.7
THETA	Mobility Modulation	V <sup>-1</sup>	0.0	0.268
THETAX	Mobility Modulation	cm/V	0.0	
TOX	Oxide Thickness	m	1.0e-07	9.6e-09
UO	Surface Mobility	cm <sup>2</sup> /V-sec	600	546.2
VMAX	Max. Carrier Drift Velocity	m/s	0.0	2.0e05
VTO	Zero-Bias Threshold Voltage	V	0.0	0.6566
WD	Lateral Diffusion Along Width	m	0.0	0.05u
XJ	Metallurgical Junction Depth	m	0.0	0.2u
XL	Mask/Etch Effect on L	m	0.0	
XW	Mask/Etch Effect on W	m	0.0	

- $I_D = \mu_{ef} C_{ox} W_{eff} / L_{eff} \cdot [V_{GS} - V_T - (1 + F_B) / 2 V_{DS}] \cdot V_{DS}$ , (Valid for  $V_{DS}$  up to  $V_{DS,sat}$ )
- $L_{eff} = L_{drawn} + XL - 2 LD$
- $W_{eff} = W_{drawn} = XW - 2 WD$



# The BSIM (Berkeley short channel IGFET model) Models

- Most widely used for **submicron MOS devices** is the BSIM model.
- The dependence of **mobility** upon the vertical field includes the **substrate voltage**.
- The **Threshold voltage** is modified for substrates with non uniform doping.
- The **current in strong and weak inversion regions** are derived such that their values and first derivatives are continuous.
- To simplify the **drain current** equations, **new expressions are devised for velocity saturation**, dependence of mobility upon the lateral field and the saturation voltage.



## Part 3: RFIC Passive Components

# Passive Components: Resistors

➤ Resistance of Planar Resistor:

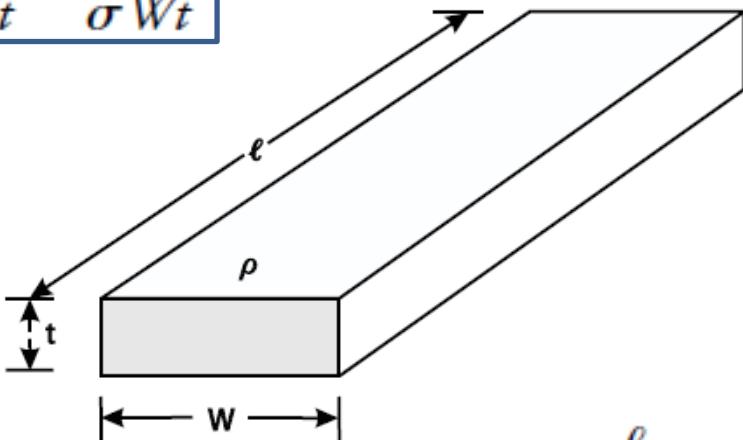
- $\rho$  is bulk resistivity in  $\Omega\text{-m}$
- $\sigma$  is bulk conductivity in  $\text{S/m}$

$$R = \rho \frac{\ell}{A} = \rho \frac{\ell}{Wt} = \frac{\ell}{\sigma Wt}$$

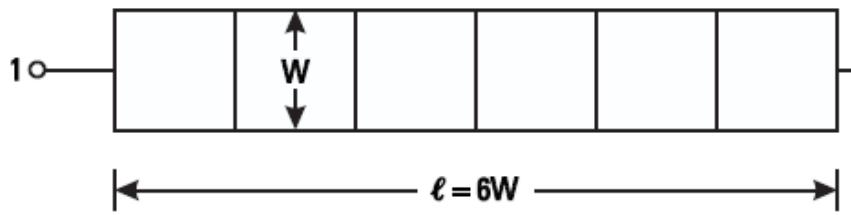
➤ Alternatively,  $R$  can be calculated in terms of **sheet resistance  $R_{Square}$  (ohms/square)** of resistive film (for given thickness  $t$ )  
 (Since  $t$  is constant in process)

$$R = R_{square} \frac{L}{W} \quad \text{where}$$

$$R_{square} = \frac{\rho}{t} = \frac{1}{\sigma t}$$



$$R = R_s \frac{\ell}{W}$$

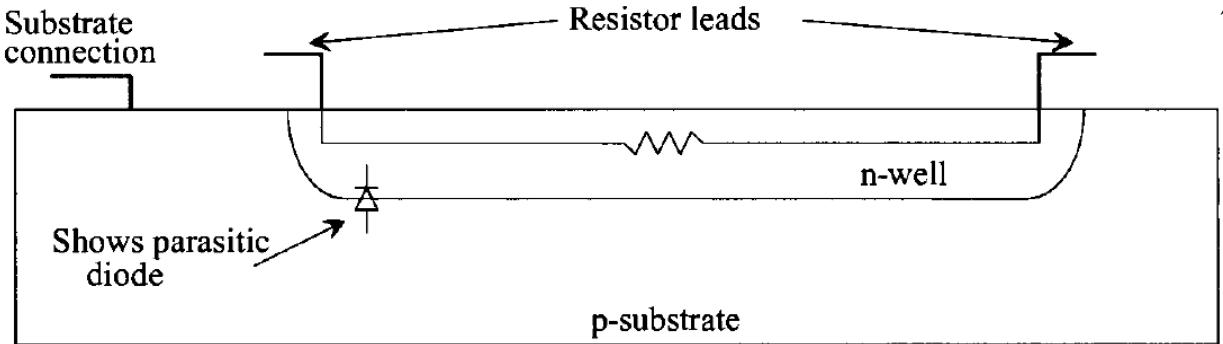


There are 6 squares between terminals 1 and 2. If  $R_s = 10 \Omega/\text{sq.}$ , then  $R = 60\Omega$ .

➤ To increase resistance, the metallization square should be kept more. E.g. a line of width 50  $\mu\text{m}$  & 1,000  $\mu\text{m}$  long has 2.5 times less resistance than a line of width 20  $\mu\text{m}$  that is also 1,000  $\mu\text{m}$  long.

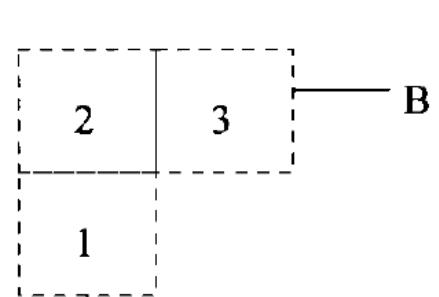
# Passive Components: Resistors in CMOS

- N-Well are mostly used to create resistors in CMOS process in addition to their main operation of providing substrate for P-MOS transistors.
- The voltage on either side of the resistor must be large enough to keep the substrate/well diode from forward biasing.

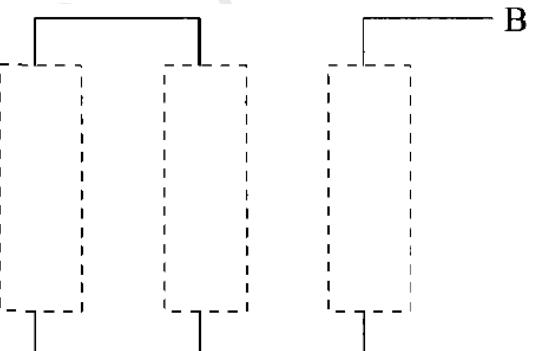


- Parasitic Diode: The substrate is tied to the lowest voltage in the circuit (generally, grounded) ensuring no current flows in the substrate (diode).

The layout of resistors is often set in Meandered to save space.



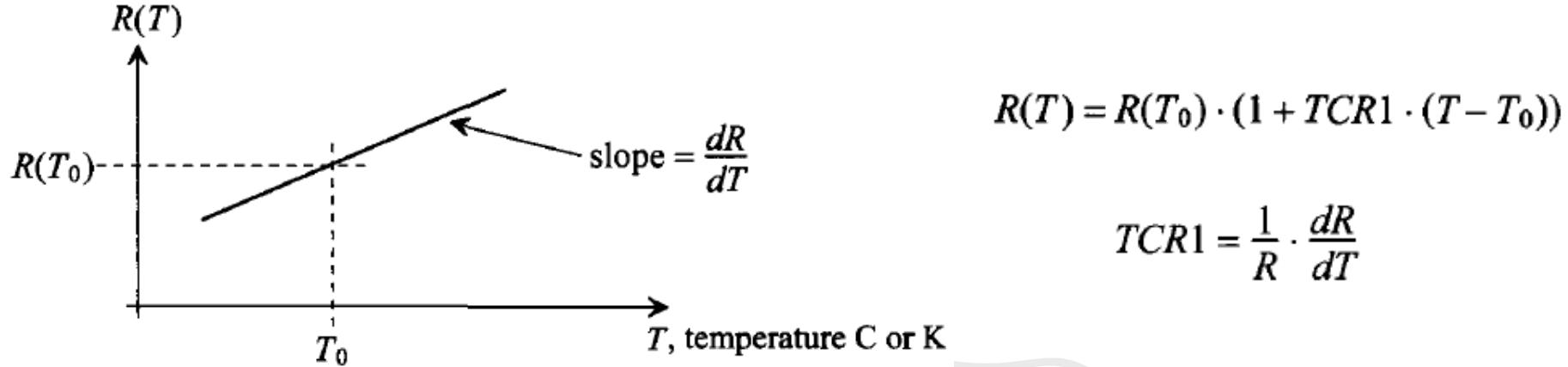
Here the corner (block 2) is not considered square.  $R_2 \approx 0.6R_{\text{square}}$ ,  $R_{AB} = 2.6R_{\text{square}}$



Avoiding Corners

# Resistors in CMOS: Variation with Temperature (1/2)

- The value of resistors in a CMOS process change with temperature.
- This change is as ppm/ $^{\circ}\text{C}$  (parts per million/  $^{\circ}\text{C}$ ) equivalent to a multiplier of  $10^{-6}/^{\circ}\text{C}$ .



SPICE uses a quadratic relation rather than the above linear relation

$$R(T) = R(T_0) \cdot [1 + TCR1 \cdot (T - T_0) + TCR2 \cdot (T - T_0)^2]$$

*As temperature increases, electron concentration in an n-well increase (exponentially increasing thermally generated carriers), Yet Resistance Increases???*

- Increased Carrier concentration results in reduction in carrier mobility (More carrier interactions result in reduced av. distance a carrier travels before the collision)

$$\therefore \rho = 1/q(\mu_n n + \mu_p n)$$

If the increase in carrier concentration with temperature > rate of mobility is dropping, a negative TCR is seen.

## Resistors in CMOS: Variation with Temperature (2/2)

➤ **Book Example:** Considering n-well resistor sheet resistance is approximately 500 Ω/square (at 27 °C), estimate the minimum and maximum resistance of an n-well resistor with a length of 100 and a width of 5 over a temperature of 0 and 100 °C.

**Solution:** There are 20 squares (of 5 widths) in 100 lengths, The  $R_0=10 \text{ K}\Omega$  (at 27 °C).

The TCR=0.0024

$$R_{\min} = 10,000 \cdot [1 + 0.0024 \cdot (0 - 27)] = 9.35 \text{ k}\Omega$$

$$R_{\max} = 10,000 \cdot [1 + 0.0024 \cdot (100 - 27)] = 11.75 \text{ k}\Omega$$

# Resistors in CMOS: Variation with Voltage (1/2)

- The value of resistors in a CMOS process change with voltage.
- This change is as ppm/ $^{\circ}\text{C}$  (parts per million/  $^{\circ}\text{C}$ ) equivalent to a multiplier of  $10^{-6}/^{\circ}\text{C}$ .

$$R(V) = R(V_0) \cdot (1 + VCR1 \cdot (V - V_0) + VCR2 \cdot (V - V_0)^2)$$

$$VCR = \frac{1}{R} \cdot \frac{dR}{dV}$$

$V$  is the average voltage applied to the resistor.

$$V = \frac{V_1 + V_2}{2}$$

- Consider  $VCR2 = 0$  for hand calculations. The value  $R(V_0)$  is the value of the resistor at the voltage  $V_0$ .
- A typical value of  $VCR1$  is 8000 ppm/V for an n-well resistor.
- The main contributor to the voltage coefficient is the depletion layer width between the n-well and the p-substrate.
- With increased av. voltage, the depletion layer extends into the n-well, resulting in a decrease in the thickness of the n-well available to conduct current.
- The thickness of the n-well available to conduct current decreases with increasing potential (reverse bias) between the n-well and the substrate.

## Resistors in CMOS: Variation with Voltage (2/2)

➤ **Book Example:** Considering n-well resistor sheet resistance is approximately 500 Ω/square (at 27 °C), estimate the average value of resistance of an n-well resistor with a length of 200 and a width of 10 at 27 °C.

**Solution:** There are 20 squares (of 10 widths) in 200 lengths, The  $R_0=10\text{ K}\Omega$  (at 27 °C).

➤ **Book Example:** Estimate the average resistance of the above resistor, for an average voltage across the resistor of 0, 5, and 10 V.

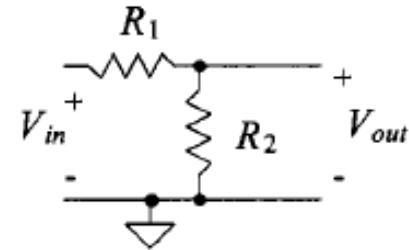
$$R(0) = 10,000 \cdot (1 + 0.008 \cdot 0) = 10\text{ k}\Omega$$

$$R(5) = 10,000 \cdot (1 + 0.008 \cdot 5) = 10.4\text{ k}\Omega$$

$$R(10) = 10,000 \cdot (1 + 0.008 \cdot 10) = 10.8\text{ k}\Omega$$

- This is a small change as compared to the change due to temperature.
- However, in the next slide, we can see this small change due to the applied voltage having a greater impact on the circuit performance than the temperature.

# Resistors in CMOS: Variation with Temperature vs Voltage



$$V_{out} = V_{in} \cdot \frac{R2(T)}{R1(T) + R2(T)} = V_{in} \cdot \frac{R2 \cdot [1 + TCR(T - T_0)]}{(R1 + R2) \cdot [1 + TCR(T - T_0)]} = V_{in} \cdot \left[ \frac{R2}{R1 + R2} \right]$$

The output voltage in the divider is independent of temperature

$$V_{out} = V_{in} \cdot \frac{R2(V)}{R1(V) + R2(V)} = V_{in} \cdot \frac{R2 \cdot (1 + VCR \cdot V_2)}{R1 \cdot (1 + VCR \cdot V_1) + R2 \cdot (1 + VCR \cdot V_2)}$$

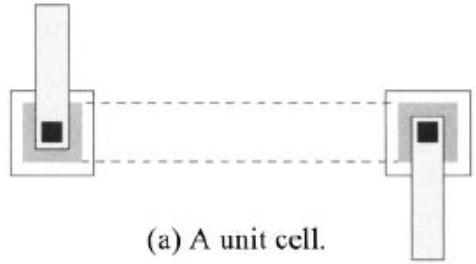
The output voltage in the divider is dependent of voltage variation

This is because the voltage across each resistor is different.

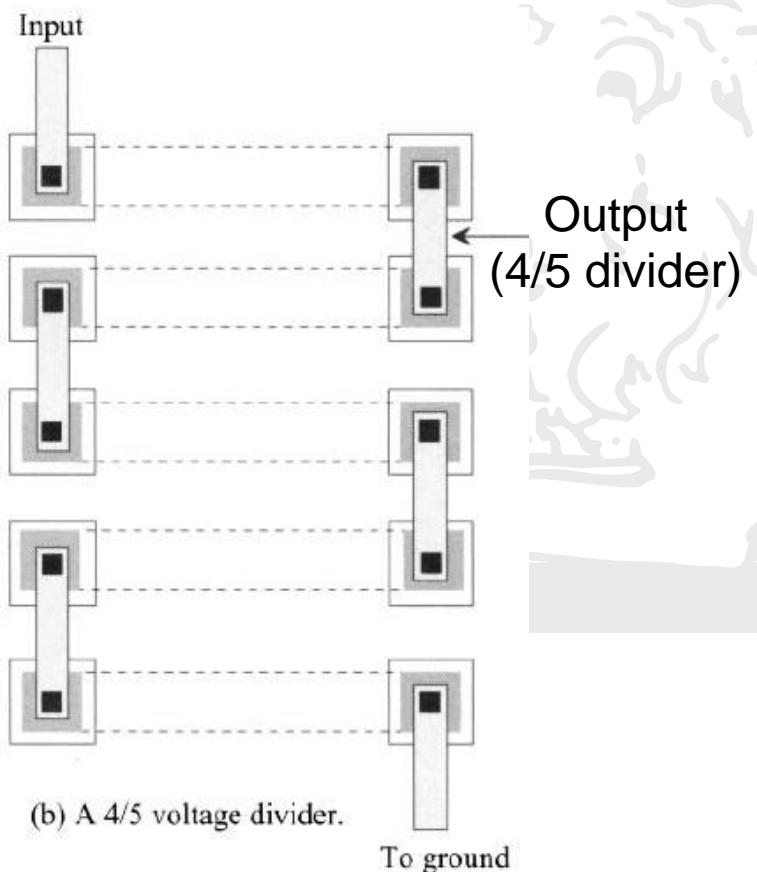
$$V_1 = \frac{V_{in} + V_{out}}{2}$$

$$V_2 = \frac{V_{out}}{2}$$

# Resistors in CMOS: Resistors Using Unit Cells



(a) A unit cell.

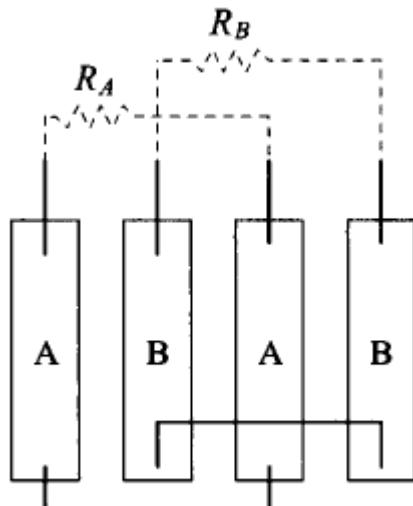


- Usually, a *unit resistor* is laid out with some nominal resistance. Eg. 5K.
- The errors due to corners in meandering are eliminated
- 5k unit cell resistor implements a 4/5 voltage divider with the resistor  $R_1$  is 5k and the resistor  $R_2$  is 20k (layout of the 20k resistor is 4 unit cells).
- Changes in the nominal resistance value due to process shifts, temperature, or how the number of squares is calculated only affect the current flowing in the divider (the power dissipation) and not the output voltage.

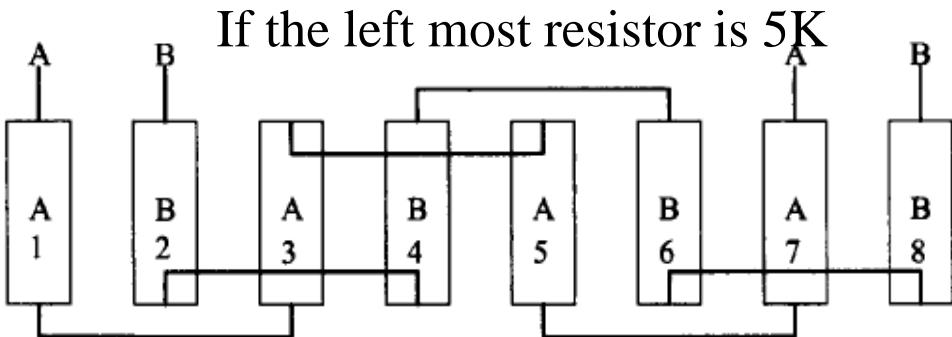
# Resistors in CMOS: Variation with Process Gradients & Mitigation

Process gradients are typically changes in the n-well, n+, or p+ doping at different places on the die.

## Interdigitated Resistors



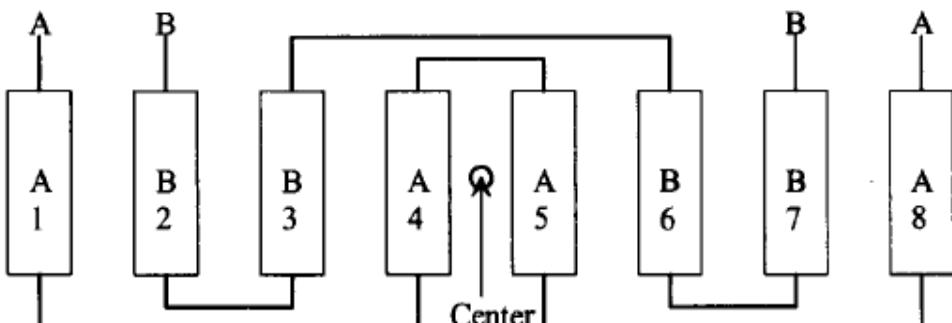
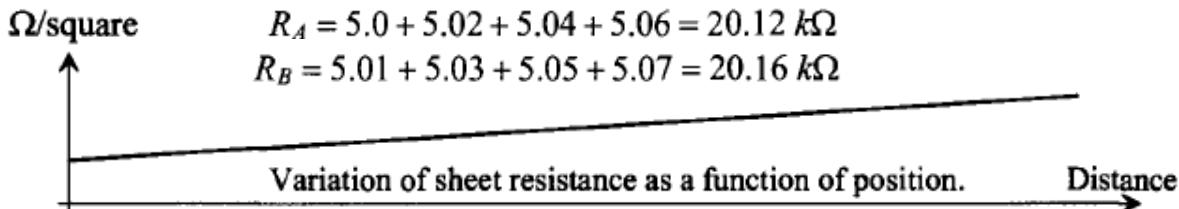
Process gradients are spread between the two resistors more evenly.



(a) Interdigitated layout

$$R_A = 5.0 + 5.02 + 5.04 + 5.06 = 20.12 \text{ k}\Omega$$

$$R_B = 5.01 + 5.03 + 5.05 + 5.07 = 20.16 \text{ k}\Omega$$

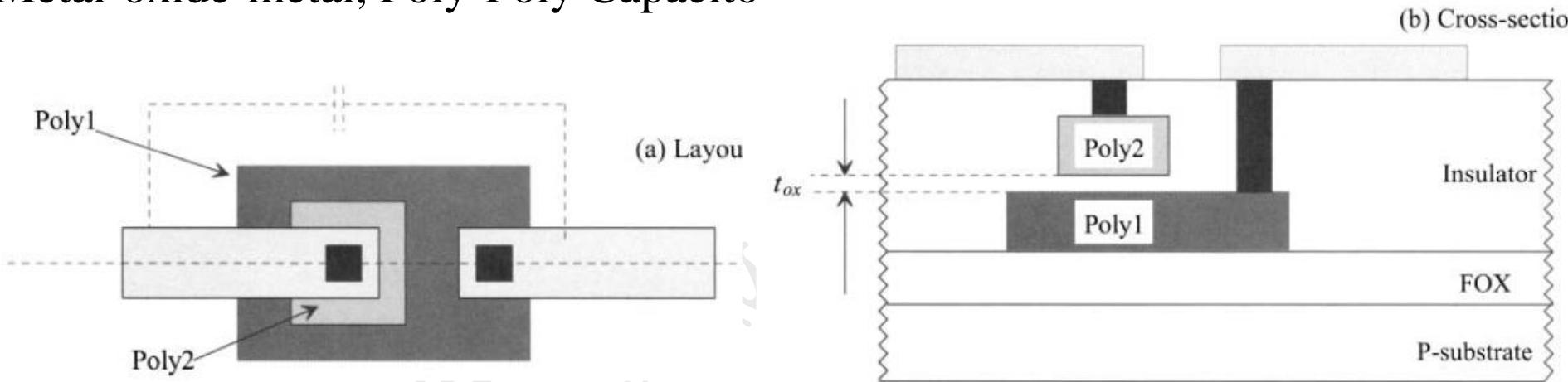


$$R_A = 5.0 + 5.03 + 5.04 + 5.07 = 20.14 \text{ k}\Omega \quad R_B = 5.01 + 5.02 + 5.05 + 5.06 = 20.14 \text{ k}\Omega$$

(b) Common-centroid layout

# Passive Components: Capacitors

➤ Many Capacitors are Available in the CMOS process: Metal-Insulator Metal, Metal-oxide-metal, Poly-Poly Capacitors



$$C_{ox} = C'_{ox} A$$

$$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{\epsilon_r \epsilon_0}{t_{ox}}$$

➤ Including Scaling Factor: 50 nm for the short channel, 1 um for Long Channel  $C_{ox} = C'_{ox} A (scale)^2$

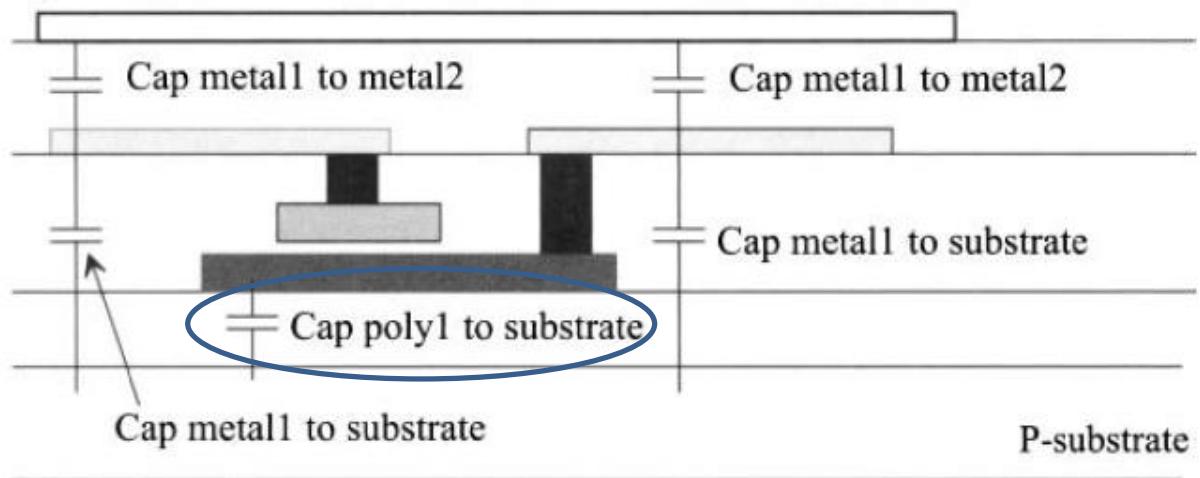
If, in the 50 nm process, a poly-poly capacitor is formed with an intersection of the poly1 and poly2 that measures 10 by 20 then the capacitor's value is

$$C = C_{ox} = 25 \text{ fF}/\mu\text{m}^2 \cdot 200 \cdot (0.05 \mu\text{m})^2 = 12.5 \text{ fF}$$

CMOS technology	Oxide thickness, $t_{ox}$	$C'_{ox}$
1 μm (long channel)	200 Å	1.75 fF/μm <sup>2</sup>
50 nm (short channel)	14 Å	25 fF/μm <sup>2</sup>

# Passive Components: Poly-Poly Capacitor

## ➤ Parasitic in Poly-Poly Capacitors



➤ The most important (largest) parasitic is the capacitance from poly 1 to substrate. Often called the bottom plate parasitic capacitance.

## ➤ Temperature Coefficient (TCC)

$$TCC = \frac{1}{C} \cdot \frac{dC}{dT}$$

$$C(T) = C(T_0) \cdot [1 + TCC \cdot (T - T_0)]$$

## ➤ Voltage Coefficient

$$VCC = \frac{1}{C} \cdot \frac{dC}{dV}$$

$$C(V) = C(V_0) \cdot (1 + VCC \cdot V)$$

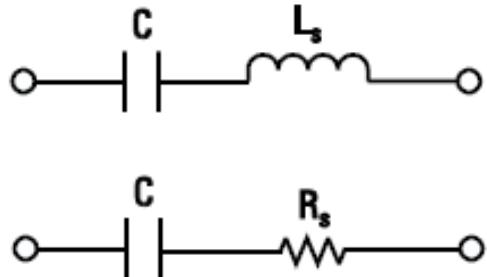
# Passive Components: Capacitors

## ➤ Series Representation of Capacitors

$$Z_c = j \left[ \omega L_s - \frac{1}{\omega C} \right] = -\frac{j}{\omega C} [1 - \omega^2 L_s C] \Rightarrow Z_c = -\frac{j}{\omega C_e}$$

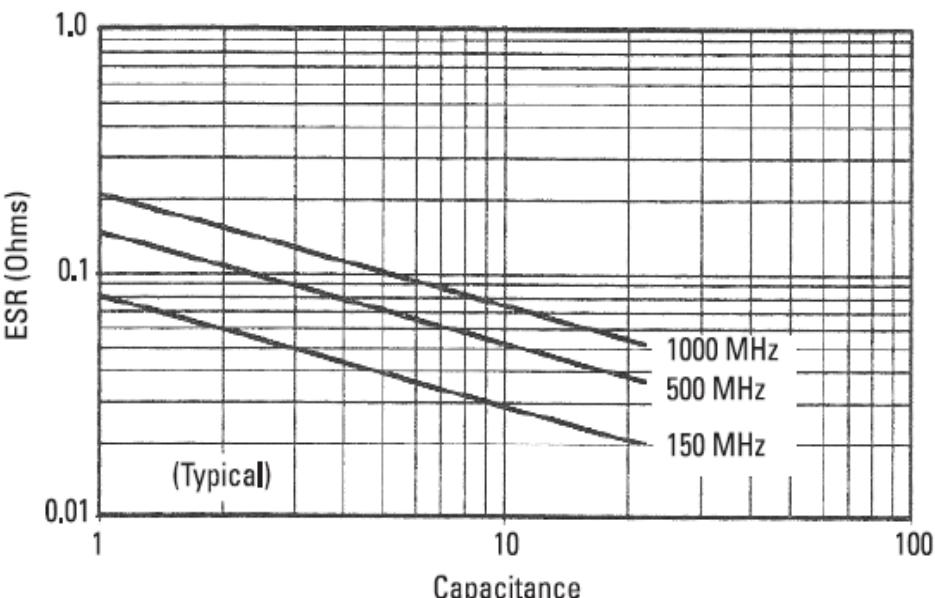
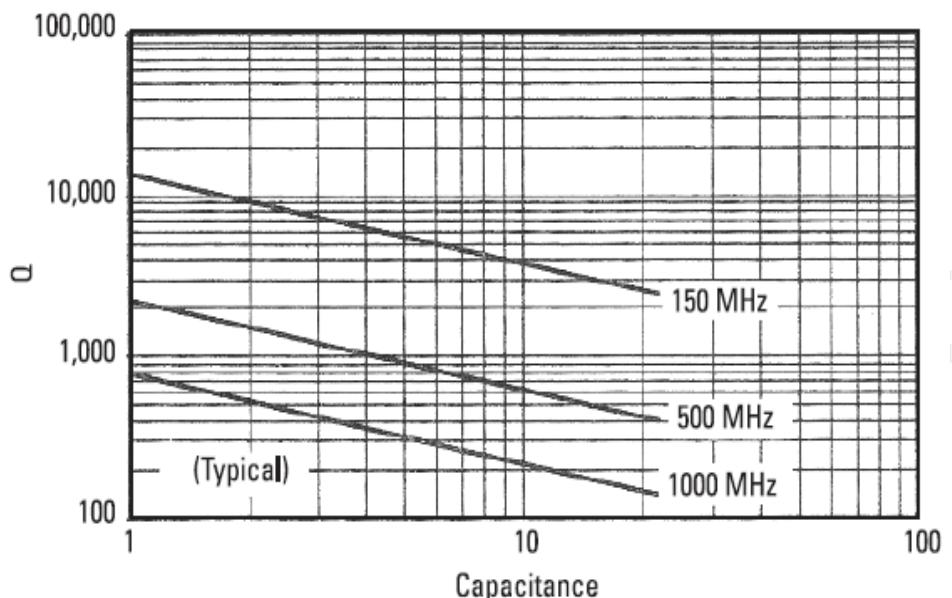
where,  $C_e = C[1 - \omega^2 L_s C]^{-1} = C[1 - (\omega/\omega_s)^2]^{-1}$

$$\omega_s = \frac{1}{\sqrt{L_s C}}; \text{series resonant frequency}$$



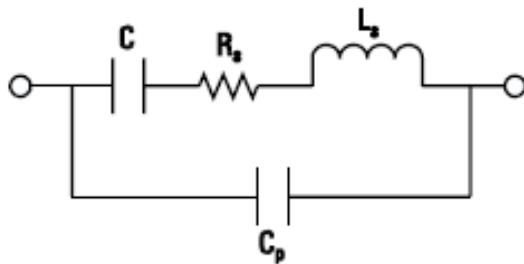
$$Q = \frac{1}{\omega C R_s} = \frac{1}{2\pi f C R_s}$$

$R_s$  is equivalent series resistance



# Passive Components: Capacitors with Parallel Resonance

- In addition to Series Resonance Capacitors also have Parallel resonance (unlike Inductors)
- After series resonance frequency, the capacitor works as inductor and after that first parallel resonance frequency appears, where the capacitor's total reactance again capacitive after the first parallel resonance frequency.



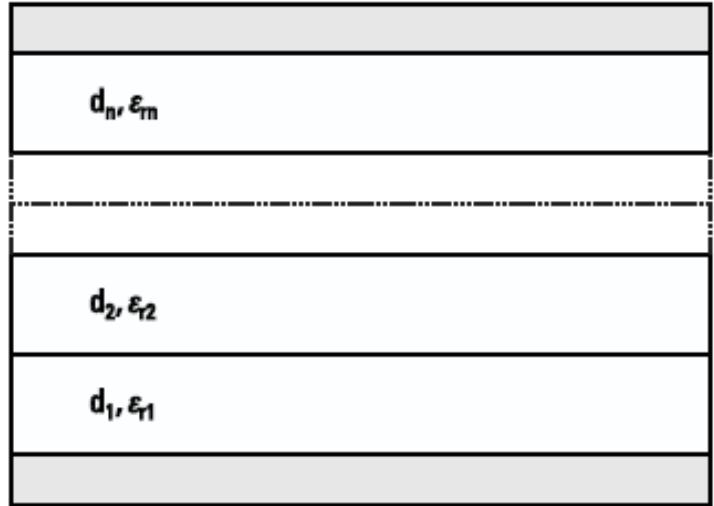
$$Z_c = \frac{1}{j\omega C_p + \left( R_s + j\omega L_s + \frac{1}{j\omega C} \right)^{-1}}$$

$$R_p = \frac{1}{R_s(\omega_p C_p)^2}$$

- When  $C \gg C_p$ , at *series resonant frequency (SRF),  $f_s$* , the reactances of **series elements  $C$  and  $L_s$  become equal** the capacitor's impedance is equal to resistor  $R_s$ .
- As the frequency increases beyond  $f_s$ , the reactance of the capacitance becomes very small, and the reactances of the **parallel elements  $L_s$  and  $C_p$  become equal**.
- At PRF,  $R_p$  is infinite when  $R_s = 0$ .

# Passive Components: Chip Capacitors

## Multilayer Capacitor

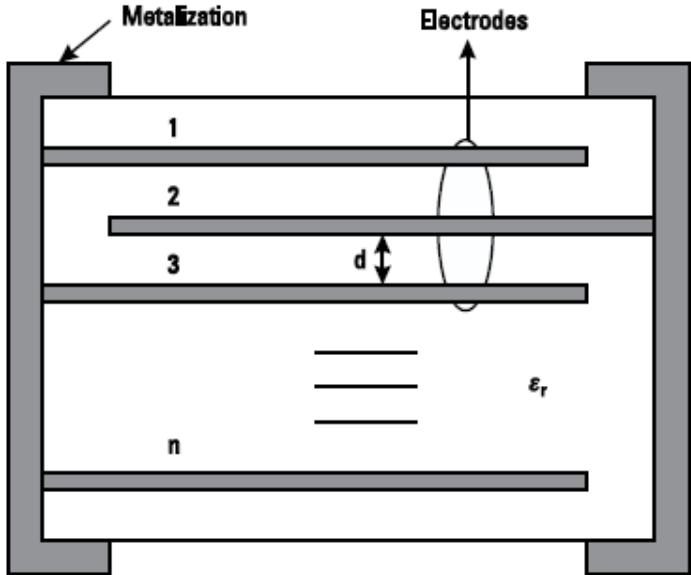


$$\epsilon_{req} = \left[ \sum_{m=1}^n \frac{d_m}{d_T \epsilon_{rm}} \right] \quad d_T = d_1 + d_2 + \dots + d_n$$

- $d_m$  is the thickness and  $\epsilon_{rm}$  is the dielectric constant of the  $m^{\text{th}}$  layer, and  $d_T$  is the total thickness.

$$C = 8.854 \times 10^{-6} \epsilon_{req} \frac{A}{d} \quad (\text{pF})$$

## Multiplate Capacitor

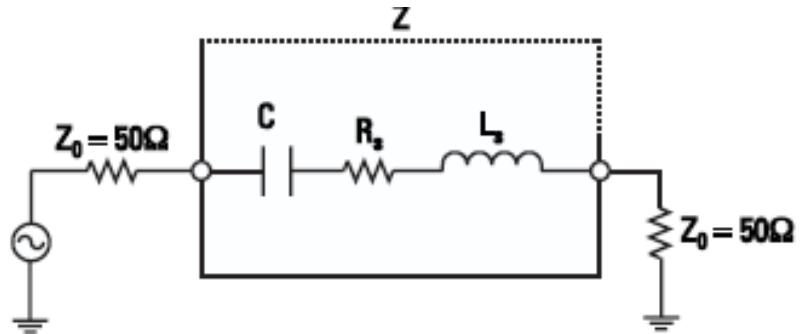
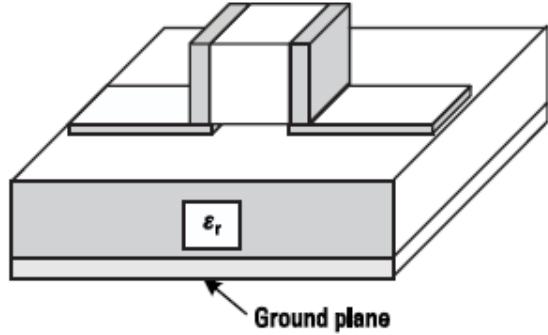


$$C = 8.854 \times 10^{-6} \frac{\epsilon_r A (n - 1)}{d} \quad (\text{pF})$$

**A and d are in square microns and microns, respectively in both the expressions of C**

# Passive Components: Measurement-Based Capacitor Model

## ➤ Series Representation of Capacitors



$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \frac{1}{Z + 2Z_0} \begin{bmatrix} Z & 2Z_0 \\ 2Z_0 & Z_0 \end{bmatrix}$$

$$\frac{R_s + j\omega L_s - \frac{j}{\omega C} + 2Z_0}{2Z_0} = \frac{S_{21r} - jS_{21i}}{S_{21r}^2 + S_{21i}^2}$$

- Comparing real and imaginary components in each side:

$$R_s = 2Z_0 \left[ \frac{S_{21r}}{S_{21r}^2 + S_{21i}^2} - 1 \right]$$

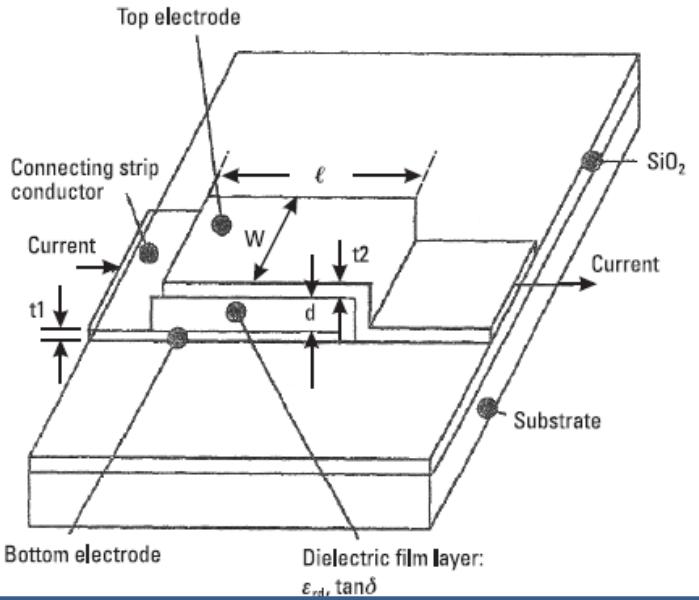
$$\frac{1}{\omega C} - \omega L_s = \frac{2Z_0 S_{21i}}{S_{21r}^2 + S_{21i}^2}$$

- At Series Resonance:  $\angle S_{21} = 0$

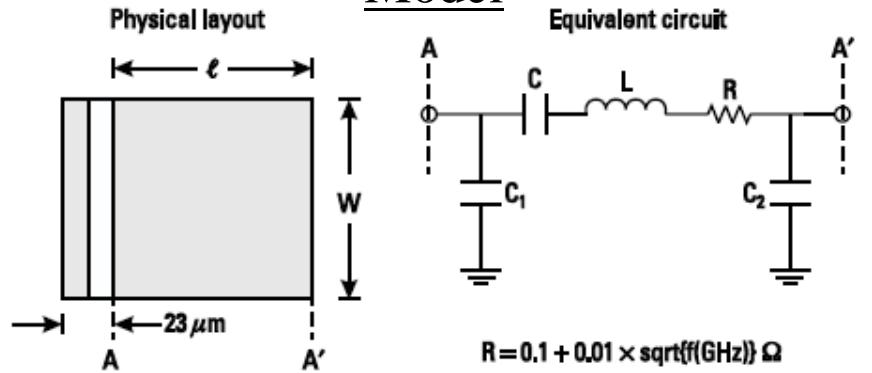
$$L_s = \frac{1}{C \omega_s^2}$$

$$C = \left[ 1 - \frac{\omega^2}{\omega_s^2} \right] \frac{S_{21r}^2 + S_{21i}^2}{2\omega Z_0 S_{21i}}$$

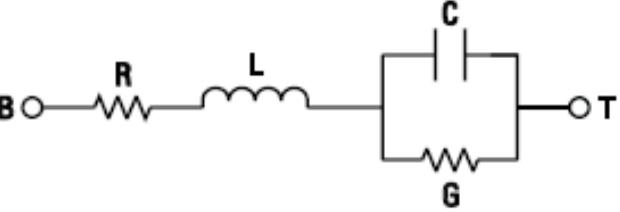
# Passive Components: MIM Capacitor



## Coupled Microstrip-based Distributed Model



Model extracted from meas. 2-port s-parameter



$$C = \epsilon_0 \epsilon_{rd} \frac{W\ell}{d} = \frac{\epsilon_{rd} 10^{-15}}{36\pi} \frac{W\ell}{d} \text{ (F)} \quad R = \frac{2}{3} \frac{R_s}{W} \ell$$

$$G = \omega C \tan \delta = \frac{1}{18} \epsilon_{rd} f \frac{W\ell}{d} \times 10^{-6} \tan \delta \text{ (mho)}$$

$$Q_c = \frac{1}{\omega RC} = \frac{3W}{2\pi f 2R_s \ell C} = \frac{27 \times 10^6 d}{f R_s \ell^2 \epsilon_r}$$

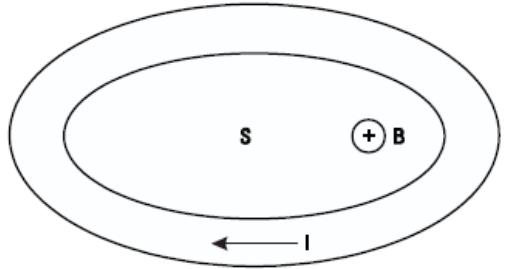
The Q factor associated with dielectric loss:

$$Q_d = \frac{1}{\tan \delta}$$

The total quality factor  $Q_T$ :

$$Q_T = \left[ \frac{1}{Q_c} + \frac{1}{Q_d} \right]^{-1}$$

# Passive Components: Inductor



## Self Inductance

$$L = \frac{1}{I} \oint_S B \cdot d\mathbf{s} = \frac{\Psi}{I}$$

$$= \mu_0 \mu_r \frac{1}{I} \oint_{\ell} H \cdot d\mathbf{l}$$

- Where,  $I$  is the current flowing through the conductor in  $A$ ,
- $B$  is magnetic flux density in tesla (T) or weber/m<sup>2</sup> ,
- $H$  is the magnetic field,  $H$  is expressed in A/m,
- $S$  = surface area enclosed by the loop of wire of length ,.

- For perfect conductors  $\mu r = 1$ . Free-space permeability is  $\mu_0 = 4\pi \times 10^{-7}$  H/m.

The change in inductance due to current flowing in another conductor in proximity is known as their **Mutual Inductance**. The total inductance of each conductor:

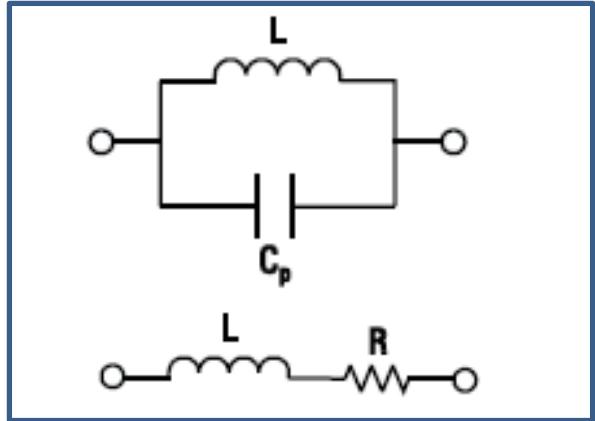
$$L_t = L + M \quad (\text{currents flow in the same direction})$$

$$= L - M \quad (\text{currents flow in the opposite direction})$$

# Passive Components: Inductors Equivalent Circuits

## ➤ Series Representation of Capacitors

$$Z_i = \frac{j\omega L \times \frac{1}{j\omega C_p}}{j\omega L + \frac{1}{j\omega C_p}} = \frac{j\omega L}{1 - \omega^2 LC_p} \Rightarrow Z_i = j\omega L_e$$



where,  $L_e = \frac{L}{1 - \left(\frac{\omega}{\omega_p}\right)^2}$

$$\omega_p = \frac{1}{\sqrt{LC_p}}; \text{ parallel resonant frequency}$$

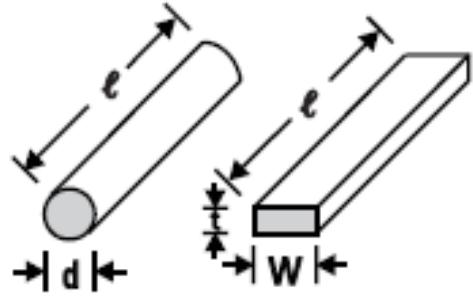
or self resonance frequency

$$Q = \frac{\omega W_S}{P_D} \Rightarrow$$

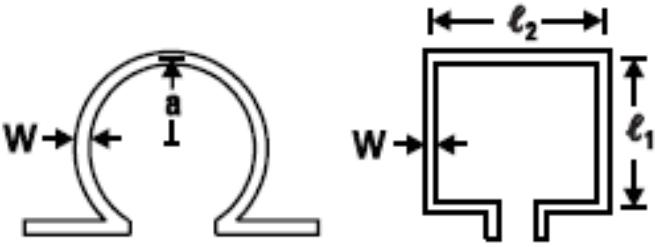
$$Q = \frac{\frac{1}{2} \omega^2 L i_0^2}{\frac{1}{2} R i_0^2} = \frac{\omega L}{R}$$

➤  $W_S$  is the energy stored and  $P_D$  is the power dissipated in the inductor per cycle

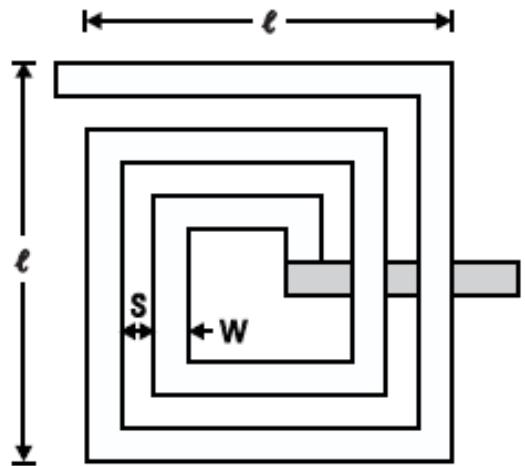
# Passive Components: Inductor Configurations



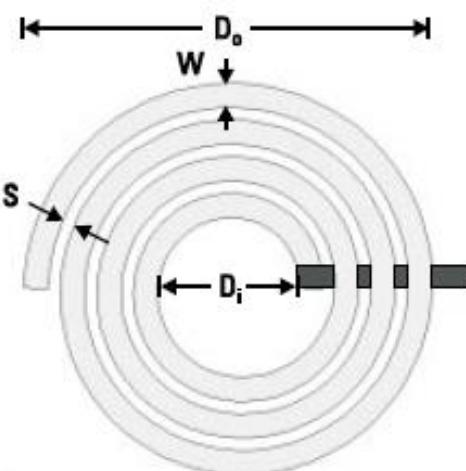
*Bond Wire or Strip*



*Loop: Circular and Rectangular*



*Spiral: Rectangular*

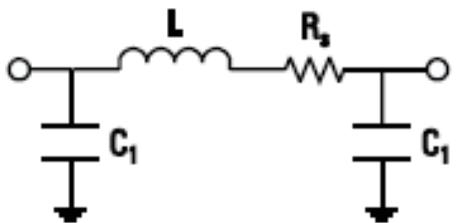


*Spiral: Circular*

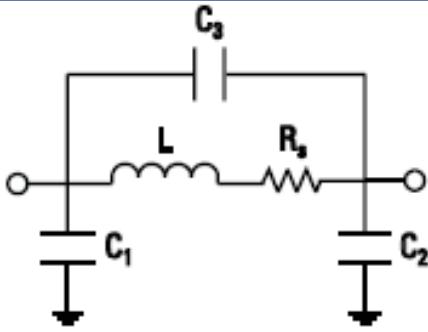
# Passive Components: Inductor Models

- There are many methods of Inductor Modeling: Lumped Element, microstrip coupled line, Mutual Inductance and Measurement-based

**Analytical:**

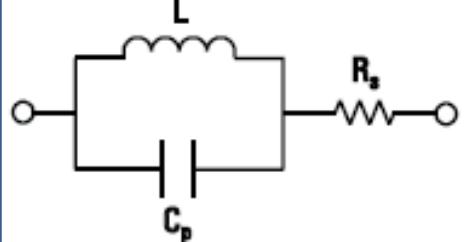


*Microstrip & Loop*



*Spiral or Coil*

**Measurement:**



$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \frac{1}{Z + 2Z_0} \begin{bmatrix} Z & 2Z_0 \\ 2Z_0 & Z_0 \end{bmatrix}$$

$$S_{21} = \frac{2Z_0}{Z + 2Z_0}$$

$$Z = R_s + \frac{j\omega L}{[1 - (\omega/\omega_p)^2]}$$

Where,

Comparing Real and Imaginary part of S21

$$R_s = 2Z_0 \left[ \frac{S_{21r}}{S_{21r}^2 + S_{21i}^2} - 1 \right] \quad L = \frac{2Z_0 S_{21i}}{S_{21r}^2 + S_{21i}^2} \frac{1 - (\omega/\omega_p)^2}{\omega} \quad \omega_p^2 = 1/LC_p$$

# Passive Components: Inductor on Si Substrate (Conductor losses) (1/2)

- One key problem with Inductor on Si substrate is high substrate losses due to low substrate resistivity of Si ( $10^3 \Omega\text{-cm}$ )
- Consequently, the Q factor of spiral inductors and T.Ls on Si substrate is less than GaAs substrate (resistivity  $10^7 \Omega\text{-cm}$ ).
- The Q factor depends on losses: Conductor Losses & Substrate Losses
- Conductor Losses: Proportional to its series resistance.

## ➤ Sheet Resistance:

- This series resistance can be calculated from the conductor sheet resistance multiplied by the number of squares of the conductor (same as resistor). **Can be reduced if thickness  $t$  is increased.**

$$R_{dc} = \frac{\ell}{Wt\sigma}$$

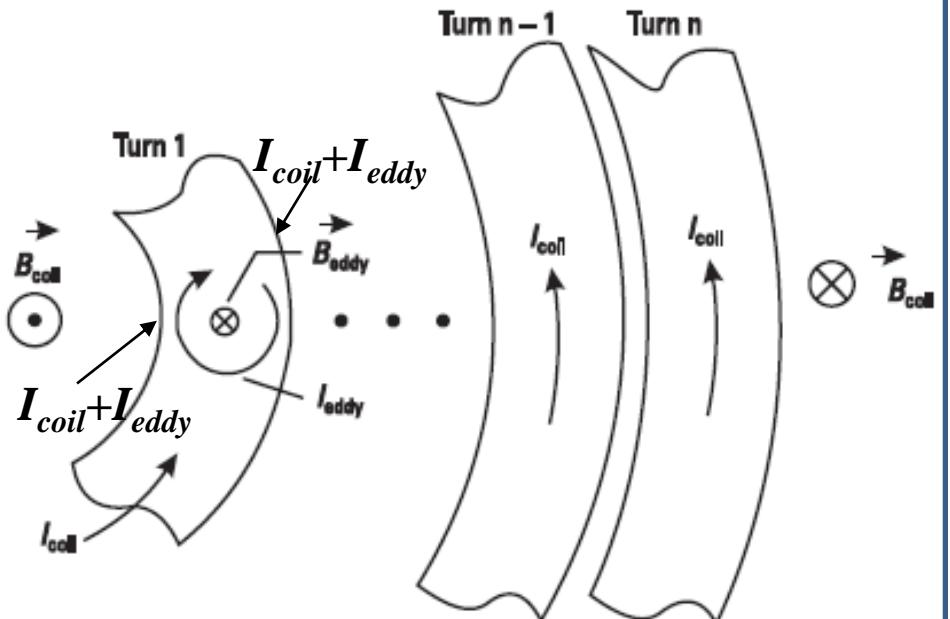
- At RF frequency, the thickness is calculated from skin-depth

$$R_{rf} = \frac{\ell}{W\sigma\delta(1 - e^{-t/\delta})} \quad \delta = \sqrt{\frac{2}{\omega\mu\sigma}}$$

**High Series resistance at higher frequencies is mainly due to eddy currents.**

# Passive Components: Inductor on Si Substrate (Conductor losses) (2/2)

- Conductor Losses Continued .....
- Other than sheet resistance there are **Eddy Current Resistance** associated in the inductor.



**Non Uniform Current Density  $\equiv$  Larger Effective resistance**

$$R_s = R_{dc} [1 + 0.1(f/f_c)^2] \quad f_c = \frac{3.1(W+S)}{2\pi\mu_0 W^2} R_{sh}$$

At  $f_c$  the current crowding become significant

- Eddy current an unwanted current induced in solid metal rather than coil in time varying magnetic field. E.g. in Transformer cores.
- The inductor carries a current  $I_{coil}$  and the associated magnetic flux is  $B_{coil}$  which enter the page plane at the far end and come out of the page plane in the center of the coil, where they have maximum intensity.
- Due to small hollow space in the center of the coil, significant magnetic flux also goes through the inner turns.
- As per Faraday law, **an induced eddy current in the inner turns**

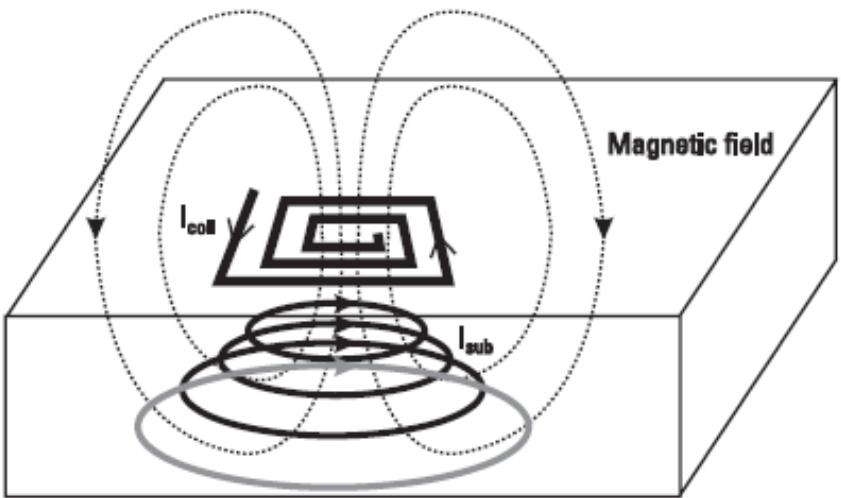


# Passive Components: Inductor on Si Substrate (Substrate losses) (1/2)

- The substrate loss consists of : Capacitive & Magnetic
- Capacitive Losses:
  - Finite resistance due to electrically induced conductive and displacement currents.
- When a coil is excited, **voltage difference occurs between the conductor and the grounded substrate** giving rise to **capacitive coupling** between the conductors.
- When the substrate has finite and low resistivity, **finite ohmic loss takes place, depending on the resistivity of the substrate.**
- Since this loss is **coupled through the shunt capacitance**, also referred to as capacitive or electric substrate loss.
- Finite resistivity loss can be minimized by either **using very high resistivity substrates or by placing a shield between the oxide layer and the substrate.**

# Passive Components: Inductor on Si Substrate (Substrate losses) (2/2)

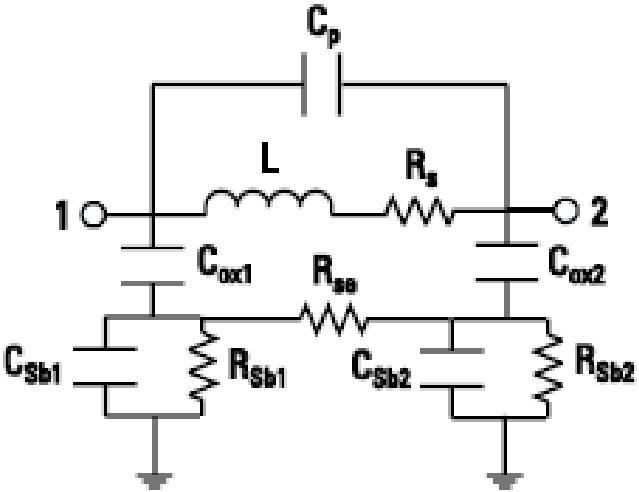
- The substrate loss consists of : Capacitive & Magnetic
- Magnetic Losses:
  - Magnetically induced Eddy Current Resistance.



**Magnetic field flux lines associated with the coil excitation current uniformly surround the inductor and penetrate into the substrate.**

- loops of eddy currents  $I_{\text{sub}}$  flow in the low-resistivity substrate underneath the coil with higher current density closer to the coil.
- The direction of  $I_{\text{sub}}$  is opposite to the direction of  $I_{\text{coil}}$ , giving rise to extra substrate loss.
- Since this loss is associated with magnetic fields, it is commonly referred to as *magnetic* or *inductive substrate loss*.
- Substrates with high resistivity have negligible magnetic losses.

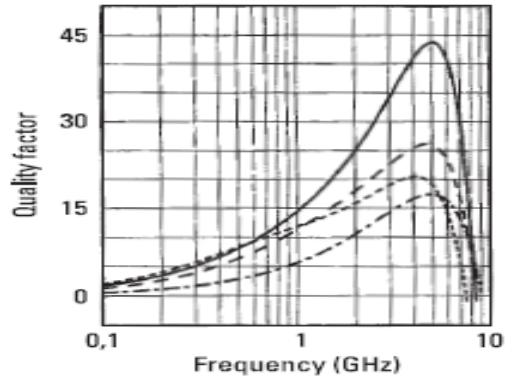
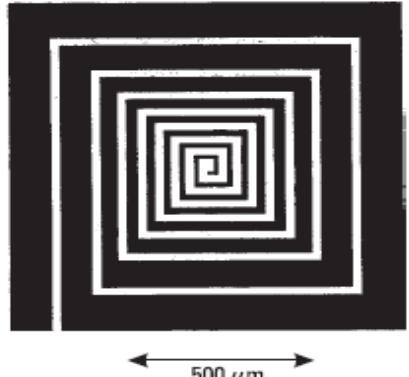
# Passive Components: Inductor Model on Si Substrate



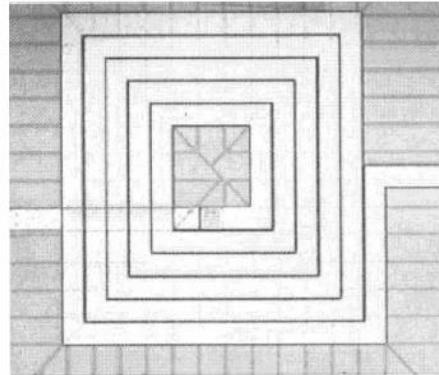
- $R_s$ : Series resistance of the inductor metal (including loops sheet resistance due to eddy currents)
- $L$ = Total Inductance
- $C_p$  = fringing capacitance between the inductor turns;
- $C_{ox1,2}$  = shunt capacitances of the oxide layer;
- $C_{sh1,2}$  = total shunt capacitance of the dielectric layers and substrate;
- $R_{sb1,2}$  = shunt resistance due to substrate losses;
- $R_{se}$  = parallel resistance due to eddy current loss in the substrate.  $I_{\text{sub}}$  flow in the **low-resistivity substrate** underneath the coil with higher current density closer to the coil.

- If the  $R_{se}$  term is not used in the model it becomes a part of  $R_{sb}$ .
- Series elements: depend on the properties and dimensions of inductor conductor trace.
- Shunt elements: depend on the dielectric parameters, substrate parameters i.e. doping and thickness.

# Passive Components: Common Q Enhancement Techniques for Inductors on Si Substrate



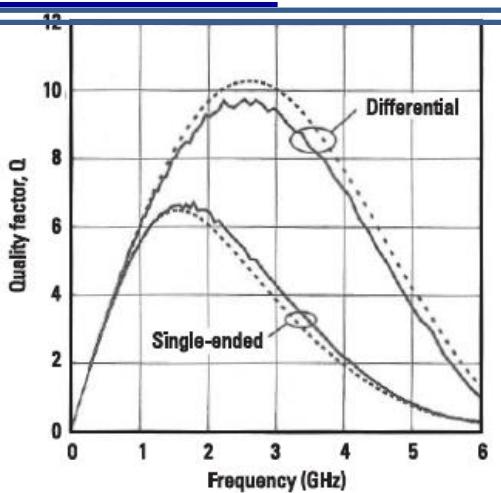
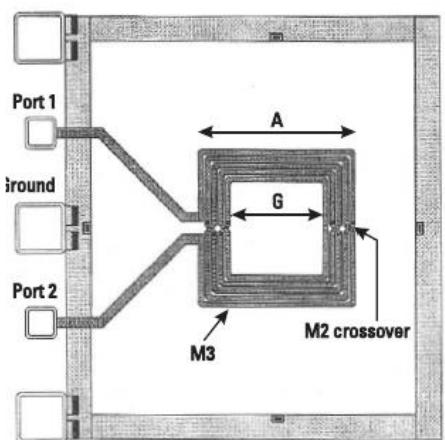
**Variable Width Layout:** Minimizing effect of Eddy current which are more in inner turns. The increased DC resistance compensated by wider outer dimensions



**Patterned ground shields:** Slots are cut perpendicular to the traces/ or the flow of eddy currents.

Slots block the eddy current flow and reduce the magnetic loss.

**Solid Ground Shield:** Large capacitances between the trace and the ground plane results lower inductance, and low SRF.



**Differential Excitation:** Smaller Substrate loss

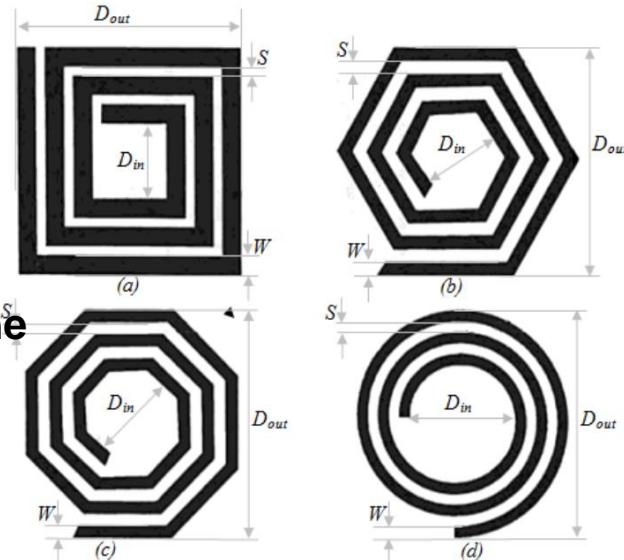
# Passive Components: On-Chip Planar Inductor Geometry

- Active circuits can be used to synthesize an Inductor.
- **DISADVANTAGES:**
  1. Higher Noise
  2. Distortion
  3. Power Consumption

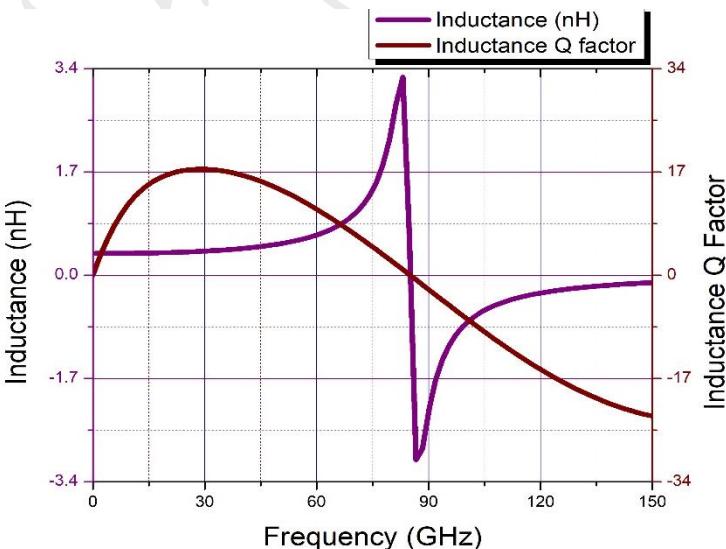
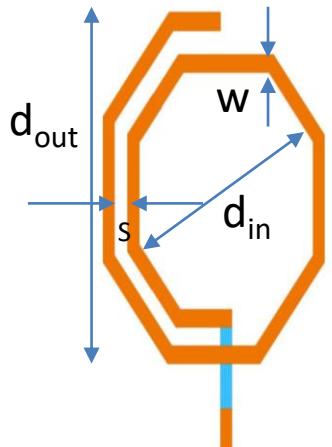
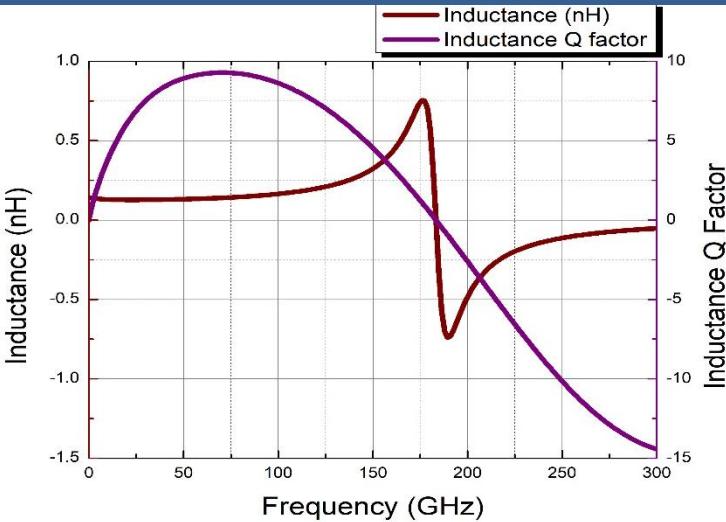
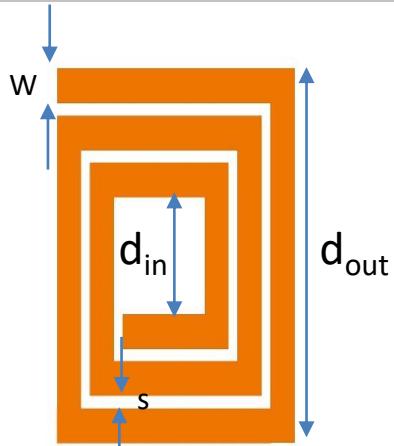
## ➤ SOLUTION: On-Chip Planar Inductors

- The most widely used on-chip Inductor is the planar spiral.
- They can assume many shapes as shown in the figure
- The **Topmost metal layer** is preferred for the main part of the inductor.
- Reason:-

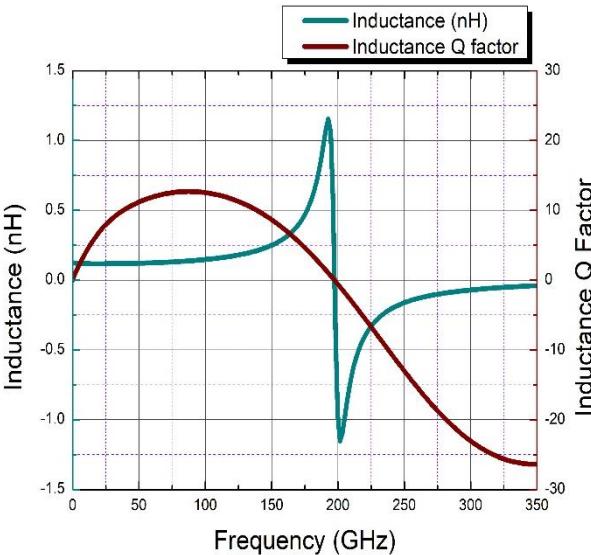
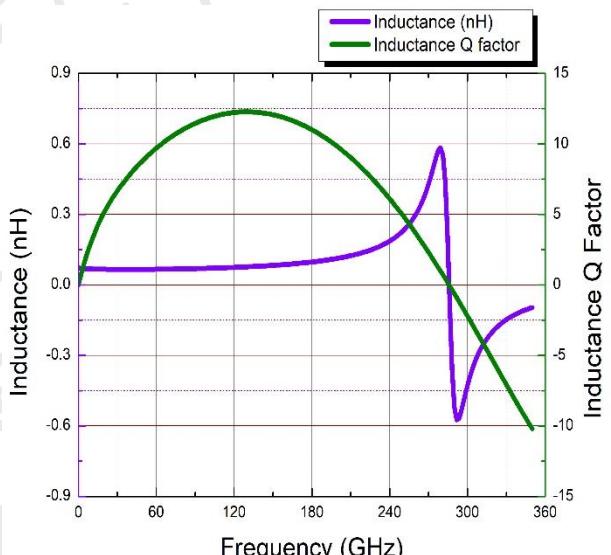
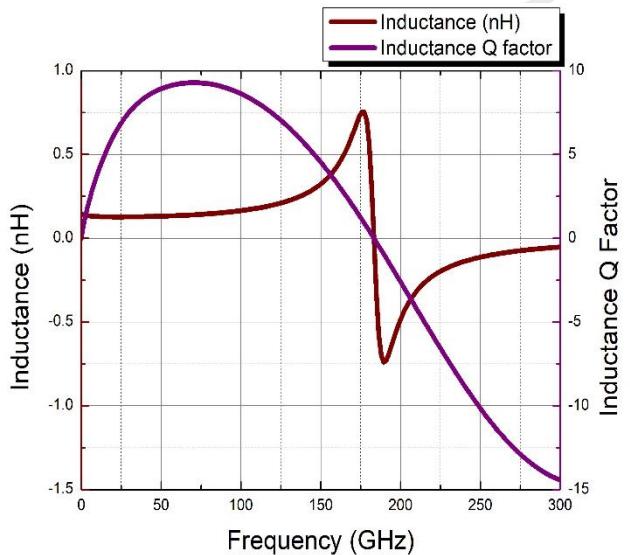
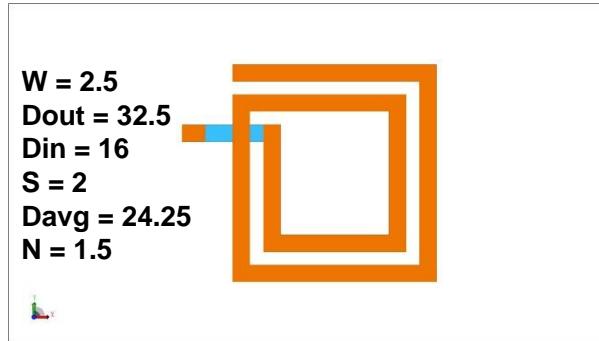
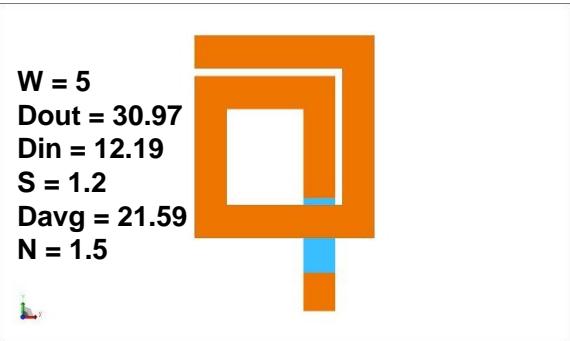
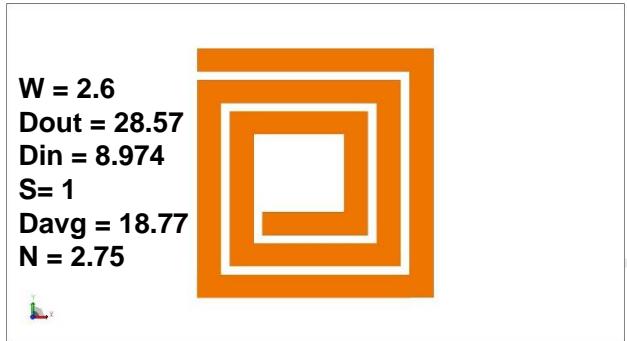
1. The topmost metal layer is usually the thickest and has the lowest resistance.
2. Maximizing the distance to the substrate minimizes the parasitic capacitance between the inductor and the substrate.



# Passive Components: On-Chip Planar Inductor in 130 nm GF SiGe BiCMOS with Rectangular and Octagonal Geometry

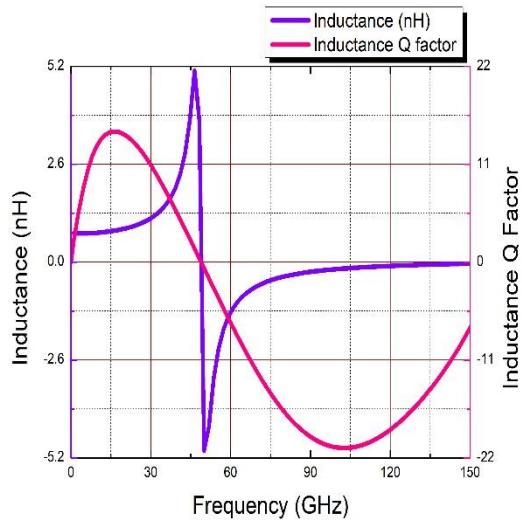
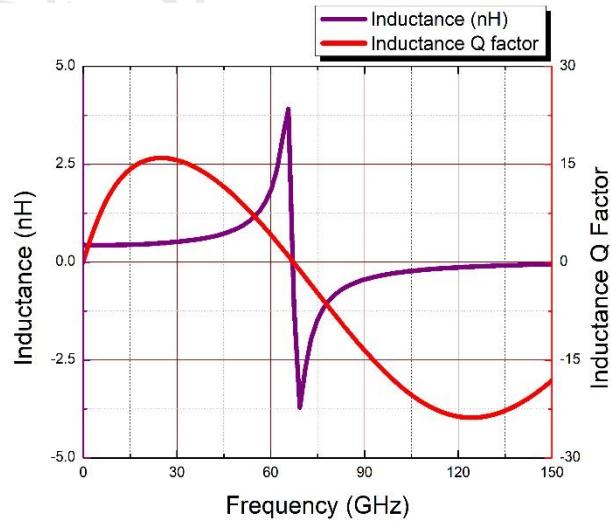
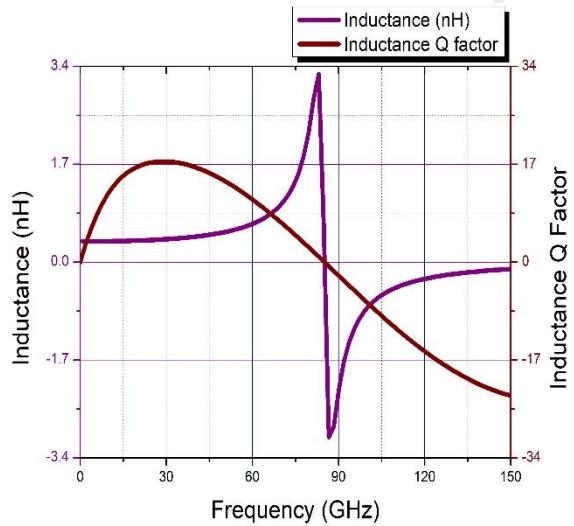
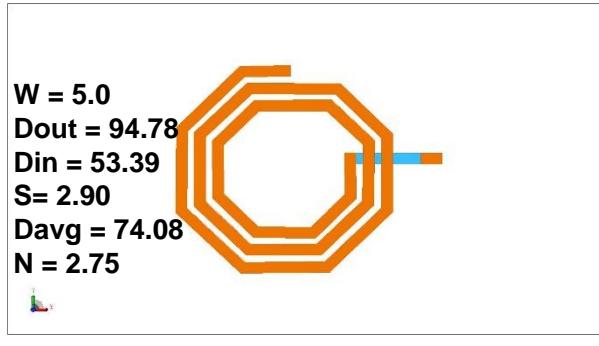
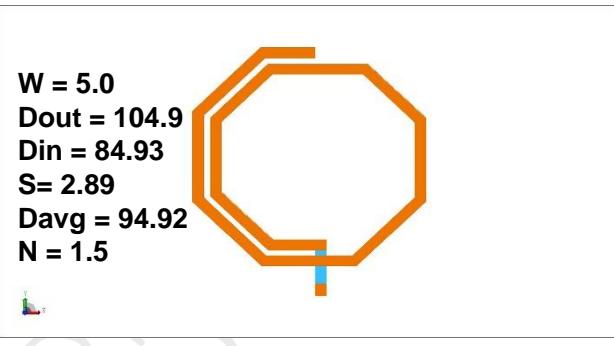


# Passive Components: On-Chip Planar Rectangular Inductor with Different Geometry in 130 nm GF SiGe BiCMOS



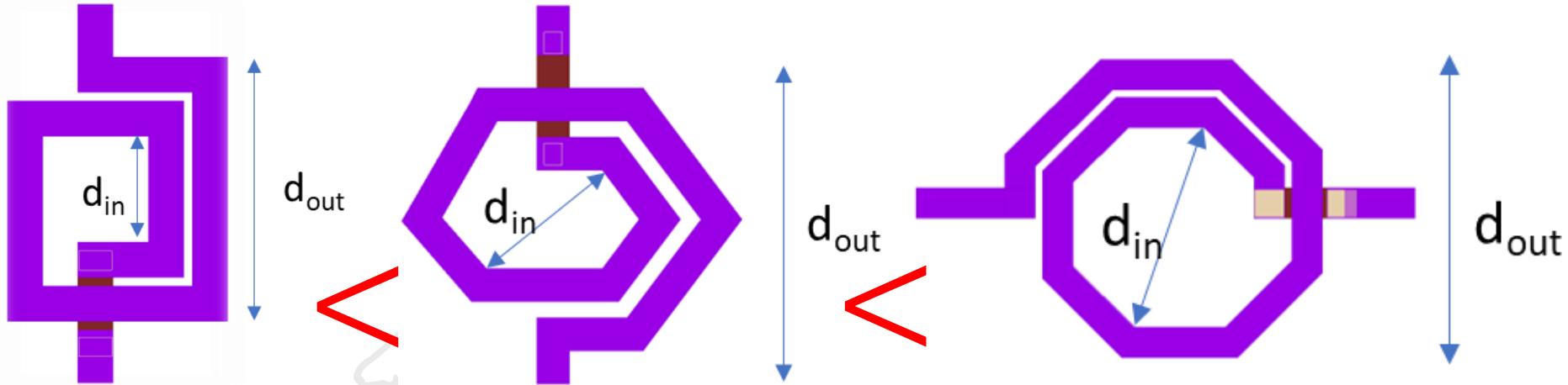
Frequency	L1 (nH)	L2 (nH)	L3 (nH)	Q1	Q2	Q3
2.5 GHz	0.127	0.069	0.121	2.78	0.9	1.20
33.0 GHz	0.117	0.065	0.117	10.25	7.21	9.30

# Passive Components: On-Chip Planar Octagonal Inductor with Different Geometry in 130 nm GF SiGe BiCMOS

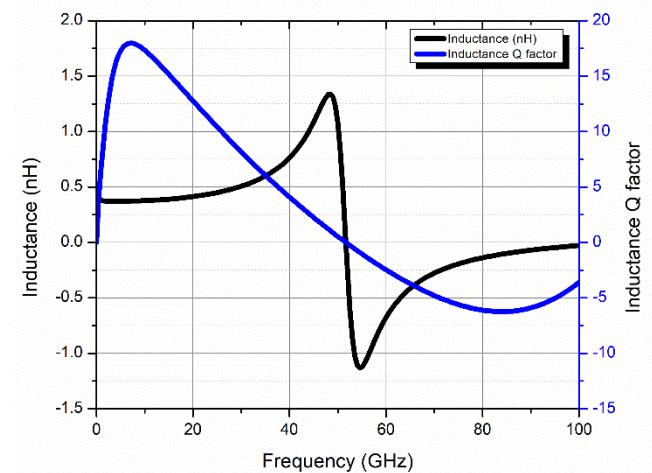


Frequency	L1 (nH)	L2 (nH)	L3 (nH)	Q1	Q2	Q3
2.7 GHz	0.360	0.429	0.761	4.28	4.10	5.53
33.0 GHz	0.410	0.544	1.33	17.027	14.94	9.13

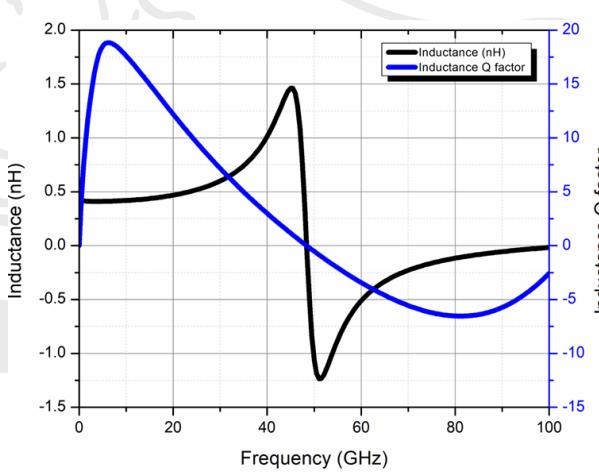
# Passive Components: On-Chip Planar Inductors with Different Geometry in 65 nm TSMC CMOS Process



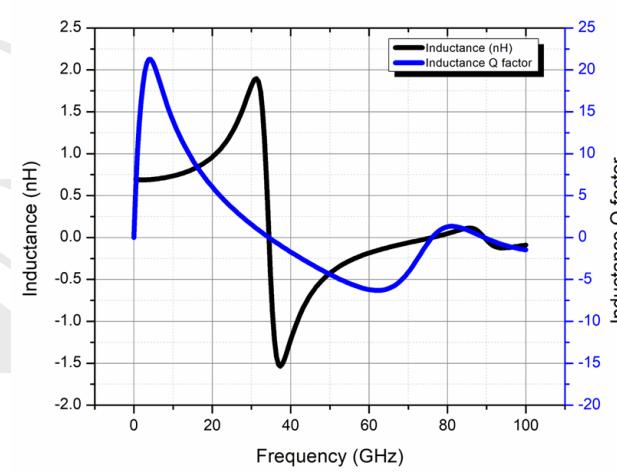
Square Inductor



Hexagonal Inductor



Octagonal Inductor



OCTAGONAL HAS THE HIGHEST INDUCTANCE VALUE AS IT HAS MORE AREA COMPARED TO THE SQUARE AND THE HEXAGON.



## References

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- R. Jacob Baker “CMOS Circuit Design, layout, and Simulation”, IEEE Press Series, Wiley
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