CS204 - Computer Architecture
Course Project - Phase 3 Description
Appending RISC-V pipeline with Caches
Deadline: 18th Apr 2023. 11.55PM.

Phase 3: Appending a cache module to Phase 2.

In this phase, you'll create the instruction (I$) and data (D$) cache modules. Instead of directly reading from .mc file (or some other temporary structure), you'll read the instructions, read/write data from these cache modules.

More details of Cache model:

1. You'll need to instantiate two caches, one will work as Instruction cache (I$) and another will work as Data cache (D$). So, all the requests from Fetch stage of your pipeline will be handled by I$. Like wise, requests from Memory stage will be handled by D$.

2. You'll give a provision to the user to specify input configurations for I$ and D$ separately.

3. Input parameters (for each cache): Cache size, Cache block size, Direct mapped (DM)/Full Assoc (FA)/ Set Assoc(SA), Number of ways for SA.

4. For FA and SA caches, LRU/FIFO/Random/LFU replacement policies as input.

5. Hit time of I$ and D$, Miss penalty in cycles. Default values can be 1 cycle and 20 cycles respectively.

6. As you are aware, when ever there is a miss in the cache, the pipeline will wait for data and has to stall. Update your Phase 2 pipeline logic to handle these memory stalls (at Fetch and Memory Access stages).

7. Output: Number of accesses, number of hits, number of misses, Number of cold, conflict, capacity misses. Total number of memory stalls. CPI (or IPC) with and without perfect caches.

8. At the end of simulation, two sets of stats will be printed - one for I$ and another for D$.

GUI requirements for bonus points (1%):

1. You would require to show the user the content of all the sets of the cache (both I$ and D$) which have non-zero data.
2. For each Fetch, Load, Store, show the set that is accessed. Show the split of Tag-Index-BO from the requested address.
3. Upon a miss, show the victim block. Show the stalls at the pipeline.
4. The number of accesses, hits, misses (cold, conflict and capacity) are required to be shown.

Revert if you have any questions.