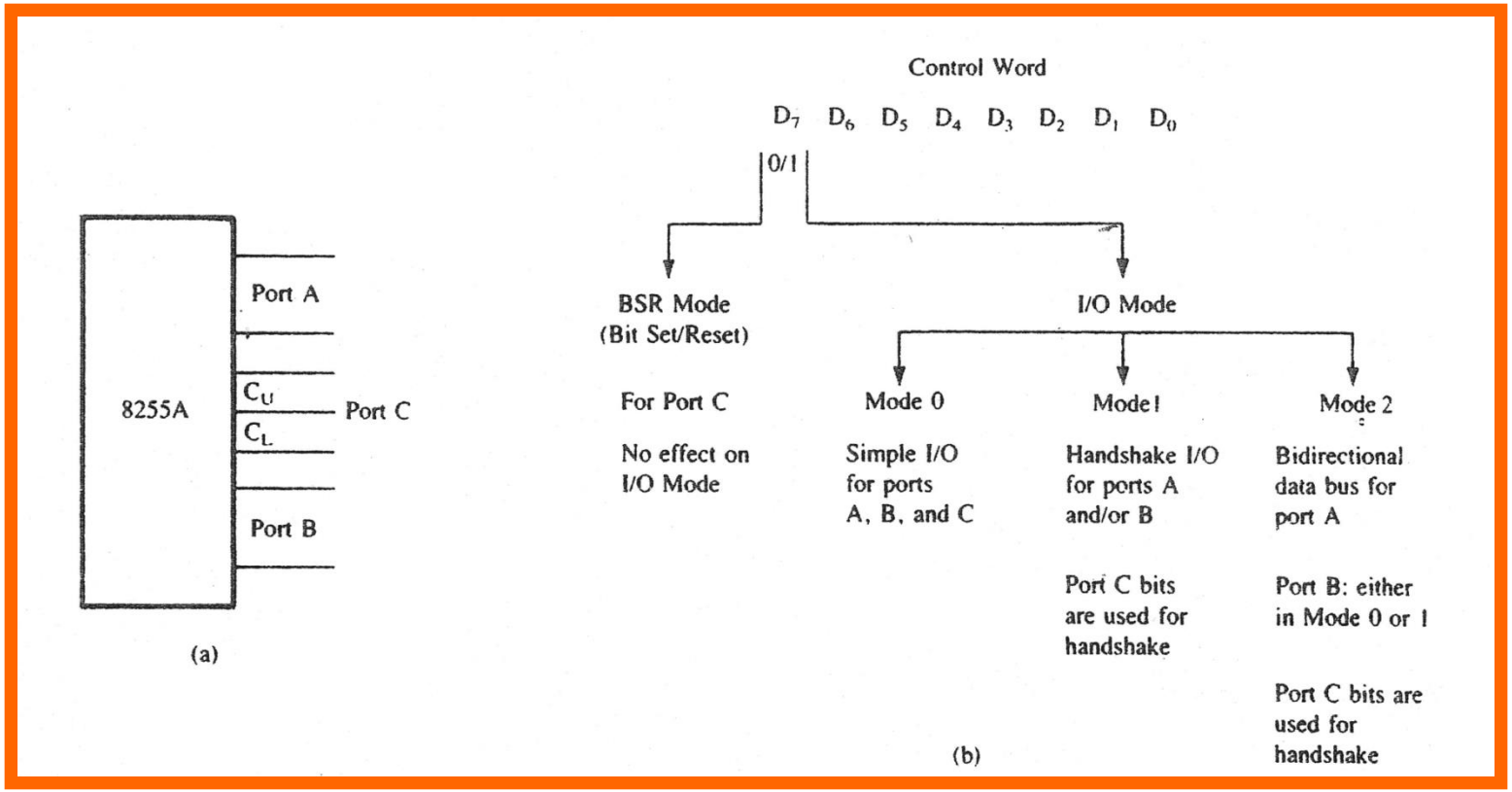
GENERAL –PURPOSE PROGRAMMABLE PERIPHERAL DEVICES.

The 8255A Programmable Peripheral Interface.

- The 8255A is a widely used, programmable, parallel I/O device.
- It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O.
- It is flexible, versatile, and economical (when multiple I/O ports are required), but somewhat complex.
- It is an important general-purpose I/O device that can be used with almost any microprocessor.

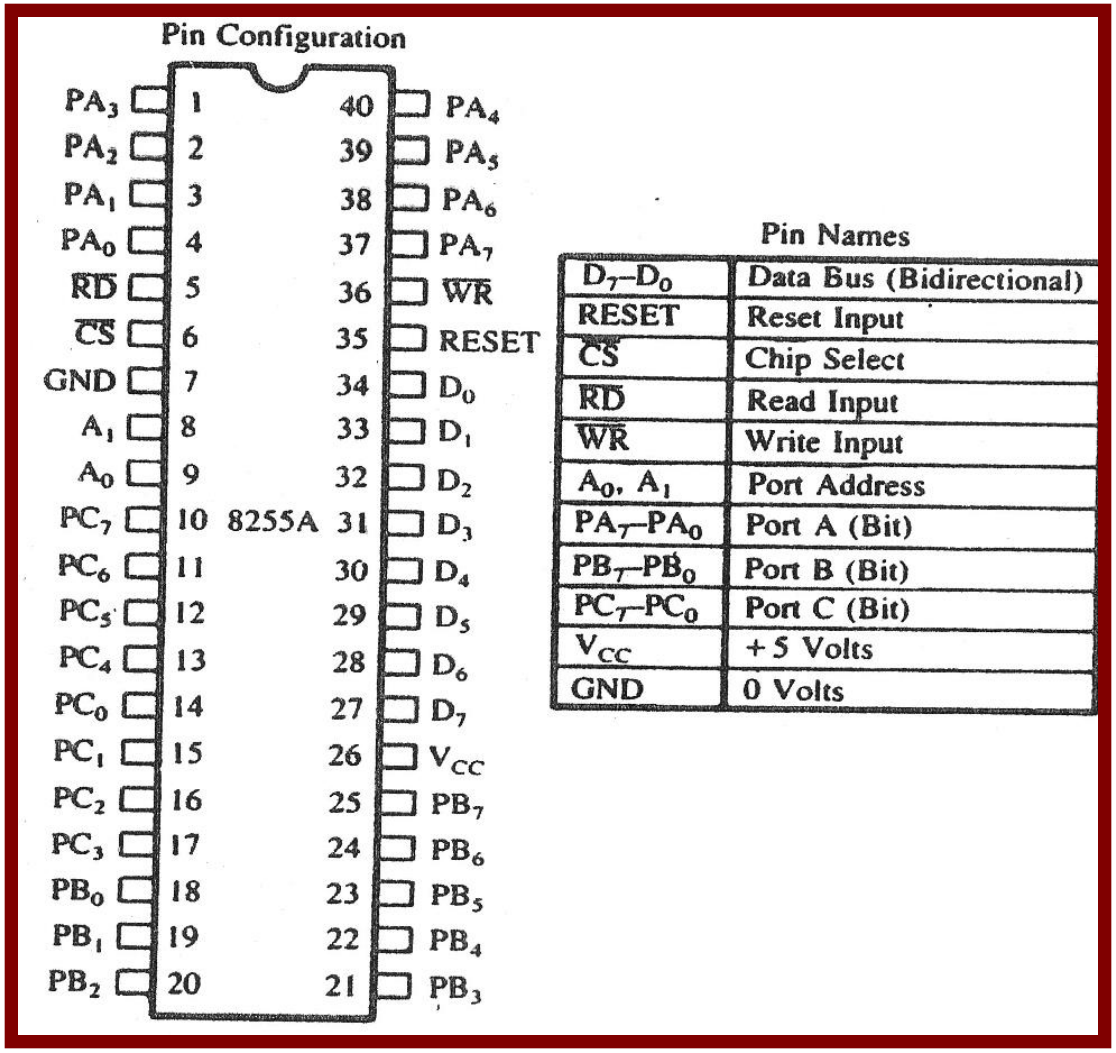
- The 8255A has 24 I/O pins that can be grouped primarily in two 8-bit parallel ports: A and B, with the remaining eight bits as port C.
- The eight bits of port C can be used as individual bits or be grouped in two 4 bit ports: C_{UPPER} (C_U) and C_{LOWER} (C_L).
- The functions of these ports are defined by writing a control word in the control register.

8255 I/O PORTS (A) AND THEIR MODES (B)



- The BSR mode is used to set or reset the bits in port C.
- The I/O mode is further divided into three modes: Mode 0, Mode 1, and Mode 2.
- In Mode 0, all ports function as simple I/O ports.
- Mode 1 is a handshake mode whereby ports A and/or B use bits from port C as handshake signals. In the handshake mode, two types of I/O data transfer can be implemented:
- (1)status check (2) interrupt.
- In Mode 2, port A can be set up for bidirectional data transfer using handshake signals from port C, and port B can be set up either in Mode 0 or Mode 1.

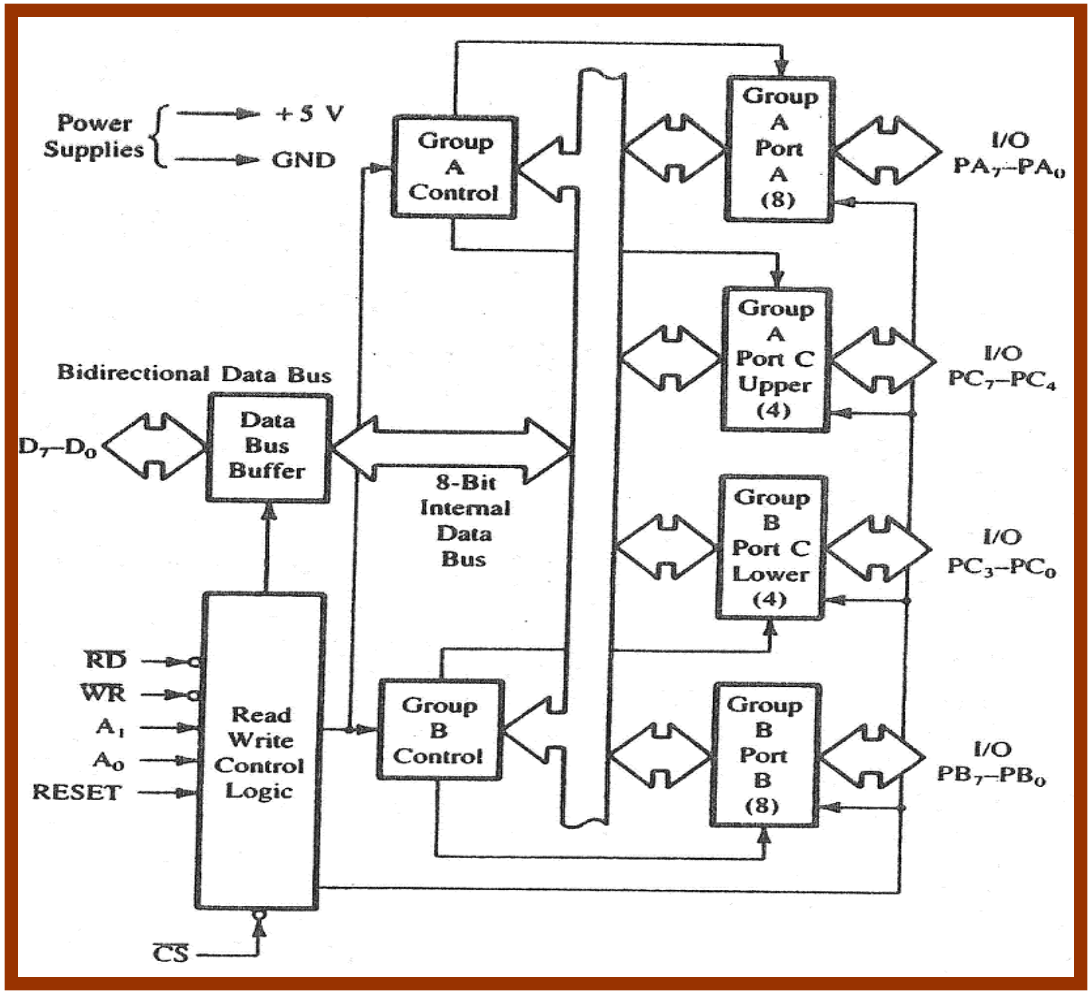
BLOCK DIAGRAM OF THE 8255A.



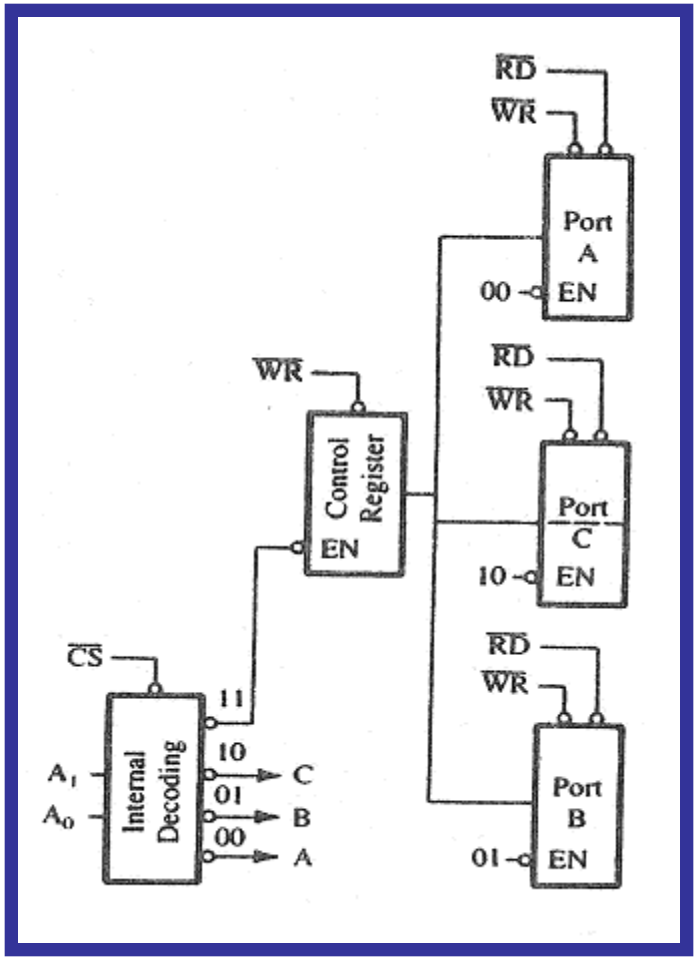
Pin Names

D_7–D_0	Data Bus (Bidirectional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7–PA_0	Port A (Bit)
PB_7–PB_0	Port B (Bit)
PC_7–PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

BLOCK DIAGRAM.



EXPANDED VERSION OF THE CONTROL LOGIC.



BLOCK DIAGRAM DESCRIPTION.

- The block diagram shows two 8-bit ports (A and B),
- Two 4-bit ports (C_U and C_L)
- The data bus buffer, and control logic.
- Simplified but expanded version of the internal structure, including a control register.
- This block diagram includes all the elements of a programmable device; port C performs functions similar to that of the status register in addition to providing handshake signals.

CONTROL LOGIC.

- The control section has six lines. Their functions and connections are as follows:
- $\overline{RD}$ (Read): This control signal enables the Read operation. When the signal is low, the MPU reads data from a selected I/O port of the 8255A.
- $\overline{WR}$ (Write): This control signal enables the Write operation. When the signal goes low, the MPU writes into a selected I/O port or the control register.

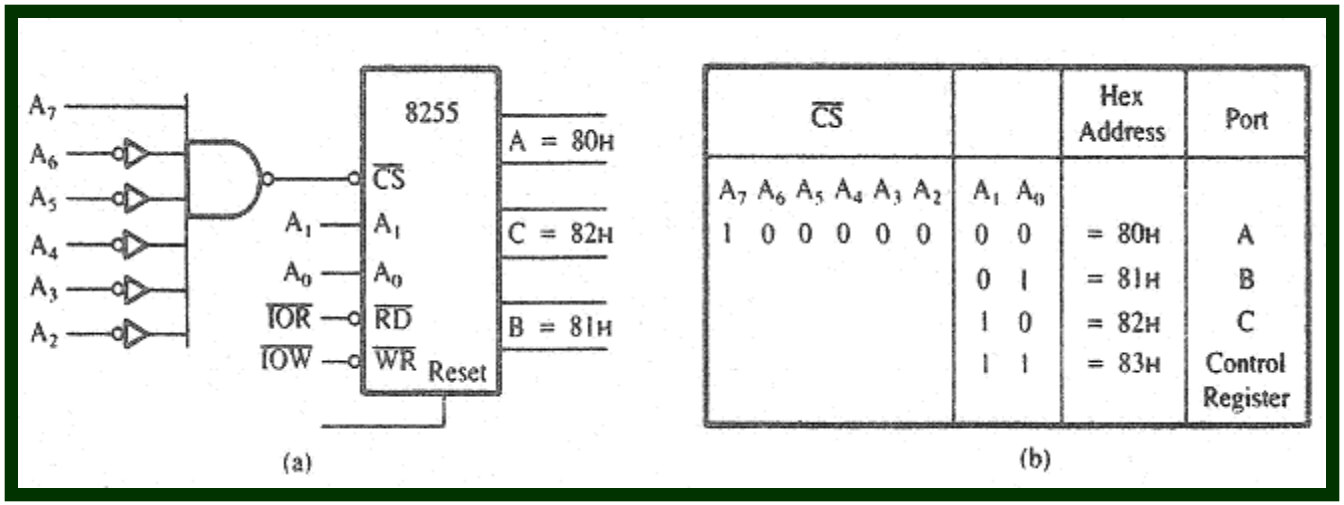
- RESET (Reset): This is an active high signal; it clears the control register and sets all ports in the input mode.
- CS, A0, A1: These are device select signals. CS is connected to a decoded address, and A0 and A1 are generally connected to MPU address lines A0 and A1, respectively.

- The CS signal is the master chip select, and A0 and A1 specify one of the I/O ports or the control register as given below:

CS	A1	A0	Selected
0	0	0	port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	x	x	8255 is not selected.

- The port addresses are determined by the CS, A0, and A1 lines.
- The CS line goes low when A7 = 1 and A6 through A2 are at logic 0.
- When these signals are combined with A0 and A1, the port addresses range from 80H to 83H.

8255 CHIP SELECT LOGIC & I/O PORT ADDRESS.



(a)

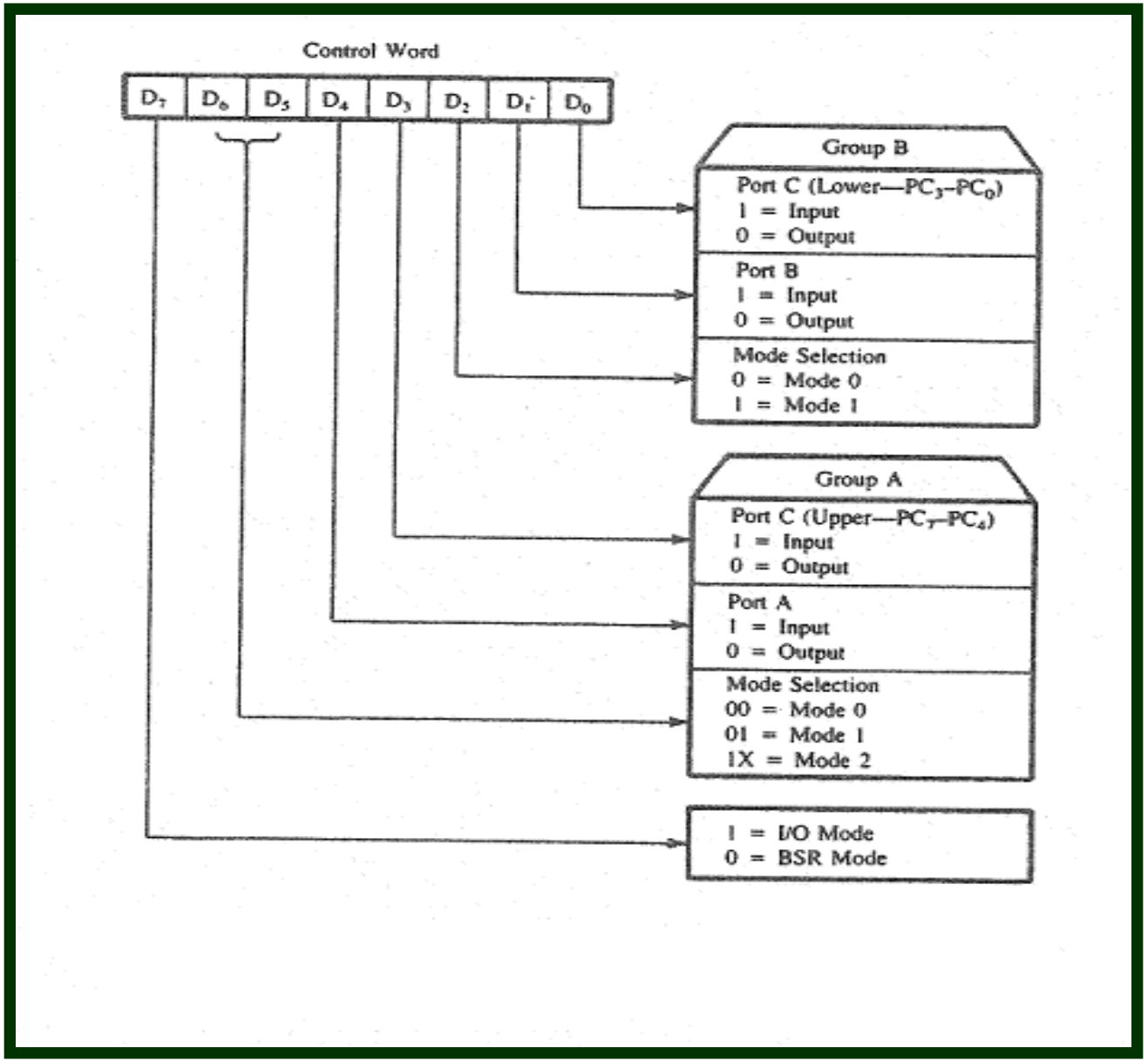
$\overline{CS}$			Hex Address	Port
A_7 A_6 A_5 A_4 A_3 A_2	A_1	A_0		
1 0 0 0 0 0	0	0	= 80H	A
	0	1	= 81H	B
	1	0	= 82H	C
	1	1	= 83H	Control Register

(b)

CONTROL WORD

- The contents of Control register, called the control word, specify an I/O function for each port.
- This register can be accessed to write a control word when A0 and A1 are at logic 1, as mentioned previously.
- The register is not accessible for a read operation.

- Bit D_7 of the control register specifies either the I/O function or the Bit Set/Reset function.
- If bit D_7 = 1 , Bits D_6-D_0 determine I/O functions in various modes.
- If bit D_7 =0, port C operates in the Bit Set/Reset (BSR) mode.
- The BSR control word does not affect the functions of ports A and B.


Control Word
D7 D6 D5 D4 D3 D2 D1 D0
Group B
Port C (Lower—PC3–PC0)
1 = Input
0 = Output
Port B
1 = Input
0 = Output
Mode Selection
0 = Mode 0
1 = Mode 1
Group A
Port C (Upper—PC7–PC4)
1 = Input
0 = Output
Port A
1 = Input
0 = Output
Mode Selection
00 = Mode 0
01 = Mode 1
1X = Mode 2
1 = I/O Mode
0 = BSR Mode

- To communicate with peripherals through the 8255A, three steps are necessary:

1. Determine the addresses of ports A, B, and C and of the control register according to the Chip Select logic and address lines A0 and A1.
2. Write a control word in the control register.
3. Write I/O instructions to communicate with peripherals through ports A, B, and C.

MODE 0: SIMPLE INPUT OR OUTPUT

- Ports A and B are used as two simple 8-bit I/O ports
- Port C as two ,4- bit ports
- The input/output features in Mode 0 are as follows:

1. Outputs are latched.
2. Inputs are not latched.
3. Ports do not have handshake or interrupt capability.

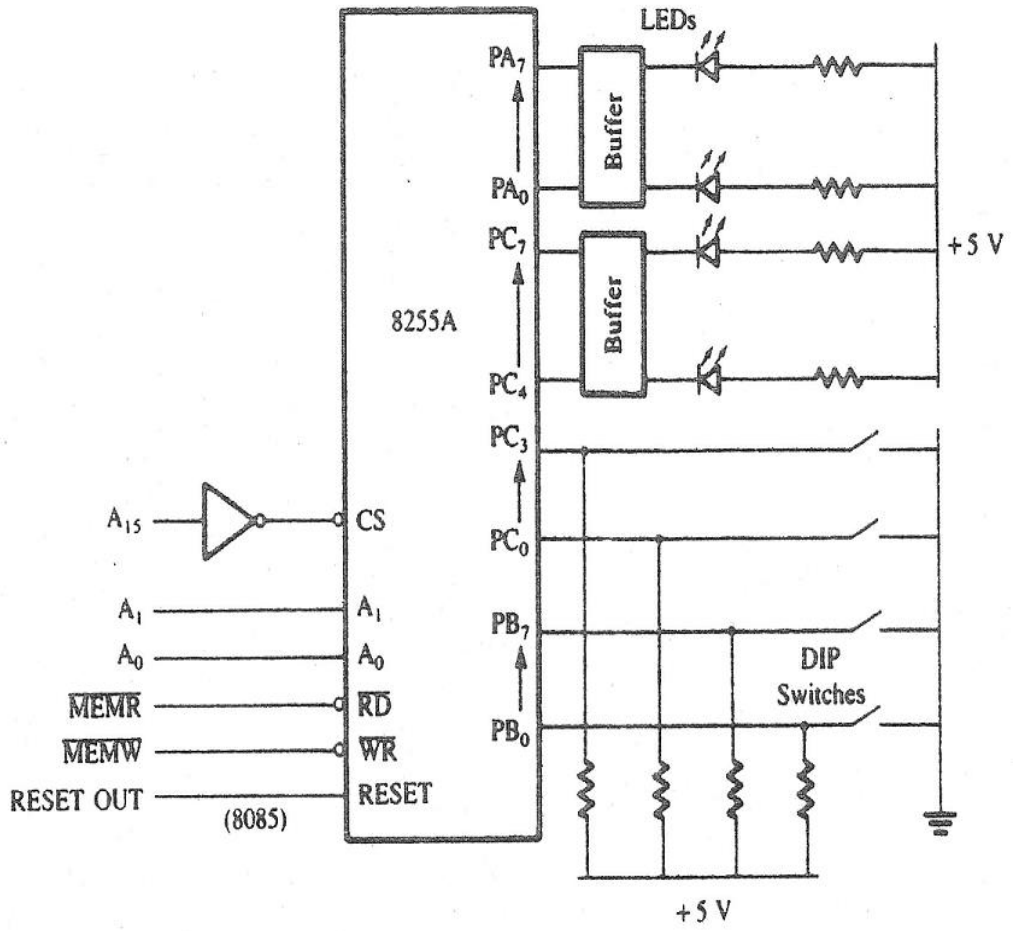
EXAMPLE

l. Identify the port addresses in Figure shown.

2. Identify the Mode 0 control word to configure port A and port C_U as output ports and port B and port C_L, as input ports.

3. Write a program to read the DIP switches and display the reading from port B at port A and from port C_L at port C_U.

INTERFACING 8255A I/O PORTS.



Interfacing 8255A I/O Ports in Mode 0

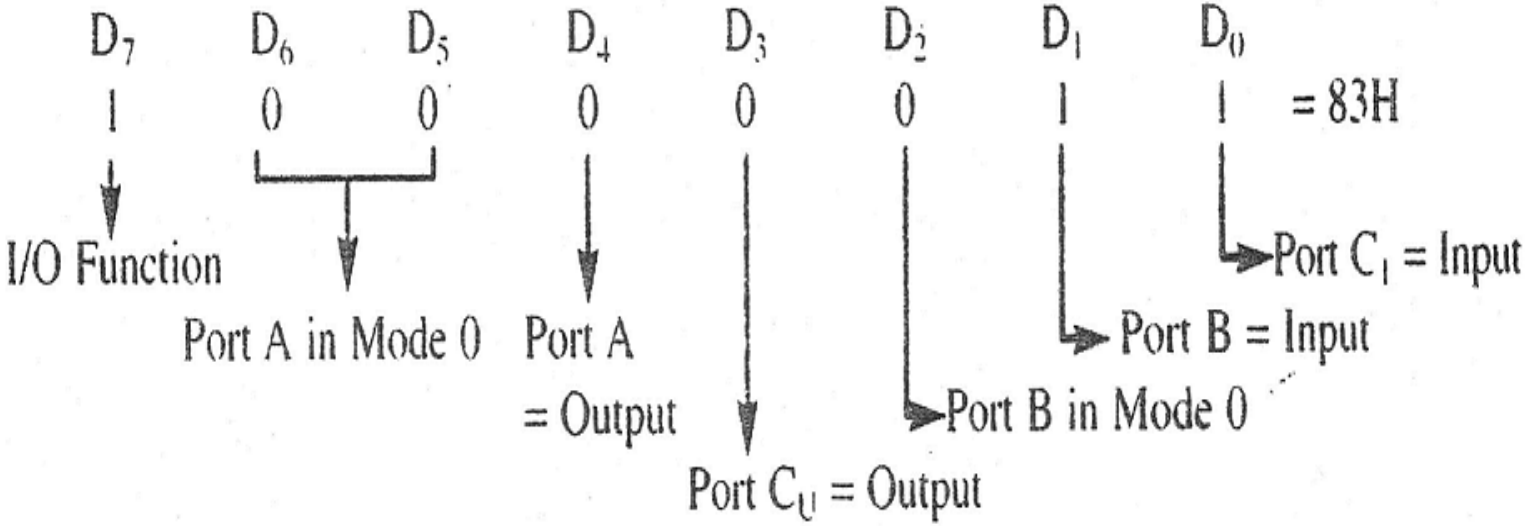
SOLUTION:

l. Port Addresses

- This is a memory-mapped l/O; when the address line A_{15} is high, the Chip Select line is enabled. Assuming all don't care lines are at logic 0, the port addresses are as follows:

Port A = 8000H {A_1 = 0, A_0, = 0)
Port B = 8001H (A_1 = 0. A_0 = l)
Port C = 8002H (A_1 = l, A_0 = 0)
Control Register = 8003H(A_1 =l, A_0= l)

Control Word



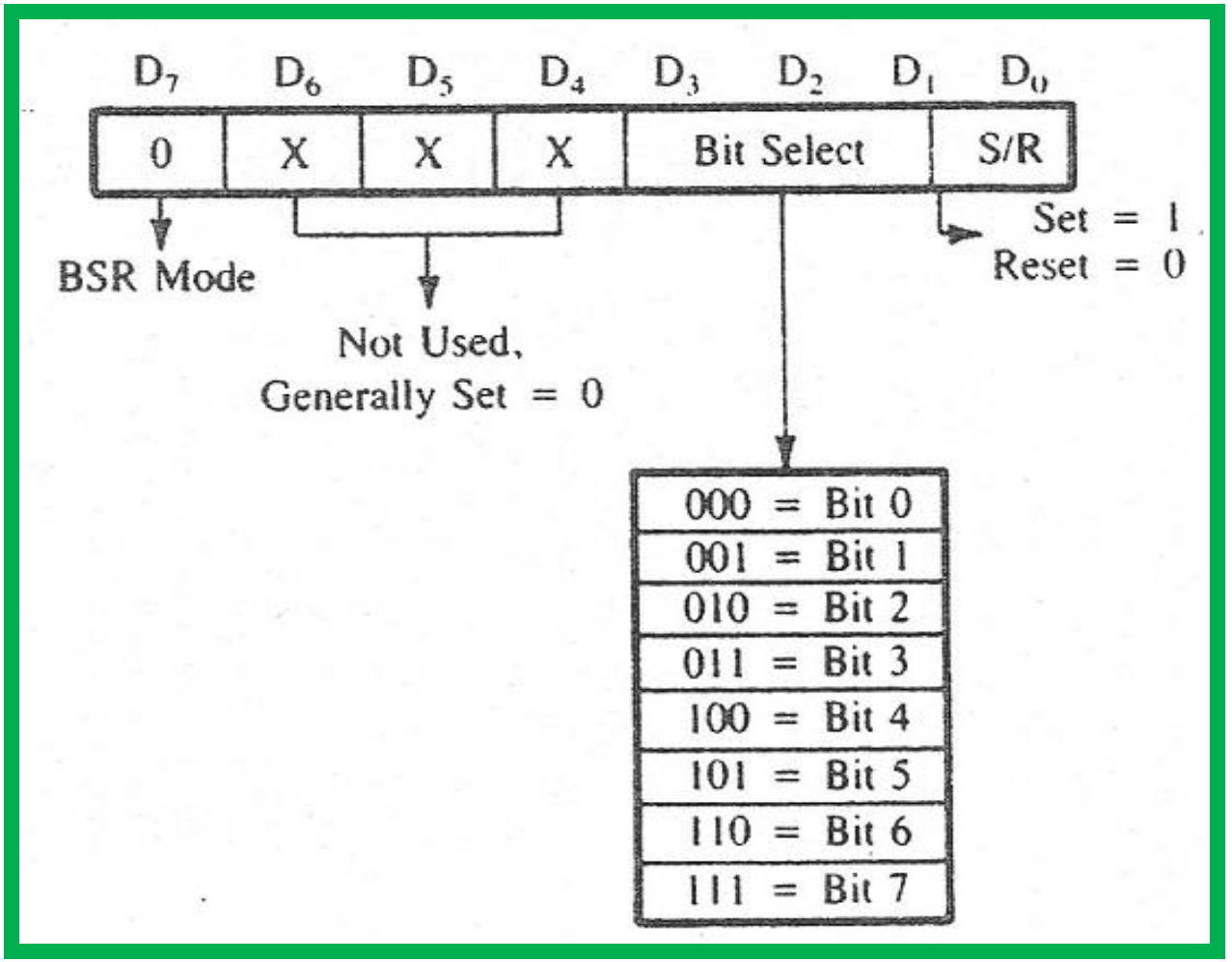
PROGRAM:

- MVI A,83H ; Load accumulator with the control word
- STA 8003H ; Write word in the control register to initialize the ports
- LDA 8001H ; Read switches at port B
- STA 8000H ; Display the reading at port A
- LDA 8002H ; Read switches at port C
- ANI 0FH ; Mask the upper four bits of port C; these ; bits are not input data
- RLC ; Rotate and place data in the upper half ; of the accumulator
- RLC
- RLC
- RLC
- STA 8002H ; Display data at port C1
- HLT

BSR (BIT SET/RESET) MODE:

- The BSR mode is concerned only with the eight bits of port C, which can be set or reset by writing an appropriate control word in the control register.
- A control word with bit D_7 = 0 is recognized as a BSR control word, and it does not alter any previously transmitted control word with bit D_7 = l; thus the I/O operations of ports A and B are not affected by a BSR control word.
- In the BSR mode, individual bits of port C can be used for applications such as an on/off switch.

BSR CONTROL WORD:



EXAMPLE:

- Write a BSR control word subroutine to set bits PC_7 and PC_3 and reset them after 10 ms. Use the schematic in Figure 8255A Chip select logic and assume that a delay subroutine is available.

SOLUTION: BSR CONTROL WORDS

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
To set bit PC_7	= 0	0	0	0	1	1	1	1	=	0FH
To reset bit PC_7	= 0	0	0	0	1	1	1	0	=	0EH
To set bit PC_3	= 0	0	0	0	0	1	1	1	=	07H
To reset bit PC_3	= 0	0	0	0	0	1	1	0	=	06H

PORT ADDRESS:

- Control register address = 83 H;

SUBROUTINE:

```
BSR:    MVI A,0FH       ;Load byte in accumulator to set PC7
        OUT 83H         ;Set PC7 = 1
        MVI A,07H       ;Load byte in accumulator to set PC3
        OUT 83H         ;Set PC3 = 1
        CALL DELAY      ;This is a 10-ms delay
        MVI A,06H       ;Load accumulator with the byte to reset PC3
        OUT 83H         ;Reset PC7
        MVI A,0EH       ;Load accumulator with the byte to reset PC7
        OUT 83H         ;Rest PC7
        RET
```

- From an analysis of the above routine, the following points can be noted:

l. To set/reset bits in port C, a control word is written in the control register and not in port C.

2. A BSR control word affects only one bit in port C.

3. The BSR control word does not affect the I/O mode.