Experiment - Integration & Differentiator Grunt
Using OP-AMP

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Experiment No - &.

Experiment Name-Integrator & Differentiator Circuits Using Operational Amplifies.

Date - 28/06/23

Integration and Differentiator circuits using op.amp.
To study the integration and differentiator circuits using operational amplifier (IC 741).

Formula Used:

(a) Integrator Circuit

$$A = \frac{V_0}{V_i} = -\frac{R_J}{R} \left[\frac{1}{j^2 \pi v R_J C_J + 1} \right]$$

$$|A| = \frac{R_J R}{1 + w^2 R_J^2 C_J^2}$$

where

A = voltage gain

Vo= 0/p voltage

Vi= i/p voltage w=Angular preguency.

(b) Differentiation circuit

1Al= Rywc VI+w2C2R2

There

A: voltage gain

Vo: op voltage

Vi: ilp voltage

w: angular frequency

R= feedback resistance
R= uput resistance in series with r;
V = frequency of v;
Cj = feedback capacitance

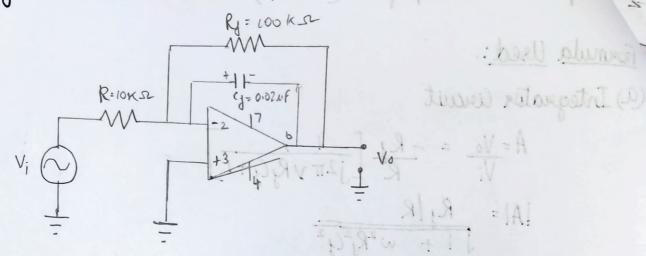
Ry: feedback resistance

R: resistance is serie with t,

C: Capacitou

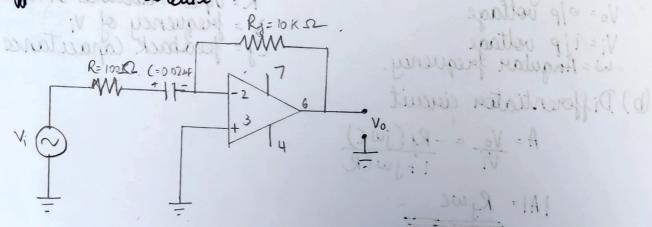
Circuit Diagram:

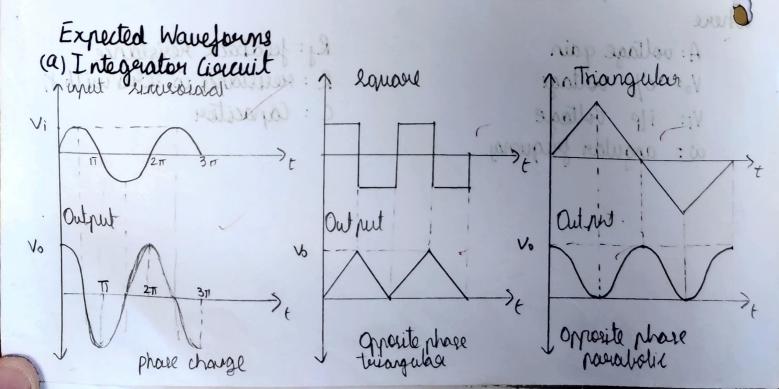
1) Integrator Gravit

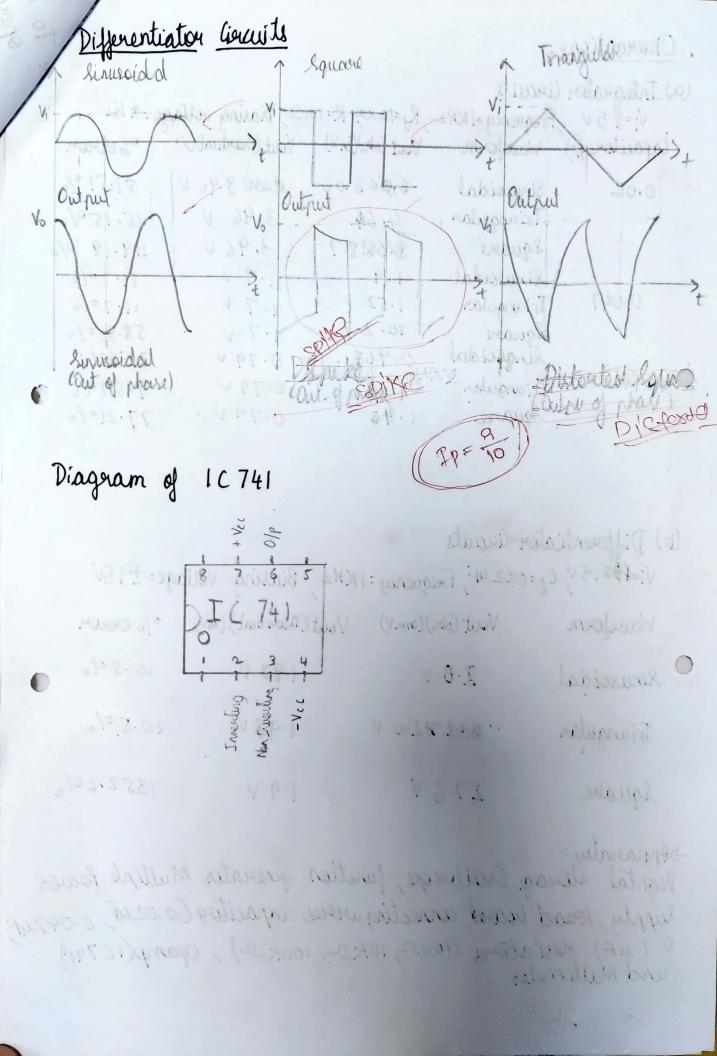


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2) Differentiation Circuit







Observations:

Tagaritan (S)	Frequency=1KH2	Vous (obs)(inV)	Vous (Theodical)(V)	% 060000
capacitoruff)	Waveform			51.51%
0.02	Sinuvoidal	6.00	2100 3.96 V	-
	Triangular	4.64	3.96 V	15,150/
	Eguare	8.06.8.7	3.96 V	119.19 0
0.047	linusoidal	1:936	1-7 V	11-7060
	Triangulas	1.52	1.7 V	11.70%
	Square,	1a 2.7	1.7 V	58.82010
0.1	Lingboida	0.968	0.79 V	21.50%
	Triangular	0.738	0.79 V	7.59%
	Square	1-40	0.792.	77.210/0

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Magram of /10741

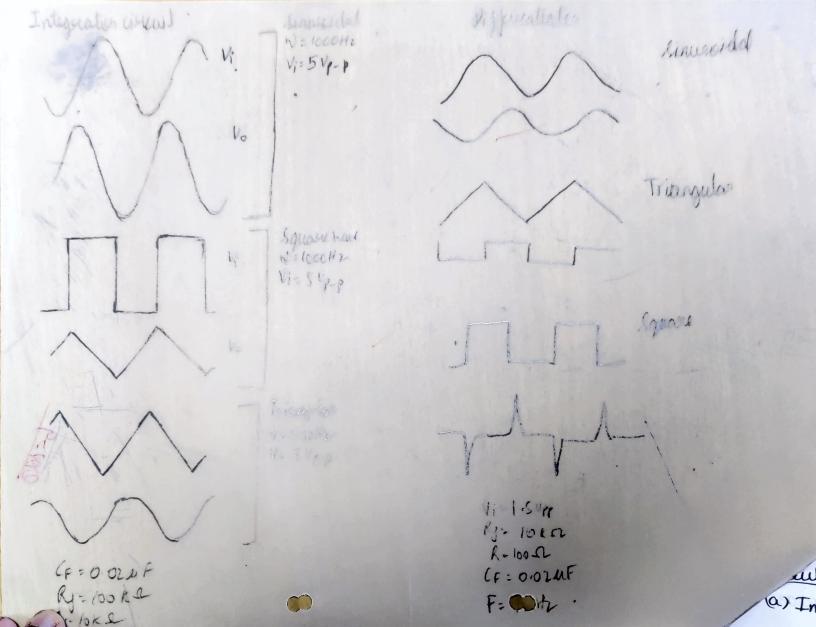
(b) Differentiator Counts

Vi=15V, Cy=0.024F, Frequency=1KHz, Biasing Voltage=±15V

Waveform	Vout (obs)(comv)	Vout (Transitual) (mV)	% 0000
Linusoidal	2.8 V	198 V	10.5%
Triangular	622702.0 V	1.95V	10.5%
Square	27.6 V	1-9 V	1352,60/0

-stypavially:
Digital storage Oscillarage, function generator, Multiple Power
Supply, bread board, correcting wises, capacitory (0.0216, 0.04746,
0.1 MF) resistory (10052, 10K5-, 100K5), Opamp(1C741)
and Mulliméles.

Styles



ulation:

(a) Integrator Circuits

 $R_{j} = 100 \text{ K-PZ} / R = 10 \text{ KPZ}$ $W = 2\pi \chi / 10^{3} / R = 10 \text{ KPZ}$ Vi= 5 V Louis rational

$$A = \sqrt{\frac{10}{11 + (2\pi)^{2} \times (6)^{2} (10^{-6}) \times (0.02)^{2} \times (0^{3})^{2}}} = 0.79$$

$$V_{0} = V_{1} \times A = \frac{10}{11 + (2\pi)^{2} \times (6)^{2} \times (0^{3})^{2}} = 0.79$$

$$3 (3 = 0.91. \mu F)$$

$$A = \frac{10}{\sqrt{1+3947}} = 0.1597 \quad \text{i. } V_0 = 0.79 \text{ V}$$

A for which is considered to disting the formula of and it down made beging its polarity is him

Due to this orth differentiation a secait we get a wonderin

The some is observed in Internation areased where square

4. In the integration never the Var decrease as the reparties

nes have auch hingles of sevies due to nelice

instead of which results in a higher you

Square Triungular

6. There is apprecably a locure could in house in site is the

resistant in the greational amplifies Vizza with and income of separation of separation of separation

The who is vix A: 1.88 Vice at the souls is tat. The william of the artell there is no display abserved in the cut pur The mest amount of especial is seen as en the

Result:			· is alatien:				
1. In the in	tegerator Gercuit, as the value walled	ue of the	Capacitar increases				
2. The output 3. Integru	to square wavefour	nows may	owner ever				
3. Integral Injust Sinusoidal	Output linusoidal	Differen	tialos Output Sinusoidal				
Iriangulau	Rosabolie		Distorted Square				
Square Precautions	and Discussion	square	Spikes (Disson, delta)				
1. Make sur	e that all connection are ti	ght	111/10 0 = b) (8) 1				
1. Make sure that all correction are tight 2. Apply hiaring voltage between 12-15 v 3. keep Vin \le 1v during differentiation circuit 4. Ensure that the polarity of capacitor is carefully checked and the circuit made keeping its polarity is mind 5. In the interestor General to triangular many							
and the circuit made keeping its polarity is mind							
generally has the least ammount of everos while the							
6. There is generally a langer error in this experiment due							
6. There is generally a langer course is this experiment due to resistance in the operational amplifier along with variance in the resistance of near too a Capacitana of Capacitana of Capacitana of The voltage that is given at the input should be reduced Untill there is no ctipping observed in the output							
Urtill 18. The most	there is no ctyping about amount of everyon is se	en mon	the output				
8. The most amount of everor is seen as on the snots where there is distortion in the input voltage due to noise. 4. Due to this in the differentiator circuit we get a wavefour							
9	instead of which	geenis	in a higher than				
The same	is observed in Integrates we much higher % evers	or cioccui	t where square to Noise				
9. In the in	tegeration circuit the Vow	decreas	es as the capacitante				

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