IL2237 Lab2 - PCB Design

Rohit Rathnam Nareshkumar

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1 Introduction

The aim was to create a development board with the following features:

- A display and buttons to interact with the device
- WiFi / Bluetooth connectivity
- Battery powered with USB charging
- Compact ECG measurement
- Real time clock to keep track of time
- Accelerometer to help with ECG signal processing

The base schematic design that this project is built on is the Open-SmartWatch (OSW) project (1).

2 Schematic Design

The Open-SmartWatch schematic is based on an ESP-32 module with support for all of the above except the ECG module. The base schematic is given in Fig 1.

The modified schematic with the ECG circuit is given in Fig 2. The ECG circuit is based on reference design from AD8232 ECG analog front end IC and ADS1015 12-bit ADC.

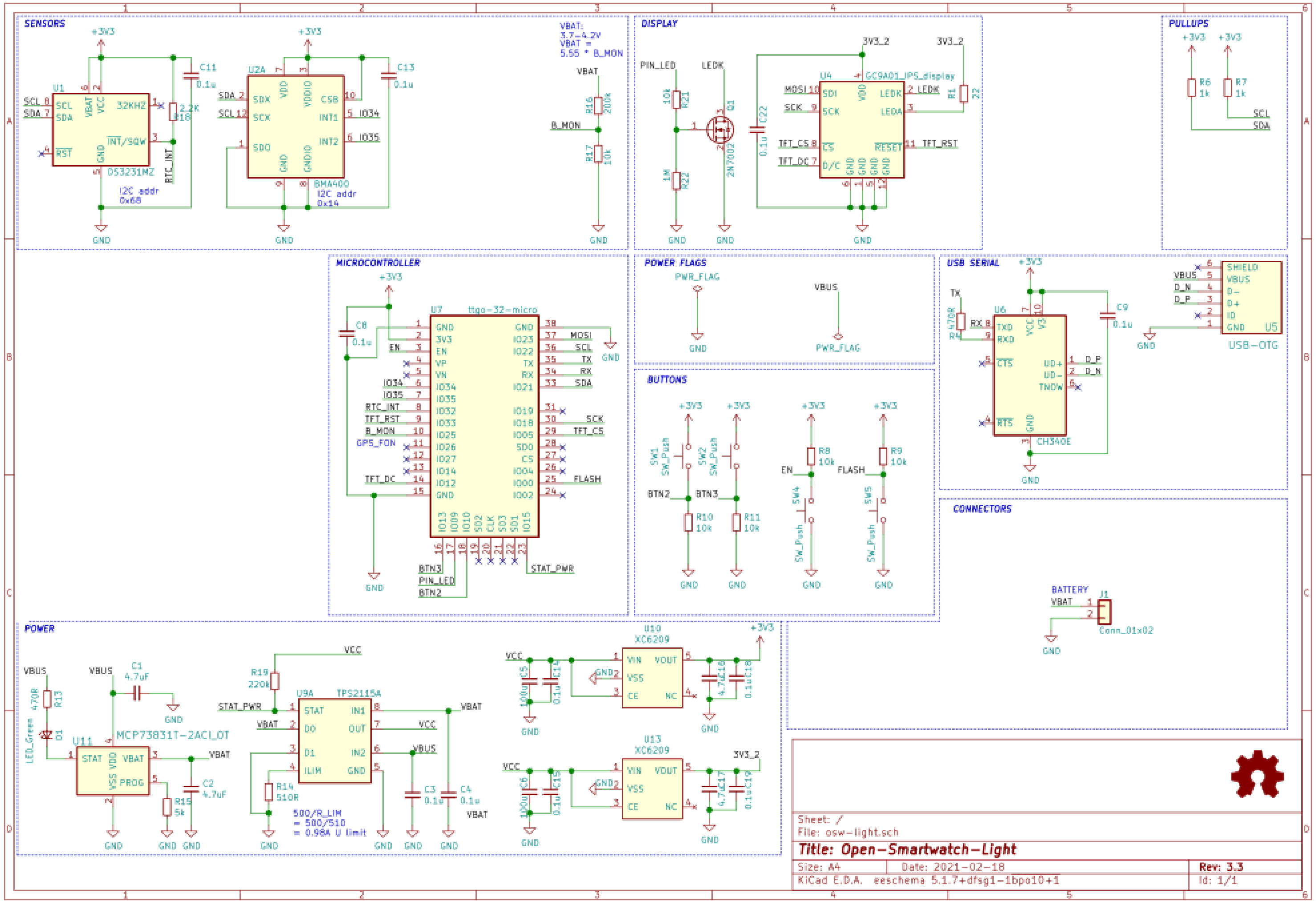


Figure 1: Original schematic

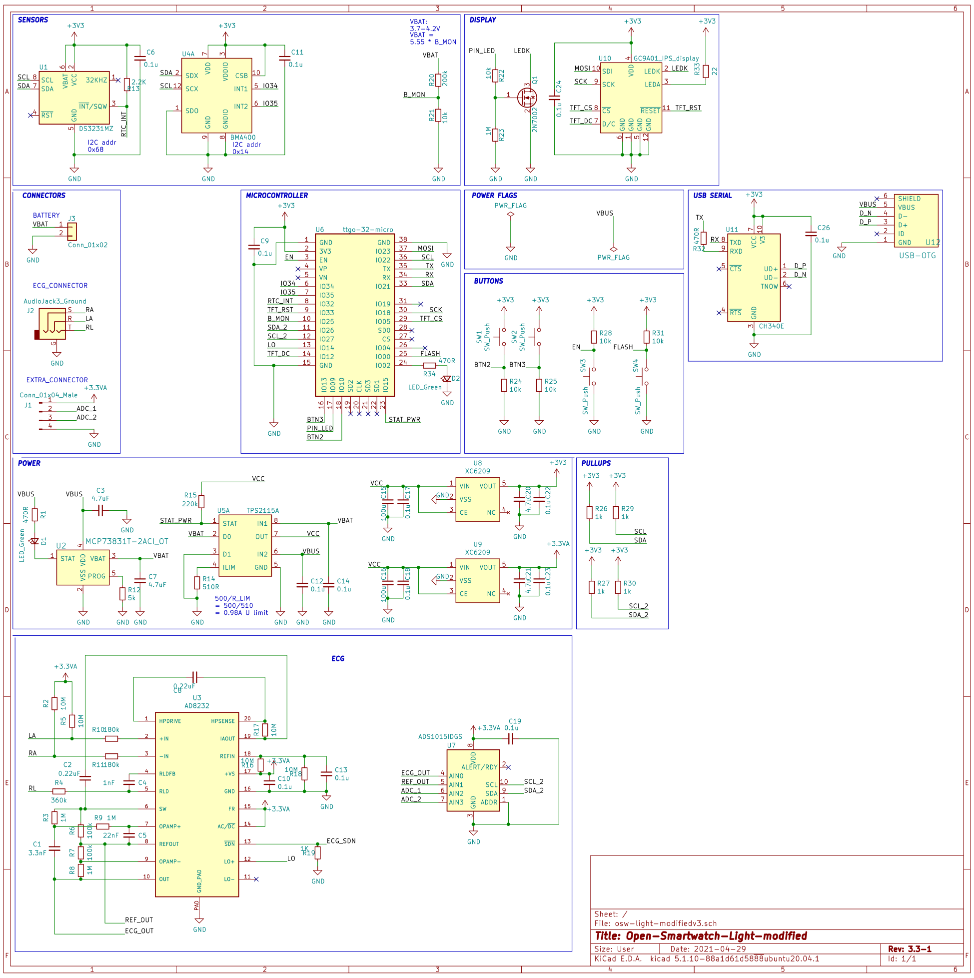


Figure 2: Modified schematic

2.1 Microcontroller

The microcontroller used in this project is an ESP-32 variant called the ttgo-32, which has a smaller form factor suitable for smartwatches. It has a PCB antenna and support for WiFi / Bluetooth. The microcontroller also features a low power core, which can be utilised to improve battery life when logging data. The PCB antenna is positioned extending from the edge of the board so that the copper does not interfere with the transmission line. The programming interface is through USB, the device goes into programming mode using the BOOT push button.

2.2 Power supply

The power supply consists of a battery management IC (MCP73831) which is responsible for charging the single cell Li battery, current limiting the battery, and producing a regulated output (VBUS). A power line multiplexer (TPS2115A) is used to switch between battery power and USB 5V. The output voltage then goes to two parallel voltage regulators (XC6209) which produce 3V3 and A3V3. Net 3V3 powers all the digital circuits, and A3V3 powers the ECG front end module and ADC. The original design had the display on a separate voltage regulator (possibly due to higher power consumption), but to accommodate a separate analog supply rail, the display was shifted to the digital supply regulator along with the other peripherals and micro-controller. The device can also monitor battery voltage through a voltage divider connected to the internal ADC of the ESP-32.

2.3 Display

The display module is a circular IPS display which interfaces over SPI. The module has a FPC connector which is placed on the back of the board to fold the display over the board.

2.4 Peripherals

The other peripherals include a BMA400 accelerometer, and a real-time clock both connected via I2C to the ESP-32. Push buttons were given for boot, turning on display and two buttons with software defined functions. A power LED

2.5 ECG module and ADC

The ECG module (AD8232) and 12-bit ADC (ADS1015) are powered by A3V3 net. The input to the ECG module is through a 3-pin 3.5mm audio jack interface. This can connect to an off the shelf module for ECG leads (2). The design for this section was adapted from the application note given in the datasheet (3). The ECG module has a differential output, which is connected to the two of the ADC input pins. Additional safety mechanism such as ESD diodes, fuses etc. were ignored due to additional complexity in schematic design, which was beyond the scope of this lab. The two extra inputs to the ADC were broken out along with A3V3 and GND to a 1mm pin header for future use. The ADC interfaces with the microcontroller over I2C, and was connected to a dedicated I2C pins so the accelerometer and ADC readings can be polled simultaneously do aid ECG signal processing and motion noise removal.

3 Layout considerations

The major factors considered was in the placement of USB connector and routing of USB differential pair, proper clearance for the antenna section of the ESP-32, and proper routing and placement of components for the ECG IC and ADC. For this design, I decided to go with a 4 layer board to allow for ground and power planes. Since this was a development board, there is not much size constraint, as such I tried to stick with a credit card size as a starting point. The final dimensions of the board is 70mm x 40mm.

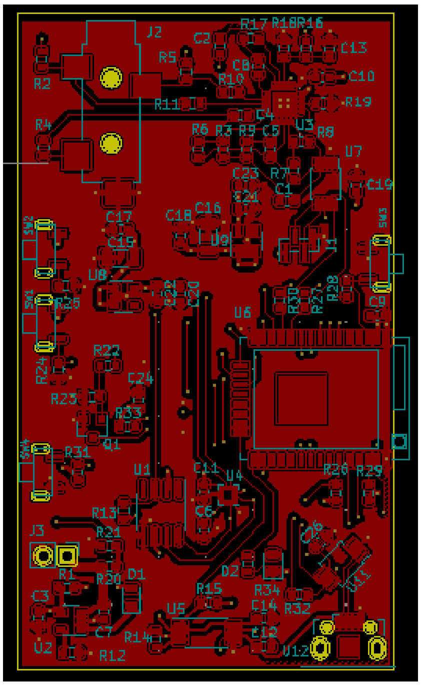
3.1 Component placement

- Priority was given to routing the differential pair to the USB IC from the connector at the edge of the board. The traces were calculated using the KiCAD PCBcalculator tool shown in Fig. 4.

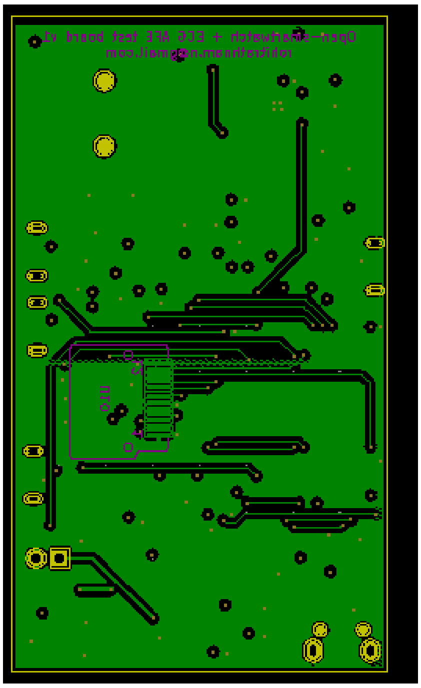
- Decoupling capacitors for all of the devices were placed as close as possible to the supply pins and vias connected to the respective layers.

- The ECG IC and the ADC were placed in a separate section of the board to minimise noise. A split ground plane was avoided for simplicity. The trace length and layer changes were minimised as much as possible.

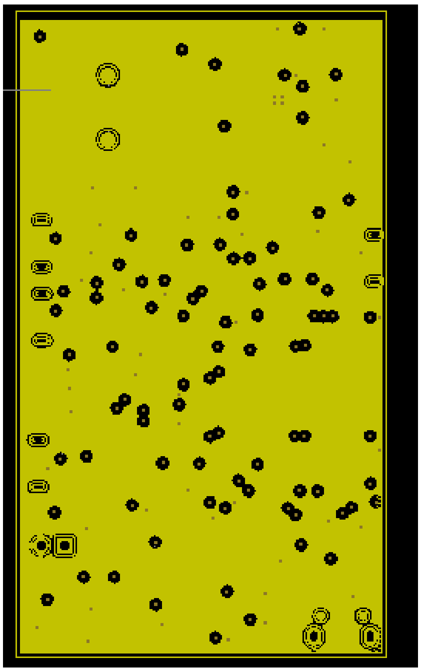
- Signal traces were 0.25mm wide and power traces were 0.5mm / 1mm



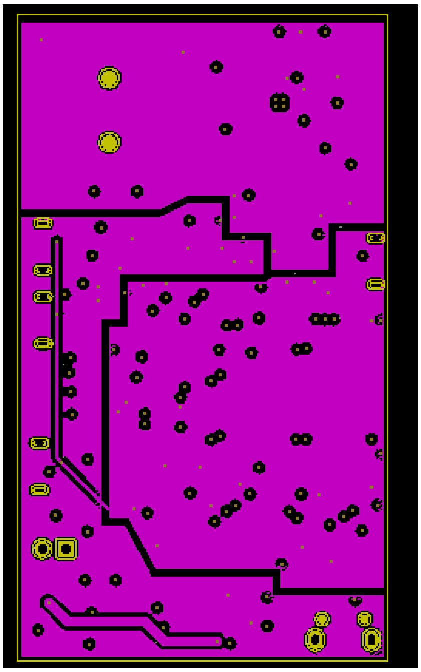
(a) Top layer 1



(b) Bottom layer 4



(c) Inner layer 2 - GND



(d) Inner layer 3 - PWR

Figure 3: PCB layers

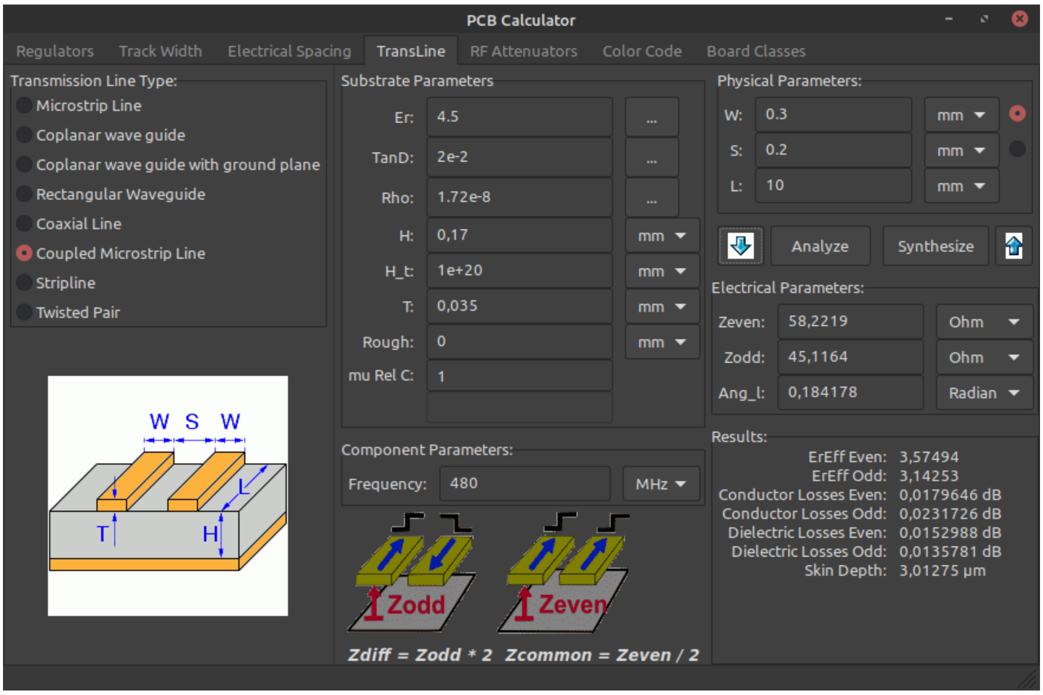


Figure 4: Differential pair trace impedance calculation

traces depending on the pad size. Routing under components was minimised as much as possible.

3.2 PCB Layers and routing

Refer Fig 3 for individual layers.

3.2.1 Top Layer 1

The top layer consists of all the components except the FPC connector for the display. Most of the routing to nearby components and long vertical traces were kept in the top layer.

3.2.2 Bottom Layer 4

The bottom layer consists of mainly of the FPC connector for the display long horizontal traces. The rest was polygon filled with GND.

3.2.3 Inner Layer 2

This layer consists of the ground plane. Care was taken to minimize or avoid slots in the ground plane under components and high frequency traces (SPI, I2C, USB).

3.2.4 Inner Layer 3

This layer was used for routing power. 3 fill zones were created - consisting of 3V3 (digital supply), A3V3 (analog supply) and VCC (supply to regulators). The slots created in this layer might lead to electromagnetic emission, but most of the slots area is covered by the GND fill from other layers to mitigate this.

3.3 Fabrication Outputs

The results of the DRC are shown in Fig.5. The Gerber files are attached to this submission, which was verified with the SeedStudio Gerber viewer as shown in Fig. 6. The bill of materials csv file and ibom.html is also included in the submitted zip folder.

References

[1] P. Smith, "Open-smartwatch." https://open-smartwatch.github.io/. Accessed on 2021-05-20.

[2] SparkFun, "Sparkfun sensor cable accessory." https://www.sparkfun.com/products/12970. Accessed on 2021-05-20.

[3] AnalogDevices, "Ad8232 datasheet." https://www.analog.com/media/en/technical-documentation/data-sheets/ad8232.pdf. Accessed on 2021-05-20.

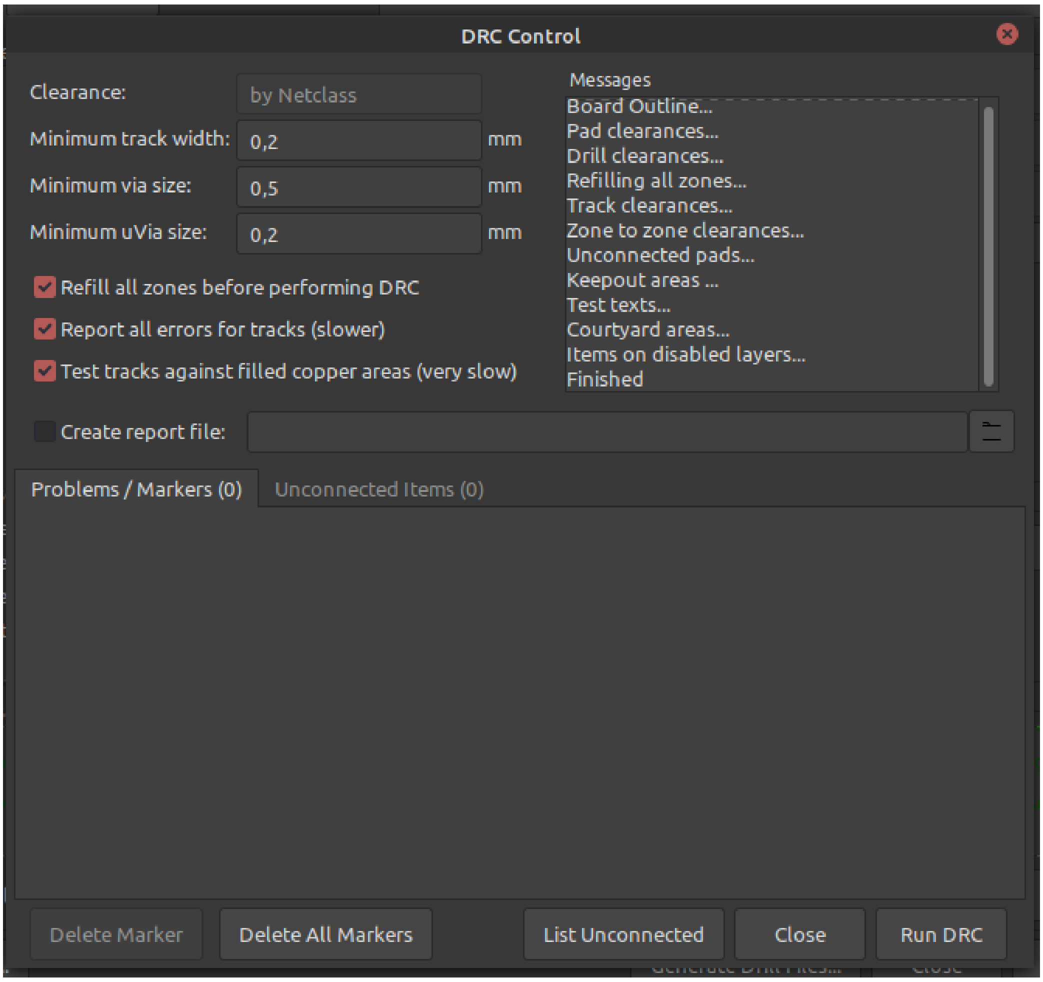


Figure 5: DRC results

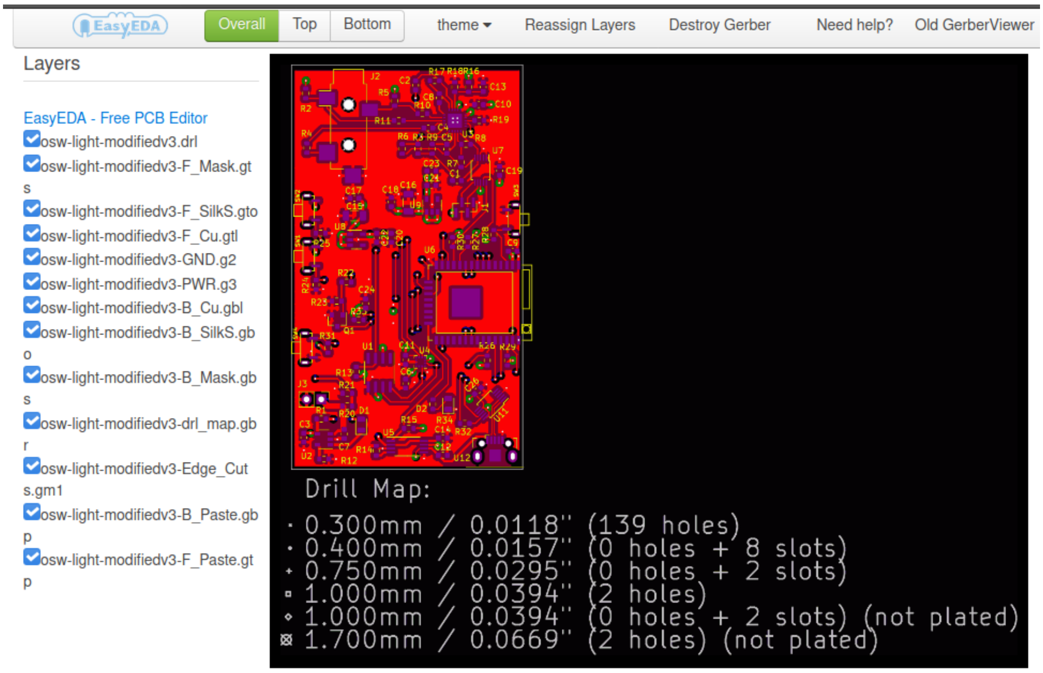


Figure 6: Seedstudio Gerber viewer