Final Report
ELEC6027: VLSI Design Project

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Contents

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Chapter 1

Introduction

Overview of the report

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Chapter 2

Architecture

Design of the datapath architecture.

Refer to the research done and how this influenced the design

Incl. diagram

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Chapter 3

Instruction Set

Design of the instruction set
- Allocation of opcodes etc
- Refer to research done and original thinking
- Feel free to use parts from the programmers guide.

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Chapter 4

Design and Implementation

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4.1 Register Block

Design of whole module, including circuit diagram
- Use of hierarchy / blocks - i.e. bit sliced, decoder
- Design of slice,
- Design of decoder,
- Design of block,
- Layout in silicon

4.2 Program Counter

Design of whole module, including circuit diagram
- Use of hierarchy / blocks - i.e. bit sliced, decoder
- Design of slice,
- Design of decoder,
- Design of block,
- Layout in silicon

4.3 Instruction Register

Design of whole module, including circuit diagram
- Use of hierarchy / blocks - i.e. bit sliced, decoder
- Design of slice,

Design of decoder,
Design of block,
Layout in silicon

4.4 Arithmetic Logic Unit

Design of whole module, including circuit diagram
Use of hierarchy / blocks - i.e. bit sliced, decoder
Design of slice,
Design of decoder,
Design of block,
Layout in silicon

4.5 Datapath

Design of whole module, including circuit diagram
Use of hierarchy / blocks - i.e. bit sliced, decoder
Design of slice,
Design of decoder (slice 17),
Design of block,
Layout in silicon

4.6 Controller

Design of - simple statemachine?
Control signals - description, use of type defs?
Description of main states:
Fetch
Execute
Interrupt
Implementation of interrupts (flags, enable...)
Synthesis and layout - I/O config, magic vs Ledit maybe?

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4.7 CPU

Overall layout
- pad ring size
- positioning of control and datapath
- power routing
- anything else?

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Chapter 5

Testing

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5.1 Register Block

Include Sub tests - of slice and decoder (if app)
Explain tests - what is done
why it is done.
How it verifies everything - why it is complete
Show simulation results

5.2 Program Counter

Include Sub tests - of slice and decoder (if app)
Explain tests - what is done
why it is done.
How it verifies everything - why it is complete
Show simulation results

5.3 Instruction Register

Include Sub tests - of slice and decoder (if app)
Explain tests - what is done
why it is done.
How it verifies everything - why it is complete
Show simulation results

5.4 Arithmetic Logic Unit

Include Sub tests - of slice and decoder (if app)
Explain tests - what is done
why it is done.
How it verifies everything - why it is complete
Show simulation results

5.5 Datapath

Include Sub tests - of slice and decoder (if app)
Explain tests - what is done
why it is done.
How it verifies everything - why it is complete
Show simulation results

5.6 Controller

Include Sub tests - of slice and decoder (if app)
Explain tests - what is done
why it is done.
How it verifies everything - why it is complete
Show simulation results

5.7 CPU

Include Sub tests - of slice and decoder (if app)
Explain tests - what is done
why it is done.
How it verifies everything - why it is complete
Show simulation results

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Chapter 6

Conclusion

Generic concluding marks

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Appendix A

Project Management

Use of git
    regular meetings

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Appendix B

Division of Labour

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	Task	Percentage Effort on task			
	ECSID:	hl13g10	ajr2g10	mw20g10	arr1g13
1	Initial Design	100	0	0	0
2	Verilog Behavioural Model	100	0	0	0
3	Multiply Program	100	0	0	0
4	Magic Datapath	100	0	0	0
4.1	Registers	100	0	0	0
4.2	Program Counter	100	0	0	0
4.3	Instruction Register	100	0	0	0
4.4	ALU	100	0	0	0
5	Verilog Cross Simulation	100	0	0	0
6	Control Unit Synthesis	100	0	0	0
7	Magic Control Unit	100	0	0	0
8	Final Floorplanning, Placement and Routing	100	0	0	0
9	Factorial Program	100	0	0	0
10	Random Program	100	0	0	0
11	Interrupt Program	100	0	0	0
11	Verilog Final Simulations and Cadence DRC	100	0	0	0
12	Assembler	100	0	0	0
13	Programmer's Guide Documentation	100	0	0	0
13.1	Architecture	100	0	0	0
13.2	Assembler	100	0	0	0
13.3	Instruction Set	100	0	0	0
13.4	Programming Tips	100	0	0	0
13.5	Programs	100	0	0	0
13.6	Register Description	100	0	0	0
13.7	Simulation	100	0	0	0
14	Final Report	100	0	0	0
14.1	Introduction	100	0	0	0
14.2	Architecture	100	0	0	0
14.3	Instruction Set	100	0	0	0
14.4	Implementation	100	0	0	0
14.5	Testing	100	0	0	0
14.6	Conclusion	100	0	0	0
14.7	Project Management	100	0	0	0
	OVERALL EFFORT	100	0	0	0

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