Final Report
ELEC6027

Team R4

17th April, 2014

Chapter 1

Introduction

Overview of the report

Chapter 2

Architecture

Design of the datapath architecture.

Refer to the research done and how this influenced the design

Incl. diagram

Chapter 3

Instruction Set

Design of the instruction set
- Allocation of opcodes etc
- Refer to research done and original thinking
- Feel free to use parts from the programmers guide.

Chapter 4

Design and Implementation

4.1 Register Block

Design of whole module, including circuit diagram
- Use of hierarchy / blocks - i.e. bit sliced, decoder
- Design of slice,
- Design of decoder,
- Design of block,
- Layout in silicon

4.2 Program Counter

Design of whole module, including circuit diagram
- Use of hierarchy / blocks - i.e. bit sliced, decoder
- Design of slice,
- Design of decoder,
- Design of block,
- Layout in silicon

4.3 Instruction Register

Design of whole module, including circuit diagram
- Use of hierarchy / blocks - i.e. bit sliced, decoder
- Design of slice,

Design of decoder,
Design of block,
Layout in silicon

4.4 Arithmetic Logic Unit

Design of whole module, including circuit diagram
Use of hierarchy / blocks - i.e. bit sliced, decoder
Design of slice,
Design of decoder,
Design of block,
Layout in silicon

4.5 Datapath

Design of whole module, including circuit diagram
Use of hierarchy / blocks - i.e. bit sliced, decoder
Design of slice,
Design of decoder (slice 17),
Design of block,
Layout in silicon

4.6 Controller

Design of - simple statemachine?
Control signals - description, use of type defs?
Description of main states:
Fetch
Execute
Interrupt
Implementation of interrupts (flags, enable...)
Synthesis and layout - I/O config, magic vs Ledit maybe?

4.7 CPU

Overall layout
- pad ring size
- positioning of control and datapath
- power routing
- anything else?

Chapter 5

Testing

5.1 Register Block

Include Sub tests - of slice and decoder (if app)
Explain tests - what is done
why it is done.
How it verifies everything - why it is complete
Show simulation results

5.2 Program Counter

Include Sub tests - of slice and decoder (if app)
Explain tests - what is done
why it is done.
How it verifies everything - why it is complete
Show simulation results

5.3 Instruction Register

Include Sub tests - of slice and decoder (if app)
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5.4 Arithmetic Logic Unit

Include Sub tests - of slice and decoder (if app)
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5.5 Datapath

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Include Sub tests - of slice and decoder (if app)
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5.7 CPU

Include Sub tests - of slice and decoder (if app)
Explain tests - what is done
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Chapter 6

Conclusion

Generic concluding marks

Appendix A

Project Management

Use of git
    regular meetings

Appendix B

Division of Labour

include div of labour table here. Include report writing sections too.