Declaration of Specialisms

		Week 4			Week 5			Week 6				Week 7			Week 9	Week 10		Week 12
Team	Name	Research Report 19 Feb 4 pm	Draft Design 20 Feb 12 noon		Initial Design 26 Feb 4 pm		Behavioural Model (4 instructions) 27 Feb 2 pm	Behavioural Model 5 Mar 4 pm		Basic Datapath Simulation (ALU + Registers) 6 Mar 12 noon	*extra* 7 Mar 4 pm	Cross Simulation 12 Mar 4 pm		Placed and Routed Control Unit Simulation 13 Mar 12 noon	Placed and Routed Pad Ring Simulation 27 Mar 12 noon	Design Submission 2 May 4 pm		Project Report 13 May 4 pm
			Instruction Set	Datapath Diagram	Instruction Set	Datapath Diagram		Verilog Model	Multiplication Code			Magic Datapath	Verilog Control			Design Files	Programmer's Guide	
R4 ar	~~ajr2~~	ALL								~~✓~~	✓		✓		✓			ALL
	hl	ALL					✓	✓						✓		✓		ALL
	mw	ALL		✓		✓			✓							✓	✓	ALL
	~~dfk~~	ALL	✓		✓				~~✓~~	✓		✓						ALL
	~~XXX~~	~~ALL~~																~~ALL~~
	~~XXX~~	~~ALL~~																~~ALL~~

Interrupts Addition Deadline

arrlg13.

ajr - Verilog
hl - Verilog
mw - Prog.
ar - Magic