Lab Assignment Report 8

Part 1

Course: COL215 – Digital Logic & System Design

Department of Computer Science & Engineering, IIT Delhi
Semester III, 2025-26

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Introduction:

In this assignment's part 1,

- we created two single port ROM, bg_rom for background of 12bits width and 38400 depth and main_car ROM of 12 bits width and 224 depth.
- We also Removed the pink colour from the car hitbox and set it to the background color.
- Simulated the design and got the data as follows:-

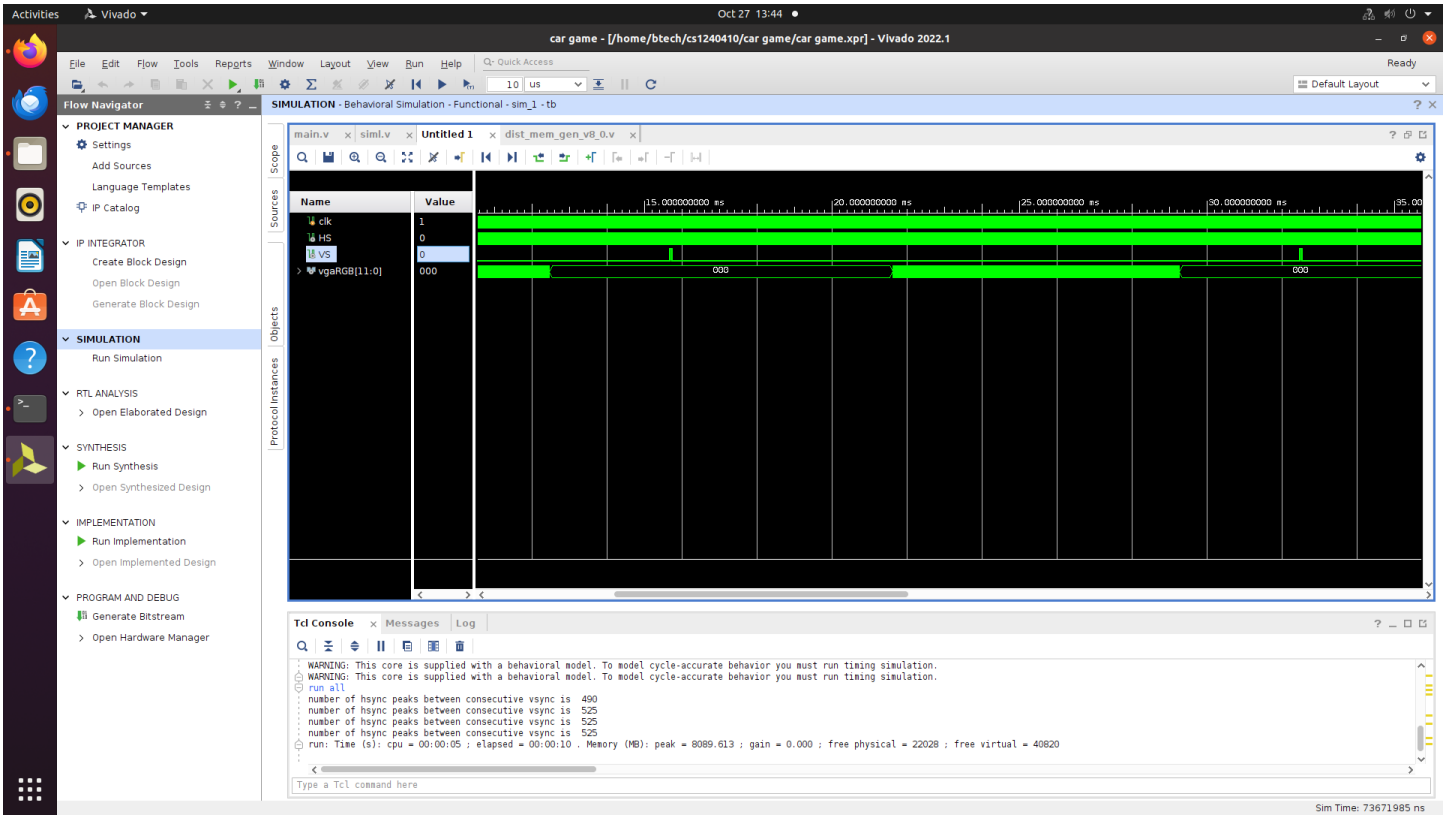
  Number of clock cycles between two VS pulses-1680000

  Number of clock cycles between two HS pulses-3200

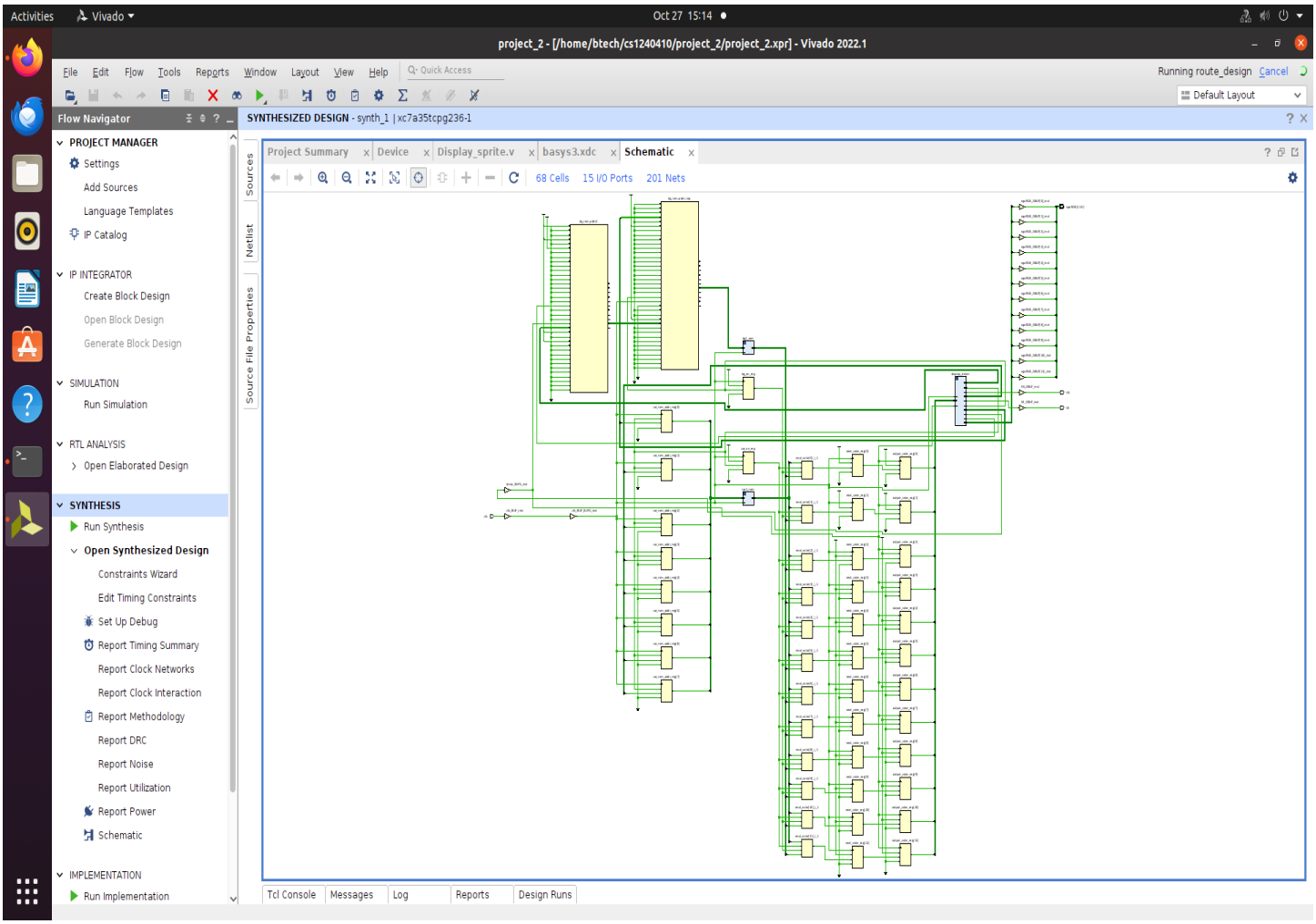
  Number of HS pulses between two consecutive VS pulses-525

- Synthesized and implemented the given Display_sprite module and validated it by loading it onto FPGA and checking the image on the VGA output to the display(without pink box).

Simulation Snapshots:



Generated Schematics:



Synthesis Report:

Resource	Used	Available	Utilization (%)
LUTs	591	20,800	2.84 %
Flip-Flops (FFs)	85	41,600	0.20 %
BRAMs	0	50	0.00%
DSPs	2	90	2.22%