Rohit Shakya

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EDUCATION

Indian Institute of Technology (IIT) Delhi *2024-2028*
B.Tech. in Computer Science and Engineering
CGPA: 9.027/10.0
SGPA: 9.474/10.0

EBENEZER SENIOR SECONDARY SCHOOL *2024*
All India Senior School Certificate Examination (XII Grade, CBSE)
Percentage: 92%

Kendriya Vidyalaya *2022*
All India Secondary School Examination (X Grade, CBSE)
Percentage: 94.5%

SCHOLASTIC ACHIEVEMENTS

Ranked among the top 1% of over 150,000 candidates in JEE Advanced
Ranked among the top 0.1% of over 12,32,000 candidates in JEE Mains

ACADEMIC PROJECTS

- **File Management System (Time-Travelling File System)** Prof. Rohit vaish, IITD
  - Developed a simplified in-memory **version control system inspired by Git** using C++, modeling file versioning and branching logic.
  - Implemented complex data structures (**Trees, HashMaps, and Heaps**) from scratch to manage file metadata, history, and system-wide analytics.
- **SocialNet Simulator** Prof. Rajendra Kumar, IITD
  - Developed 'SocialNet Simulator' — a command-line social network backend in C++ implementing self-built Graph and AVL Tree data structures to manage users, friendships, and posts efficiently.
- **Digital Logic Design: Linked List** Prof. Preeti R. panda, IITD
  - Implemented a parameterized singly linked list in **Verilog HDL using reg arrays for data storage and explicit index pointers to support insertion, deletion,** and traversal operations within hardware constraints.
  - Integrated **overflow and underflow** detection logic and validated the design on an **FPGA board**, displaying linked list data via **7-segment displays.**
- **Digital Logic Design: ROM/RAM Control and Vector Processing** Prof. Preeti R. panda, IITD
  - Designed and synthesized a **memory control unit** in **Verilog** on an **FPGA (Basys3)**.
  - Integrated ROM, dual RAMs, and registers to perform a parallel **1024-element vector addition** with real-time output on 7-segment displays.
- **Digital Logic Design: Car Arcade Game on Basys3 board** Prof. Preeti R. panda, IITD
  - Developed a car racing arcade game on the Basys 3 FPGA board, implementing **VGA interfacing, sprite rendering, and animation using Verilog HDL**.
  - Designed and simulated **Finite State Machines (FSMs)** for car movement, /**collision detection, and pseudo-random rival generation**, achieving smooth real-time gameplay logic

RELEVANT COURSEWORK

Computer Science: Introduction to computer science, Data structures and algorithm, Digital logic and system design, programming languages*, computer networks*, signals and systems*,computer Architecture*,Design practices*.

Mathematics: Introduction to Probability Theory and Stochastic Processes, Discrete maths, Linear algebra and differential equations, Calculus.

Miscellaneous: Introduction to Electrical engineering, Introduction to Engineering Visualization, Electromagnetism and Quantum mechanics.

* (to be done by April 2026)

TECHNICAL SKILLS

Languages: C++, Python, Verilog
Hardware: FPGA
Software/Tools: FreeCAD, LaTeX, Xilinx Vivado