Gangapuram Varun Reddy

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Skills

Hardware Description Languages: Verilog HDL
Verification Languages: System Verilog (SV), Universal Verification Methodology (UVM)
Programming Languages: C, Python
EDA Tools: Synopsys VNC, EDA Playground

Professional Training

Design Verification Trainee July 2025 - Present

SumedhaIT, JNTU - Hyderabad

- Underwent intensive professional training focused on the VLSI Design and Verification lifecycle.
- Developed expertise in Verilog HDL for writing Register Transfer Level (RTL) code for digital modules like RAM and FIFO.
- Mastered SystemVerilog (SV) for building robust verification environments, focusing on constrained random stimulus and functional coverage.
- Utilized Synopsys VCS for high-performance simulation and debugging of complex digital designs.
- Applied advanced verification techniques, including waveform analysis and directed testcases, to ensure data integrity and functional correctness.

Education

Maturi Venkata Subba Rao Engineering College Dec 2021 - May 2025
B.E. in Electronics and Communication & Engineering ***Percentage: 64.4%***

Narayana Junior College Oct 2019 - May 2021
Intermediate ***Percentage: 89.4%***

Projects

Synchronous FIFO Design

- Implemented a Synchronous FIFO in Verilog using read/write pointers and a memory array.
- Developed control logic for full and empty conditions.
- Designed synchronous read/write operations on a single clock.
- Verified data flow, boundary conditions, and pointer behavior through testbench simulations.

Packet Decoder

- Designed an RTL-based module to extract and process packets into header, payload, and CRC fields.
- Implemented logic for packet validation, payload routing, and output signaling.
- Ensured data integrity through CRC/parity checking.
- Verified functional behavior using waveform analysis and directed testcases.
- Performed advanced verification using SystemVerilog to ensure robust design performance and coverage.

Awards and Certificates

- **SumedhaIT:** DV Engineer Training Certificate.