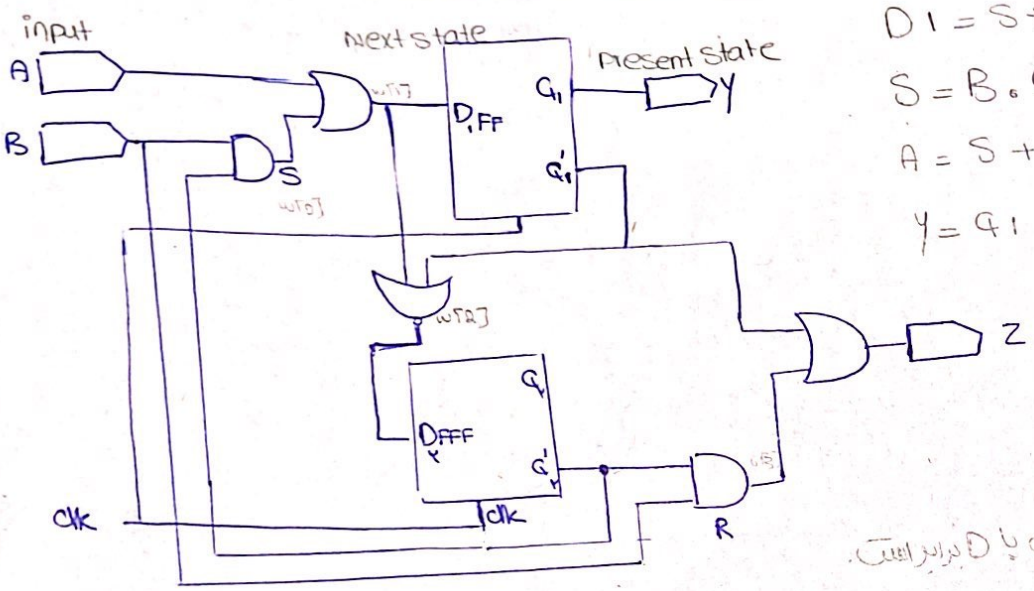

$D_1 = S + A$

$S = B \cdot Q_2'$

$A = S + B$

$Y = Q_1$

$D_2 = (Q_1' + D_1)'$

$R = Q_2' \cdot B$

$Z = Q_1' \cdot R =$

$Z = Q_1' + (Q_2' \cdot B)$

D-FF ←

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

← خروجی با D برابر است.

present state		inputs				Next state		outputs	
$Q_1(t)$	$Q_2(t)$	A	B	R	S	$Q_1(t+1)$	$Q_2(t+1)$	Y	Z
0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	1	1	0	0	1
0	0	1	0	0	0	1	0	0	1
0	0	1	1	1	1	1	0	0	1
0	1	0	0	0	0	0	0	0	1
0	1	0	1	0	0	0	0	0	1
0	1	1	0	0	0	1	0	0	1
0	1	1	1	0	0	1	0	0	1
1	0	0	0	0	0	1	0	1	0
1	0	0	1	1	1	1	0	1	1
1	0	1	0	0	0	1	0	1	0
1	0	1	1	1	1	1	0	1	1
1	1	0	0	0	0	0	0	1	0
1	1	0	1	0	0	0	0	1	0
1	1	1	0	0	0	1	0	1	0
1	1	1	1	0	0	1	0	1	0

این مدار Moore است

زیرا خروجی‌های مدار وابسته به clock یا فلیپ‌فلاپ است

```
module seq_circuit (
    input rst,
    input clk,
    input a,
    input b,
    output y,
    output z
);

    wire [3:0]w;
    wire qp1, qp2;
    and #10 g1(w[0], b, qp2);
    or  #10 g2 (w[1], a, w[0]);
    nor #10 g3 (w[2], w[1], qp1);
    and #10 g4 (w[3], b, qp2);

    dflop_negedge g0 (.din[w1], .clk(clk), .rst(rst), .qout(y), .qbout(qp1
                  g1 (.din (w[2]), .clk(clk), .rst(rst)) .qout(), .qbout
                                                          (qp2

    or #10 g7 (z, qp1, w[3]);
```

```
module dflop_negedge (
    input rst,
    input clk,
    input  din,
    out reg qout
); output qbout

    always @ (negedge clk or posedge rst)
      #5
       begin
          if ( rst == 1'b1 )
              qout <= 1'b1;
          else
              qout <= din;
       end
         assign qbout = ~qout;
    endmodule
```