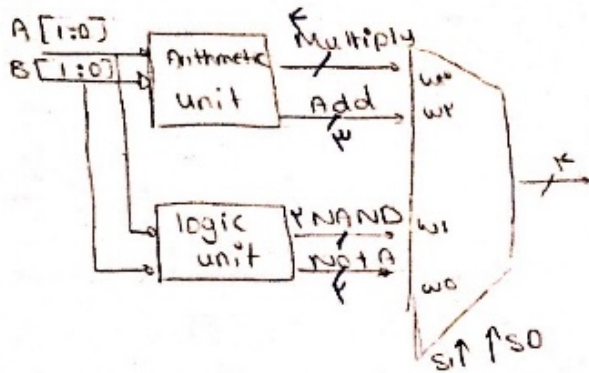
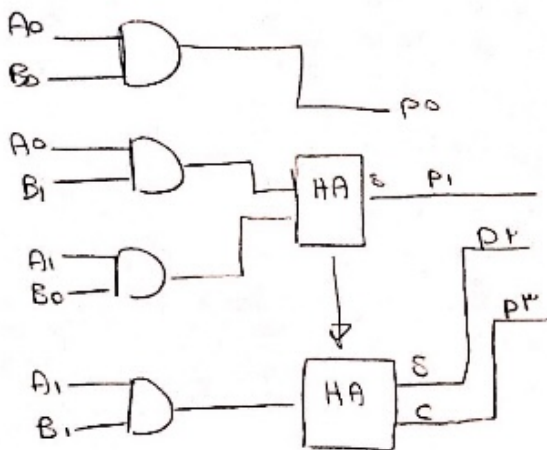
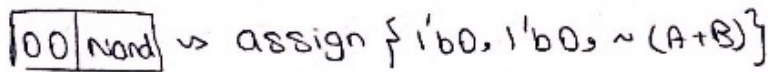
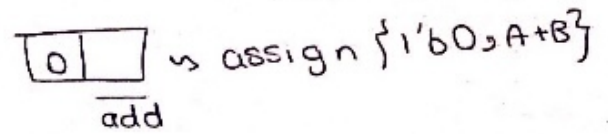
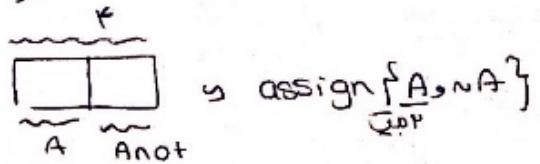


ALU → (۲۲/۱۵/۱۰/۵/۱) انتخاب
 → (۲) منطق (NOR/Not/Or/and)
 → (۳) کنترل



بلایه و دروسها Multiplexer با سبک بر این

۲ بیت به هر پورت و ۱ بیت به سبکها اضافه می‌شود



module multiplexer (

input [3:0] w3,
 input [3:0] w2,
 input [3:0] w1,
 input [3:0] w0,
 input [1:0] sel,
 output [3:0] y

);

assign y = sel[1] ? (sel[0] ? w3 : w2) : (sel[0] ? w1 : w0);

```
module alu {
    input [1:0] A,
    input [1:0] B,
    input [1:0] sel,
    output [3:0] y
}
```

);

wire [3:0] Add;

wire [3:0] Not;

wire [3:0] NAND;

wire [3:0] Multiply;

assign Add = {1'b0, 1'b0, A} + {1'b0, B};

assign Not = {A, ~A};

assign NAND = {1'b0, 1'b0, ~(A & B)};

assign Multiply = {1'b0, 1'b0, A} * {1'b0, 1'b0, B};

multiplexer mux (Multiply, Add, NAND, Not, sel, y);

endmodule

1 Half Adder) 870556

```
module all {
  input [1:0] A,
  input [1:0] B,
  input [1:0] sel,
  output [3:0] y;
};

wire [2:0] w;
wire [3:0] multiple;
wire c;

// not
wire [3:0] Not;
wire [1:0] anot;
assign anot = ~A;
assign Not = {A, anot};
```

```
# nand
wire [3:0] Nand;
wire [1:0] w3;
assign w3 = N(A, B);
assign Nand = {1'b0, 1'b0, w3};
```

```
# add
wire [3:0] Add;
wire [2:0] w2;
assign w2 = (A + B);
assign Add = {1'b0, w2};
```

```
# Multiple
wire [2:0] w;
wire [3:0] Multiple;
wire c;

and g1(Multiple[0], A[0], B[0]),
g2(w[0], A[1], B[0]),
g3(w[1], A[0], B[1]),
g4(w[2], A[1], B[1]);
```

```
'halfAdder
HA1(w[0], w[1], Multiple[1], c),
HA2(w[2], c, Multiple[2], Multiple[3]);
multiplexer mux(Multiple, Add, Nand, Not, sel, y);
endmodule
```

module halfAdder(

```
  input A,
  input B,
  output sum,
  output c;
```

```
);
```

```
Xor g1(sum, A, B);
and g2(c, A, B);
```

endmodule

module multiplexer(

```
  input [3:0] w0,
  input [3:0] w1,
  input [3:0] w2,
  input [3:0] w3,
  input [1:0] sel,
  output [3:0] y;
```

```
);
```

```
assign y = sel[1] ? (sel[0] ? w2 : w1) : (sel[0] ? w0 : w3);
```