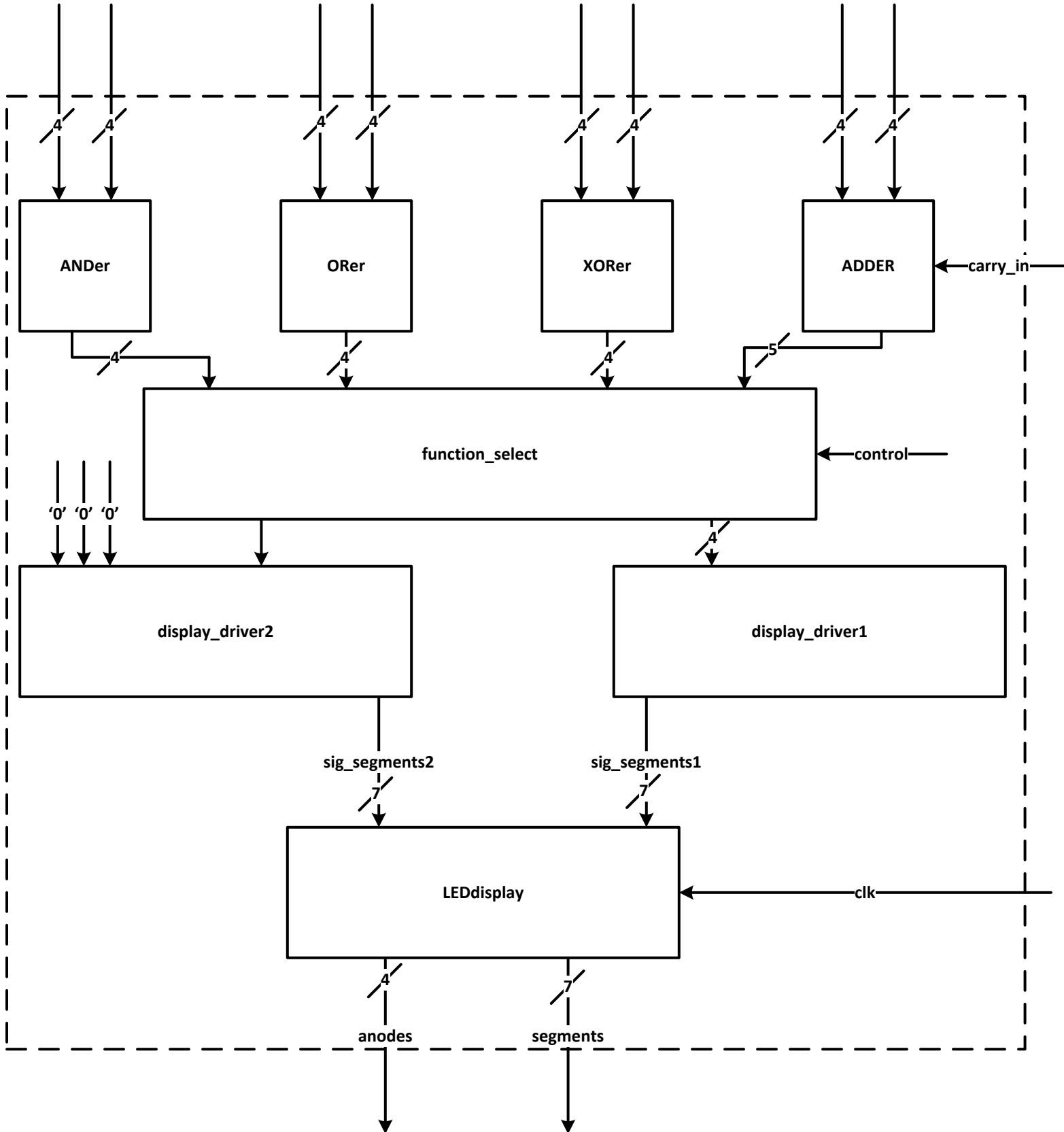


# ALU



**Inputs:** SW<0>, SW<1>, ..., SW<7>, carry\_in, clk, control

**Outputs:** segments<0>, segments<1>, ..., segments<6>, anodes<0>, anodes<1>, ..., anodes<3>

**Internal signals:** out\_and, out\_or, out\_xor, out\_adder, out\_select, sig\_segments1, sig\_segments2