

2023 超大型積體電路電腦輔助設計概論

2023 Introduction to VLSI CAD

Lab 12

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※作業要求的圖請使用**電腦截圖程式**截取，請勿用手機拍照的方式繳交

※Report 檔請以 pdf 的格式繳交

- One bit fulladder
 - Presim
 - 請截取 terminal 顯示 job concluded 的圖



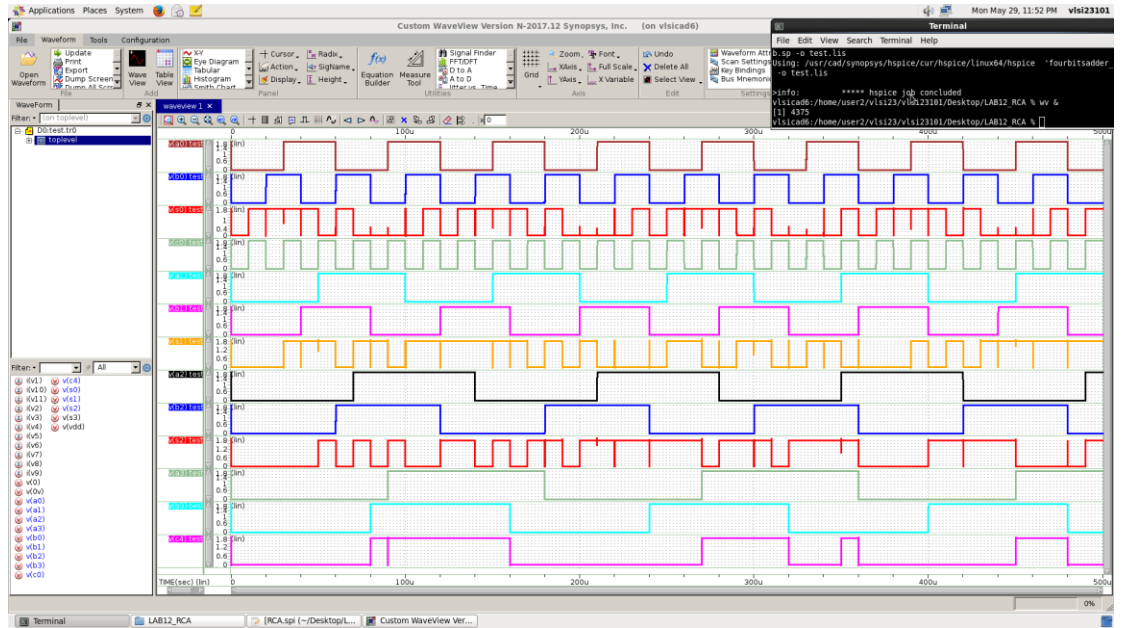
```
connection with this process to deliver software updates and pursue software pir
ates and infringers.

Display localhost:34.0 ==> Current mode : TrueColor
The PseudoColor mode is not available under current setting. Switch to use Tr
ueColor mode.
*** Limitation: Blinking is not supported under TrueColor mode.
fontPath(SPS FONT PATH) = /usr/cad/synopsys/laker/cur/TTFont
Feature "Laker FPD L2" checked out successfully (Elapsed Time: 0.16s)
vlsicad6:/home/user2/vlsi23/vlsi23101 % cd Desktop/
calibre/ lab11_post_halfaddr/ RCA_lvs.png
cic018.l* lab12/ rca.png
E94096110/ LAB12_RCA/ rca_post/
example/ lab7_I-9.5/ RCA_post_C.png
example.tar* lab8_total/ RCA_post_W.png
fourbitsadder_tb.sp- lab9_nand/ RCA_W.png
fourbitsadder_tb.sp- lab9_nor/ test.sp-
LAB/ lab9_nor_new/ test.sp
lab10_xor/ onebits_ORC.png vlsilab10/
lab10_xor_post/ onebits_LVS.png vlsilab11/
lab11_l/ onebits.png 未命名資料夾/
lab11_final/ RCA_C.png
lab11_post_dff/ rca_drc.png
vlsicad6:/home/user2/vlsi23/vlsi23101 % cd Desktop/lab12/
vlsicad6:/home/user2/vlsi23/vlsi23101/Desktop/lab12 % hspice -o test.lis
cic018.l* onebitadder.sp* test.lis
fulladder.sp* sxcmd.log test.pa0
onebitadder.sp- test.ic0 test.tr0
vlsicad6:/home/user2/vlsi23/vlsi23101/Desktop/lab12 % hspice one -o test.lis
onebitadder.sp- onebitadder.sp*
vlsicad6:/home/user2/vlsi23/vlsi23101/Desktop/lab12 % hspice onebitadder.sp -o t
est.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice 'onebitadder.sp' -o t
est.lis
>info: ***** hspice job concluded
vlsicad6:/home/user2/vlsi23/vlsi23101/Desktop/lab12 %
```

- 請截取 WaveView 中的波形

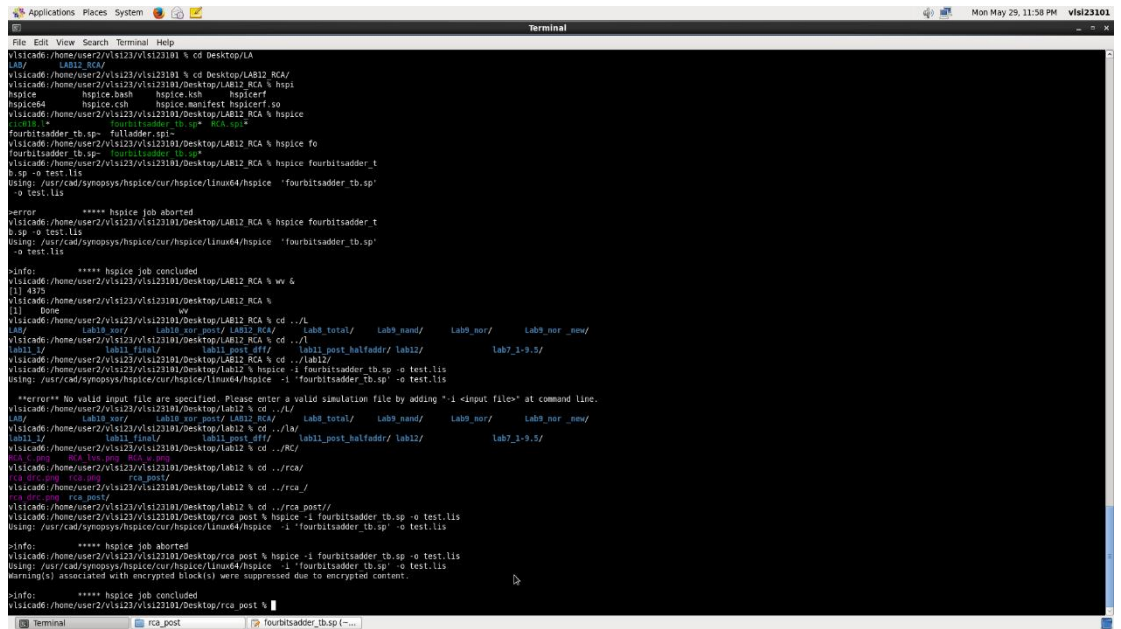
LVS

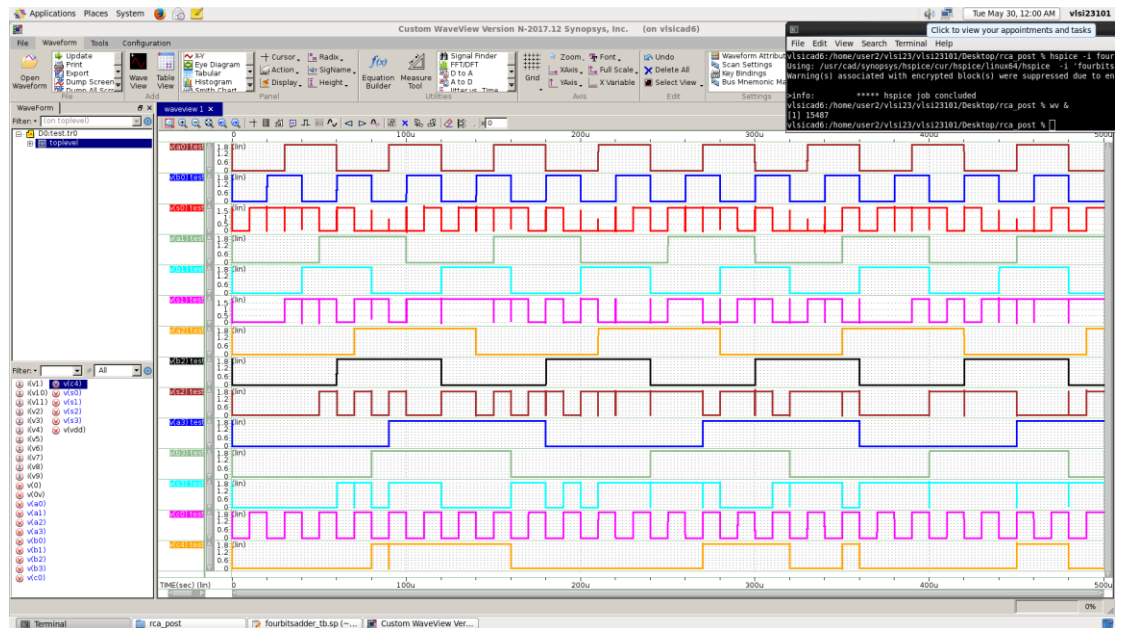
- 請截取 WaveView 中



的波形

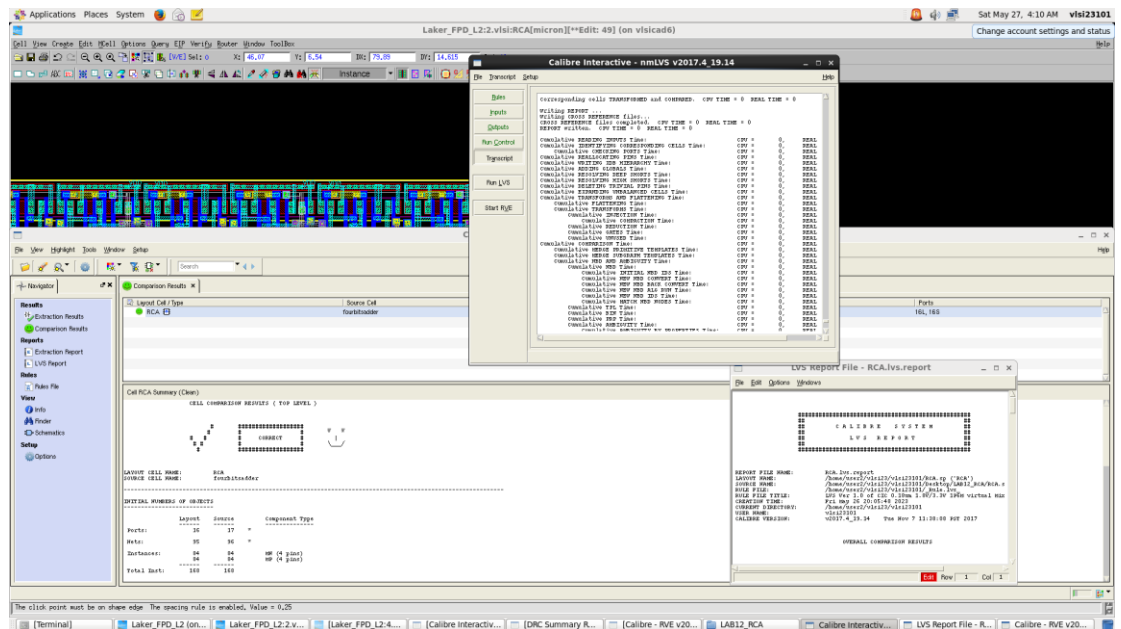
- Post-sim
 - 請截取 terminal 顯示 job concluded 的圖



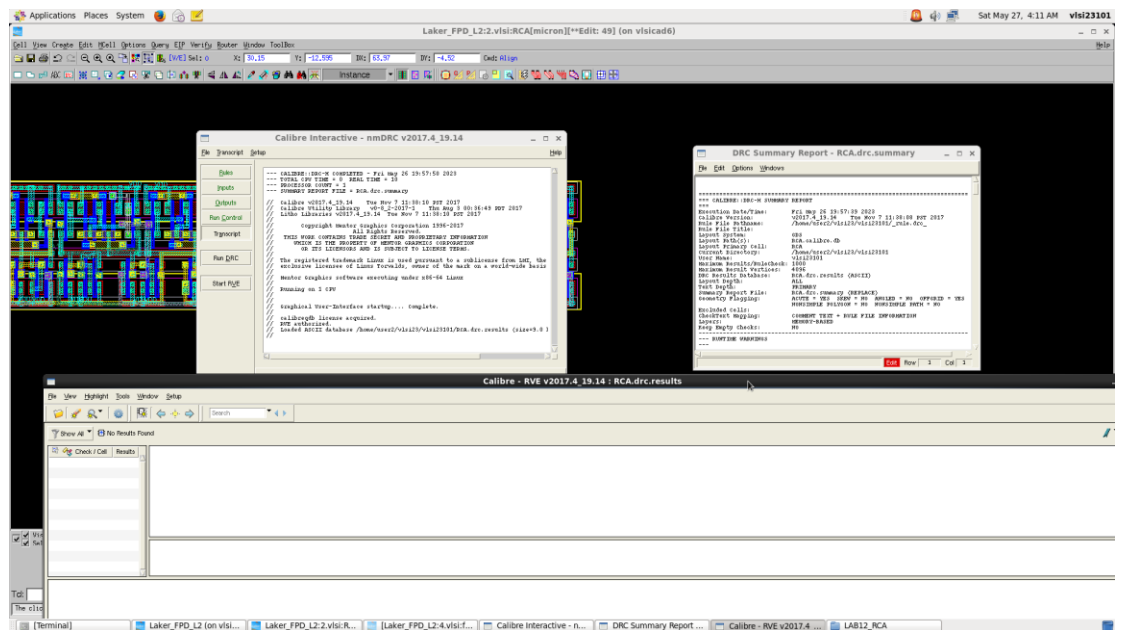


- 請截取 WaveView 中的波形
- DRC/LVS 結果

DRC

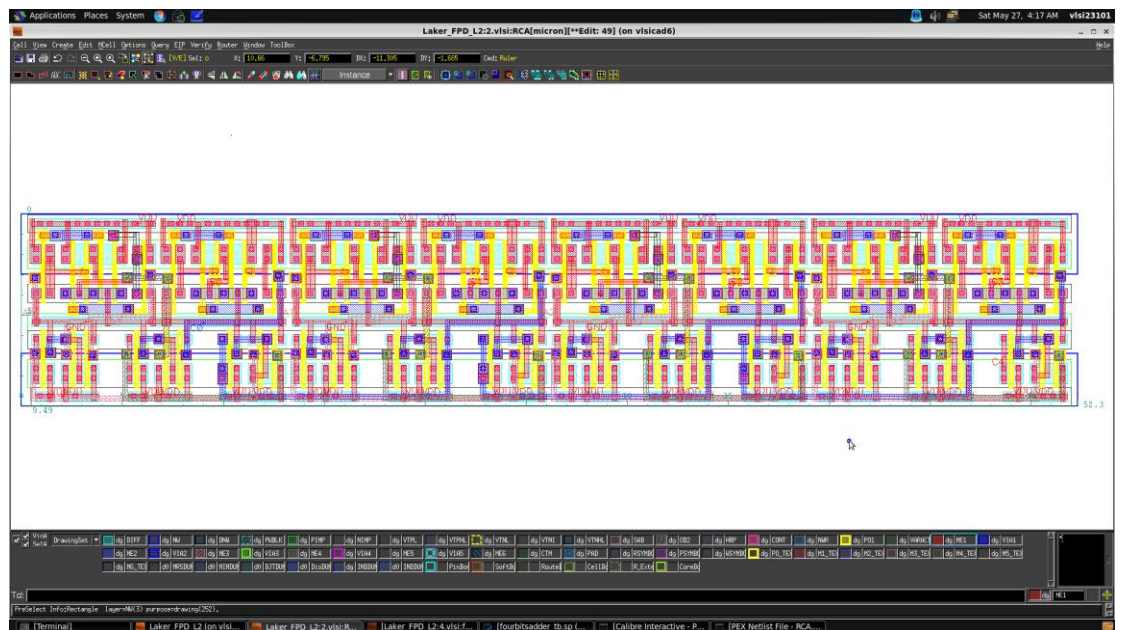


LVS



- Layout 截圖(顯示長寬)

$$9.49 \times 52.3 = 496.327$$



- 嘗試簡單說明 Presim 與 Post-sim 結果比較

整體看起來差不多，放大仔細觀察波型變化處，變化率 post 比 pre 比較小一點

- 心得討論

在這次 lab 中加強練習了不同元件間的連接，實作手感好很多。

過程中也學習並熟練使用許多 DRC 的小技巧，像是 nimp 和 pimp 可以共用，也透過這周將其他次 lab 畫的更好。