**National Cheng Kung University**

**Department of Electrical Engineering**

***Introduction to VLSI CAD (Spring 2023)***

**Lab Session 5**

**Synthesis of Sequential Logic and Some Tips**

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Student ID | | |
| 鄭智宇 | E94096110 | | |
| Practical Sections: | | Points | Marks |
| ProbA | | 30 |  |
| ProbB | | 35 |  |
| ProbC | | 35 |  |
| Notes | | | |

**Due Date: 14:59, March 22, 2023 @ moodle**

**Deliverables**

1. All Verilog codes including testbenches for each problem should be uploaded.

NOTE: Please **DO NOT** include source code in the paper report!

1. All homework requirements should follow the naming rule in this file hierarchy or you will not get the full credit.

NOTE: Please **DO NOT** upload waveforms!

1. Important! TA will use the command in Appendix A to check your design under SoC Lab environment, if your code can not be recompiled by TA successfully using the commands, you will not get the full credit.
2. **If you upload a dead body, which we cannot even compile, you will get NO credit!**
3. **All Verilog file before synthesizing should get at least 95% Superlint Coverage.**
4. Lab5\_Student\_ID.tar (English alphabet of Student\_ID should be **capital**.)

Lab5\_studentID.tar

Lab5\_studentID

studentID.docx

ProbA

det\_seq.v

det\_seq\_tb.v

det\_seq\_syn.v

det\_seq\_syn.sdf

ProbB

mini\_vending.v

mini\_vending\_tb.v

mini\_vending\_syn.v

mini\_vending\_syn.sdf

ProbC

pattern\_gen.v

pattern\_gen\_syn.v

pattern\_gen\_syn.sdf

pattern\_gen\_tb.v

Fig.1 File hierarchy for Homework submission

**Objectives:**

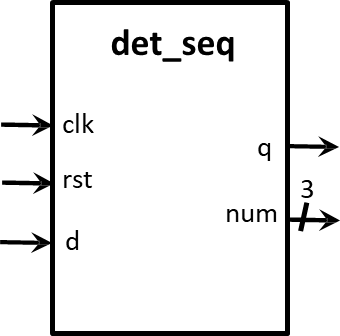
**To make you be familiar with some designs of sequential logic and Design Complier. You can follow this document to practice. Please show your best.**

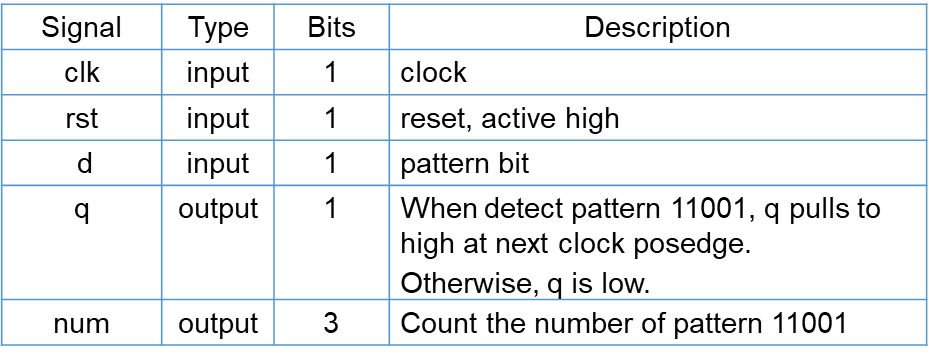
Note that you can extend the spacing if it is not enough for you to answer.

All labs should be synthesized, and clock period should not over 10 ns.

ProbA: Design a circuit “detecting pattern 11001”

1. **Design a pattern seq-detecting circuit that can be synthesized with moore machine. The following is det\_seq module’s specification. (Do NOT add or delete I/O ports, but you can change their behavior.)**





1. **Please describe your FSM in detail**

|  |
| --- |
| Explanation about your FSM |
| **有限狀態機從初始狀態開始，根據輸入信號d進行狀態轉移，直到達到最終狀態。具體而言，有限狀態機的狀態轉移圖如下：**  **s0狀態下，如果輸入信號d為1，則進入s1狀態，否則保持在s0狀態；**  **s1狀態下，如果輸入信號d為1，則進入s2狀態，否則返回到s0狀態；**  **s2狀態下，如果輸入信號d為1，則保持在s2狀態，否則進入s3狀態；**  **s3狀態下，如果輸入信號d為1，則返回到s1狀態，否則進入s4狀態；**  **s4狀態下，如果輸入信號d為1，則進入s5狀態，否則返回到s0狀態；**  **s5狀態下，如果輸入信號d為1，則返回到s2狀態，否則保持在s0狀態。** |

1. **After synthesizing your design, you may have some information about the circuit. Please fill in the following form.**

|  |  |  |
| --- | --- | --- |
| **Timing (slack)** | **Area (total cell area)** | **Power (total)** |
| **2.42** | **364.9** | **1.8079e-02mW** |

**一張含有 文字, 收據, 螢幕擷取畫面 的圖片

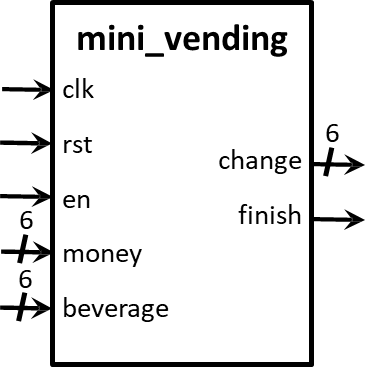
自動產生的描述**

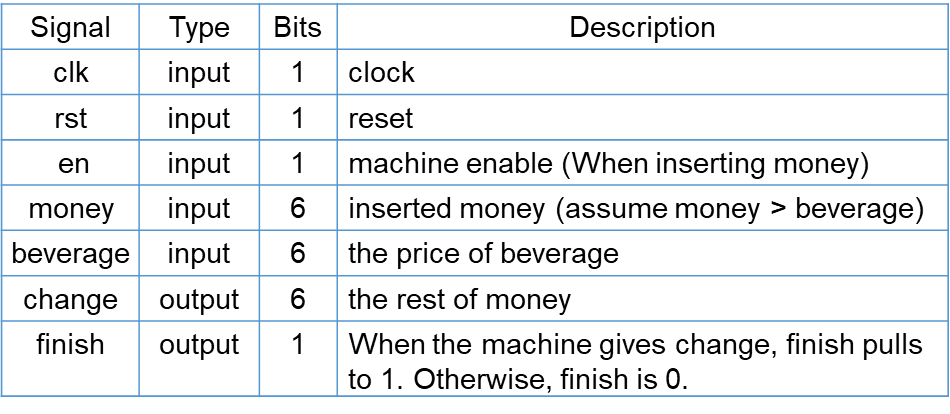
1. **Please attach your design waveforms.**

|  |
| --- |
| Your simulation result on the terminal. |
|  |
| Your waveform : |
|  |
| Explanation of your waveform : |
| **q : 當有限狀態機進入s5狀態時，輸出信號q被置為1，表示達到了目標狀態。**  **num :**  **1. 用於計算有限狀態機達到最終狀態的次數。**  **2. 每當有限狀態機進入s5狀態時，計數器num會自增1。**  **3. 計數器的值被輸出到輸出端口num中。**  **4. 當復位信號rst被觸發時，計數器num被清零。** |
| Superlint Coverage |
| Coverage : 100% |

ProbB: Design a mini vending machine

1. **Design a mini vending machine with moore machine. The following is mini vending machine module’s specification.** **(Do NOT add or delete any I/O ports, but you can change their behavior.)**





1. **Please describe your FSM in detail.**

|  |
| --- |
| Explanation about your FSM |
| **PHASE0：等待money輸入的狀態，若啟用輸入(en)，則轉移到PHASE1。**  **PHASE1：儲存beverage，直接轉移到PHASE2。**  **PHASE2：計算change，然後轉移到PHASE0。** |

1. **After synthesizing your design, you may have some information about the circuit. Please fill in the following form.**

|  |  |  |
| --- | --- | --- |
| **Timing (slack)** | **Area (total cell area)** | **Power (total)** |
| **1.12** | **641.61** | **3.9283e-02mW** |

**一張含有 資料表 的圖片

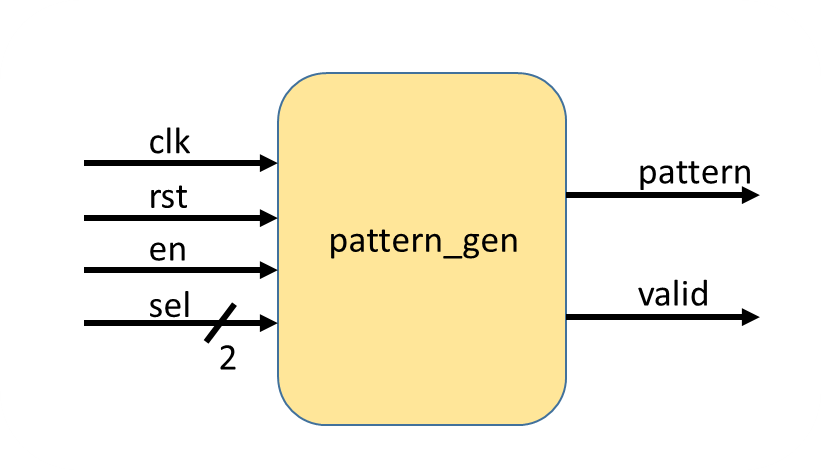
自動產生的描述**

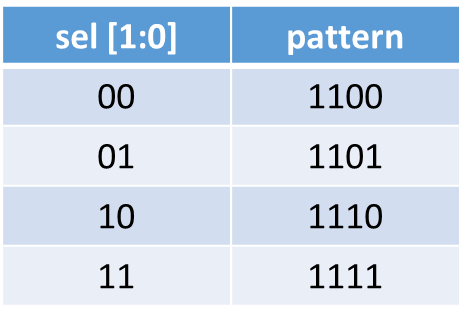
1. **Please attach your design waveforms.**

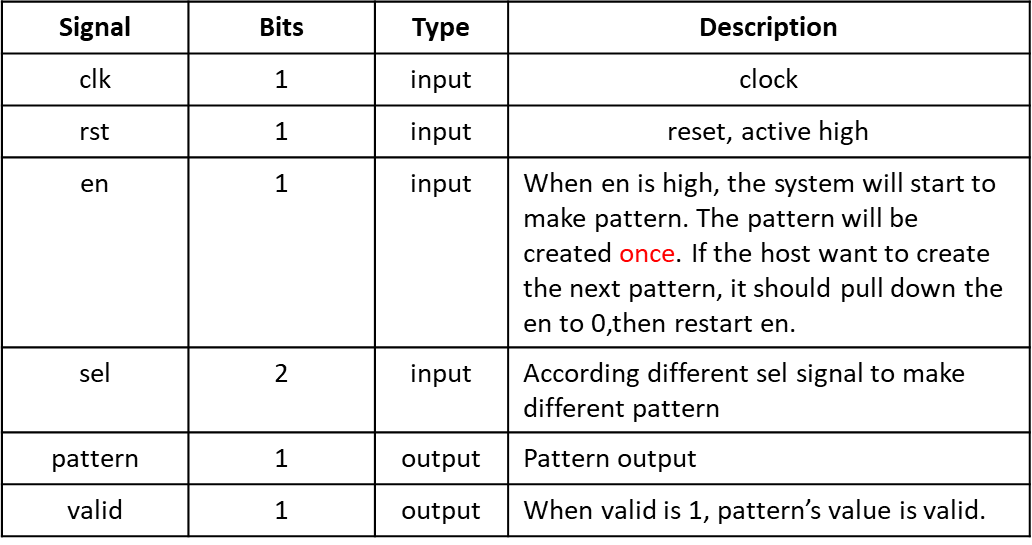
|  |
| --- |
| Your simulation result on the terminal. |
|  |
| Your waveform : |
|  |
| Explanation of your waveform : |
| **PHASE0=2'd0;**  **PHASE1=2'd1;**  **PHASE2=2'd2;**  **money\_s** 用來存儲投入的錢的暫存器，money\_s 用於計算剩餘的錢。  1.當狀態機處於 PHASE0 時， money\_s 就會被設置為 money。  2.當狀態機處於 PHASE1 時， money\_s 就會減去 beverage 的值。  **change :** 用於存儲需要找給使用者的錢。  1.當狀態機處於 PHASE2 時， change 就會被設置為 money\_s。  2.在其它狀態下， change就會被設置為 0。  **Finish :** 用於表示交易是否完成。  1.當狀態機處於 PHASE2 時， finish 就會被設置為 1，表示交易完成。  2.在其它狀態下， finish 就會被設置為 0。 |
| Superlint Coverage |
| 1 warning  Coverage : 98.5% |

ProbC: Design a pattern generator

1. **Design a pattern generator which can create pattern 1100, 1101, 1110, 1111 and use mealy machine. The following is pattern generator specification.**

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1. **Please describe your FSM in detail.**

|  |
| --- |
| Explanation about your FSM |
| **1. 分成 5 個狀態**  **2. 初始狀態為 INIT，在該狀態下如果 en 信號為 1，則轉移到 s0 狀態；否 則保持在 INIT 狀態。**  **3. 其餘狀態的轉移均為循環狀態，即 s0 -> s1 -> s2 -> s3 -> INIT –(en)> s0…。** |

1. **After synthesizing your design, you may have some information about the circuit. Please fill in the following form.**

|  |  |  |
| --- | --- | --- |
| **Timing (slack)** | **Area (total cell area)** | **Power (total)** |
| **3.61** | **162.95** | **1.1065e-02mW** |

**一張含有 文字, 收據, 螢幕擷取畫面 的圖片

自動產生的描述**

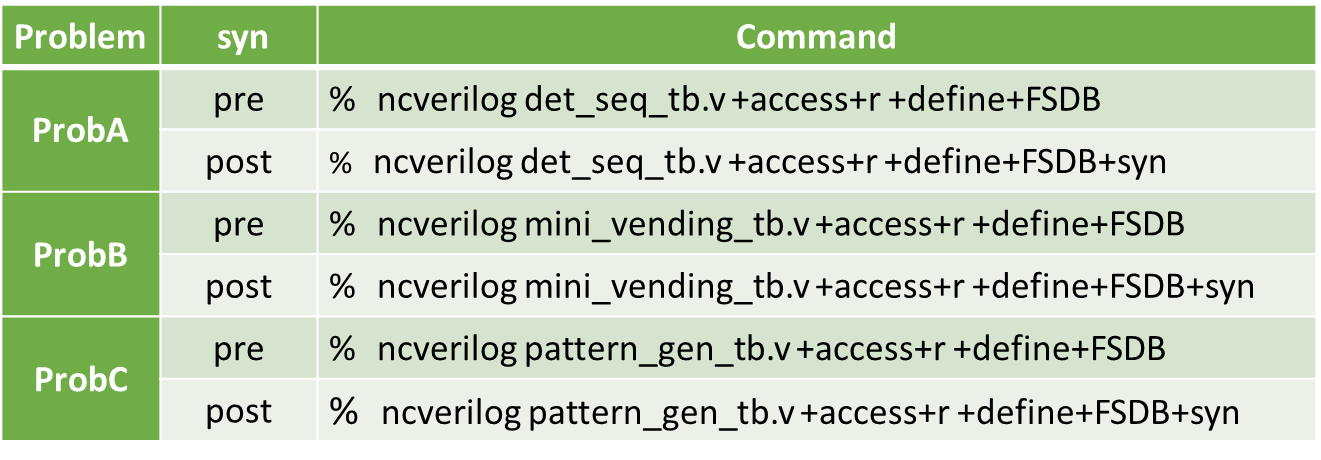
1. **Please attach your design waveforms.**

|  |
| --- |
| Your simulation result on the terminal. |
|  |
| Your waveform : |
|  |
| Explanation of your waveform : |
| 除了初始狀態 INIT 和循環狀態 s0 外，每個狀態都有不同的輸出信號。  1.pattern  當狀態為 s2 時，輸出信號 pattern 為 sel 的第 2 位；  當狀態為 s3 時，輸出信號 pattern 為 sel 的第 1 位；  在其餘狀態下，pattern 輸出為 1。  2.valid  除了 INIT 狀態外，信號始終與 en 信號同步，即當 en 為 1 時，valid 為 1。 |
| Superlint Coverage |
| Coverage : 100% |

1. **At last, please write the lessons learned from this lab session, or some suggestions for this lab session. Thank you.**

**學習到verdi的使用方法與狀態機的應用**

Appendix A : Commands we will use to check your homework

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