Building the SAP-3 Computer

The almost end result. Missing the interrupt controller and the 320*240 LCD screen.

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2020

Rev: 1.0

Chapter 1, The Start

Ben Eater has made a very good series on Youtube on building an SAP-1 computer, were SAP stands for Simple as Possible. The idea is to build a computer from first principles with integrated circuits as available in the 1980's. And I am going to heavily deviating from that in building SAP-3.

The basis of Ben Eaters design is extensively described by Albert Paul Malvino in his book Digital Computer Electronics. Similar describtions can be found on Buildingyourcomputer.org. Or the book, An introduction to microprocessors from D.K.Kaushik. This books as well as the book from Albert Paul Malvino describes not only the SAP-1 but also the more capable SAP-2 and SAP-3.

The differences between SAP-1, 2 and 3 will be discussed in the next paragraph

The purpose of this document is to describe my design and built of the SAP-3 computer starting from the SAP-1. This also means that nothing will be repeated or explained from the SAP-1 computer since this is as all explained by Ben Eater on Youtube.

It is a must to fully understand all aspects of SAP-1 before proceeding to SAP-2 or 3. Without the basic knowlegde of SAP-1 it's not recommended to built SAP-2 or SAP-3. It can ofcourse be done, but troubleshooting will be far more difficult if not impossible and the learning experience is far less.

I also strongly recommend any builder to read and implement the lessons learned from u/lordmonoxide on Reddit.

Chapter 2, SAP-2

SAP-1 can be summarized as follws:

- 4 bit program counter
- A and B register
- ALU with addition and subtraction function
- 1 HEX display
- Instuction register
- 16 byte RAM
- Clock Module upto 300 HZ

In the book from AP.Malvino there is no summary of the characteristics of SAP-2. So one has to make this yourself, going through the chapter on SAP-2 the following can be found:
(Chapter 5 discusses all below items and more in detail)

- Variable machine cycle
- Includes Jump instructions, Ben Eater's SAP-1 computer already has this
- 16 bit program counter PC
- 16 bit memory address register MAR
- 16 bit W-Bus
- 2K ROM from 0000[h] to 07ff[h], 8 bit wide (to initialize the computer etc)
- 62K RAM from 0800[h] to FFFF[h], 8 bit wide
- Memory Data Register MDR, but a really good explanation is not given why this is required
- Instruction register 8 bit
- Temporary 8 bit register connected to the 8 bit ALU
- 8 bit B and C register
- Two input ports. One HEX display, one serial
- Two output ports. One Hex keyboard entry, one serial
- ALU with arithmetic and logical operations, control by means of control bits
- Two flags zero and sign. Ben Eaters SAP-1 already has a zero and carry flag
- 44 Instructions, from 16 possible in the SAP-1 from Ben Eater
- Maximum of 18 T states, which is mainly for the CALL instuction

In my build I did not implement the CALL instruction as described for SAP-2. The use of the Stack Pointer mechanism in SAP-3 is far more efficient and more flexible to save a return address.

Chapter 3, SAP-3

In the book from AP.Malvino there is no summary of the characteristics of SAP-3. So one has to make this yourself, going through the chapter on SAP-3 the following can be found:

- Four additional registers D, E, H, L
- 16 bit Stack Pointer
- More flags, carry and parity
- 33 extra instructions
- Functionality to use register pair DE and HL

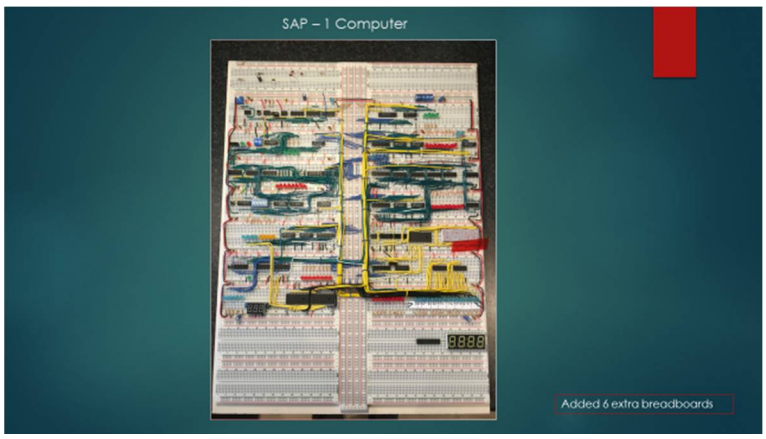
In general it can be concluded that the step from SAP-1 to SAP-2 is a lot larger than from SAP-2 to SAP-3

Chapter 4,

Additional functionality I built include:

- Use of a device to program the RAM and ROM onboard. Especially for programming the RAM another solution has tob e found. With 32K RAM and 8 bits one has to toggle a quarter of a million DIP switch settings to enter a program. Even programming one page, 256 bytes would already be 256*8 ~2000 DIP switch settings. Debugging and altering is even worse.
- An interrupt controller alike the 8085
- An 2*16 LCD screen
- An 320*240 LCD screen
- Fixed crystal controlled clock speed possibilty to allow for time critical applications.

The SAP-1 computer



Chapter 5, Choices I made in building SAP-2

The following choices are made by me in building the SAP-2. Beside the choices I made there is also more detail on each of the subjects on why and how I did certain things.

(*) Deviates from the A.P.Malvino design.

- The baseplate, breadboards and power distribution.

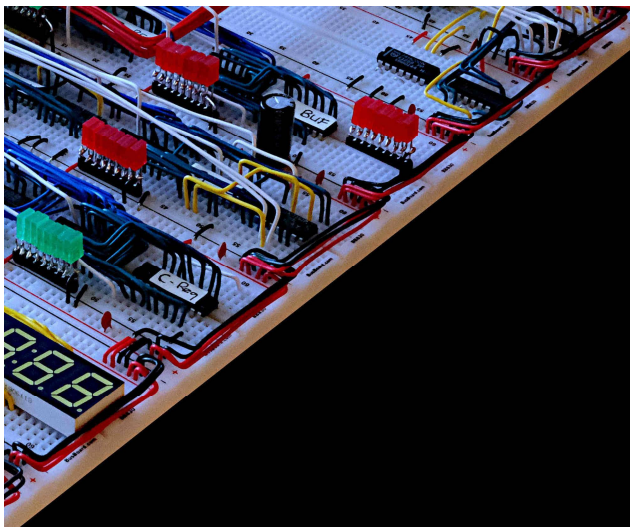
I made a plywood base of 51 (height)* 38 (width)* 15 cm (thickness). On that I mounted 20 BB830 breadboards according the system as used by Ben Eater. So between two boards there is one power rail. Best is to first draw some marking lines on the plywoord on where to allign the breadboards. Not doing so could lead up in the end to a serious mismatch on the bottom if you start at the top, or the other way around. And once you mount a breadboard on the plywood they cannot be taken from the plywood anymore without seriously damaging them. This is a way one exercise. The big advantage of this construction however is that wires between breadboards do not move it is a very rigid construction. Additionally you can easily store the thing somewere. Save from cats, dogs children etc.

When mounting the breadboards take care that the black power rail goes up.

And yes, On my build I have a small misallignment on the bottom breadboards and my top right breadboard is mounted the wrong way around.

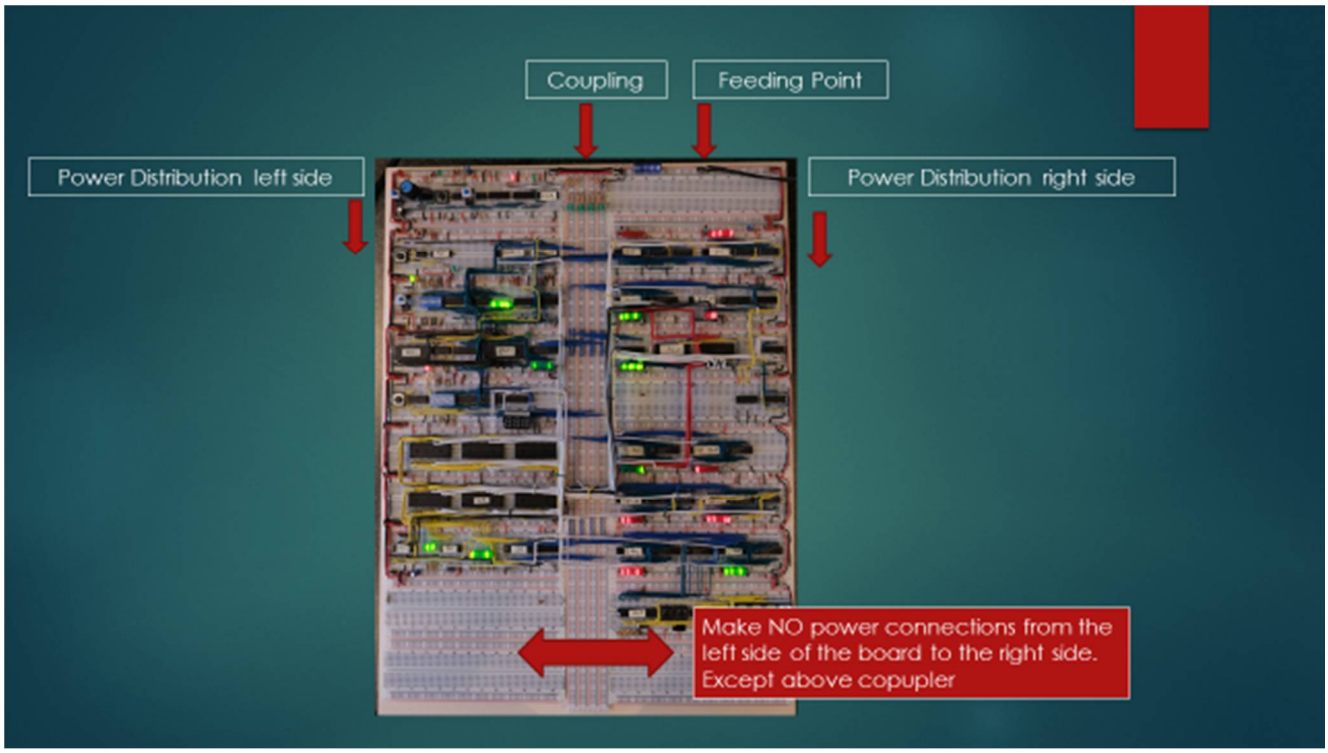
Additionally I doubled up the power wiring, see below picture. Without this the chips most distant away from the feeding point of the board had a Vcc of 4.2 Volt. With the doubled up wiring Vcc went up to 4.8 to 4.9 Volt.

Board with doubled up power wiring



Every power rail has a 0.1 uF capacitor. On the middle of the board left and right I place two 1000 uF capacitors and on the feeding point a 220 uF capacitor.

This is how I made the power distribution over the board. Power is fed from one point and distributed over two strings, one for the boards on the left and one for boards on the right side. One shall not connect the left side of the board wih the right side, except the shown coupler. Reason for this is as follows. By making a link on the bottom breadboards between the left and the right power rail a run around loop is created for spurious signals.



- **Variable machine cycle**
- **8 bit program counter, PC (*)**
- **8 bit page register, PR. (paging or segment register as explained by A.P.Malvino) (*)**
- **16 bit memory address register, MAR**
- **8 bit W-bus (*)**
- **No Memory data register, MDR. Explanation on next slide (*)**
- **8 bit wide ROM and RAM**
- **8K ROM and 32K RAM (*), choise made on available chips. 28C64 and 62256**
- **8 bit instruction register**
- **8 bit temporary register and flag register**
- **8 bit B and C register**

- **8 bit ALU with 74HCT181**,
- **The original Ring counter is changed into a step Counter.**

  design must be modified, explained later. 5 bits are required for 18 states
- **Extra LCD screen and pushbutton input**
- **44 Instructions**
- **16 T states**