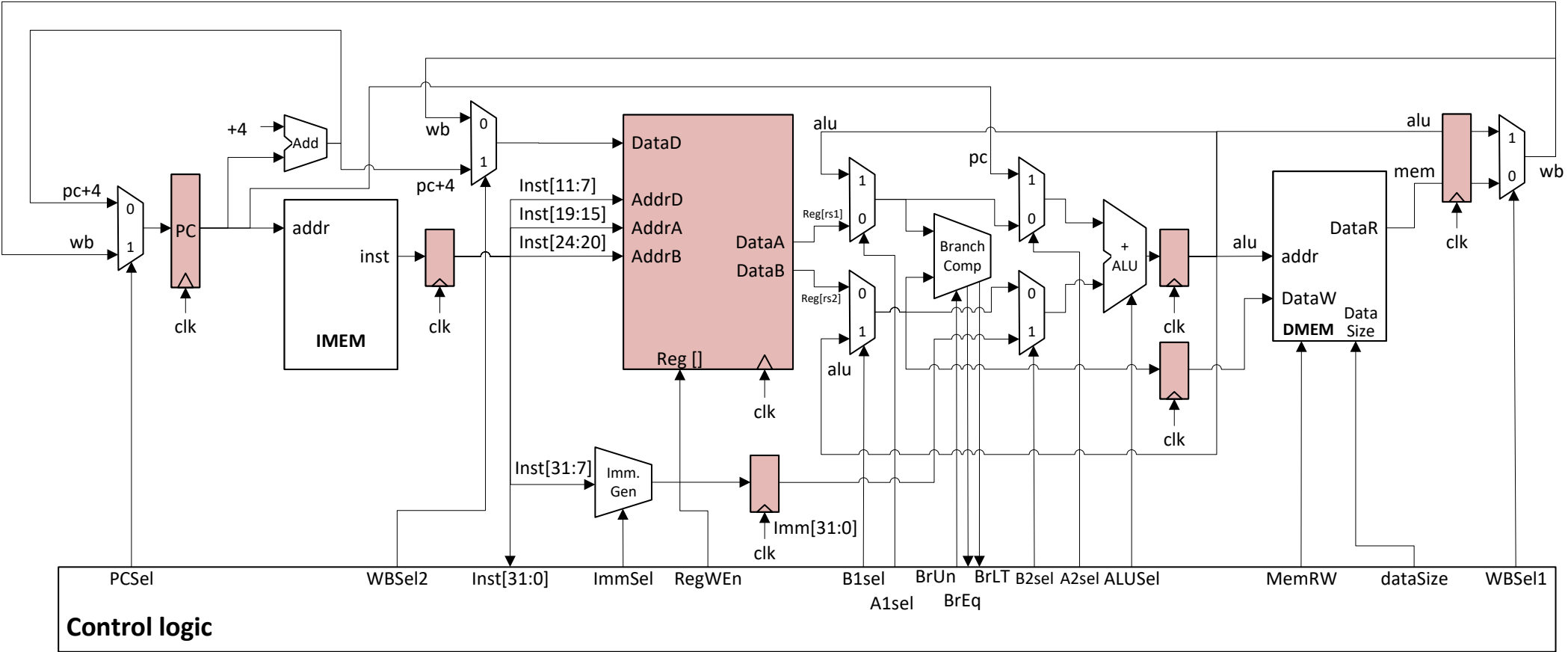


RISC V Project main architecture



Control logic architecture

