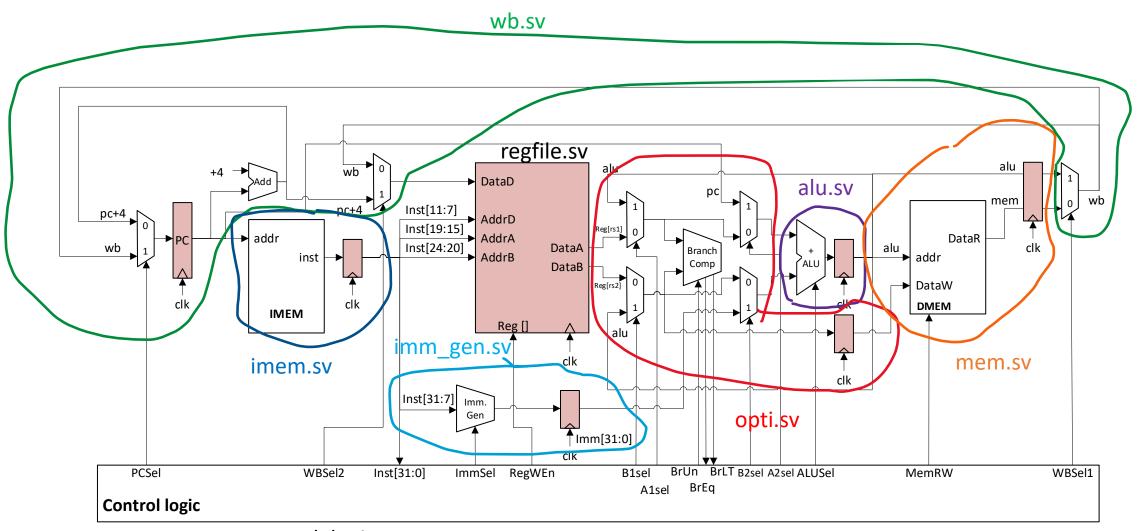
RISC V Project main architecture



control_logic.sv