

FPGA Keypad Scanner and Display

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Prompt:

Target device: Lattice iCE40 UP5K FPGA with internal high-speed oscillator (~20 MHz).

Write synthesizable SystemVerilog to scan a 4x4 matrix keypad and display the last two hex keys pressed on a dual 7-segment display. Implement:

A clock divider that derives a scan clock on the order of 100–200 Hz from the internal oscillator.

A keypad scanning controller that iterates one active-low column at a time and samples active-low rows, registering at most one key per press (debounce-by-design), ignoring additional presses while any key is held, and allowing a new registration only after release.

A top level that updates two hex digits (older and most recent) when a new key is registered and drives a time-multiplexed two-digit 7-segment display without visible flicker and with balanced brightness.

Use idiomatic SystemVerilog (e.g., logic, always_ff, enumerated states for FSMs). Provide clean module boundaries and keep all state synchronous. Include brief comments explaining the design choices.

Response:

Here are the SystemVerilog files to implement your keypad scanner. I've broken the design into four clean, hierarchical modules as requested.

1. `pulse_generator.sv`: A general-purpose clock divider that generates a single-cycle pulse at a specified frequency. We'll use this for both the keypad

scan clock and the 7-segment multiplexing clock.

2. `seven_seg_hex.sv`: A simple combinational module to convert a 4-bit hex value into 7-segment display signals (assuming common anode, active-low segments).
3. `keypad_scanner.sv`: The core FSM for scanning the 4x4 keypad, handling debounce, and preventing key repeat, all based on the slow scan clock.
4. `top_keypad_7seg.sv`: The top-level module that integrates everything, stores the last two key presses, and drives the final outputs.

Here are the files:

Clock Pulse Generator - Nov 3, 12:12 AM

Hex to 7-Segment Decoder - Nov 3, 12:12 AM

4x4 Keypad Scanner FSM - Nov 3, 12:12 AM

Top Level Module - Nov 3, 12:12 AM

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