Date:

R E S U M E

Full name: **Roman Kaplan**

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ACADEMIC DEGREES

2016 – present	Doctoral Candidate, Electrical Engineering, Technion
2016	MSc., Electrical Engineering, Technion
2009	BSc., Computer Engineering, Technion

PROFESSIONAL EXPERIENCE (outside academia, if relevant)

2012 – 2014	Systems Architect, IDF Navy, Tikshuv Center
2009 – 2012	Software Engineer, IDF Navy, Tikshuv Center

TEACHING EXPERIENCE

W2014/15 – present	Teaching Assistant, *Introduction to Data Structures and Algorithms*, undergraduate. Head teaching assistance since winter 2015/16.
S2017	Teaching Assistant, *Introduction to Faculty Research*, graduate and undergraduate.
W2016/17	Teaching Assistant, *Parallel Computing Architecture*, graduate. Wrote benchmarks and produced datasets for new homework assignments. Also taught the introduction to convolutional neural networks.

AWARDS AND HONORS

Jun 2017	ISC HPC 2017, Research Poster Award Winner in the 'Architectures and Networks' category
Sep 2016	PACT 2016 Student Research Competition Award (gold medal)
Winter 2016/17	Outstanding Teaching Assistant
Spring 2016	Outstanding Teaching Assistant
Winter 2015/16	Outstanding Teaching Assistant

PUBLICATIONS

Refereed papers in professional journals

Published papers

Roman Kaplan, Leonid Yavits, and Ran Ginosar and Uri Weiser, "A Resistive CAM Processing-in-Storage Architecture for DNA Sequence Alignment," IEEE Micro Special Issue on Architectures for the Post Moore Era, vol. 37, no. 4, pp. 20-28, 2017.

Roman Kaplan, Leonid Yavits, and Ran Ginosar, "From Processing-in-Memory to Processing-in-Storage," Journal of Supercomputing Frontiers and Innovations, vol. 4, no. 3, pp. 99-116, .

Submitted papers

Roman Kaplan, Leonid Yavits, and Ran Ginosar, "PRINS: PRocessing-in-Storage Acceleration of Machine Learning", IEEE Transactions on Nanotechnology.

Leonid Yavits, Roman Kaplan, and Ran Ginosar, "PRINS: Resistive CAM Processing in Storage", IEEE Transactions on VLSI.

Refereed Papers in Conference Proceedings

Roman Kaplan, Leonid Yavits, Amir Morad, and Ran Ginosar, "Deduplication in resistive content addressable memory based solid state drive," 26th Power and Timing Modeling, Optimization and Simulation, pp. 100-106, 2016.

CONFERENCES

Lectures

Roman Kaplan and Ran Ginosar, "Accelerating Sparse Matrix-Vector Multiplication Using Compression on a Many-Core Processor," *ChipEx,* May 2015, Tel-Aviv.

Roman Kaplan, Leonid Yavits and Ran Ginosar, "Deduplication in Resistive CAM Based Solid State Drive", *ChipEx,* May 2016, Tel-Aviv.

Roman Kaplan, Leonid Yavits and Ran Ginosar, "An In-Storage Smith-Waterman Algorithm in Resistive CAM," in *In-Memory and In-Storage Computing with Emerging Technologies Workshop*, PACT, Sep 2016, Haifa.

Roman Kaplan, Leonid Yavits and Ran Ginosar, "Resistive CAM: A Processing-in-Storage (PRinS) Device," *4th Memristor Technology, Design, Automation and Computing Workshop*, HiPEAC, Jan 2017, Stockholm.

Poster Presentations

Roman Kaplan and Ran Ginosar, "Accelerating Sparse Matrix-Vector Multiplication Using Compression on a Many-Core Processor," *Intel ICRI-CI retreat*, May 2016.

Roman Kaplan and Ran Ginosar, "Accelerating Sparse Matrix-Vector Multiplication Using Compression on a Many-Core Processor," in the *International Symposium on Computer Architecture*, Jun 2015, Portland, OR.

Roman Kaplan, Leonid Yavits, and Ran Ginosar, "In-Memory Implementation of Smith-Waterman Algorithm on a Resistive CAM," *Intel ICRI-CI retreat,* May 2016, Haifa

Roman Kaplan, Leonid Yavits, and Ran Ginosar, "In-Storage Implementation of K-Means in Resistive CAM," *International Conference on Memristive Materials, Devices & Systems*, Apr 2017, Athens.

Roman Kaplan, Leonid Yavits, and Ran Ginosar, "From Processing-in-Memory to Processing-in-Storage," *Intel ICRI-CI retreat*, May 2017, Haifa.

Roman Kaplan, Leonid Yavits, and Ran Ginosar, "From Processing-in-Memory to Processing-in-Storage," International Supercomputing Conference for High Performance Computing, Jun 2017, Frankfurt.

SPECIAL ACTIVITIES

Feb 2018	"Accelerator Architecture in Computational Biology and Bioinformatics" workshop, in conjunction with IEEE International Symposium on High-Performance Computer Architecture (HPCA) 2018
May 2017	Faculty of Electrical Engineering representative at the Technion open day for undergraduate students, Azrieli tower
Spring 2017	Taking part in improving and re-defining the next semester of Introduction to Faculty Research course