



**ALPHA & OMEGA**  
SEMICONDUCTOR

**AONS62604**  
60V N-Channel AlphaSGT™

### General Description

- Trench Power AlphaSGT™ technology
- Low  $R_{DS(ON)}$
- Logic Level Gate Drive
- Excellent Gate Charge  $\times R_{DS(ON)}$  Product (FOM)
- RoHS and Halogen-Free Compliant

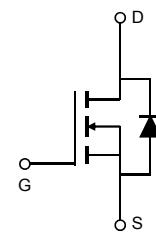
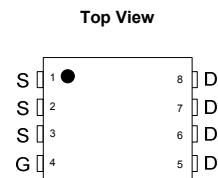
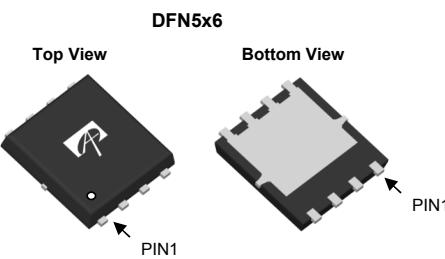
### Product Summary

$V_{DS}$	60V
$I_D$ (at $V_{GS}=10V$ )	100A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 2.5mΩ
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	< 3.4mΩ

### Applications

- High Frequency Switching and Synchronous Rectification

100% UIS Tested  
100%  $R_g$  Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONS62604	DFN 5x6	Tape & Reel	3000

### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$I_D$	100	A
$T_C=100^\circ C$		100	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	320	
Continuous Drain Current	$I_{DSM}$	37	A
$T_A=70^\circ C$		30	
Avalanche Current <sup>C</sup>	$I_{AS}$	42	A
Avalanche energy $L=0.3mH$ <sup>C</sup>	$E_{AS}$	265	mJ
$V_{DS}$ Spike <sup>I</sup>	$V_{SPIKE}$	72	V
Power Dissipation <sup>B</sup>	$P_D$	119	W
$T_C=100^\circ C$		47.5	
Power Dissipation <sup>A</sup>	$P_{DSM}$	6.2	W
$T_A=70^\circ C$		4.0	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	°C

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup> $t \leq 10s$	$R_{\theta JA}$	15	20	°C/W
Maximum Junction-to-Ambient <sup>AD</sup> Steady-State		40	50	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	0.85	1.05	°C/W

**Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	60			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=60\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$		1	5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			$\pm 100$	nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.2	1.6	2.2	V
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=20\text{A}$ $T_J=125^\circ\text{C}$		2.1	2.5	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=20\text{A}$		3.4	4.1	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}, I_D=20\text{A}$		110		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.67	1	V
$I_S$	Maximum Body-Diode Continuous Current <sup>G</sup>				100	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=30\text{V}, f=1\text{MHz}$		3660		pF
$C_{oss}$	Output Capacitance			1160		pF
$C_{rss}$	Reverse Transfer Capacitance			108		pF
$R_g$	Gate resistance	$f=1\text{MHz}$	0.3	0.75	1.2	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=30\text{V}, I_D=20\text{A}$		64	90	nC
$Q_g(4.5\text{V})$	Total Gate Charge			32	50	nC
$Q_{gs}$	Gate Source Charge			8.5		nC
$Q_{gd}$	Gate Drain Charge			11.5		nC
$Q_{oss}$	Output Charge	$V_{GS}=0\text{V}, V_{DS}=30\text{V}$		57		nC
$t_{D(\text{on})}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=30\text{V}, R_L=1.5\Omega, R_{\text{GEN}}=3\Omega$		7.5		ns
$t_r$	Turn-On Rise Time			7		ns
$t_{D(\text{off})}$	Turn-Off Delay Time			44		ns
$t_f$	Turn-Off Fall Time			12.5		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=20\text{A}, di/dt=500\text{A}/\mu\text{s}$		26		ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=20\text{A}, di/dt=500\text{A}/\mu\text{s}$		92		nC

A. The value of  $R_{0JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $R_{0JA} \leq 10\text{s}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

B. The power dissipation  $P_D$  is based on  $T_{J(\text{MAX})}=150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature  $T_{J(\text{MAX})}=150^\circ\text{C}$ .

D. The  $R_{0JA}$  is the sum of the thermal impedance from junction to case  $R_{0JC}$  and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

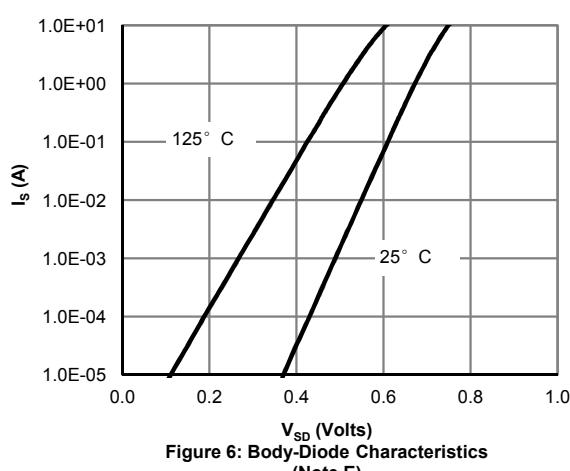
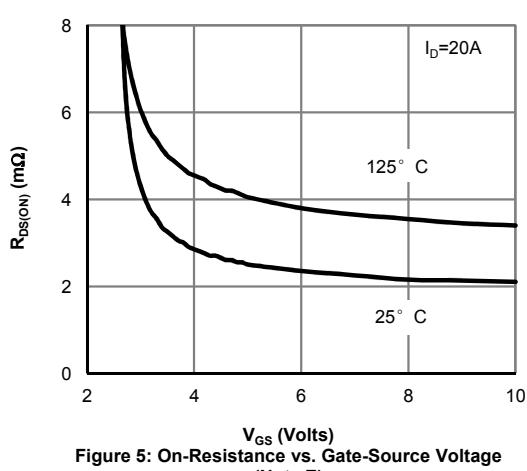
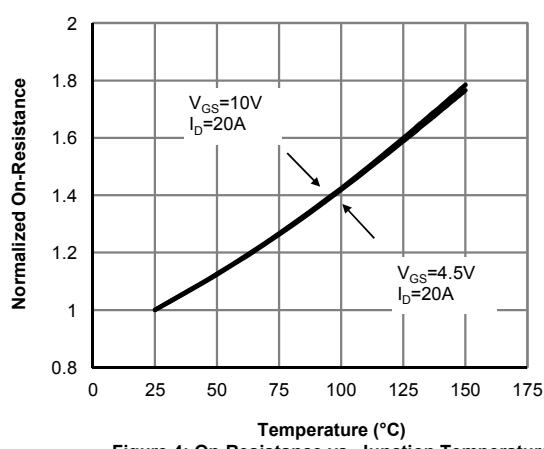
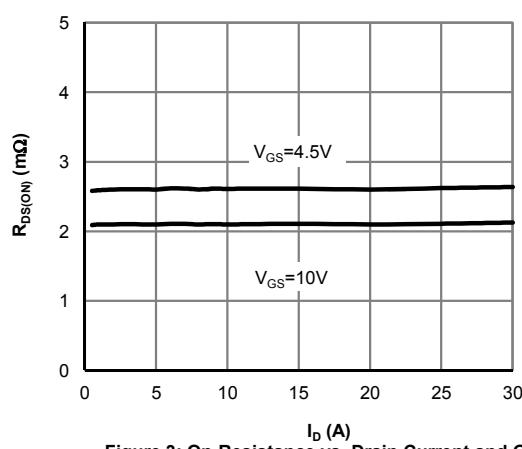
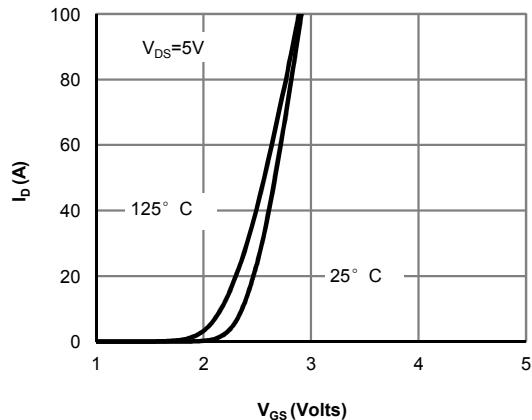
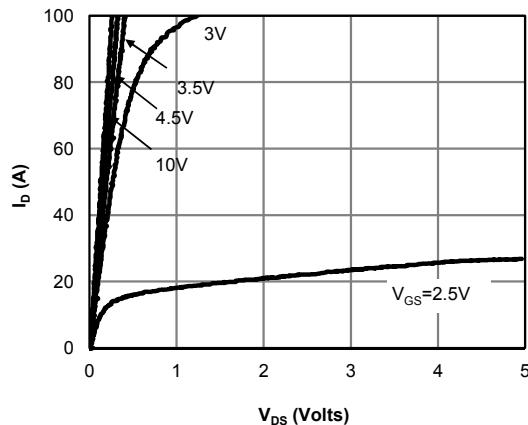
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(\text{MAX})}=150^\circ\text{C}$ . The SOA curve provides a single pulse rating.

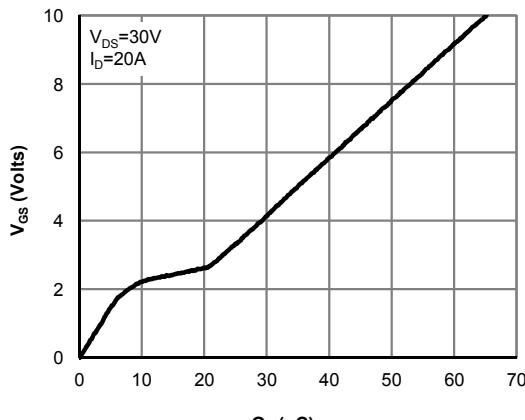
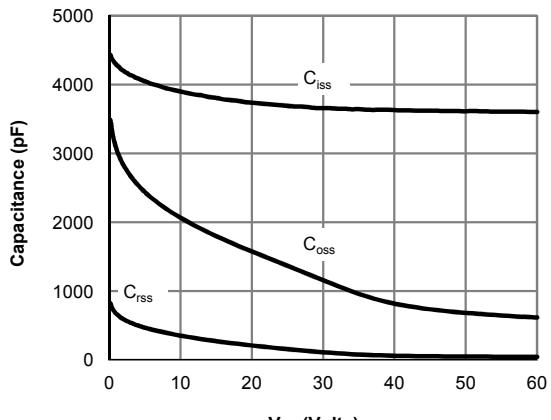
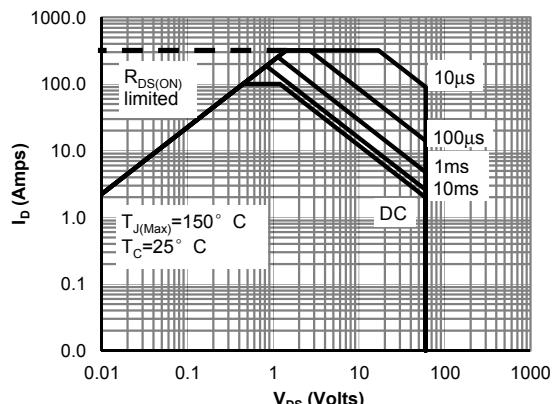
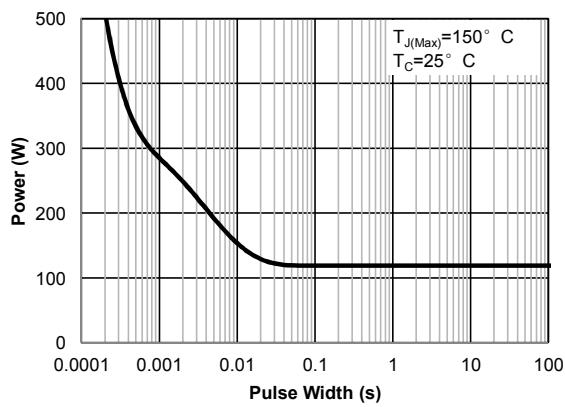
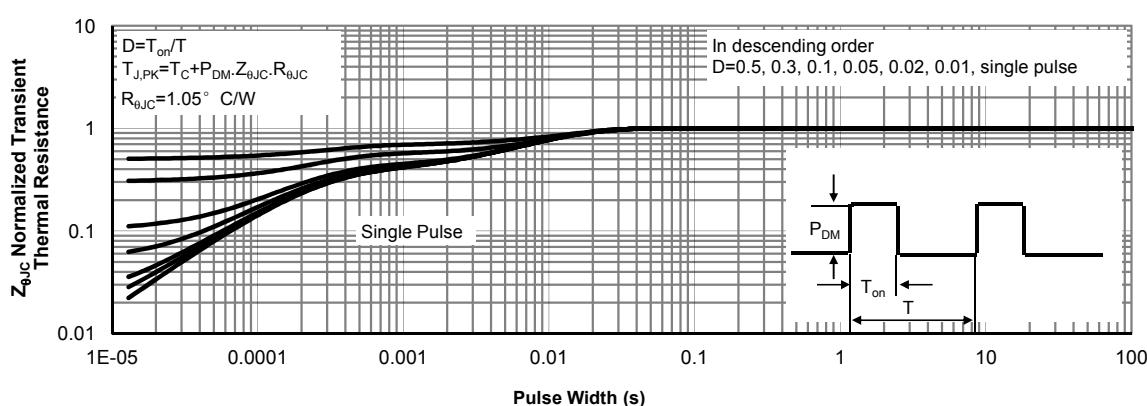
G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ .

I. The spike duty cycle 5% max, limited by junction temperature  $T_{J(\text{MAX})}=125^\circ\text{C}$ .

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**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**


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**Figure 7: Gate-Charge Characteristics**

**Figure 8: Capacitance Characteristics**

**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

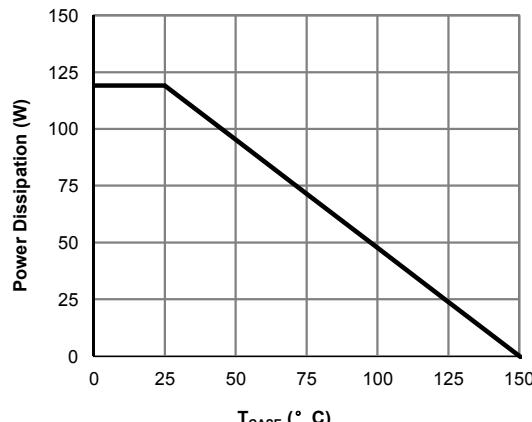
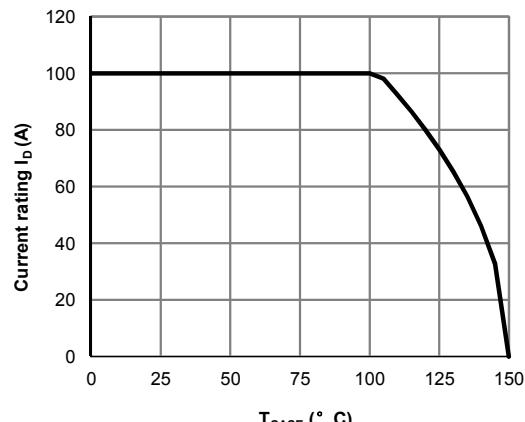
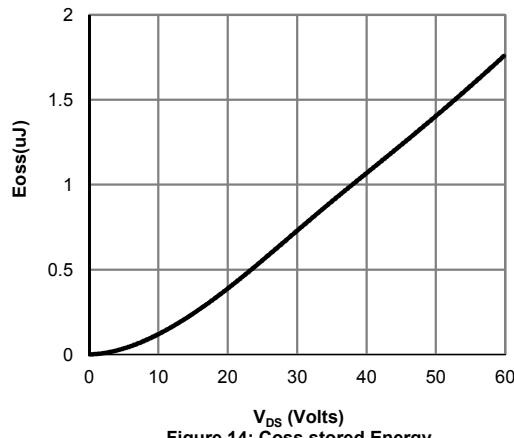
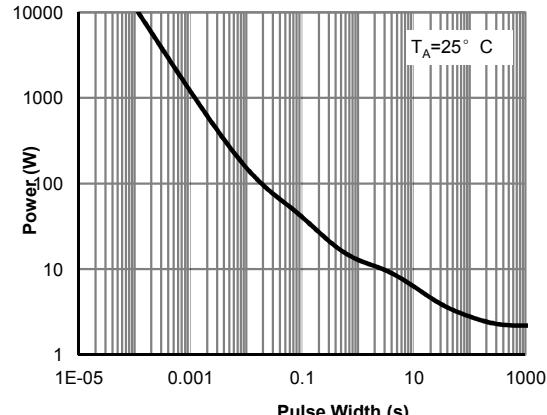
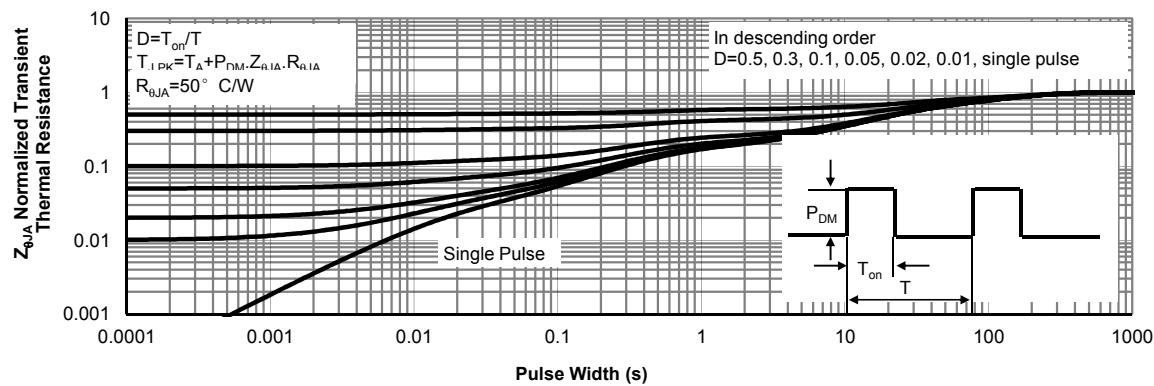
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Figure 12: Power De-rating (Note F)**

**Figure 13: Current De-rating (Note F)**

**Figure 14: Coss stored Energy**

**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

Figure A: Gate Charge Test Circuit &amp; Waveforms

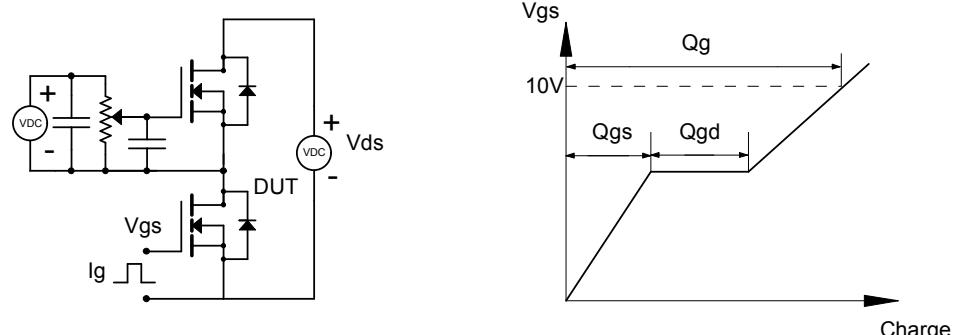


Figure B: Resistive Switching Test Circuit &amp; Waveforms

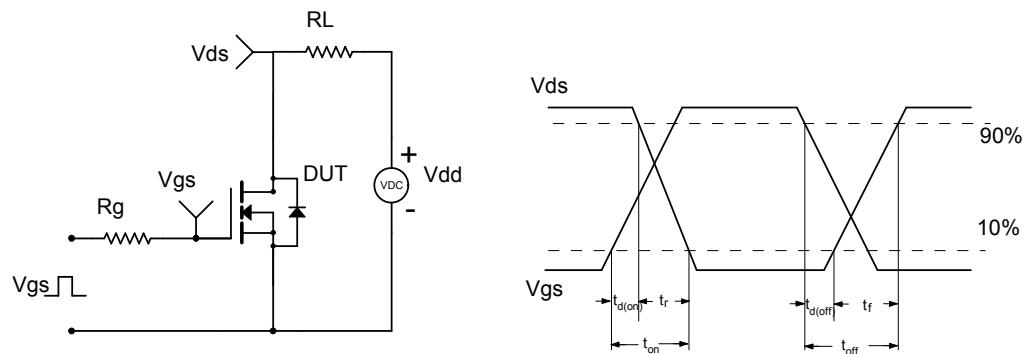


Figure C: Unclamped Inductive Switching (UIS) Test Circuit &amp; Waveforms

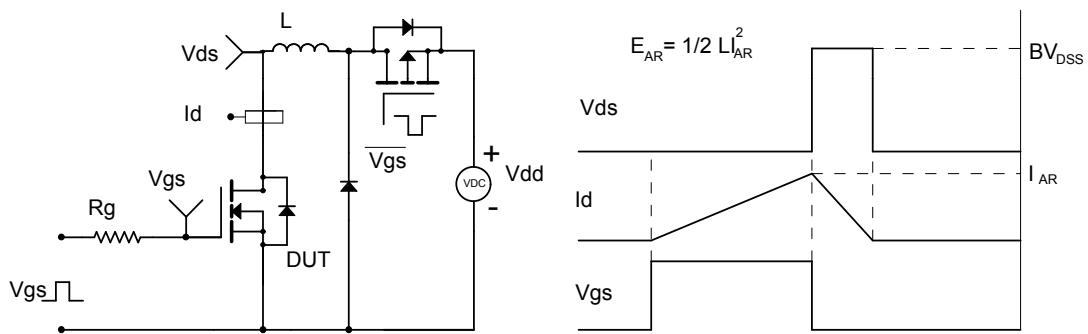


Figure D: Diode Recovery Test Circuit &amp; Waveforms

