**TEXAS INSTRUMENTS**

**TPS7A19**

SBVS256A –MAY 2016–REVISED SEPTEMBER 2016

# TPS7A19
## 40-V, 450-mA, Wide V$_{IN}$, Low I$_Q$, Low-Dropout Voltage Regulator with Power Good

## 1 Features

- Wide Input Voltage Range: 4 V to 40 V
- Adjustable Output Voltage: 1.5 V to 18 V
- Output Current: 450 mA
- Low Quiescent Current (I$_Q$): 15 µA
- Low Dropout Voltage: 450 mV (max) at 400 mA
- Power Good with Programmable Delay
- Thermal Shutdown and Overcurrent Protection
- Stable with Ceramic Output Capacitors:
  - 10 µF to 500 µF for V$_{OUT}$ ≥ 2.5 V
  - 22 µF to 500 µF for V$_{OUT}$ < 2.5 V
- Operating Temperature: –40°C to +125°C
- Package: 3-mm × 3-mm SON-8

## 2 Applications

- Smart Grid Infrastructure and Metering
- Power Tools
- Motor Drives
- Access Control Systems
- Test and Measurement

## 3 Description

The TPS7A19 is a low-dropout linear regulator (LDO) with a wide input voltage (V$_{IN}$) range up to 40 V, capable of sourcing high output current (I$_{OUT}$) up to 450 mA. This voltage regulator is ideal for generating a low-voltage supply from wide input-voltage rails. Not only does the TPS7A19 supply a well-regulated voltage rail, but the device also withstands and maintains regulation during voltage transients by acting as a simple surge protection circuit.

The TPS7A19 consumes only 15 µA of quiescent current (I$_Q$) at light loads, thereby lowering the power consumption for always-on or battery-powered applications.
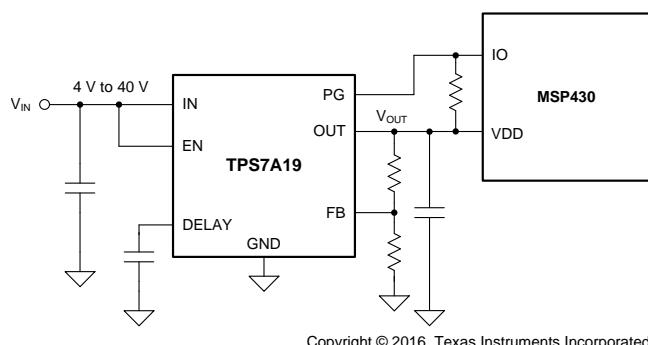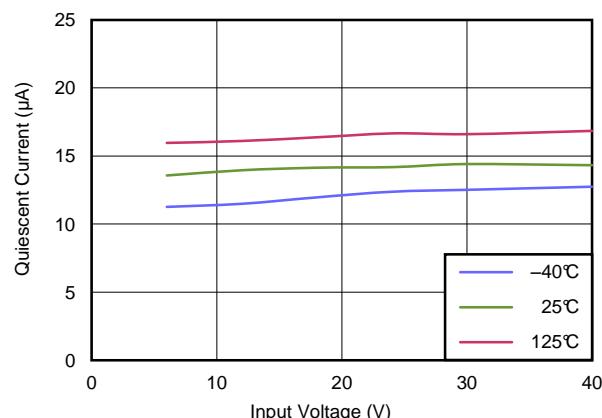
The TPS7A19 features integrated thermal shutdown and overcurrent protection. The TPS7A19 also offers a power good output (PG) with a programmable delay that indicates when the output voltage is in regulation. This feature is useful for power-rail sequencing functions.

This LDO is available in a small, 3-mm × 3-mm, thermally-enhanced, 8-pin SON package.

### Device Information[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
| --- | --- | --- |
| TPS7A19 | SON (8) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.

### Typical Application Schematic



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### Quiescent Current vs Input Voltage at V$_{OUT}$ = 1.5 V

# Table of Contents

# 4 Revision History

**Changes from Original (May 2016) to Revision A**          **Page**
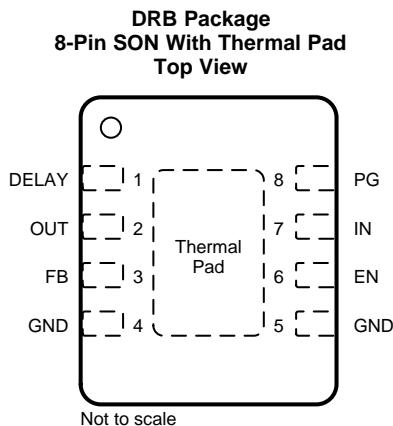
• Changed from product preview to production data ........................................................................................................... 1

# 5  Pin Configuration and Functions

**DRB Package**
**8-Pin SON With Thermal Pad**
**Top View**



Not to scale

## Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DELAY | 1 | — | Delay pin. Connect a capacitor to GND to adjust the PG delay time; leave open if the PG function is not needed. |
| EN | 6 | I | Enable pin. This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_HI}$, the regulator is enabled. If $V_{EN} \leq V_{EN\_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. |
| FB | 3 | I | Feedback pin. The feedback pin is the input to the control-loop error amplifier. |
| GND | 4,5 | — | Ground pin. |
| IN | 7 | I | Regulator input supply pin. |
| OUT | 2 | O | Regulator output pin. When the output voltage is larger than 2.5 V, connect a 10-$\mu$F to 500-$\mu$F ceramic capacitor with an equivalent series resistance (ESR) from 0.001 to 20 $\Omega$ to assure stability. When the output voltage is from 1.5 V to 2.5 V, the minimum, stable capacitor value should be 22 $\mu$F. |
| PG | 8 | O | Power good. This open-drain pin must be connected to $V_{OUT}$ through an external resistor. PG is pulled low when the output voltage goes below threshold. |
| Thermal pad | | — | Solder to printed-circuit-board (PCB) to enhance thermal performance. Although the thermal pad can be left floating, connect the thermal pad to the ground plane for optimal performance. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range –40°C to 125°C(unless otherwise noted)[1]

|  |  |  | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage[2] | Input | IN, EN | −0.3 | 45 | V |
|  | Output | OUT[3] | −0.3 | $V_{IN}$ + 0.3 |  |
|  |  | DELAY[4] | −0.3 | 45 |  |
|  |  | FB, PG | −0.3 | 22 |  |
| Current | Peak output |  | Internally limited |  |  |
| Temperature | Operating junction, $T_J$ |  | −40 | 150 | °C |
|  | Storage, $T_{stg}$ |  | −65 | 150 |  |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) The absolute maximum rating is VIN + 0.3 V or 22 V, whichever is lower.
(4) The voltage at the DELAY pin must be lower than the $V_{IN}$ voltage.

## 6.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
|  |  | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±500 |  |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage | 4 | 40 | V |
| $V_{OUT}$ | Output voltage | 1.5 | 18 | V |
| $V_{EN}$ | Enable voltage | 0 | 40 | V |
| $T_J$ | Operating junction temperature | −40 | 125 | °C |

## 6.4 Thermal Information

|  | THERMAL METRIC[1] | TPS7A19 DRB (VSON) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 48 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 56.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 22.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 22.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 4.6 | °C/W |

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

at $T_J$ = –40°C to +125°C, $V_{IN}$ = 14 V , $V_{EN}$ = $V_{IN}$, $I_{OUT}$ = 200 μA, $C_{IN}$ = 22 μF, and $C_{OUT}$ = 47 μF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE AND CURRENT** | | | | | | | |
| $V_{IN}$ | Input voltage | $V_{OUT}$ ≤ 3.5 V , $I_{OUT}$ = 0 mA to 450 mA | | 4 | | 40 | V |
| | | $V_{OUT}$ ≥ 3.5 V , $I_{OUT}$ = 0 mA to 450 mA | | $V_{OUT}$ + 0.5 | | 40 | V |
| $I_Q$ | Quiescent current | $V_{IN}$ = 4 V to 40 V, $V_{OUT}$ = 1.5 V, $V_{EN}$ = 5 V, $I_{OUT}$ = 0.2 mA | | | 15 | 25 | μA |
| | | $V_{IN}$ = 18.5 V to 40 V, $V_{OUT}$ = 18 V, $V_{EN}$ = 5 V, $I_{OUT}$ = 0.2 mA | | | 25 | 40 | |
| $I_{SHDN}$ | Shutdown current | $V_{EN}$ = 0 V, $I_{OUT}$ = 0 mA , $V_{IN}$ = 18 V, $V_{OUT}$ = 1.5 V | | | | 4 | μA |
| $V_{FB}$ | Feedback voltage | Reference voltage for FB pin | | 1.208 | 1.233 | 1.258 | V |
| $V_{IN\_UVLO}$ | Undervoltage lockout | Ramp $V_{IN}$ down until output is turned off | | | | 2.6 | V |
| $UVLO_{Hys}$ | Undervoltage detection hysteresis | $V_{IN}$ rising | | | 1 | | V |
| **ENABLE INPUT (EN)** | | | | | | | |
| $V_{EN\_LO}$ | Logic input low level | | | 0 | | 0.4 | V |
| $V_{EN\_HI}$ | Logic input high level | | | 1.7 | | | V |
| $I_{EN}$ | EN pin current | $V_{EN}$ = 40 V , $V_{IN}$ = 14 V | | | | 1 | μA |
| **REGULATED OUTPUT** | | | | | | | |
| $V_{OUT}$ | Regulated output[1] | $V_{IN}$ = $V_{OUT}$ + 1 V to 40 V and $V_{IN}$ ≥ 4 V, $I_{OUT}$ = 100 μA to 450 mA | | –2% | | 2% | |
| $\Delta V_{O(\Delta VI)}$ | Line regulation | $V_{IN}$ = $V_{OUT}$ + 1 V to 40 V and $V_{IN}$ ≥ 4 V, $I_{OUT}$ = 100 mA | | | | 10 | mV |
| $\Delta V_{O(\Delta IL)}$ | Load regulation | $I_{OUT}$ = 1 mA to 450 mA, $V_{IN}$ = $V_{OUT}$ + 1 V and $V_{IN}$ ≥ 4 V | | | | 10 | mV |
| $V_{DO}$ | Dropout voltage | $V_{IN}$ – $V_{OUT}$, $I_{OUT}$ = 400 mA | | | 240 | 450 | mV |
| | | $V_{IN}$ – $V_{OUT}$, $I_{OUT}$ = 200 mA | | | 160 | 300 | |
| $I_{OUT}$ | Output current | $V_{OUT}$ in regulation | | 0 | | 450 | mA |
| $I_{CL}$ | Output current-limit | $V_{OUT}$ short to ground | | 140 | | 360 | mA |
| | | $V_{OUT}$ = $V_{OUT}$ nominal × 0.9 | | 470 | | 850 | |
| PSRR | Power-supply ripple rejection[2] | $I_{OUT}$ = 100 mA, $C_{OUT}$ = 22 μF | f = 100 Hz | | 60 | | dB |
| | | | f = 100 kHz | | 40 | | |
| **PG** | | | | | | | |
| $V_{OL}$ | PG output low voltage | $I_{OL}$ = 0.5 mA | | | | 0.4 | V |
| $I_{OH}$ | PG leakage current | PG pulled to $V_{OUT}$ with 10-kΩ resistor | | | | 1 | μA |
| $V_{T(PG)}$ | Power good threshold | $V_{OUT}$ power-up | | 89.6 | 91.6 | 93.6 | % of $V_{OUT}$ |
| $V_{hys}$ | Hysteresis | $V_{OUT}$ power-down | | | 2 | | % of $V_{OUT}$ |
| **PG DELAY** | | | | | | | |
| $I_{Delay}$ | Delay capacitor charging current | | | 5 | 9.5 | 14 | μA |
| $V_{T(PG\_DLY)}$ | Delay pin comparator threshold voltage | | | | 1 | | V |
| **TEMPERATURE** | | | | | | | |
| $T_{sd}$ | Junction shutdown temperature | Temperature increasing | | | 175 | | °C |
| $T_{hys}$ | Hysteresis of thermal shutdown | | | | 24 | | °C |

(1) Accuracy specification does not apply on any application condition that exceeds the power dissipation limit of the package under test. External resistor divider variation is not considered for accuracy measurement.
(2) Design information; not tested, specified by characterization.
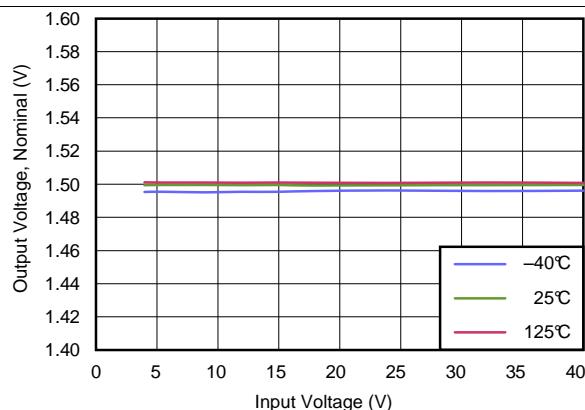
## 6.6 Timing Requirements

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **TIMING FOR PG** | | | | | | |
| $t_{PG\_DLY}$ | Power good delay | C = delay-capacitor value capacitance = 100 nF[1] | | 10.5 | | ms |
| $t_{PG-fixed}$ | Power good delay | No capacitor on pin | | 325 | | μs |
| $t_{PG(HL)}$ | PG falling propagation delay | $V_{OUT}$ low to PG low | | 180 | | μs |

(1) Information only; not tested in production. The equation is based on: (C × 1) / (9.5 × 10$^{-6}$) = $t_{PG\_DLY}$, where C = delay capacitor value capacitance; range = 100 pF to 500 nF.
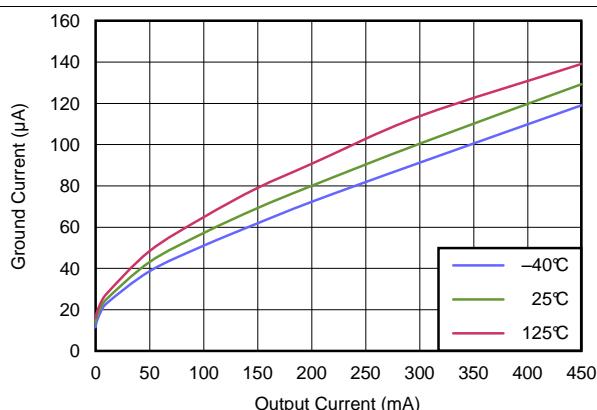
## 6.7 Typical Characteristics

at $T_J$ = –40°C to +125°C, $V_{IN}$ = 14 V , $V_{EN}$ = $V_{IN}$, $I_{OUT}$ = 200 µA, $C_{IN}$ = 22 µF, and $C_{OUT}$ = 47 µF (unless otherwise noted)
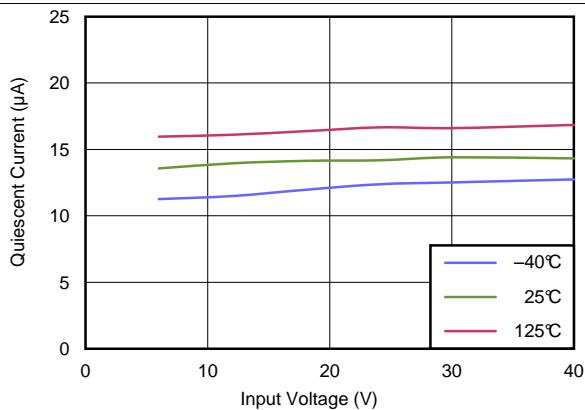
$V_{OUT}$ = 1.5 V, $I_{OUT}$ = 100 mA

**Figure 1. Line Regulation**
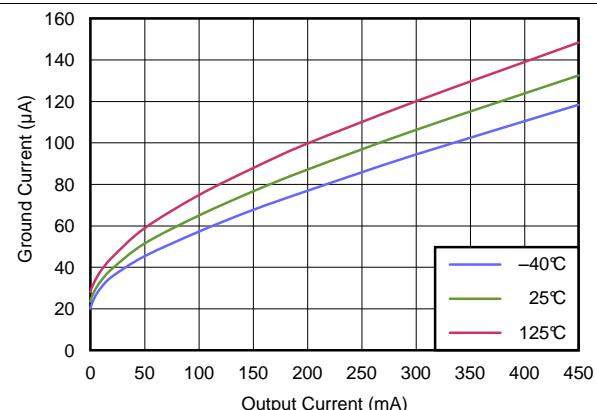
$V_{IN}$ = 14 V, $V_{OUT}$ = 1.5 V

**Figure 2.  Ground Current vs Output Current**
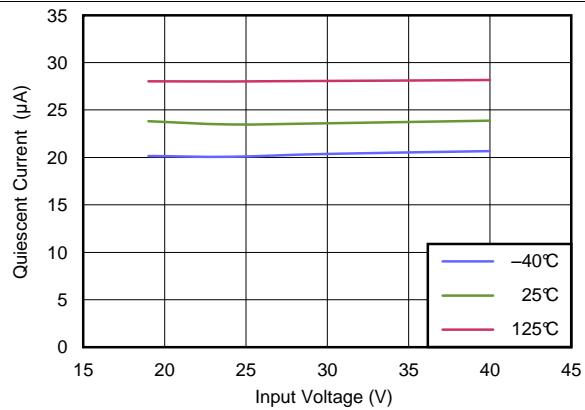
$V_{OUT}$ = 1.5 V

**Figure 3.  Quiescent Current vs Input Voltage**
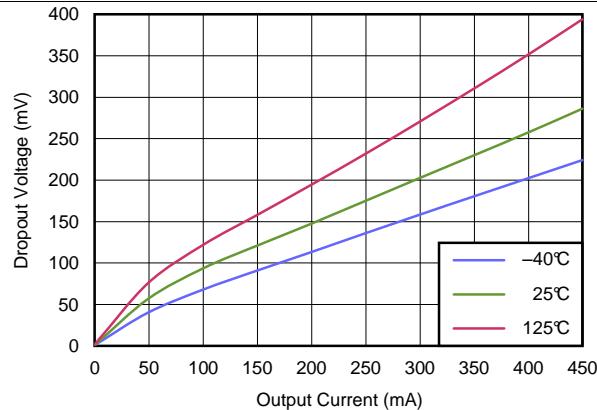
$V_{IN}$ = 24 V, $V_{OUT}$ = 18 V

**Figure 4.  Ground Current vs Output Current**

$V_{OUT}$ = 18 V
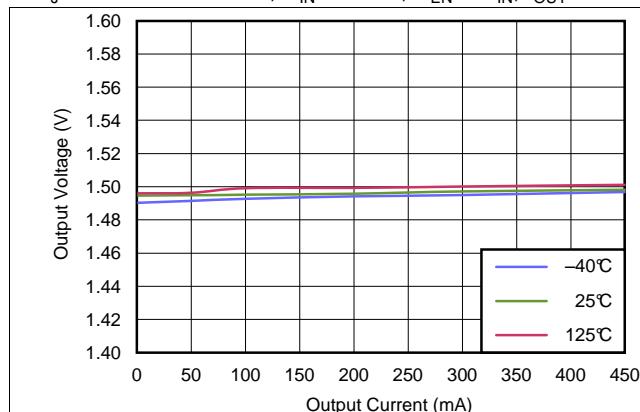
**Figure 5.  Quiescent Current vs Input Voltage**

**Figure 6. Dropout Voltage vs Output Current**

Product Folder Links: *TPS7A19*
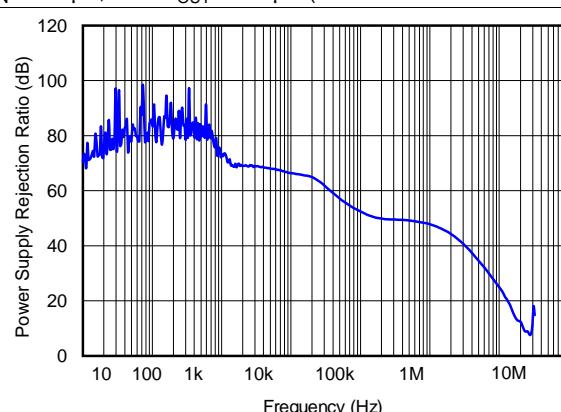
## Typical Characteristics (continued)

at $T_J$ = –40°C to +125°C, $V_{IN}$ = 14 V , $V_{EN}$ = $V_{IN}$, $I_{OUT}$ = 200 μA, $C_{IN}$ = 22 μF, and $C_{OUT}$ = 47 μF (unless otherwise noted)
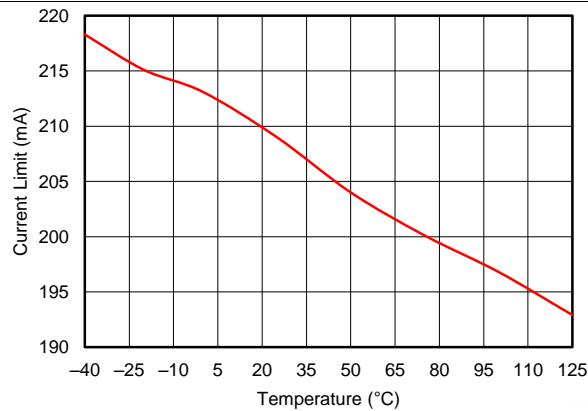


$V_{IN}$ = 14 V, $V_{OUT}$ = 1.5 V

**Figure 7. Load Regulation**
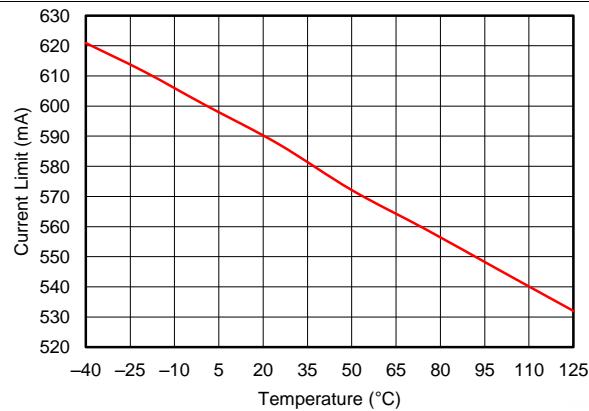


$V_{OUT}$ = 5 V, $C_{OUT}$ = 47 μF, $I_{OUT}$ = 10 mA
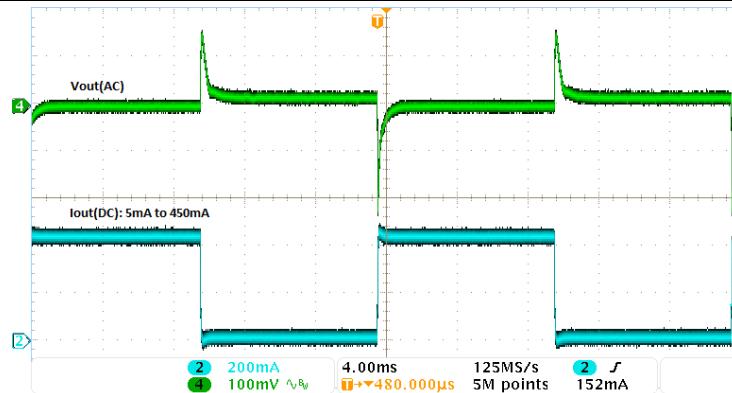
**Figure 8. Power-Supply Rejection Ratio vs Frequency**



**Figure 9. Short to GND Current-Limit vs Temperature**



**Figure 10. Current-Limit vs Temperature**
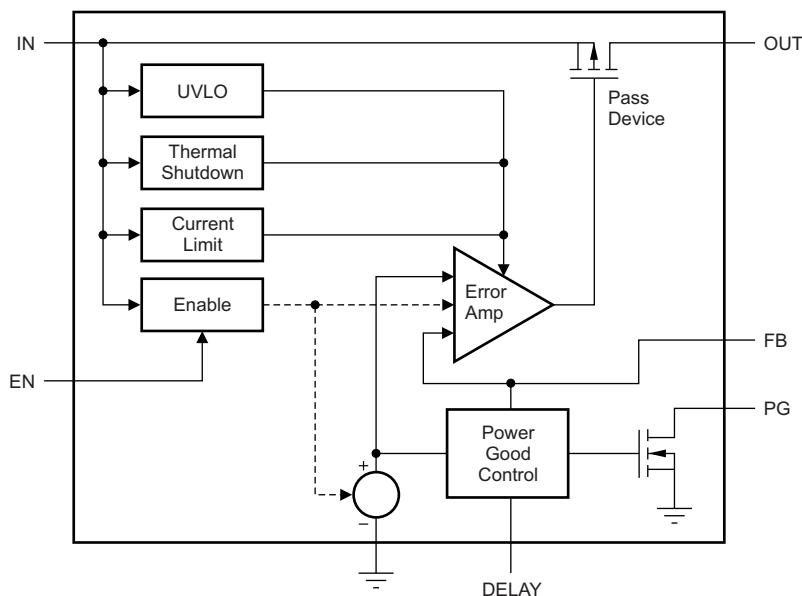


**Figure 11. Load Transient**
**10-μF Ceramic Output Capacitor**

# 7 Detailed Description

## 7.1 Overview

The TPS7A19 is a low-dropout linear regulator (LDO) combined with enable and power good functions. The power good pin initializes when the output voltage, $V_{OUT}$, exceeds $V_{T(PG)}$. The power good delay is a function of the value set by an external capacitor on the DELAY pin before releasing the PG pin high.

## 7.2 Functional Block Diagram



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## 7.3 Feature Description

### 7.3.1 Enable Pin (EN)

The enable pin is a high-voltage-tolerant pin. A logic-high input on EN actives the device and turns on the LDO. For self-bias applications, connect this input to the IN pin.

### 7.3.2 Regulated Output Pin (OUT)

The OUT pin is the regulated output based on the required voltage. The output is protected by internal current limiting. During initial power up, the LDO has a soft start feature incorporated to control the initial current through the pass element.

In the event that the LDO drops out of regulation, the output tracks the input minus a voltage drop based on the load current. When the input voltage drops below the UVLO threshold, the LDO shuts down until the input voltage exceeds the minimum start-up level.

### 7.3.3 Power-Good Pin (PG)

The power good pin is an output with an external pullup resistor to the regulated supply. The output remains low until the regulated $V_{OUT}$ exceeds approximately 91.6% of the set value, and the power good delay has expired. The regulated output falling below the 89.6% level asserts this output low after a short deglitch time of approximately 180 µs (typical).

## Feature Description (continued)
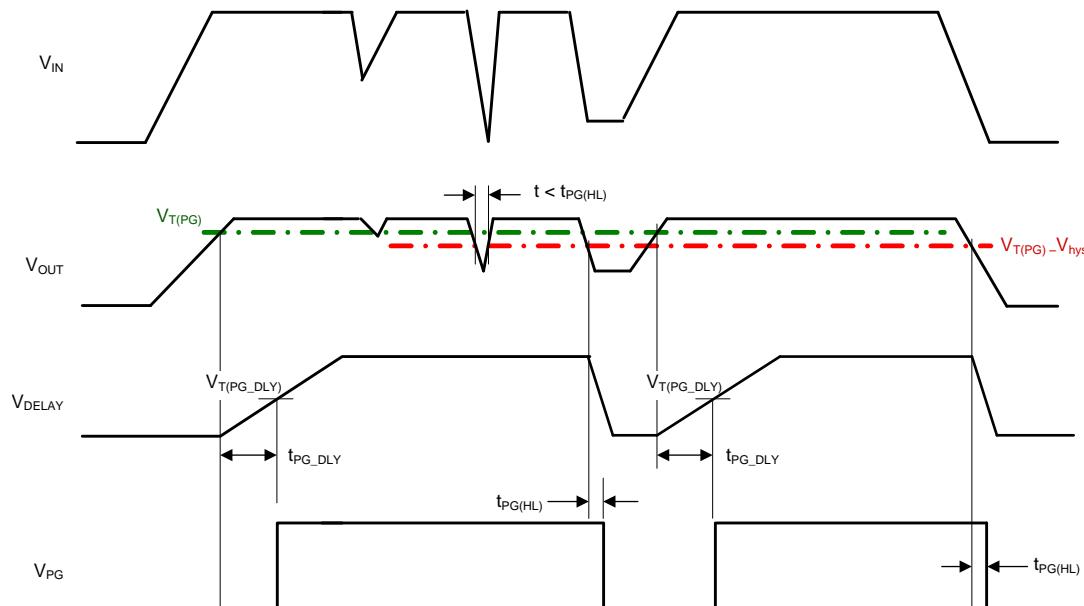
### 7.3.4 Delay Timer Pin (DELAY)

An external capacitor on the DELAY pin sets the timer delay before the PG pin is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold that trips an internal comparator. If this pin is open, the default delay time is 325 µs (typical).

The pulse delay time, $t_{PG\_DLY}$, is defined with the charge time of an external capacitor DELAY, as shown in Equation 1.

$$t_{PG\_DLY} = \left( \frac{C_{DELAY} \times 1\ V}{9.5\ \mu A} \right) + 325\ \mu s$$

(1)

The PG pin initializes when $V_{OUT}$ exceeds 91.6% of the programmed value. The delay is a function of the value set by an external capacitor on the DELAY pin before the PG pin is released high.



**Figure 12.  Conditions to Activate PG**

### 7.3.5 Adjustable Output Voltage (ADJ for TPS7A1901)

An output voltage between 1.5 V and 18 V can be selected by using the external resistor dividers. Use Equation 2 to calculate the output voltage, where $V_{FB} = 1.233\ V$. In order to avoid a large leakage current and to prevent a divider error, the value of (R1 + R2) must between 10 kΩ and 100 kΩ.

$$V_{OUT} = V_{FB} \times \left( 1 + \frac{R1}{R2} \right)$$

(2)

### 7.3.6 Undervoltage Shutdown

The TPS7A19 family of devices has an internally-fixed, undervoltage-shutdown threshold. Undervoltage shutdown activates when the input voltage on $V_{IN}$ drops below $V_{IN\_UVLO}$. This activation makes sure that the regulator is not latched in an unknown state when there is a low-input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up, similar to a typical power-up sequence when the input voltage exceeds the required levels.

## Feature Description (continued)

### 7.3.7 Thermal Shutdown

The TPS7A19 incorporates a thermal shutdown (TSD) circuit as protection from overheating. For continuous standard operation, the junction temperature must not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point minus the TSD hysteresis value, the output turns on again.

Thermal protection disables the output when the junction temperature rises to approximately 175°C, and allows the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the temperature of the regulator, and protects the device from damage as a result of overheating.

Although the internal protection circuitry of the TPS7A19 device is designed to protect against overload conditions, the circuitry is not intended to replace proper heat-sink methods. Continuously running the TPS7A19 device into thermal shutdown degrades device reliability.

## 7.4 Device Functional Modes

### 7.4.1 Operation With $V_{IN}$ < 4 V

The devices operate with input voltages above 4 V. The devices do not operate at input voltages below the actual UVLO voltage.

### 7.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.7 V, maximum. When the EN pin is held above 1.7 V, and the input voltage is greater than the UVLO rising voltage, the device enables.

The enable falling edge is 0.4 V, minimum. When the EN pin is held below 0.4 V, the device is disabled. The quiescent current is reduced in this state.

Product Folder Links: *TPS7A19*

# 8  Application and Implementation

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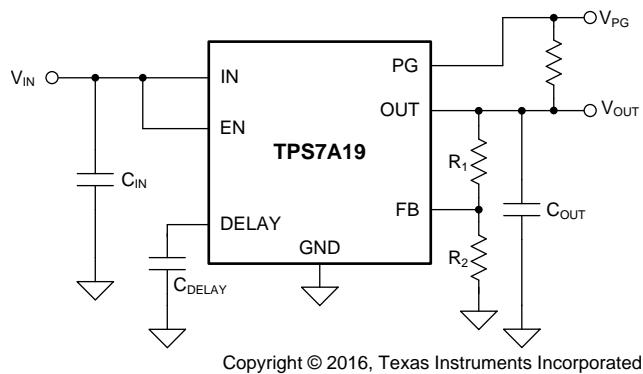
**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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## 8.1  Application Information

Figure 13 shows a typical application circuit for the TPS7A1901. Based on the end-application, different values of external components can be used. Some applications may require a larger output capacitor during fast load steps in order to prevent a PG low from occurring. Use a low-ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

## 8.2  Typical Application

**Figure 13.  Adjustable Operation**

### 8.2.1  Design Requirements

For this design example, use the parameters listed in Table 1.

**Table 1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage | 12 V, ±10% |
| Output voltage | 3.3 V |
| Output current | 50 mA (max) |
| PG delay time | 1 ms |

### 8.2.2  Detailed Design Procedure

To begin the design process:

1. First, make sure that the combination of maximum current, maximum ambient temperature, maximum input voltage, and minimum output voltage does not exceed the maximum operating condition of $T_J$ = 125°C. The *Power Dissipation and Thermal Considerations* section describes how to calculate the maximum ambient temperature and power dissipation.
2. Next, set the feedback resistors to give the desired output voltage. See Equation 2 for the $V_{OUT}$ relationship to R1 and R2. A good nominal value for R2 is 10 kΩ.
3. Then, calculate the required $C_{DELAY}$ capacitor to achieve the desired PG delay time using Equation 1. For 1 ms of delay, the nearest standard value capacitor is 10 nF.
4. Finally, select an output capacitor with a total effective capacitance between 22 µF and 500 µF, a sufficient voltage rating, and an ESR below 20 Ω. Higher capacitance gives improved transient response, but results in higher inrush current at startup.

### 8.2.2.1 *Power Dissipation and Thermal Considerations*

Device power dissipation is calculated with Equation 3.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN}$$

where

- $P_D$ = continuous power dissipation
- $I_{OUT}$ = output current
- $V_{IN}$ = input voltage
- $V_{OUT}$ = output voltage                                                                                          (3)

As $I_Q \ll I_{OUT}$, the term $I_Q \times V_{IN}$ in Equation 3 can be ignored.

For a device under operation at a given ambient air temperature ($T_A$), calculate the junction temperature ($T_J$) with Equation 4.

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where

- $\theta_{JA}$ = junction-to-ambient air thermal impedance                                                          (4)
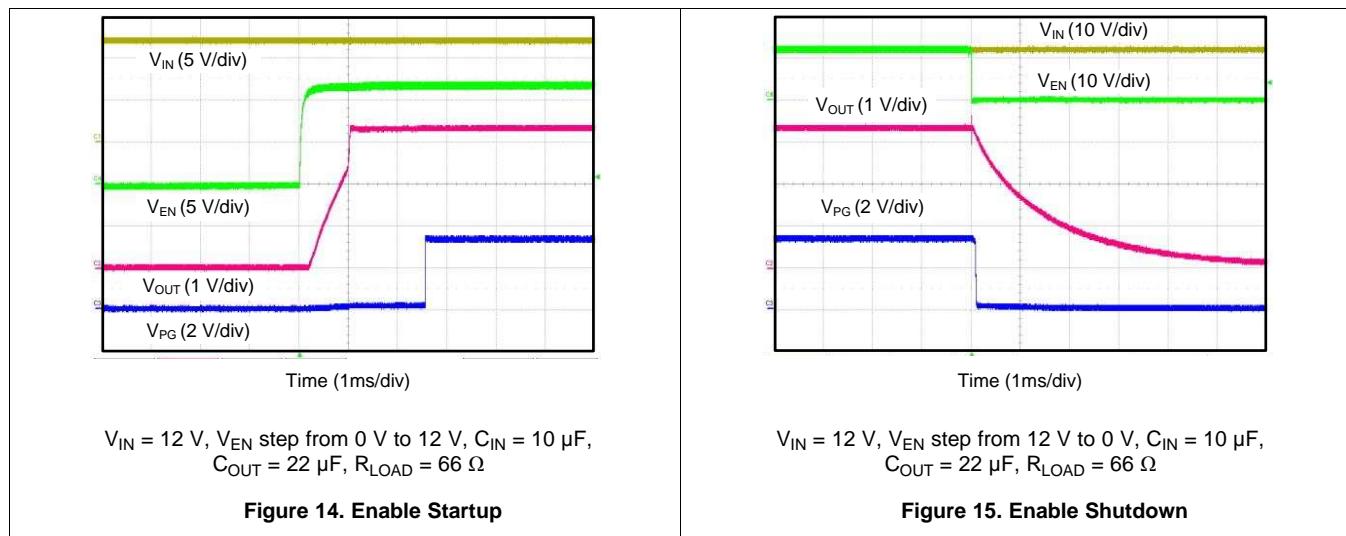
A rise in junction temperature because of power dissipation can be calculated with Equation 5.

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D)$$
                                                                                                                      (5)

For a given maximum junction temperature ($T_{JM}$), the maximum ambient air temperature ($T_{AM}$) at which the device can operate is calculated with Equation 6.

$$T_{AM} = T_{JM} - (\theta_{JA} \times P_D)$$
                                                                                                                      (6)

### 8.2.3 Application Curves



$V_{IN}$ = 12 V, $V_{EN}$ step from 0 V to 12 V, $C_{IN}$ = 10 μF, $C_{OUT}$ = 22 μF, $R_{LOAD}$ = 66 Ω

**Figure 14. Enable Startup**



$V_{IN}$ = 12 V, $V_{EN}$ step from 12 V to 0 V, $C_{IN}$ = 10 μF, $C_{OUT}$ = 22 μF, $R_{LOAD}$ = 66 Ω

**Figure 15. Enable Shutdown**

Product Folder Links: *TPS7A19*

# 9 Power Supply Recommendations

The device operates from an input voltage supply range between 4 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A19 device, add an electrolytic capacitor with a value of 47 μF and a ceramic bypass capacitor at the input.

# 10 Layout

## 10.1 Layout Guidelines

- To improve ac performance such as PSRR, output noise, and transient response, design the board with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the GND pin of the device. In addition, connect the ground connection for the output capacitor directly to the GND pin of the device.
- Minimize equivalent series inductance (ESL) and equivalent series resistance (ESR) in order to maximize performance and stability. Place every capacitor as close to the device as possible, and on the same side of the PCB as the regulator.
- Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces are strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.
- If possible, and to maximize the performance listed in this data sheet, use the same layout pattern used for the TPS7A19 evaluation module, TPS7A1901EVM-760 (SBVU031).

## 10.2 Layout Example
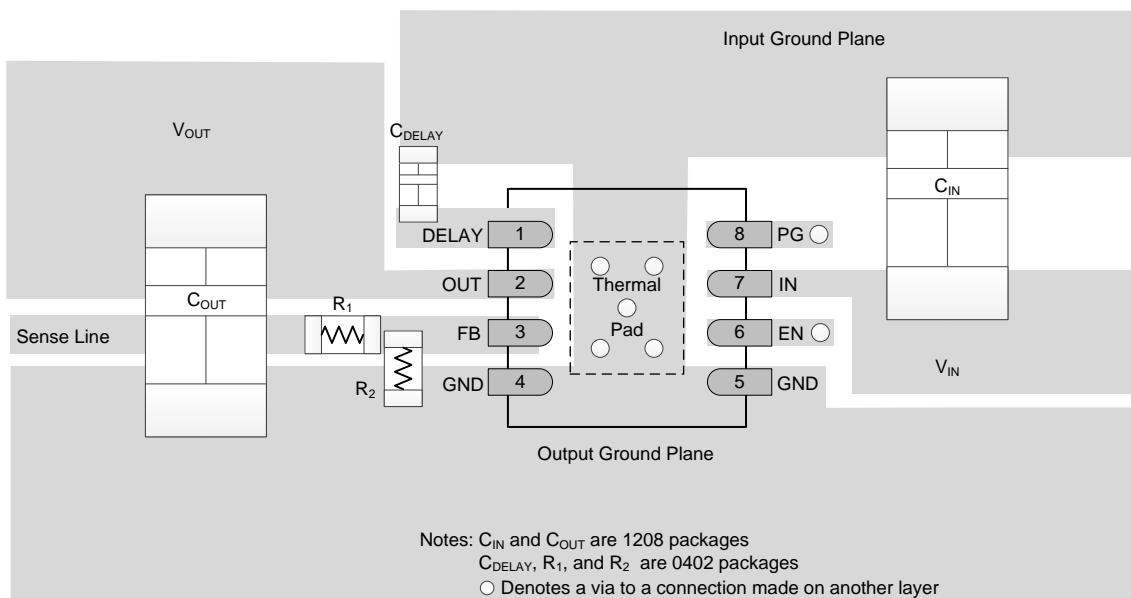


**Figure 16. TPS7A19 Layout Example**

Product Folder Links: *TPS7A19*

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Development Support

#### 11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A19. The summary information for this fixture is shown in Table 2.

**Table 2. Evaluation Modules**

| NAME | EVM FOLDER |
| --- | --- |
| TPS7A19 40-V, 450-mA, High-Voltage, Ultra-Low IQ Low-Dropout Regulator Evaluation Module | TPS7A1901EVM-760 |

#### 11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A19 is available through the TPS7A19 product folder under the tools and software tab.

### 11.1.2 Device Nomenclature

**Table 3. Ordering Information[1]**

| PRODUCT | DESCRIPTION |
| --- | --- |
| TPS7A19**XXYYYZ** | **XX** is the nominal output voltage option; 01 for adjustable.<br>**YYY** is the package designator.<br>**Z** is the package quantity. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

## 11.2 Documentation Support

### 11.2.1 Related Documentation

TPS7A1901EVM-760 Evaluation Module User's Guide (SBVU031)

## 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7A1901DRBR | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A1901 |
| TPS7A1901DRBR.A | Active | Production | SON (DRB) \| 8 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A1901 |
| TPS7A1901DRBT | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A1901 |
| TPS7A1901DRBT.A | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A1901 |
| TPS7A1901DRBTG4 | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A1901 |
| TPS7A1901DRBTG4.A | Active | Production | SON (DRB) \| 8 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A1901 |

**(1)** **Status:** For more details on status, see our product life cycle.

**(2)** **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3)** **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4)** **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5)** **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
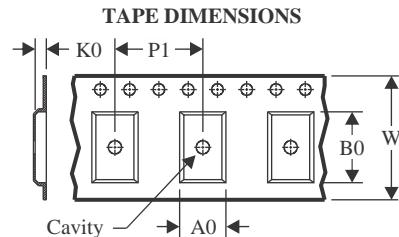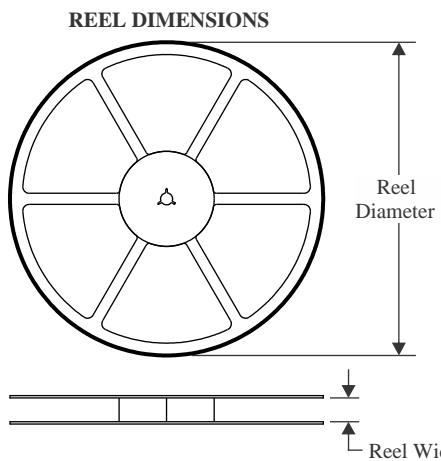
**(6)** **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.
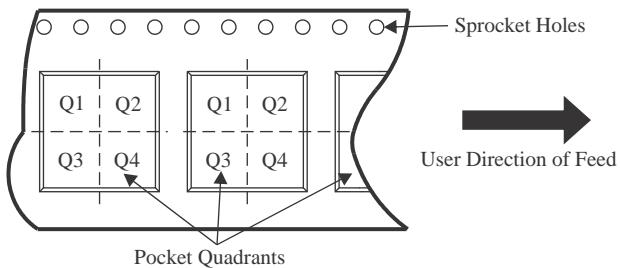
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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
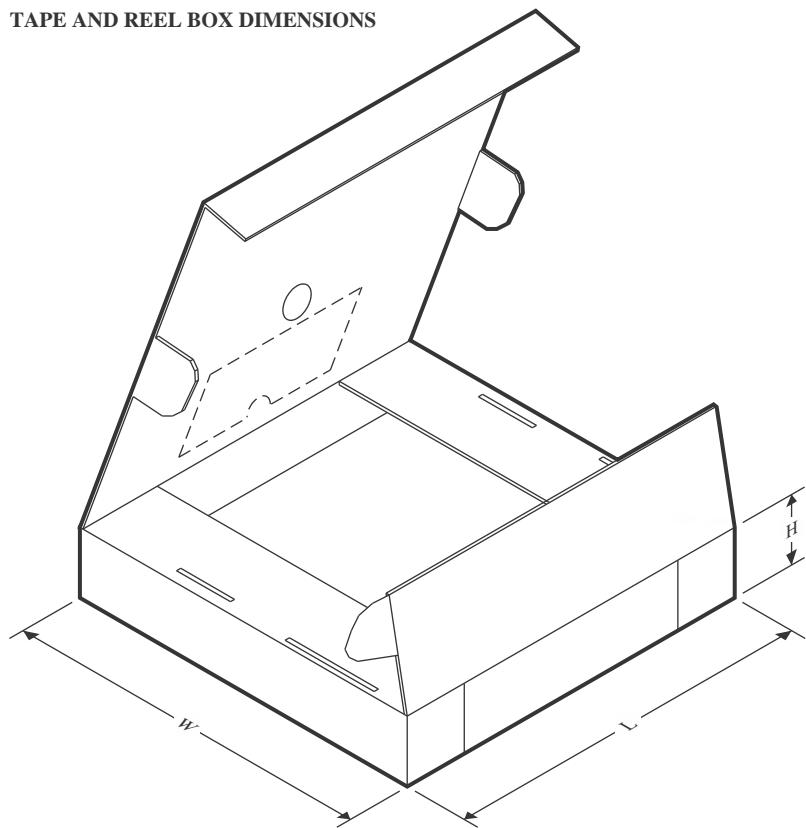
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|-------------------------------------------------------|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|-------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS7A1901DRBR | SON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A1901DRBT | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS7A1901DRBTG4 | SON | DRB | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L
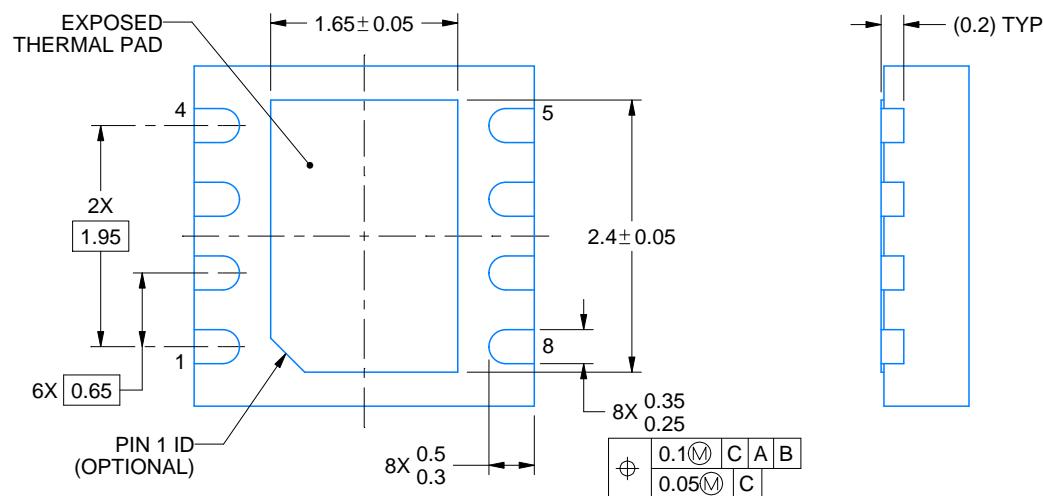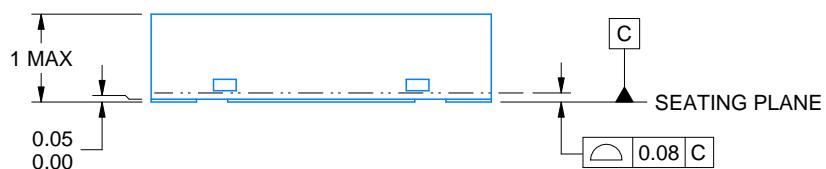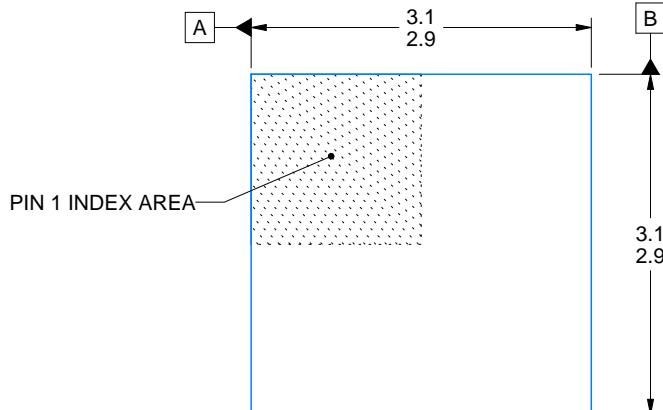
TEXAS
INSTRUMENTS

A

3.1
2.9

B

PIN 1 INDEX AREA

3.1
2.9

1 MAX

0.05
0.00

C

SEATING PLANE

$\bigcirc$ 0.08 C

EXPOSED
THERMAL PAD

1.65 ± 0.05

(0.2) TYP

4

5

2X
1.95

2.4 ± 0.05

1

8

6X 0.65

8X 0.35
0.25

PIN 1 ID
(OPTIONAL)

8X 0.5
0.3

⊕ 0.1 Ⓜ C A B

0.05 Ⓜ C

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NOTES:
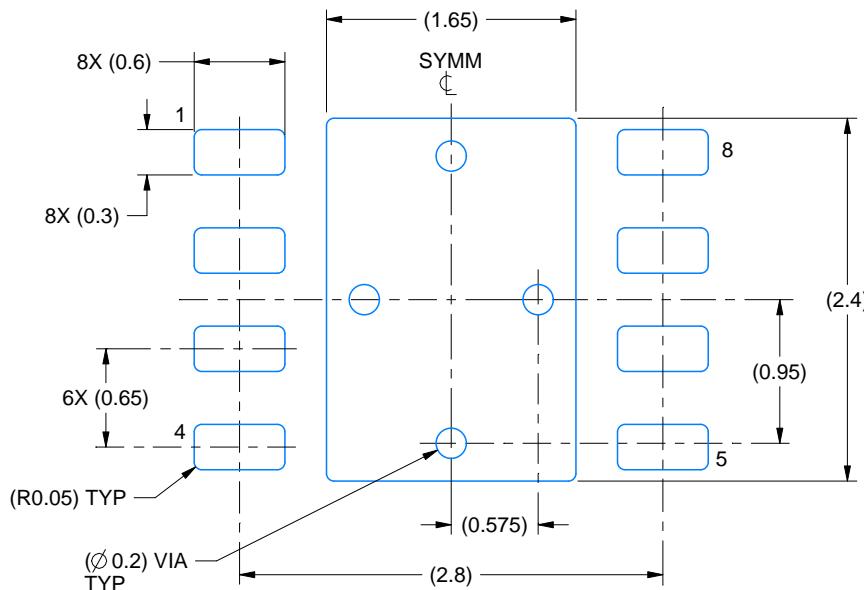
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

8X (0.6)

1

8X (0.3)

(1.65)

SYMM

8

(2.4)

(0.95)

6X (0.65)

4

5

(R0.05) TYP

(0.575)

(⌀ 0.2) VIA
TYP

(2.8)
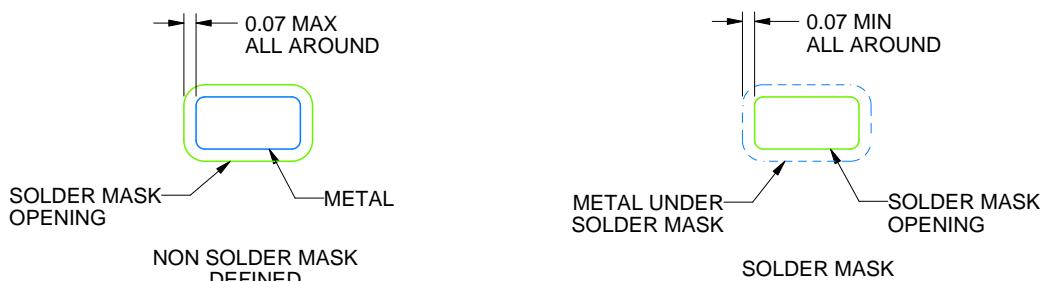
LAND PATTERN EXAMPLE
SCALE:20X

0.07 MAX
ALL AROUND

SOLDER MASK
OPENING

METAL

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)
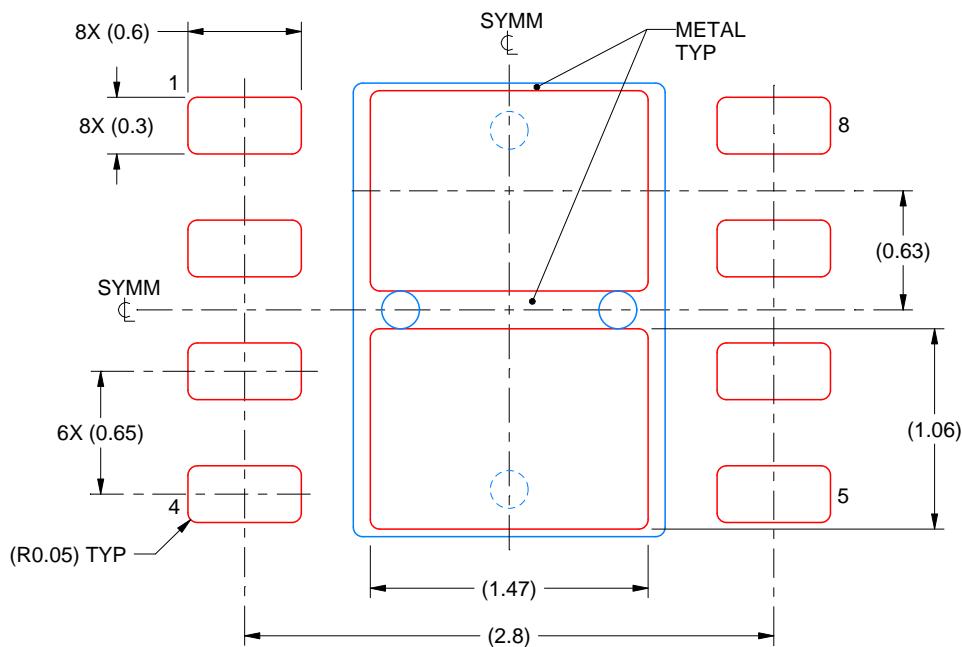
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

8X (0.6)

1

8X (0.3)

SYMM

SYMM

METAL
TYP

8

(0.63)

6X (0.65)

4

(R0.05) TYP

(1.06)

5

(1.47)

(2.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

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