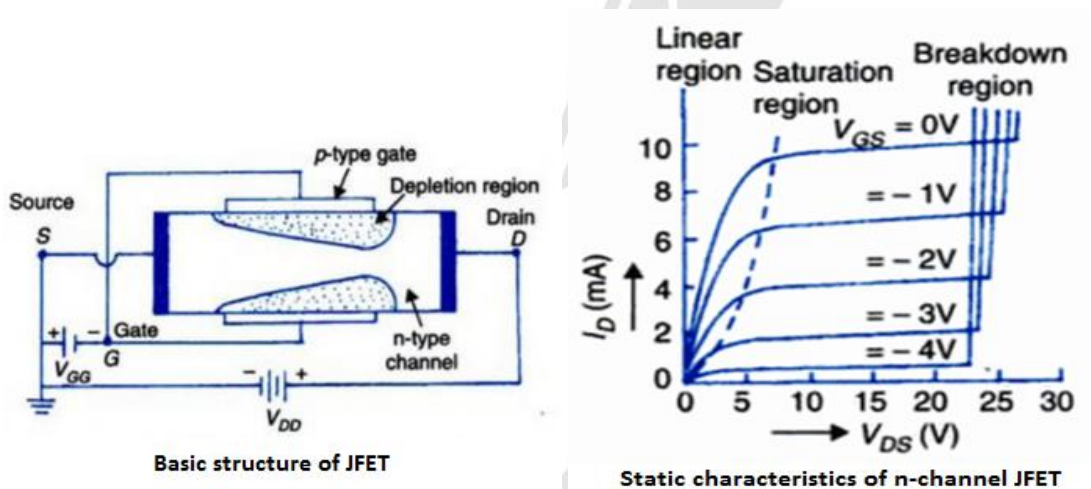


**Subject** : Basics of electronics engineering

**Question** : In JFET, How current increases linearly when  $V_{DS}$  is increased and the resistance is also increased?

**Answer** :

The behaviour of  $I_D$  versus  $V_{DS}$  can be studied in the static characteristics of JFET.

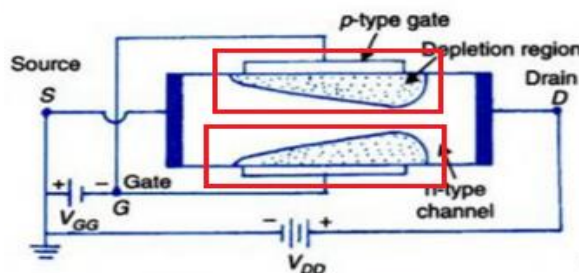


$V_{GS} = V_{GG}$  = gate to source voltage

$V_{DS} = V_{DD}$  = drain to source voltage

$I_D$  = Drain current

- When no voltage is applied to any one of terminals, the width of the depletion region remains very small. So, the semiconductor bar will behave like a simple resistor.
- Since the width of the depletion region remains very small, the drain current  $I_D$  increases linearly with respect to  $V_{DS}$  when  $V_{DS}$  is increased gradually from zero, keeping  $V_{GS}$  = constant.



- If  $V_{DS}$  is further increased keeping  $V_{GS} = \text{constant}$ , the width of the depletion region starts to increase, which in turn narrows down the channel opening.
- This will result in the increase of channel resistance and drain current  $I_d$  will increase less than linearly with respect to  $V_{DS}$ .

