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Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Science and Engineering

Continuous Assessment Test – II, MAR 2018

B-Tech Computer Science and Engineering

Course Code	**: CSE 2006**	**Duration: 90mns**
Course Name	**: Microprocessor and Interfacing**	**Max. Marks: 50**
Slot	**: B1**	

Answer ALL questions (5X10=50 Marks)

1. Explain how the interrupt vector table is designed in 8086 family processor and list the sequence of events when an interrupt is encountered by processor [10]
2. A) Given the frequency of the 8253 timer f=1.5MHz, configure the timer for rate generation mode for a time period of 400μs. [5]

   B) Explain about the functional pins of 8253 with necessary diagram [5]
3. Generate the system model to operate the 8259A in cascade mode and show that 64 interrupts can be accommodated in this mode. [10]
4. A) Given the control word is 8BH then list the configurations performed by 8255. [5]

   B) Design a system for driving a common anode seven segment display from an 8-bit port in mode 0, which in turn connected to 8086μp and also write a program using 8086 instruction that will cause the number "5" to appear on this display [5]
5. A) List serial data communication modes with brief explanation of each type and also draw the structure of asynchronous serial data transfer format [5]

   B) Present the template of command instruction format that aids to write a byte to the control register of 8251 and also generate the eight bit command when request to send (RTS) and data terminal ready (DTR) are programmed to be low [5]