Final Assessment Test – November 2017

VIT UNIVERSITY (Estd. u/s 3 of UGC Act 1956)

Course: CSE2001 - Computer Architecture and Organization

Class NBR(s):1253 / 1254 / 1257 / 1258 / 1259 / 1260 / 1261 / 1262 / 1263 / 1264 / 1959

Slot: B1+TB1

Time: Three Hours

Max. Marks: 100

Answer any TEN Questions
(10 X 10 = 100 Marks)

1. a) Explain the organization of Von-Neumann architecture in details. [5]

   b) A benchmark program is running on a 40 MHz processor. The executed program consists of 1,00,000 instruction executions, with the following instruction mix and clock cycle count: [5]

Instruction type	Instruction count	Cycles per instruction
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

   Determine the effective CPI, MIPS rate, and execution time for this program.

2. Derive an algorithm in flowchart form for the multiplication of signed 2's complement numbers. Solve (-9)X(-13) by using modified Booth's algorithm.

3. a) X=C17FFFFF H Compute X+1 [5]
   i. *if X is an integer*
   ii. *if X is a single precision floating point number*

   b) Perform restoring division operation on (8/3). [5]

4. Show the steps involved in multi-cycle data path design.

5. Evaluate a = (b+c)*d – e by 4-3-2-1-0 address IAS machine instructions and compute the memory traffic.

6. Design a cache memory unit with the capacity of 8KB, word size is 32-bits and block size is 8 words by using 4-way set associative mapping. Give the size of TAG memory as well as the data memory if the main memory capacity is 4 GB.

7. a) Suppose an 8-bit data word stored in memory is 11000010. Using the Hamming algorithm, determine what check bits would be stored in memory with the data word. [5]

   b) A virtual memory system has an address space of 8K words, a memory space of 4K words. The page and block sizes of 1K words. The following page reference changes occur during a given time interval. Determine the number of frames. And show the frames that are reside in main memory after each page reference, if the algorithm is Optimal page replacement algorithm. [5]

   4 3 2 0 1 2 0 4 3 5 2 0 1 2 3

8. a) A non-pipeline system takes 50ns to process a task. The same task can be processed in a six segments pipeline with a clock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup ratio that can be achieved? [5]

   b) Identify and explain possible hazards that can deviate the normal execution of pipeline with the help of instructions. [5]

9. a) What is the basic advantage of using iterrupt-initiated data transfer over transfer under program control without an interrupt? [5]

   b) Compare and contrast interrupt-initiated i/o and programmed i/o. [5]

10. Write short notes on a) Polling b) Daisy chaining priority.

11. Illustrate the organization and structure of magnetic disk drive.

12. a) Explain various components and features of superscalar processors. [5]

    b) Write short notes on memory hierarchy in terms of cost, size, and speed. [5]

13. Identify the all types of hazards for the given sequence of instructions of the mentioned expression and compute the number of clock cycles to complete the execution of all these instructions. Show pipeline diagram if MUL instruction takes 3 clock cycles, DIV -5 ADD and Subtract instructions takes 1 clock cycle.

    Z=(A*B)+(C/D)-E

    I_0 MUL R6,R0,R1 I1:DIV R7,R2,R3

    I2: ADD R8,R6,R7 I3:R5,R8,R4