Immediate, Direct, Register, Register Indirect, Indirect, Register Indexed, Based Indexed
Intersegment Direct / Indirect

Final Assessment Test – April 2018

VIT Vellore Institute of Technology

Course: CSE2006 - Microprocessor and Interfacing
Class NBR(s):3448 / 3471 / 3473 / 3476 / 3478 / 3482 / 3485 / 3486 / 4329
Slot: B1
Time: Three Hours
Max. Marks: 100

PART – A (8 X 5 = 40 Marks)
Answer ALL Questions

1. Illustrate the various advantages of 8086 architecture. More no of GP registers, powerful instruction set High speed, high memory addressing capability,
2. Categorize the addressing modes in 8086 according to type of instruction, execution with an example for each. Sequential transfer instructions, Control Transfer instructions
3. Write a program to multiply the two ASCII values in CH and CL and leave the ASCII result in AH and AL. Determine the contents of AX if CX = 3639H.
4. Illustrate the need for Interrupt Vector Table (IVT) in 8086. Explain the address calculation for a random interrupt INT n.
5. Explain how 8255 supports various modes of data transfer techniques to handle IO devices with a neat block diagram.
6. Justify how 8253 combines hardware and software approach for precise delay generation with an example. Mode 5 & Mode 4
7. Explain various serial data transmission modes. Give the frame format for asynchronous data transfer mode. Simplex, Half Duplex, Duplex.
8. Categorize the 8087 instruction set and list out the instructions for transcendental functions.
Data transfer, Arithmetic, Compare, Transcendental, Load Constant, Processor Control.
From Trigonometric & Exponential

PART – B (6 X 10 = 60 Marks)
Answer any SIX Questions

FPTAN, FSXM1, MYLSX

9. Discuss how 8086 operates in minimum mode with necessary functional diagram and timing diagram.
10. Write an ALP to arrange given series of hexadecimal bytes in an ascending order.
11. Illustrate various programming control structures with a real time example for each.
(Give Pseudo-code, flowchart and assembly code)
12. Draw and Discuss the internal architecture of coprocessor 8087.
13. Discuss in detail the need for programmable interrupt controller 8259 with necessary block diagram and initialization command words.
14. Design the hard ware interface circuit for interfacing 8251 with 8086.
Write an ALP to transmit 100 bytes of data string starting at location 2000:5000H by setting the 8251A in asynchronous mode as a transmitter and receiver with even parity enabled, 1 Stop bit, 5-bit Character length, frequency 160 KHz and baud rate 10K.
15. Explain 8255 control word format in detail.
Derive the control word to initialize the 8255 for the following specifications:
    a) Port B as an input port in mode-1
    b) Port A as an output port in mode-0
    c) Port C upper as an input port
    d) Port C bit 3 as output

12. a) List various 8087 instructions for data transfer.
    b) Write an 8086/8087 procedure to calculate the area of circle. Assume that the integer radius is passed in register AH and return the area (rounded to the nearest integer) in BX:AX

13. a) Specify the asynchronous mode instruction format and command instruction format for 8251A.
    b) Write the initialization routine required to program the 8251A USART for asynchronous transmission with 7 data bits, 2 stop bits, and odd parity. Select a 16 X clock and Program DTR and RTS to be low.

14. Design a programmable timer using 8253 and 8086. Interface 8253 at an address 0040H for counter 0 and write the following ALPs. The 8086 and 8253 run at 6 MHz and 1.5 MHz respectively.
    a) To generate a square wave of period 1ms.
    b) To interrupt the processor after 10 ms.
    c) To derive a monoshot pulse with quasistable state duration 5 ms.

15. With a neat sketch explain the internal block diagram and operating modes of 8255 programmable parallel port device.

16. Briefly explain about your CAL 'J' component project work in the following illustrations.
    a) Objectives H/w and s/w components identification
    b) Block diagram/schematic diagram and
    c) Pseudocode and challenges faced during your project work.