VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Science and Engineering
Continuous Assessment Test – I, JAN 2018

B-Tech Computer Science and Engineering

Course Code	: CSE 2006	Duration : 90mns
Course Name	: Microprocessor and Interfacing	Max. Marks: 50
Slot	: B1	

Answer ALL questions (5X10=50 Marks)

1. A) Determine the contents of register AL after the following instructions are executed.

```
MOV AL, 3AH
MOV CH, 0A9H
ADD CH, 06H
ADD AL, CH
NEG AL
DEC AL
```

   B) Illustrate with an ALP code to show how the following control structures are implemented using 8086.
   Repeat- Until
   FOR Loop

2. A)Explain the function of the following pins
   NMI, HOLD, ALE, $\overline{BHE}$, READY.
   B) [I] What physical memory location is accessed by the instruction MOV [BP], AL. If BP = 2C30H? Assume the stack segment base address = 5D27H. (2)
   [II] If Register AL=0FFH, and the instruction ADD AL, 01H is given, Specify the contents of the six status flags. (3)
3. With necessary diagram explain the internal architecture of 8086 along with the overlapping of the instruction fetch and execution mechanism called pipelining.
4. Discuss how 8086 operates in minimum mode with timing diagram.
5. a) Write an assembly language program to find smallest among N numbers. (5)
   b) Identify the addressing mode for each of the following instructions. (5)
      i) MOV AH, 47H
      ii) MOV SP, BX
      iii) MOV AH, [BP+SI]
      iv) OUT DX, AX
      v) MOV DX, [BX+SI+0AH]