B2

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Science and Engineering

Continuous Assessment Test I – August – 2018
B.Tech Computer Science and Engineering- III Semester

CSE2001 –Computer Architecture and Organization

Answer all the questions **(5 x10 = 50Marks)**

1.(a) Compare and Contrast Von-Neumann and Harvard architecture. [3]

1.(b) If the last operation performed on a computer with an 8-bit word was an addition in which the two operands were binary 2 and 9, what would be the value of the following status flags: carry, zero, overflow, sign, and even parity? [2]

1. (c) Match the following columns: [5]

instruction	Operation
Shift left	SUBTRACT
Compare	DIVISION
Exclusive-or of same register	AND
Shift right	CLEAR
TEST instruction	MULTIPLICATION

2. Comment on the Booth's algorithm and its efficiency for multiplication representing the steps as a flow chart. Demonstrate step by step multiplication of (-9) × (-15) using Booth's algorithm. [10]

3. With divisor as 2 and dividend as 9, perform step by step restoring binary division. [10]

4.(a) Explain the big-endian and little-endian memory storage formats. Illustrate with an example for a 4 byte value. [5]

4 (b) Discuss in detail various stages of instruction execution cycle with a neat sketch. [5]

5. Given a mathematical operation "a = b + c", where a, b and c are memory locations. CPU has 128 different instructions, If word length of memory is given to be 2 bytes and the address length to store the data is given as 16 bits. calculate [10]

(i) Memory to encode these instructions
(ii) Memory traffic for these instructions

for following instruction formats:

(a) 3 Address instruction format
(b) 2 Address instruction format
(c) 1 Address instruction format
(d) 0 Address instruction format

Mention assumptions if made any.

**** All the best ****