



VIT

Vellore Institute of Technology
(Deemed to be University) established by an Act of Parliament No. 15 of 1984

B1

School of Computer Science and Engineering
Continuous Assessment Test I – August – 2018

B.Tech Computer Science and Engineering- III Semester

CSE2001 –Computer Architecture and Organization

PART - A

Answer all the questions

(5 x 10 = 50 Marks)

1. Identify the instruction type (Data transfer, Arithmetic, Logical and Program Control) for the following instructions

- a. Exchange – swap contents of source and destination
- b. Negate – Change sign of the operand
- c. Test – Test specified conditions; (set flags based on outcome)
- d. Halt – Stop program Execution
- e. Skip – increment PC to skip next instruction

2. Identify the addressing mode for the following specification:

An instruction is stored at location 2000 with its address field at location 2001. The address field has the value 800. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate (c) relative (d) register (e) index with R1 as the index register.

3. Explain the expanded structure of IAS Architecture in detail with the help of diagram.

3. a) A benchmark program is on a 40 MHz processor. The executed program consist of 1,100 instruction executions with the following instruction mix and clock cycle count.

Instruction Type	Instruction Count	Cycles Per Instruction
Integer Arithmetic	300	1
Data transfer	200	2
Floating point	100	2
Control transfer	500	2

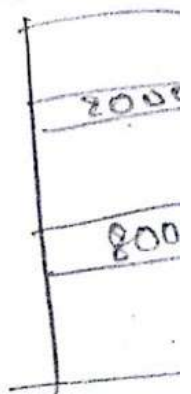
Determine the effective CPI, MIPS rate, and execution time for this program

- b) Perform Booth's multiplication on the given data of $6 * (-3)$.

4. Compute Memory traffic, total memory for encoding and storing code that implements the expression evaluation for the following code. Assume that the opcode occupy one byte, addresses occupy two bytes, and data values also occupy two bytes and 1 byte word length for 3-, 2-, 1-, 0- address machines.

3 addr	2-addr	1-addr	0-addr
MUL A,B,C	MUL B,C	LOAD D	PUSH B
DIV D,D,E	DIV D,E	DIV E	PUSH C
SUB A,A,D	SUB B,D	STOR D	MUL
	STOR A,B	LOAD B	PUSH D
		MUL C	PUSH E
		SUB D	DIV
		STOR A	SUB
			POP A

5. Draw the flowchart for restoring division and perform the same for 12 by 3.



Handwritten notes: "B*", "C", and a checkmark.