VIT® UNIVERSITY (Estd. u/s 3 of UGC Act 1956)

Final Assessment Test (FAT) – May 2017

Course : CSE1003 - Digital Logic and Design

Class NBR(s):1661 / 1670 / 1679 / 1685 / 1690 / 1701 / 1715 / 1728 / 1734 / 1742 / 1743 Slot: B2

Time: Three Hours Max. Marks: 100

Answer any TEN Questions
(10 X 10 = 100 Marks)

1. a) Formulate a weighted binary code for decimal digits using weights [5]
   i. 6, 3, 1, 1
   ii. 6, 4, 2, 1

   b) Represent the decimal number **5.137** in [5]
   i) BCD ii) excess-3 code
   iii) 2421 code iv) a 6311 code

2. a) The following function is in minimum sum of products form. Implement it using **only 2- input NAND gates**. No gate may be used as a NOT gate. Show both block diagram and the equation. (You should not use more than 12 NAND gates) [6]
   G = A B C E' + A' B' E' + B' C' E + A' B C E + A D'

   b) Show that the dual of the exclusive-OR is equal to its Complement. [4]

3. Minimize the following Boolean function F using Quine -McCluskey method and find the essential prime implicants:

$$F(A, B, C, D) = \Sigma m\,(2, 3, 7, 9, 11, 13) + \Sigma\, d(1, 10, 15)$$

4. Design a circuit that counts the number of 1's present in 3 inputs **A, B** and **C**. Its output is a two-bit number X_1X_0, representing that count in binary. Assume active-HIGH logic.

5. An 8 × 1 multiplexer has inputs A, B and C connected to the selection inputs S_2, S_1, and S_0 respectively. The data inputs I_0 through I_7 are as follows:
   a) $I_1 = I_2 = I_7 = 0$; $I_3 = I_5 = 1$; $I_0 = I_4 = D$; and $I_6 = D'$.
   b) $I_1 = I_2 = 0$; $I_3 = I_7 = 1$; $I_4 = I_5 = D$; and $I_0 = I_6 = D'$.

   Determine the Boolean function that the multiplexer implement.

6. Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

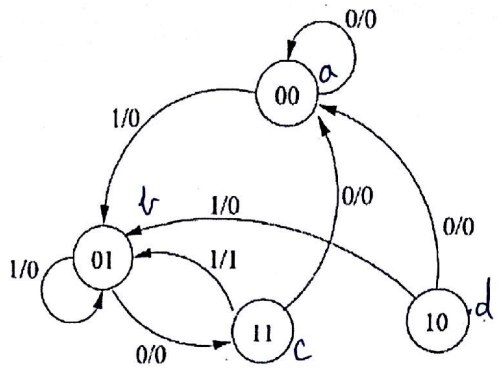
   $F_1 = (y' + x)\,z$

   $F_2 = y'z' + xy' + yz'$

   $F_3 = (x' + y)\,z$

7. Design a combinational circuit that generates the 9's complement of BCD digit.

8. Consider the following state diagram for a synchronous circuit with one input **X** and one output **Z**. Analyze this state diagram and draw its circuit implementation using **JK flip-flop** (for state Q_0) and **T flip-flop** (for state Q_1).



9. a) What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed? [5]

   b) The contents of a four-bit register are initially **1011**. The register is shifted six times to the right, with the serial input being **101 101**. What are the contents of the register after each shift? [5]

10. Designs a counter with **T flip -flops** that goes through the following binary repeated sequence: **0, 1, 3, 7, 6, 4**. Show that when binary states **010** and **101** are taken to be don't-care conditions. The counter may not operate properly. Find a way to correct the design.

11. List the modes of operation of a Shift register. Illustrate the data bit flow in all the modes.

12. Write a short note on VLSI and FPGA architectures.

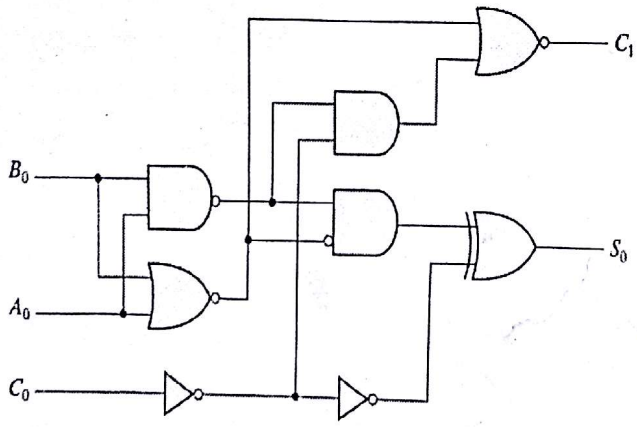
13. Define the carry propagate and carry generate as

$$P_i = A_i + B_i$$
$$G_i = A_i B_i$$

respectively. Show that the output carry and output sum of a full adder becomes

$$C_{i+1} = (C_i' G_i' + P_i')'$$
$$S_i = (P_i G_i') \oplus C_i$$

If the logic diagram of the first stage of a four-bit parallel adder is as shown below. Identify the P_i' and G_i' terminals and show that the circuit implements a full-adder circuit. Also Derive the Boolean functions for the lookahead carries C_2, C_3, and C_4.



⇔⇔⇔