		Serial	Deterministic	Nondeterministic	
				n=5	n = 10
VectorAdd (f32, 500000) @ 28 SM's [17.46 blocks/SM]					
DRAM	t = 4	195 V	125K~(0%)	125K~(0%)	125K~(0%)
reads	t = 8	125K	125K~(0%)	125K~(0%)	125K~(0%)
DRAM	t = 4	62.5K	62.5K~(0%)	62.5K~(0%)	62.5K~(0%)
writes	t = 8	02.5K	62.5K~(0%)	62.5K~(0%)	62.5K~(0%)
L1D	t = 4	0.0%	0% (0%)	0% (0%)	0% (0%)
hit rate	t = 8	0.076	0% (0%)	0% (0%)	0% (0%)
L2D	t = 4	0%	0% (0%)	0% (0%)	0% (0%)
hit rate	t = 8	070	0% (0%)	0% (0%)	0% (0%)
Cycles	t = 4	28.3K	28.3K~(0%)	28.3K~(0.4%)	28.3K~(0.2%)
Cycles	t = 8	20.511	28.3K~(0%)	28.5K~(0.6%)	28.4K~(0.3%)
Exec	t = 4	32.0s	$13.4s\ (2.4x)$	9.2s~(3.5x)	$9.2s\ (3.5x)$
time	t = 8	32.00	12.0s(2.7x)	6.7s(4.8x)	$6.3s\left(5.1x ight)$
VectorAdd (f32, 500000) @ 112 SM's [4.37 blocks/SM]					
DRAM	t = 4	125K	125K~(0%)	125K~(0%)	125K~(0%)
reads	t = 8	12011	125K~(0%)	125K~(0%)	125K~(0%)
DRAM	t=4	62.5K	62.5K~(0%)	62.5K~(0%)	62.5K~(0%)
writes	t = 8	02.011	62.5K~(0%)	62.5K~(0%)	62.5K~(0%)
L1D	t = 4	0.0%	0% (0%)	0% (0%)	0% (0%)
hit rate	t = 8	0.070	0% (0%)	0% (0%)	0% (0%)
L2D	t = 4	0%	0% (0%)	0% (0%)	0% (0%)
hit rate	t = 8	070	0% (0%)	0% (0%)	0% (0%)
Cycles	t = 4	28.3K	28.3K~(0%)	28.3K~(0%)	28.3K~(0.1%)
0,0.00	t = 8	20.011	28.3K~(0%)	28.3K~(0.2%)	28.4K~(0.3%)
Exec	t=4	144.9s	$44.2s\ (3.3x)$	37.9s(3.8x)	$37.4s\ (3.9x)$
time	t = 8		$29.4s\ (4.9x)$	23.0s(6.3x)	$22.5s\ (6.4x)$
Average VectorAdd (12 configurations) @ 28 SM's					
DRAM	t = 4		0%	0%	0%
reads	t = 8		0%	0%	0%
DRAM	t = 4		0%	0%	0%
writes	t = 8		0%	0%	0%
L1D	t = 4		0%	0%	0%
hit rate	t = 8		0%	0%	0%
L2D	t=4		0%	0%	0%
hit rate	t = 8		0%	0%	0%
Cycles	t = 4		0%	0.2%	0.3%
	t = 8		0%	0.3%	0.3%
Exec time	t=4		1.5x	1.7x	1.8x
	t = 8		1.6x	2x	2.1x
Average VectorAdd (12 configurations) @ 112 SM's					
DRAM	t = 4		0%	0%	0%
reads	t = 8		0%	0%	0%
DRAM	t=4		0%	0%	0%
writes	t = 8		0%	0%	0%
L1D hit rate	t=4		0%	0%	0%
	t = 8		0%	0%	0%
L2D hit rate	t=4		0%	0%	0%
ini rate	t = 8		0%	0%	0%
Cycles	t=4		0%	8.5%	8.6%
	t = 8		0%	8.6%	8.6%
Exec time	t=4		1.7x	2x	2.1x
une	t = 8		2.1x	2.5x	2.6x