		Serial	Deterministic	Nondeterministic	
				$n = 5$	$n = 10$
MatrixMul (f32, 512×512×512) @ 28 SM's [9.14 blocks/SM]					
DRAM reads	$t = 4$	65.5K	65.5K (0%)	65.5K (0%)	65.5K (0%)
	$t = 8$		65.5K (0%)	65.5K (0%)	65.5K (0%)
DRAM writes	$t = 4$	1.4K	1.4K (0%)	1.4K (0.6%)	1.5K (1.7%)
	$t = 8$		1.4K (0%)	1.4K (0.8%)	1.5K (1.3%)
L1D hit rate	$t = 4$	0.0%	0% (0%)	0% (0%)	0% (0%)
	$t = 8$		0% (0%)	0.1% (0.1%)	0% (0%)
L2D hit rate	$t = 4$	93.8%	93.8% (0%)	93.8% (0%)	93.8% (0%)
	$t = 8$		93.8% (0%)	93.8% (0%)	93.8% (0%)
Cycles	$t = 4$	302.3K	302.3K (0%)	302.3K (0%)	302.1K (0.1%)
	$t = 8$		302.3K (0%)	302.1K (0.1%)	302.5K (0.1%)
Exec time	$t = 4$	600.1s	217.0s (2.8x)	179.1s (3.4x)	**174.9s (3.4x)**
	$t = 8$		160.9s (3.7x)	128.9s (4.7x)	**124.2s (4.8x)**
MatrixMul (f32, 512×512×512) @ 112 SM's [2.29 blocks/SM]					
DRAM reads	$t = 4$	65.5K	65.5K (0%)	65.5K (0%)	65.5K (0%)
	$t = 8$		65.5K (0%)	65.5K (0%)	65.5K (0%)
DRAM writes	$t = 4$	2.3K	2.3K (0%)	2.3K (2.1%)	2.2K (1.7%)
	$t = 8$		2.3K (0%)	2.3K (1.8%)	2K (7.3%)
L1D hit rate	$t = 4$	6.3%	6.3% (0%)	6.3% (0.2%)	6.4% (0.3%)
	$t = 8$		6.3% (0%)	6.1% (0.2%)	5.9% (0.4%)
L2D hit rate	$t = 4$	93.3%	93.3% (0%)	93.3% (0%)	93.3% (0%)
	$t = 8$		93.3% (0%)	93.3% (0%)	93.4% (0.1%)
Cycles	$t = 4$	110.3K	110.3K (0%)	110.9K (1%)	111.3K (0.9%)
	$t = 8$		110.3K (0%)	110.2K (0.1%)	110.2K (0.2%)
Exec time	$t = 4$	883.0s	396.2s (2.3x)	259.4s (3.4x)	**251.8s (3.5x)**
	$t = 8$		305.9s (3x)	166.0s (5.3x)	**161.4s (5.5x)**