		Serial	Deterministic	Nondeterministic	
				n=5	n = 10
VectorAdd (f32, 500000) @ 28 SM's [17.46 blocks/SM]					
DRAM reads	t = 4	125K	125K~(0%)	125K~(0%)	125K~(0%)
	t = 8		125K~(0%)	125K~(0%)	125K~(0%)
DRAM writes	t = 4	62.5K	62.5K~(0%)	62.5K~(0%)	62.5K~(0%)
	t = 8		62.5K~(0%)	62.5K~(0%)	62.5K~(0%)
L1D hit rate	t = 4	0.0%	0% (0%)	0% (0%)	0% (0%)
	t = 8		0% (0%)	0% (0%)	0% (0%)
L2D hit rate	t = 4	0%	$0\% \ (0\%)$	0% (0%)	0% (0%)
	t = 8		0% (0%)	0% (0%)	0% (0%)
Cycles	t = 4	28.3K	28.3K~(0%)	28.3K~(0.4%)	28.3K~(0.2%)
	t = 8		28.3K~(0%)	28.5K~(0.6%)	28.4K~(0.3%)
Exec time	t = 4	32.0s	$13.4s\ (2.4x)$	9.2s~(3.5x)	$9.2s\ (3.5x)$
	t = 8		12.0s(2.7x)	6.7s(4.8x)	6.3s~(5.1x)
VectorAdd (f32, 500000) @ 112 SM's [4.37 blocks/SM]					
DRAM reads	t = 4	125K	125K~(0%)	125K~(0%)	125K~(0%)
	t = 8		125K~(0%)	125K~(0%)	125K~(0%)
DRAM writes	t = 4	62.5K	62.5K~(0%)	62.5K~(0%)	62.5K~(0%)
	t = 8		62.5K~(0%)	62.5K~(0%)	62.5K~(0%)
L1D hit rate	t = 4	0.0%	0% (0%)	0% (0%)	0% (0%)
	t = 8		0% (0%)	0% (0%)	0% (0%)
L2D	t = 4	0%	0% (0%)	0% (0%)	0% (0%)
hit rate	t = 8		0% (0%)	0% (0%)	0% (0%)
Cycles	t = 4	28.3K	28.3K~(0%)	28.3K~(0%)	28.3K~(0.1%)
Oycles	t = 8	20.5K	28.3K~(0%)	28.3K~(0.2%)	28.4K~(0.3%)
Exec time	t = 4	144.9s	$44.2s\ (3.3x)$	37.9s(3.8x)	$37.4s\left(3.9x ight)$
	t = 8	144.98	$29.4s\ (4.9x)$	23.0s(6.3x)	$22.5s\left(6.4x\right)$