		Serial	Deterministic	Nondeterministic	
				n=5	n = 10
Transpose (coalesced, 512×512) @ 28 SM's [36.57 blocks/SM]					
DRAM reads	t = 4	32.8K	32.8K~(0%)	32.8K~(0%)	32.8K~(0%)
	t = 8		32.8K~(0%)	32.8K~(0%)	32.8K~(0%)
DRAM writes	t = 4	0	0 (0%)	0 (0%)	0 (0%)
	t = 8		0 (0%)	0 (0%)	0 (0%)
L1D hit rate	t = 4	0.0%	0% (0%)	0% (0%)	$0\% \ (0\%)$
	t = 8		0% (0%)	0% (0%)	$0\% \ (0\%)$
L2D hit rate	t = 4	50%	50% (0%)	50% (0%)	50%~(0%)
	t = 8		50% (0%)	50% (0%)	50%~(0%)
Cycles	t = 4	12K	12K~(0%)	12K~(0.2%)	$12K\ (1\%)$
	t = 8		12K~(0%)	12.2K~(1.2%)	12K~(0.5%)
Exec time	t = 4	13.4s	6.4s(2.1x)	$5.0s\left(2.7x ight)$	5.0s(2.7x)
	t = 8		5.6s(2.4x)	4.2s(3.2x)	$3.7s\left(3.6x ight)$
Transpose (coalesced, 512×512) @ 112 SM's [9.14 blocks/SM]					
DRAM	t = 4	32.8K	32.8K~(0%)	32.8K~(0%)	32.8K~(0%)
reads	t = 8		32.8K~(0%)	32.8K~(0%)	32.8K~(0%)
DRAM writes	t = 4	0	0 (0%)	0 (0%)	0 (0%)
	t = 8		0 (0%)	0 (0%)	0 (0%)
L1D hit rate	t = 4	0.0%	0% (0%)	0% (0%)	0% (0%)
	t = 8		0% (0%)	0% (0%)	0% (0%)
L2D hit rate	t = 4	50%	50% (0%)	50% (0%)	50% (0%)
	t = 8		50% (0%)	50% (0%)	50%~(0%)
Cycles	t = 4	10.8K	10.8K~(0%)	10.8K~(0.4%)	10.8K~(0.4%)
Cycles	t = 8		10.8K~(0%)	10.8K~(0.5%)	10.8K~(0.4%)
Exec time	t = 4	39.0s	$13.5s\ (2.9x)$	$12.4s\ (3.2x)$	$12.4s\ (3.1x)$
	t = 8		$10.2s\ (3.8x)$	8.9s(4.4x)	$8.4s\left(4.7x ight)$