

		Serial	Deterministic	Nondeterministic	
				$n = 5$	$n = 10$
VectorAdd (f32, 500000) @ 28 SM's [17.46 blocks/SM]					
DRAM reads	$t = 4$	125 <i>K</i>	125 <i>K</i> (0%)	125 <i>K</i> (0%)	125 <i>K</i> (0%)
	$t = 8$		125 <i>K</i> (0%)	125 <i>K</i> (0%)	125 <i>K</i> (0%)
DRAM writes	$t = 4$	62.5 <i>K</i>	62.5 <i>K</i> (0%)	62.5 <i>K</i> (0%)	62.5 <i>K</i> (0%)
	$t = 8$		62.5 <i>K</i> (0%)	62.5 <i>K</i> (0%)	62.5 <i>K</i> (0%)
L1D hit rate	$t = 4$	0.0%	0% (0%)	0% (0%)	0% (0%)
	$t = 8$		0% (0%)	0% (0%)	0% (0%)
L2D hit rate	$t = 4$	0%	0% (0%)	0% (0%)	0% (0%)
	$t = 8$		0% (0%)	0% (0%)	0% (0%)
Cycles	$t = 4$	28.3 <i>K</i>	28.3 <i>K</i> (0%)	28.3 <i>K</i> (0.4%)	28.3 <i>K</i> (0.2%)
	$t = 8$		28.3 <i>K</i> (0%)	28.5 <i>K</i> (0.6%)	28.4 <i>K</i> (0.3%)
Exec time	$t = 4$	32.0 <i>s</i>	13.4 <i>s</i> (2.4 <i>x</i>)	9.2<i>s</i> (3.5<i>x</i>)	9.2 <i>s</i> (3.5 <i>x</i>)
	$t = 8$		12.0 <i>s</i> (2.7 <i>x</i>)	6.7 <i>s</i> (4.8 <i>x</i>)	6.3<i>s</i> (5.1<i>x</i>)
VectorAdd (f32, 500000) @ 112 SM's [4.37 blocks/SM]					
DRAM reads	$t = 4$	125 <i>K</i>	125 <i>K</i> (0%)	125 <i>K</i> (0%)	125 <i>K</i> (0%)
	$t = 8$		125 <i>K</i> (0%)	125 <i>K</i> (0%)	125 <i>K</i> (0%)
DRAM writes	$t = 4$	62.5 <i>K</i>	62.5 <i>K</i> (0%)	62.5 <i>K</i> (0%)	62.5 <i>K</i> (0%)
	$t = 8$		62.5 <i>K</i> (0%)	62.5 <i>K</i> (0%)	62.5 <i>K</i> (0%)
L1D hit rate	$t = 4$	0.0%	0% (0%)	0% (0%)	0% (0%)
	$t = 8$		0% (0%)	0% (0%)	0% (0%)
L2D hit rate	$t = 4$	0%	0% (0%)	0% (0%)	0% (0%)
	$t = 8$		0% (0%)	0% (0%)	0% (0%)
Cycles	$t = 4$	28.1 <i>K</i>	28.1 <i>K</i> (0%)	28.2 <i>K</i> (0.3%)	28.3 <i>K</i> (0.5%)
	$t = 8$		28.1 <i>K</i> (0%)	28.3 <i>K</i> (0.5%)	28.3 <i>K</i> (0.7%)
Exec time	$t = 4$	142.3 <i>s</i>	44.0 <i>s</i> (3.2 <i>x</i>)	37.5 <i>s</i> (3.8 <i>x</i>)	37.2<i>s</i> (3.8<i>x</i>)
	$t = 8$		29.8 <i>s</i> (4.8 <i>x</i>)	22.4 <i>s</i> (6.4 <i>x</i>)	22.3<i>s</i> (6.4<i>x</i>)
Average VectorAdd (12 configurations) @ 28 SM's					
DRAM reads	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
DRAM writes	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
L1D hit rate	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
L2D hit rate	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
Cycles	$t = 4$		0%	0.2%	0.3%
	$t = 8$		0%	0.3%	0.3%
Exec time	$t = 4$		1.5 <i>x</i>	1.7 <i>x</i>	1.8<i>x</i>
	$t = 8$		1.6 <i>x</i>	2 <i>x</i>	2.1<i>x</i>
Average VectorAdd (12 configurations) @ 112 SM's					
DRAM reads	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
DRAM writes	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
L1D hit rate	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
L2D hit rate	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
Cycles	$t = 4$		0%	0.1%	0.2%
	$t = 8$		0%	0.2%	0.2%
Exec time	$t = 4$		1.7 <i>x</i>	2.2 <i>x</i>	2.2<i>x</i>
	$t = 8$		2 <i>x</i>	2.7 <i>x</i>	2.8<i>x</i>