		Serial	Deterministic	Nondeterministic	
				n=5	n = 10
Transpose (coalesced, 512×512) @ 28 SM's [36.57 blocks/SM]					
DRAM reads	t = 4	22 0 V	32.8K~(0%)	32.8K~(0%)	32.8K~(0%)
	t = 8	32.8K	32.8K~(0%)	32.8K~(0%)	32.8K~(0%)
DRAM	t = 4	0	0 (0%)	0 (0%)	0 (0%)
writes	t = 8	0	0 (0%)	0 (0%)	0 (0%)
L1D	t = 4	0.0%	0% (0%)	0% (0%)	0% (0%)
hit rate	t = 8	0.070	0% (0%)	0% (0%)	0% (0%)
L2D	t = 4	50%	50% (0%)	50% (0%)	50%~(0%)
hit rate	t = 8	3070	50% (0%)	50% (0%)	50%~(0%)
Cycles	t = 4	12K	12K~(0%)	12K~(0.2%)	12K~(1%)
Cycles	t = 8	1211	12K~(0%)	12.2K~(1.2%)	12K~(0.5%)
Exec	t = 4	13.4s	6.4s(2.1x)	5.0s~(2.7x)	5.0s(2.7x)
time	t = 8	10.10	5.6s(2.4x)	4.2s(3.2x)	3.7s~(3.6x)
Transpose (coalesced, 512×512) @ 112 SM's [9.14 blocks/SM]					
DRAM	t = 4	32.8K	32.8K~(0%)	32.8K~(0%)	32.8K~(0%)
reads	t = 8	52.GI	32.8K~(0%)	32.8K~(0%)	32.8K~(0%)
DRAM writes	t = 4	0	0 (0%)	0 (0%)	0 (0%)
	t = 8	0	0 (0%)	0 (0%)	0 (0%)
L1D hit rate	t = 4	0.0%	0% (0%)	0% (0%)	0% (0%)
	t = 8		0% (0%)	0% (0%)	0% (0%)
L2D hit rate	t = 4	50%	50% (0%)	50% (0%)	50%~(0%)
	t = 8		50% (0%)	50% (0%)	50% (0%)
Oveles	t = 4	10.9 <i>V</i>	10.8K~(0%)	10.8K~(0.4%)	10.8K~(0.4%)
Cycles	t = 8	10.8K	10.8K~(0%)	10.8K~(0.5%)	10.8K~(0.4%)
Exec	t = 4	39.0s	$13.5s\ (2.9x)$	$12.4s\ (3.2x)$	12.4s(3.1x)
time	t = 8	39.08	$10.2s\ (3.8x)$	8.9s(4.4x)	$8.4s\left(4.7x ight)$
Average Transpose (6 configurations) @ 28 SM's					
DRAM	t = 4		0%	0%	0%
reads	t = 8		0%	0%	0%
DRAM	t = 4		0%	0%	0%
writes	t = 8		0%	0%	0%
L1D	t = 4		0%	0%	0%
hit rate	t = 8		0%	0%	0%
L2D	t = 4		0%	0%	0%
hit rate	t = 8		0%	0%	0%
Cycles	t = 4		0%	0.4%	0.5%
Cycles	t = 8		0%	0.5%	0.3%
Exec	t = 4		1.9x	2.4x	2.4x
time	t = 8		2x	2.8x	2.9x
Average Transpose (6 configurations) @ 112 SM's					
DRAM	t = 4		0%	0%	0%
reads	t = 8		0%	0%	0%
DRAM	t = 4		0%	0%	0%
writes	t = 8		0%	0%	0%
L1D	t = 4		0%	0%	0%
hit rate	t = 8		0%	0%	0%
L2D	t = 4		0%	0%	0%
hit rate	t = 8		0%	0%	0%
Cycles	t = 4		0%	1.6%	1.6%
Cyclos	t = 8		0%	1.6%	1.4%
Exec	t = 4		2.4x	2.9x	2.9x
time	t = 8		3x	3.7x	3.8x