		Serial	Deterministic	Nondeterministic	
				$n = 5$	$n = 10$
MatrixMul (f32, 512×512×512) @ 28 SM's [9.14 blocks/SM]					
DRAM reads	$t = 4$	$65.5K$	$65.5K$ (0%)	$65.5K$ (0%)	$65.5K$ (0%)
	$t = 8$		$65.5K$ (0%)	$65.5K$ (0%)	$65.5K$ (0%)
DRAM writes	$t = 4$	$1.4K$	$1.4K$ (0%)	$1.4K$ (0.6%)	$1.5K$ (1.7%)
	$t = 8$		$1.4K$ (0%)	$1.4K$ (0.8%)	$1.5K$ (1.3%)
L1D hit rate	$t = 4$	0.0%	0% (0%)	0% (0%)	0% (0%)
	$t = 8$		0% (0%)	0.1% (0.1%)	0% (0%)
L2D hit rate	$t = 4$	93.8%	93.8% (0%)	93.8% (0%)	93.8% (0%)
	$t = 8$		93.8% (0%)	93.8% (0%)	93.8% (0%)
Cycles	$t = 4$	$302.3K$	$302.3K$ (0%)	$302.3K$ (0%)	$302.1K$ (0.1%)
	$t = 8$		$302.3K$ (0%)	$302.1K$ (0.1%)	$302.5K$ (0.1%)
Exec time	$t = 4$	$600.1s$	$217.0s$ ($2.8x$)	$179.1s$ ($3.4x$)	**$174.9s$ ($3.4x$)**
	$t = 8$		$160.9s$ ($3.7x$)	$128.9s$ ($4.7x$)	**$124.2s$ ($4.8x$)**
MatrixMul (f32, 512×512×512) @ 112 SM's [2.29 blocks/SM]					
DRAM reads	$t = 4$	$65.5K$	$65.5K$ (0%)	$65.5K$ (0%)	$65.5K$ (0%)
	$t = 8$		$65.5K$ (0%)	$65.5K$ (0%)	$65.5K$ (0%)
DRAM writes	$t = 4$	$2.3K$	$2.3K$ (0%)	$2.3K$ (1%)	$2.2K$ (1.8%)
	$t = 8$		$2.3K$ (0%)	$2.2K$ (3.5%)	$2.3K$ (1.2%)
L1D hit rate	$t = 4$	6.4%	6.4% (0%)	6.4% (0.3%)	6.6% (0.2%)
	$t = 8$		6.4% (0%)	6.1% (0.3%)	6.5% (0.1%)
L2D hit rate	$t = 4$	93.3%	93.3% (0%)	93.3% (0%)	93.3% (0%)
	$t = 8$		93.3% (0%)	93.3% (0%)	93.3% (0%)
Cycles	$t = 4$	$111.3K$	$111.3K$ (0%)	$111.2K$ (0.4%)	$113.6K$ (2.1%)
	$t = 8$		$111.3K$ (0%)	$111.6K$ (0.3%)	$112.8K$ (1.4%)
Exec time	$t = 4$	$894.7s$	$279.6s$ ($3.2x$)	$260.6s$ ($3.4x$)	**$253.0s$ ($3.5x$)**
	$t = 8$		$190.3s$ ($4.7x$)	$164.4s$ ($5.4x$)	**$162.7s$ ($5.5x$)**
Average Matrixmul (5 configurations) @ 28 SM's					
DRAM reads	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
DRAM writes	$t = 4$		0%	0.1%	0.3%
	$t = 8$		0%	0.2%	0.3%
L1D hit rate	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
L2D hit rate	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
Cycles	$t = 4$		0%	0.2%	0.2%
	$t = 8$		0%	0.1%	0.2%
Exec time	$t = 4$		$2x$	$2.4x$	**$2.5x$**
	$t = 8$		$2.3x$	$2.9x$	**$3x$**
Average Matrixmul (5 configurations) @ 112 SM's					
DRAM reads	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
DRAM writes	$t = 4$		0%	0.2%	0.4%
	$t = 8$		0%	0.7%	0.2%
L1D hit rate	$t = 4$		0%	0.1%	0%
	$t = 8$		0%	0.1%	0%
L2D hit rate	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
Cycles	$t = 4$		0%	7.2%	7.6%
	$t = 8$		0%	5.4%	5.7%
Exec time	$t = 4$		$2x$	$2.4x$	**$2.5x$**
	$t = 8$		$2.5x$	$3.1x$	**$3.2x$**