

		Serial	Deterministic	Nondeterministic	
				$n = 5$	$n = 10$
Naive MatrixMul (f32, 512×32×512) @ 28 SM's [9.14 blocks/SM]					
DRAM reads	$t = 4$	0	0 (0%)	0 (0%)	0 (0%)
	$t = 8$		0 (0%)	0 (0%)	
DRAM writes	$t = 4$	0	0 (0%)	0 (0%)	0 (0%)
	$t = 8$		0 (0%)	0 (0%)	
L1D hit rate	$t = 4$	96.1%	96.1% (0%)	96.1% (0%)	96.1% (0.1%)
	$t = 8$		96.1% (0%)	96.2% (0.1%)	96.1% (0%)
L2D hit rate	$t = 4$	100%	100% (0%)	100% (0%)	100% (0%)
	$t = 8$		100% (0%)	100% (0%)	100% (0%)
Cycles	$t = 4$	50.2 <i>K</i>	50.2 <i>K</i> (0%)	50.4 <i>K</i> (0.3%)	50.3 <i>K</i> (0.2%)
	$t = 8$		50.2 <i>K</i> (0%)	50.4 <i>K</i> (0.3%)	50.4 <i>K</i> (0.3%)
Exec time	$t = 4$	85.5 <i>s</i>	29.8 <i>s</i> (2.9 <i>x</i>)	27.0 <i>s</i> (3.2 <i>x</i>)	25.9<i>s</i> (3.3<i>x</i>)
	$t = 8$		24.2 <i>s</i> (3.5 <i>x</i>)	21.1 <i>s</i> (4.1 <i>x</i>)	19.6<i>s</i> (4.4<i>x</i>)
Naive MatrixMul (f32, 512×32×512) @ 112 SM's [2.29 blocks/SM]					
DRAM reads	$t = 4$	0	0 (0%)	0 (0%)	0 (0%)
	$t = 8$		0 (0%)	0 (0%)	0 (0%)
DRAM writes	$t = 4$	0	0 (0%)	0 (0%)	0 (0%)
	$t = 8$		0 (0%)	0 (0%)	0 (0%)
L1D hit rate	$t = 4$	96.8%	96.8% (0%)	96.7% (0%)	96.7% (0%)
	$t = 8$		96.8% (0%)	96.7% (0.1%)	96.7% (0%)
L2D hit rate	$t = 4$	100%	100% (0%)	100% (0%)	100% (0%)
	$t = 8$		100% (0%)	100% (0%)	100% (0%)
Cycles	$t = 4$	20.2 <i>K</i>	20.2 <i>K</i> (0%)	20.2 <i>K</i> (0.2%)	20.2 <i>K</i> (0.3%)
	$t = 8$		20.2 <i>K</i> (0%)	20.2 <i>K</i> (0.3%)	20.2 <i>K</i> (0.3%)
Exec time	$t = 4$	122.4 <i>s</i>	40.9 <i>s</i> (3 <i>x</i>)	37.7 <i>s</i> (3.2 <i>x</i>)	37.3<i>s</i> (3.3<i>x</i>)
	$t = 8$		29.2 <i>s</i> (4.2 <i>x</i>)	25.9 <i>s</i> (4.7 <i>x</i>)	25.1<i>s</i> (4.9<i>x</i>)
Average Naive Matrixmul (29 configurations) @ 28 SM's					
DRAM reads	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
DRAM writes	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
L1D hit rate	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
L2D hit rate	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
Cycles	$t = 4$		0%	0.5%	0.5%
	$t = 8$		0%	0.5%	0.6%
Exec time	$t = 4$		1.6 <i>x</i>	1.9 <i>x</i>	2<i>x</i>
	$t = 8$		1.5 <i>x</i>	1.8 <i>x</i>	1.9<i>x</i>
Average Naive Matrixmul (29 configurations) @ 112 SM's					
DRAM reads	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
DRAM writes	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
L1D hit rate	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
L2D hit rate	$t = 4$		0%	0%	0%
	$t = 8$		0%	0%	0%
Cycles	$t = 4$		0%	0.5%	0.5%
	$t = 8$		0%	0.5%	0.5%
Exec time	$t = 4$		1.3 <i>x</i>	2.2 <i>x</i>	2.4<i>x</i>
	$t = 8$		1.3 <i>x</i>	2.2 <i>x</i>	2.4<i>x</i>