| | | Deterministic | Nondeterministic | |
|--|-------|---------------|------------------|--------|
| | | | n = 5 | n = 10 |
| Average (55 benchmark configurations) @ 28 SM's | | | | |
| DRAM reads | t = 4 | 0% | 0% | 0% |
| | t = 8 | 0% | 0% | 0% |
| DRAM writes | t = 4 | 0% | 0% | 0% |
| | t = 8 | 0% | 0% | 0% |
| L1D hit rate | t = 4 | 0% | 0% | 0% |
| | t = 8 | 0% | 0% | 0% |
| L2D hit rate | t = 4 | 0% | 0% | 0% |
| | t = 8 | 0% | 0% | 0% |
| Cycles | t = 4 | 0% | 0.4% | 0.4% |
| | t = 8 | 0% | 0.4% | 0.4% |
| Exec time | t = 4 | 1.7x | 2x | 2x |
| | t = 8 | 1.7x | 2.1x | 2.2x |
| Average (55 benchmark configurations) @ 112 SM's | | | | |
| DRAM reads | t = 4 | 0% | 0% | 0% |
| | t = 8 | 0% | 0% | 0% |
| DRAM writes | t = 4 | 0% | 0% | 0% |
| | t = 8 | 0% | 0.1% | 0% |
| L1D hit rate | t = 4 | 0% | 0% | 0% |
| | t = 8 | 0% | 0% | 0% |
| L2D hit rate | t = 4 | 0% | 0% | 0% |
| | t = 8 | 0% | 0% | 0% |
| Cycles | t = 4 | 0% | 3.4% | 3.4% |
| | t = 8 | 0% | 3.2% | 3.2% |
| Exec | t = 4 | 1.6x | 2.2x | 2.3x |
| time | t = 8 | 1.9x | 2.5x | 2.6x |