

A**B****C****D****E****F**

NOTE:

One LpGBT: 28 data pairs @ 320Mbps

10.24Gbps&FEC5 EDIN[6:0][3:0]. 8 CHs ADC

--> CSM use 18 of 28 links per chip

One GBT-SCA: 31 ADC INPUT CHs, 31 used by FE Monitoring

32th for embedded temp sensor

--> FE use 18*6=108 of 109(31*3+8*2)

1 CHs for CSM 2V5 voltage

LpGBT0 Group 6 Elink 3&2

MEZZ 0

LpGBT0 Group 6 Elink 1&0

MEZZ 2

LpGBT0 Group 4 Elink 3&2

MEZZ 4

Summary:

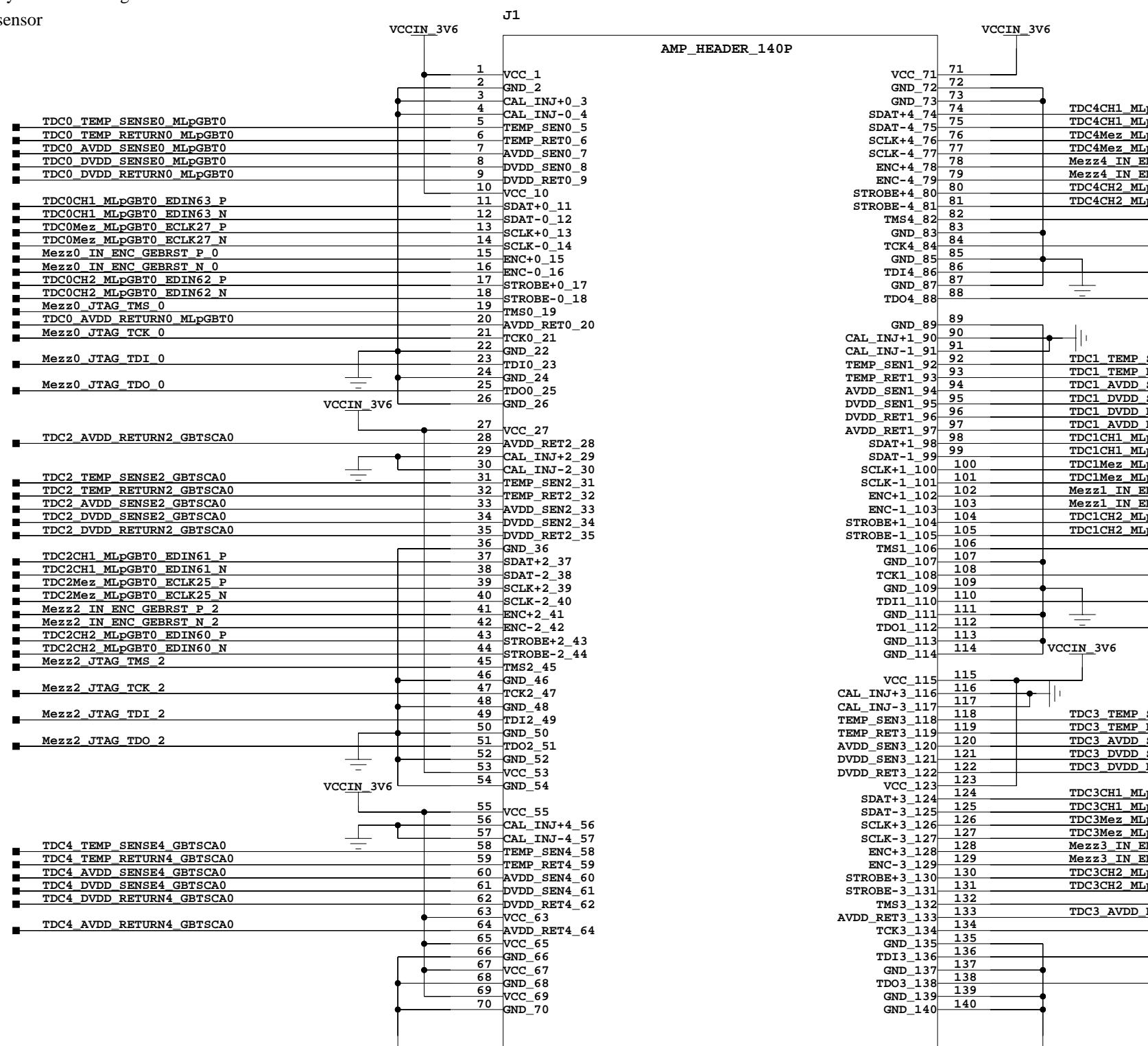
CN0 140pin AMP connector handle 5 TDC Mezzs: TDC0-TDC4

TDC Mezz 0-4 Data handled by master LpGBT0

One TDC Mezz: 6 SENSE, 2 DATA PAIRS, 1 Mezz CLK, 1 CAL_INJ, 1 EN_RESET, 4 JTAG Signals

To LpGBT Chip 0

CN0



AMP-5179031-6

LpGBT0: MEZZ 0-9

LpGBT1: MEZZ 10-17

LpGBT0 Group 4 Elink 3&2

MEZZ 4 Cont'

LpGBT0 Group 4 Elink 1&0

MEZZ 1

LpGBT0 Group 3 Elink 3&2

MEZZ 3

TE/AMP 5179031-6 140PIN CONN.

COMPANY
University of Michigan

TITLE
LpGBT_CSM Prototype v2

SIZE	B	REV	SHEET	1	OF	N
DRAWN	XUEYE HU		DATE	31/05/2020:18:36		

**A****B****C****D****E****F**

A**B****C****D****E****F**

NOTE:

One LpGBT: 28 data pairs @ 320Mbps

10.24Gbps&FEC5 EDIN[6:0][3:0]. 8 CHs ADC

--> CSM use 18 of 28 links per chip

One GBT-SCA: 31 ADC INPUT CHs, 31 used by FE Monitoring
32th for embedded temp sensor

--> FE use 18*6=108 of 109(31*3+8*2)

1 CHs for CSM 2V5 voltage

To LpGBT Chip 0

LpGBT0: MEZZ 0-9

LpGBT1: MEZZ 10-17

LpGBT0 Group 0 Elink 0&1

MEZZ 6

LpGBT0 Group 0 Elink 2&3

MEZZ 8

LpGBT0 Group 2 Elink 0&1

MEZZ 9

Summary:

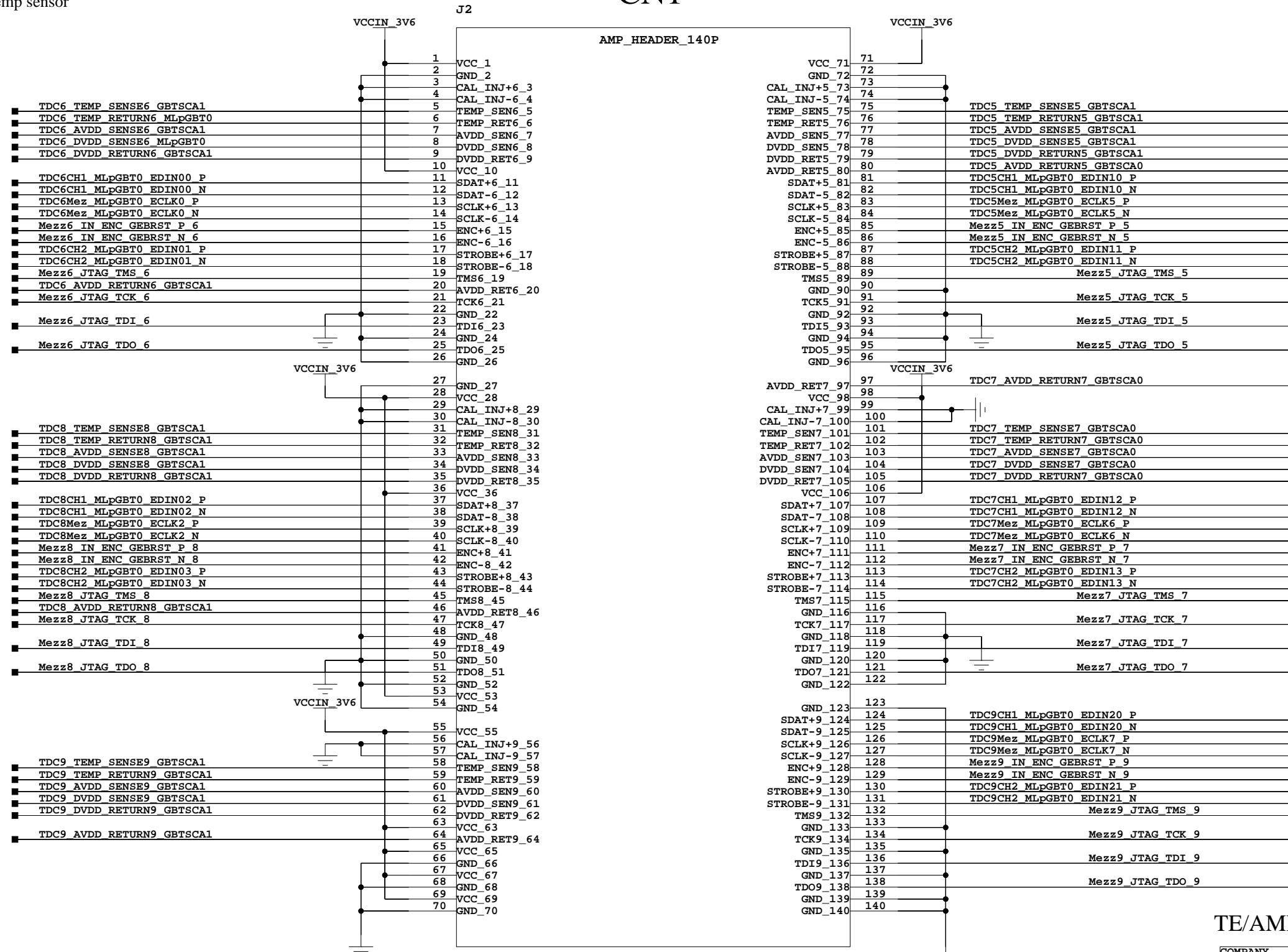
CN1 140pin AMP connector handle 5 TDC Mezzs: TDC5-TDC9

TDC Mezz 5-8 Data handled by master LpGBT0

TDC Mezz 9 Data handled by slave LpGBT1

One TDC Mezz: 6 SENSE, 2 DATA PAIRS, 1 Mezz CLK, 1 CAL_INJ, 1 EN_RESET, 4 JTAG Signals

CN1



AMP-5179031-6

TE/AMP 5179031-6 140PIN CONN.

COMPANY
University of Michigan

TITLE
LpGBT_CSM Prototype v2

SIZE B REV SHEET 2 OF N
DRAWN XUEYE HU DATE 30/05/2020:23:15



LpGBT0 Group 1 Elink 0&1

MEZZ 5

LpGBT0 Group 1 Elink 2&3

MEZZ 7

LpGBT0 Group 2 Elink 0&1

MEZZ 9 Cont'

A B C D E F

NOTE:

One LpGBT: 28 data pairs @ 320Mbps

10.24Gbps&FEC5 EDIN[6:0][3:0]. 8 CHs ADC

-> CSM use 18 of 28 links per chip

One GBT-SCA: 31 ADC INPUT CHs, 31 used by FE Monitoring

32th for embedded temp sensor

-> FE use 18*6=108 of 109(31*3+8*2)

1 CHs for CSM 2V5 voltage

LpGBT1 Group 6 Elink 3&2**MEZZ 10****LpGBT1 Group 6 Elink 1&0****MEZZ 12**

* Source RESET For All Mezz. -->

Was named as RESET_AMT_A7_SERVING

LpGBT1 Group 4 Elink 3&2**MEZZ 14****Summary:**

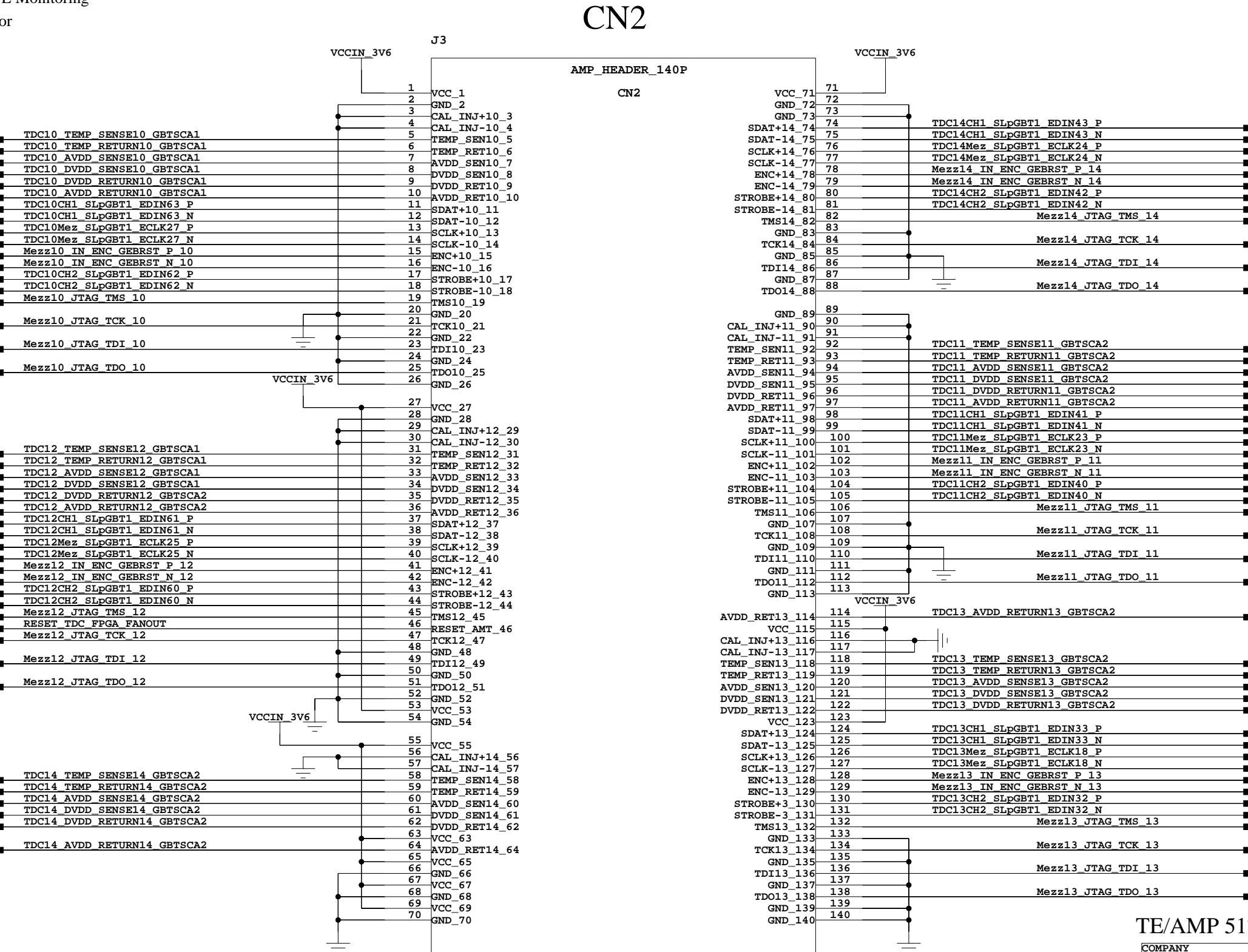
CN2 140pin AMP connector handle 5 TDC Mezzs: TDC10-TDC14

TDC Mezz 10-14 Data handled by slave LpGBT1

One TDC Mezz: 6 SENSE, 2 DATA PAIRS, 1 Mezz CLK, 1 CAL_INJ, 1 EN_RESET, 4 JTAG Signals

To LpGBT Chip 1**LpGBT0: MEZZ 0-9****LpGBT1: MEZZ 10-17****LpGBT1 Group 4 Elink 3&2****MEZZ 14 Cont'****LpGBT1 Group 4 Elink 1&0****MEZZ 11****LpGBT1 Group 3 Elink 3&2****MEZZ 13**

TE/AMP 5179031-6 140PIN CONN.

COMPANY
University of MichiganTITLE
LpGBT_CSM Prototype v2SIZE B REV SHEET 3 OF N
DRAWN XUEYE HU DATE 01/06/2020:18:34

A**B****C****D****E****F**

NOTE:

One LpGBT: 28 data pairs @ 320Mbps

10.24Gbps&FEC5 EDIN[6:0][3:0]. 8 CHs ADC

-> CSM use 18 of 28 links per chip

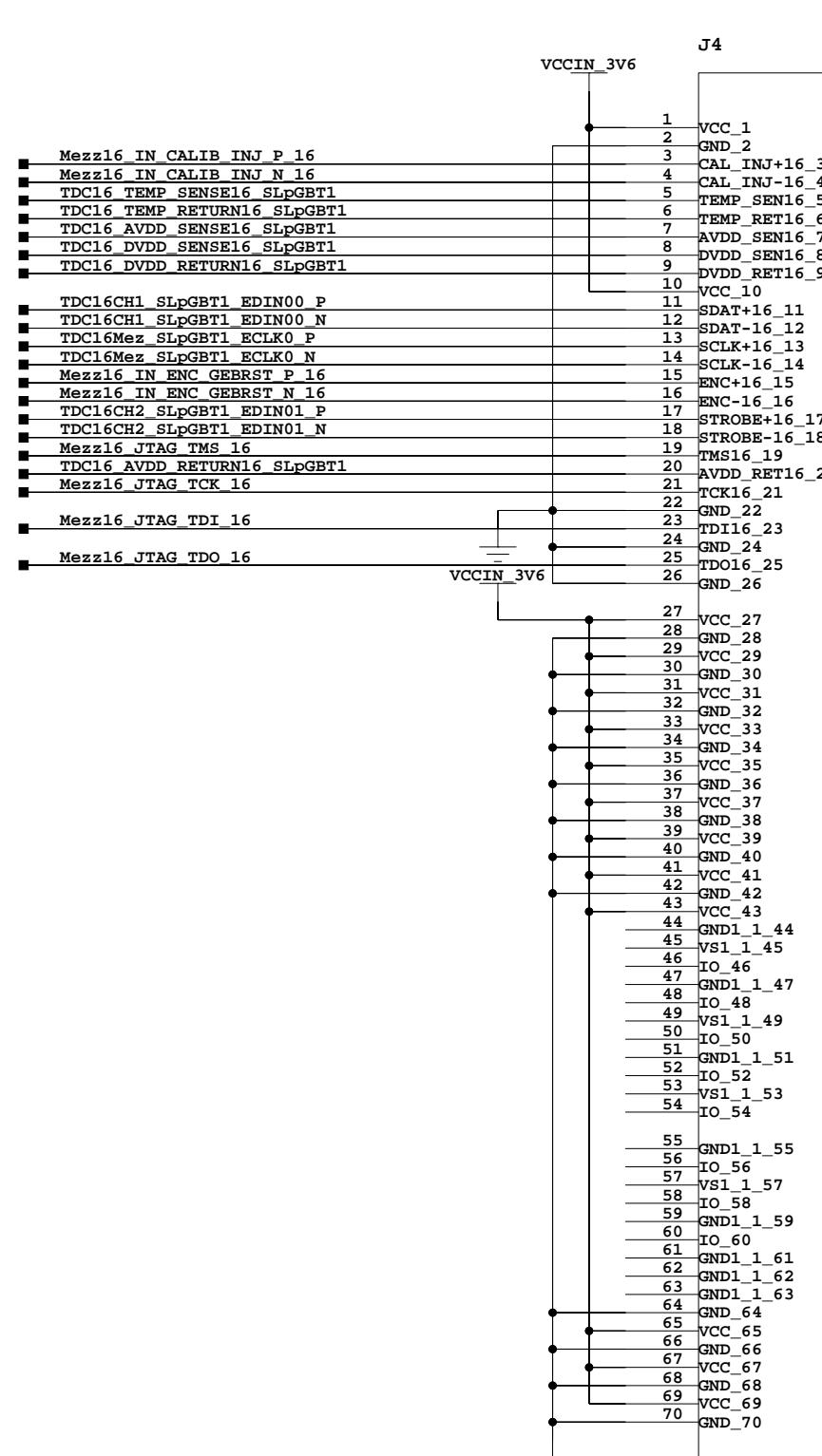
One GBT-SCA: 31 ADC INPUT CHs, 31 used by FE Monitoring

--> FE use 18*6=108 of 109(31*3+8*2)

1 CHs for CSM 2V5 voltage

LpGBT1 Group 0 Elink 0&1

MEZZ 16



Summary:

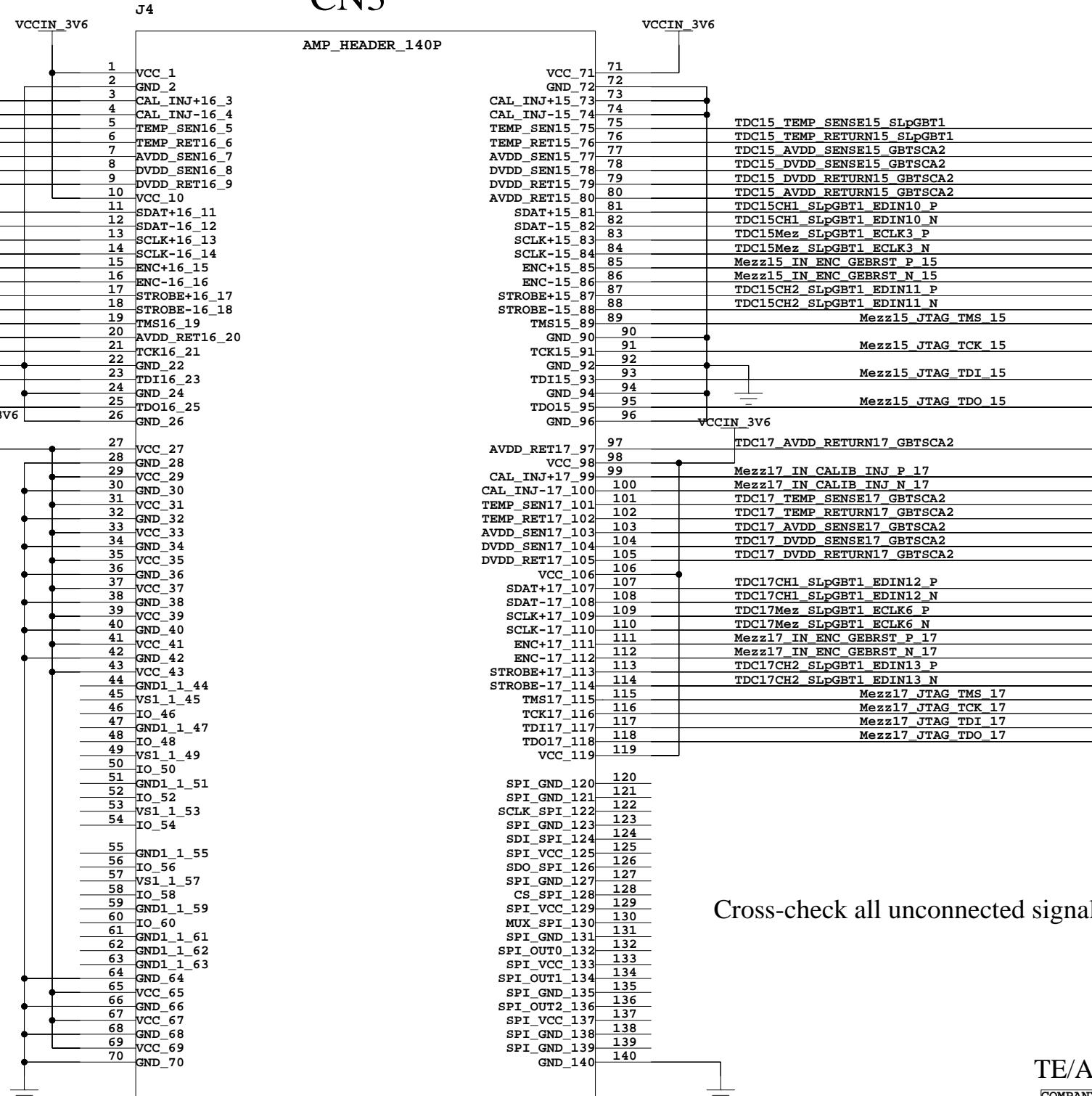
CN2 140pin AMP connector handle 5 TDC Mezzs: TDC15-TDC17

TDC Mezz 15-17 Data handled by slave LpGBT1

One TDC Mezz: 6 SENSE, 2 DATA PAIRS, 1 Mezz CLK, 1 CAL_INJ, 1 EN_RESET, 4 JTAG Signals

To LpGBT Chip 1

CN3



AMP-5179031-6

Cross-check all unconnected signals!!

TE/AMP 5179031-6 140PIN CONN.

COMPANY
University of Michigan



TITLE
LpGBT_CSM Prototype v2

SIZE B REV SHEET 4 OF N
DRAWN XUEYE HU DATE 31/05/2020:22:35

LpGBT0: MEZZ 0-9

LpGBT1: MEZZ 10-17

LpGBT1 Group 1 Elink 0&1

MEZZ 15

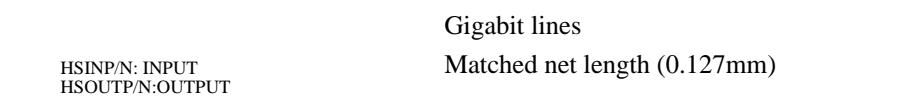
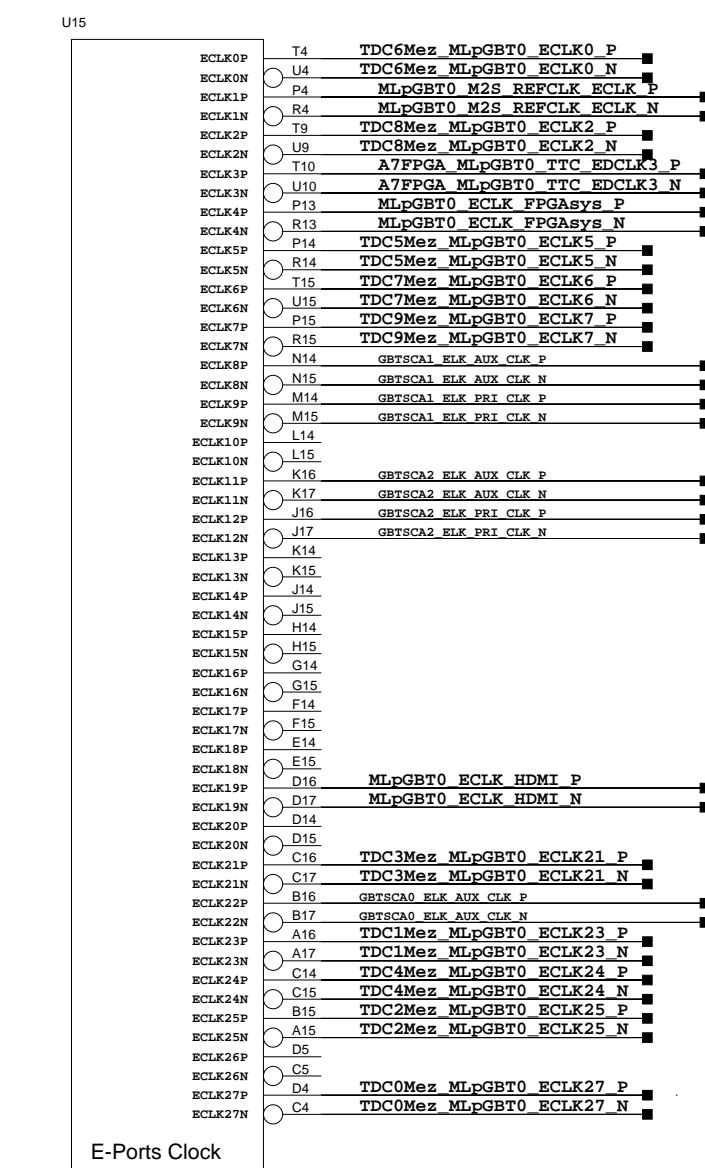
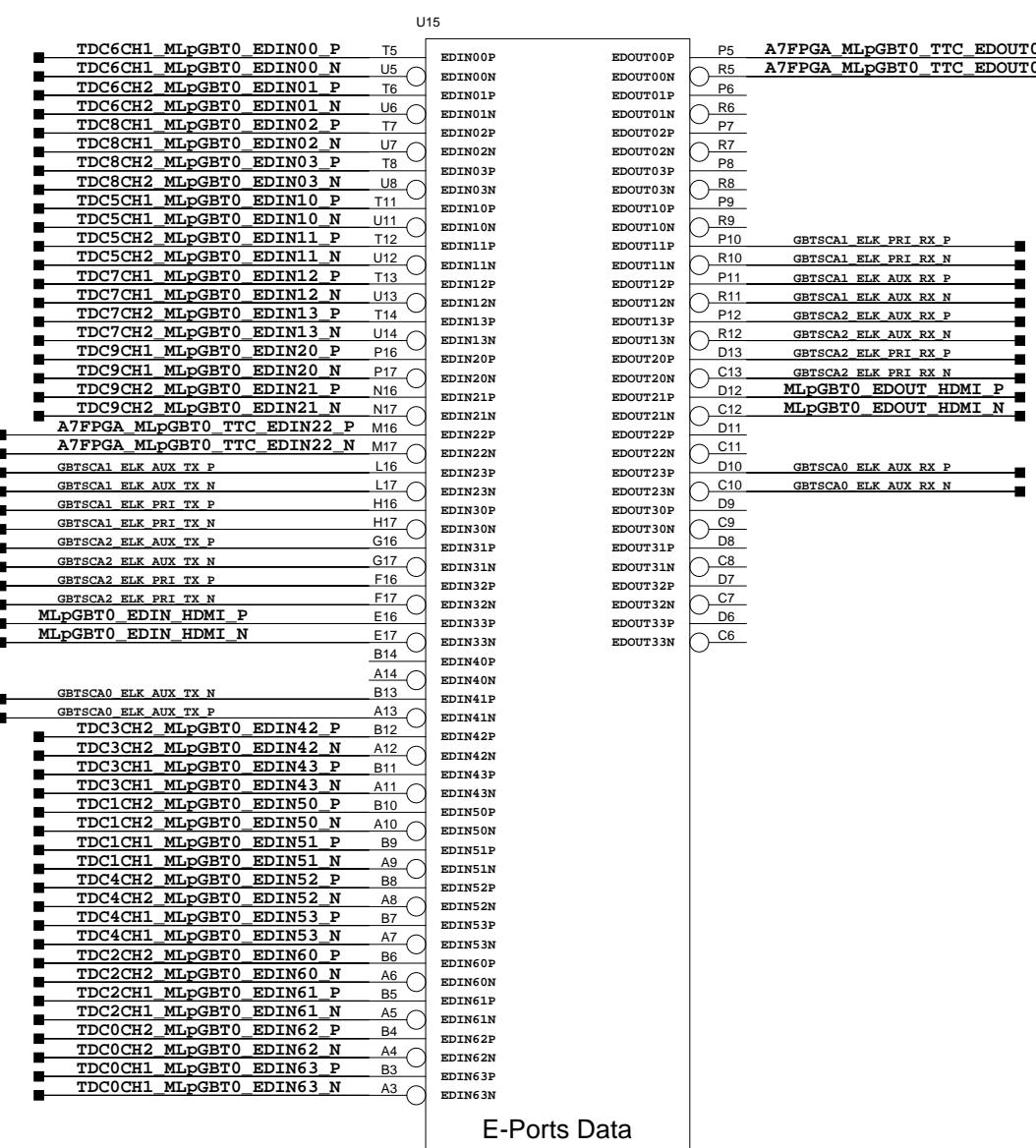
LpGBT1 Group 1 Elink 2&3

MEZZ 17

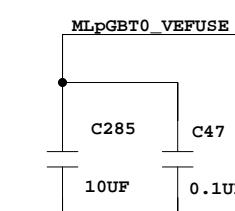
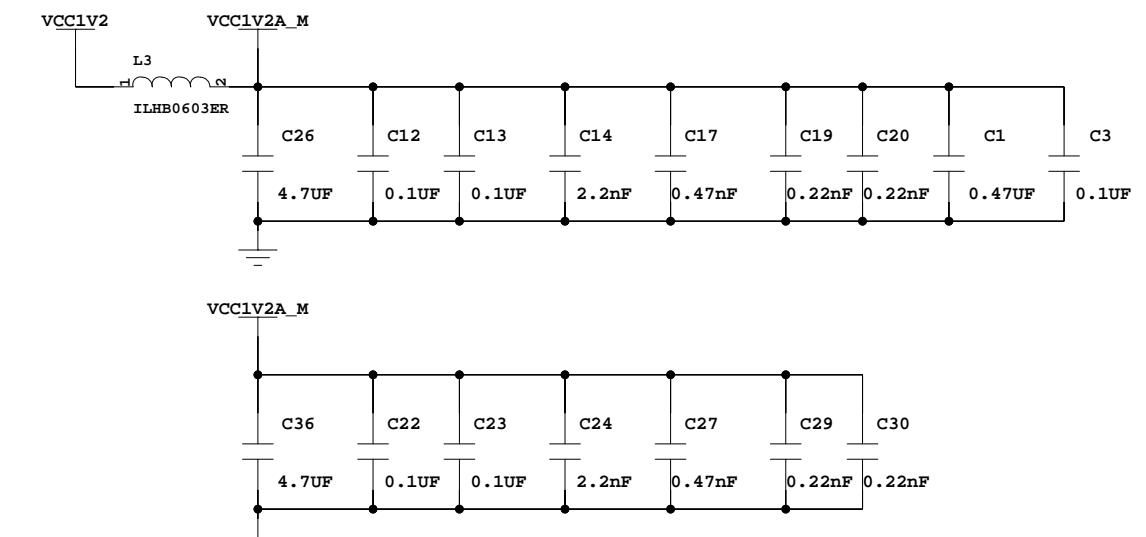
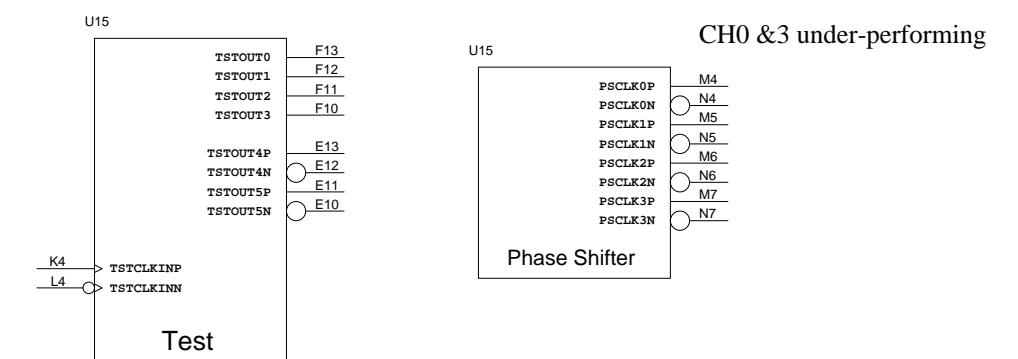
A B C D E F

Master LpGBT0

Transceiver mode



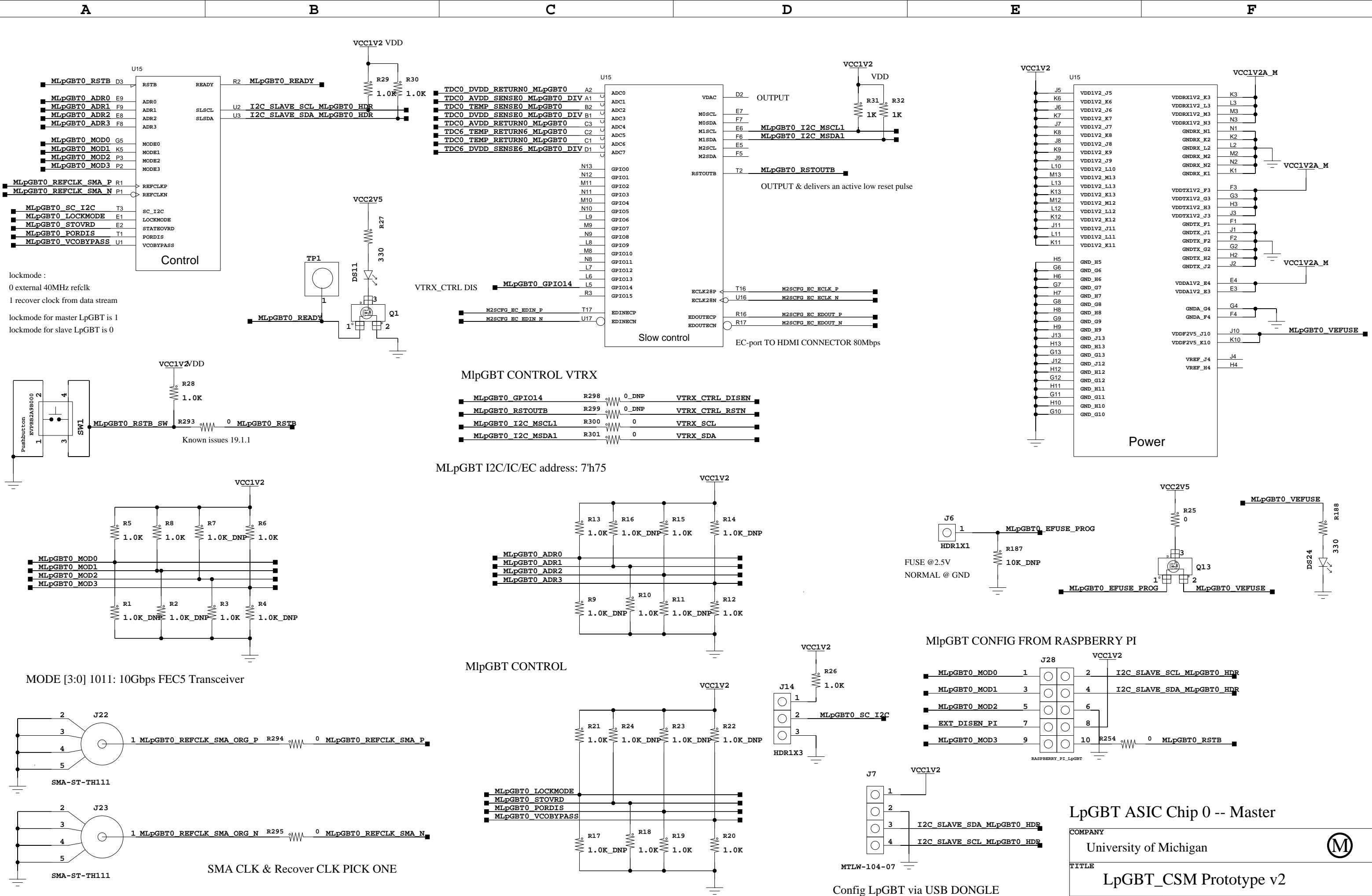
AC coupling with Laser Driver



LpGBT ASIC Chip 0 -- Master

COMPANY
University of MichiganTITLE
LpGBT_CSM Prototype v2SIZE B REV SHEET 5 OF N
DRAWN XUEYE HU DATE 04/06/2020:16:55

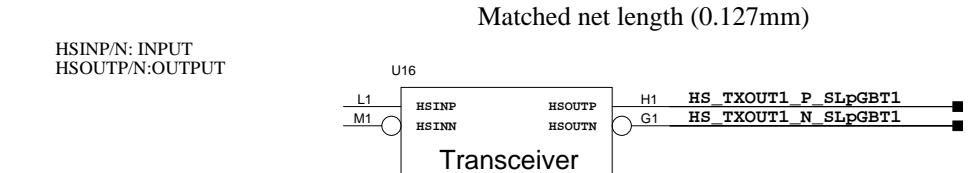
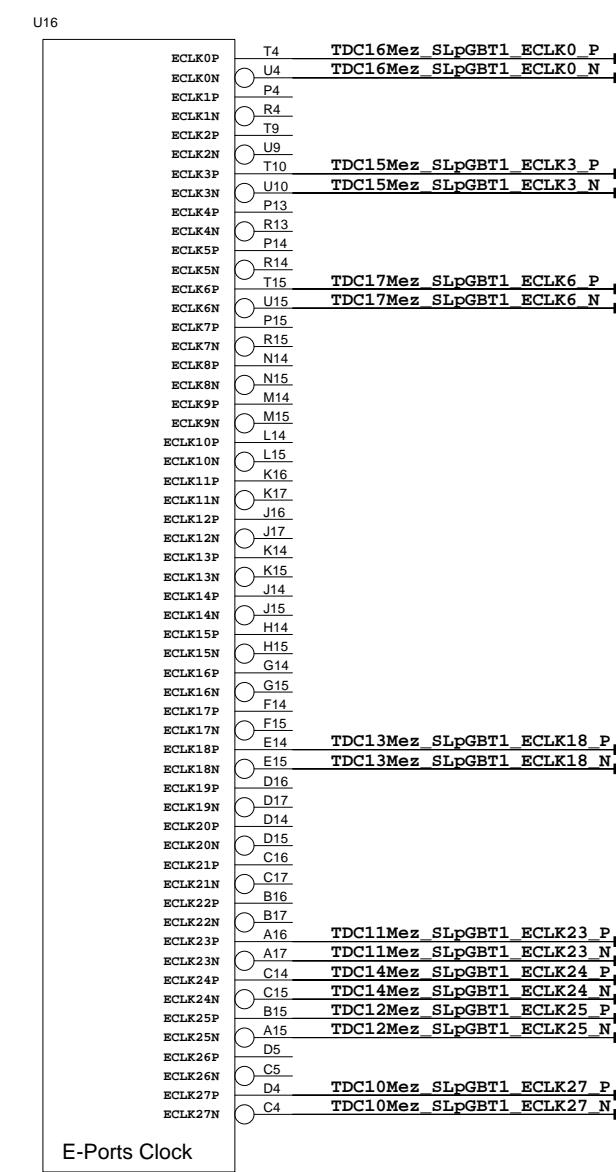
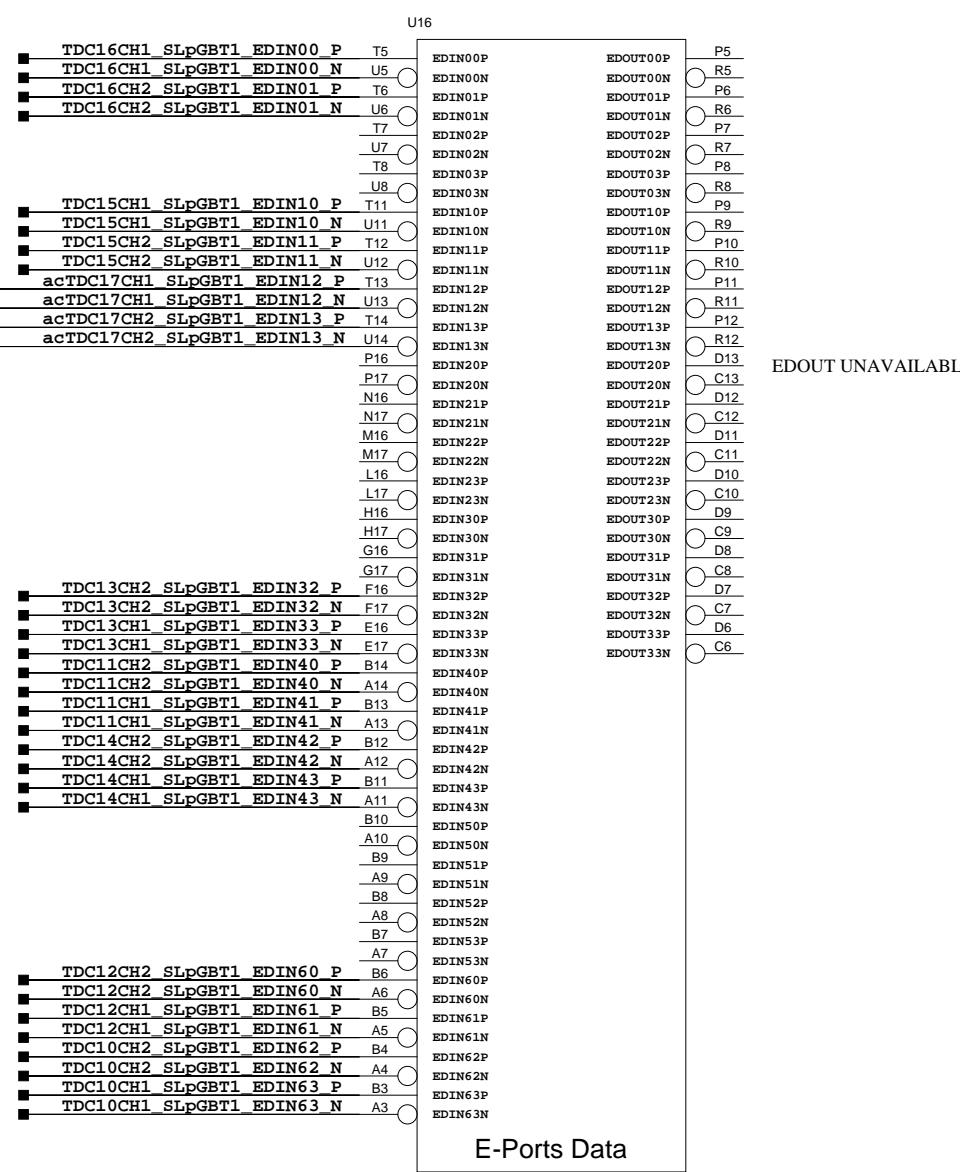
A B C D E F



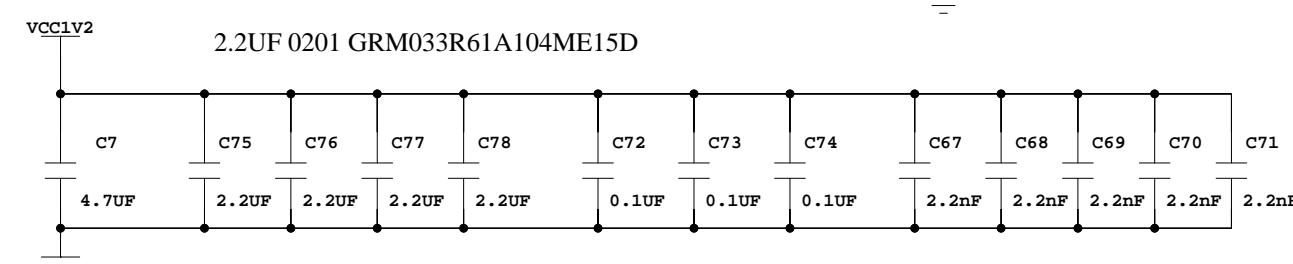
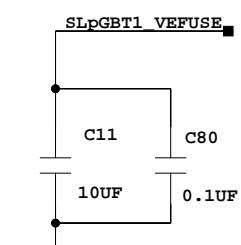
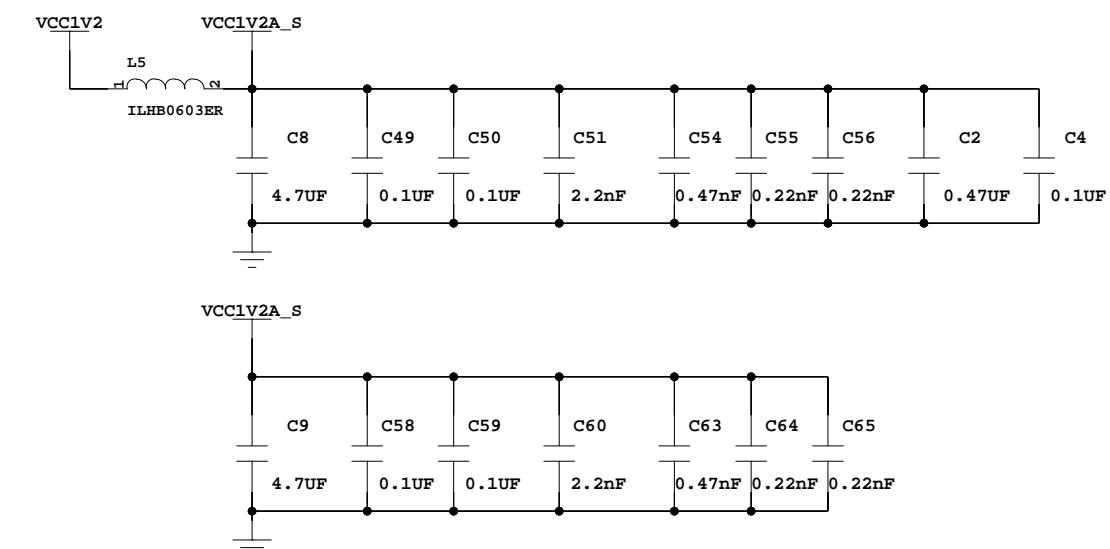
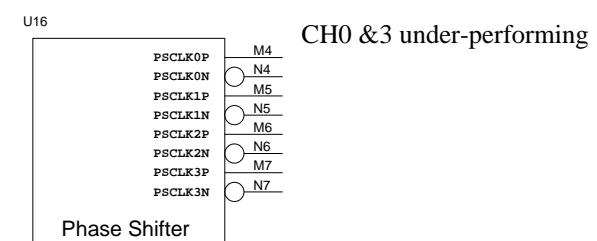
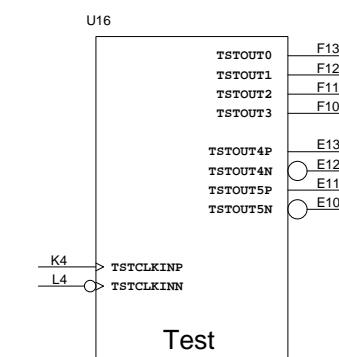
A **B** **C** **D** **E** **F**

Slave LpGBT1

Simplex TX mode



AC coupling with Laser Driver



LpGBT ASIC Chip 1 -- Slave

COMPANY

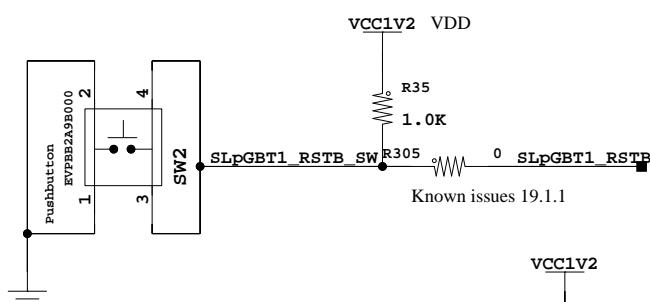
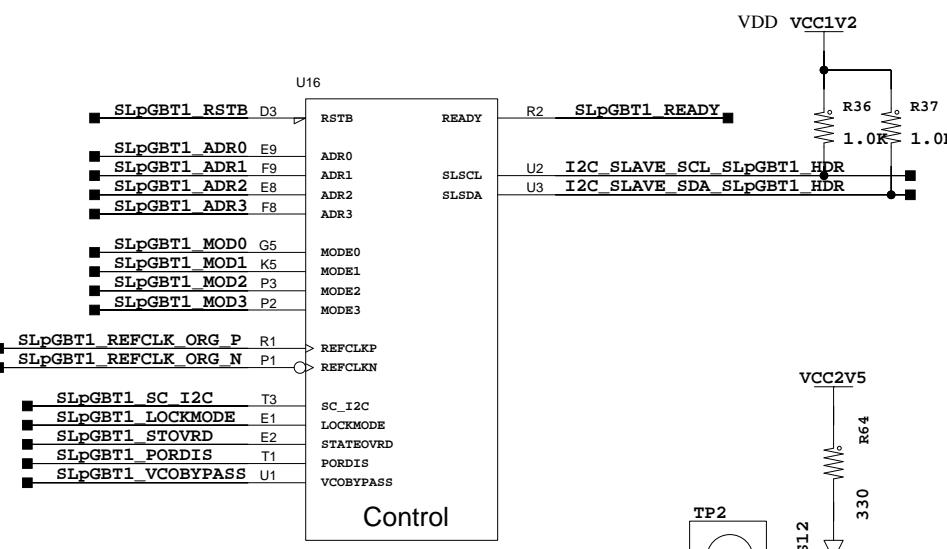
University of Michigan



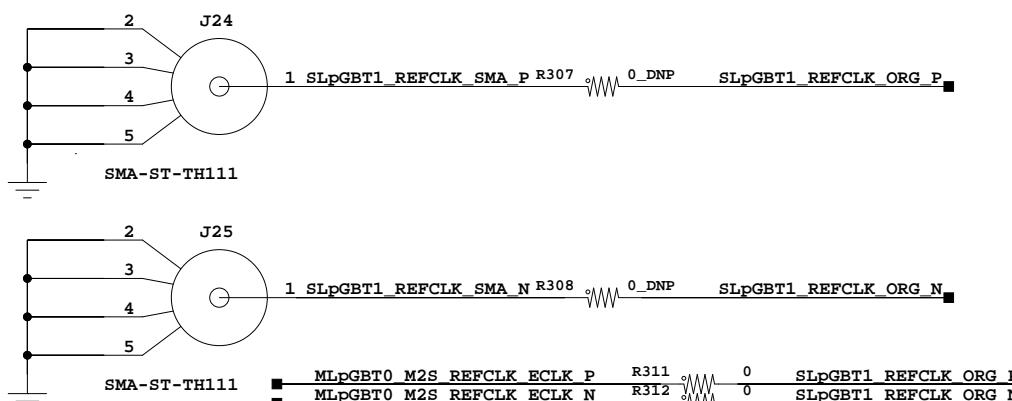
TITLE

LpGBT_CSM Prototype v2

SIZE B REV SHEET 7 OF N
DRAWN XUEYE HU DATE 04/06/2020:16:56**A** **B** **C** **D** **E** **F**

A**B****C****D****E****F**

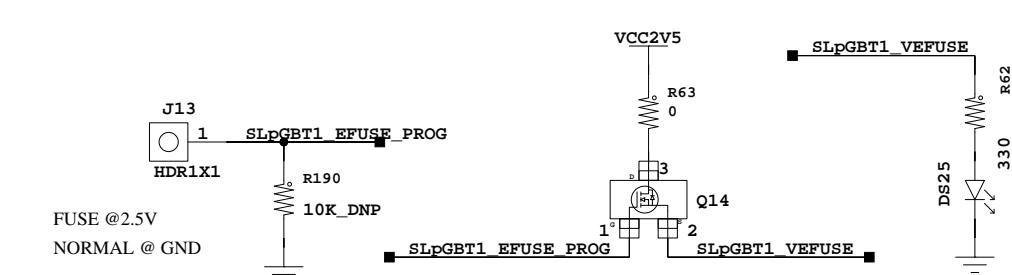
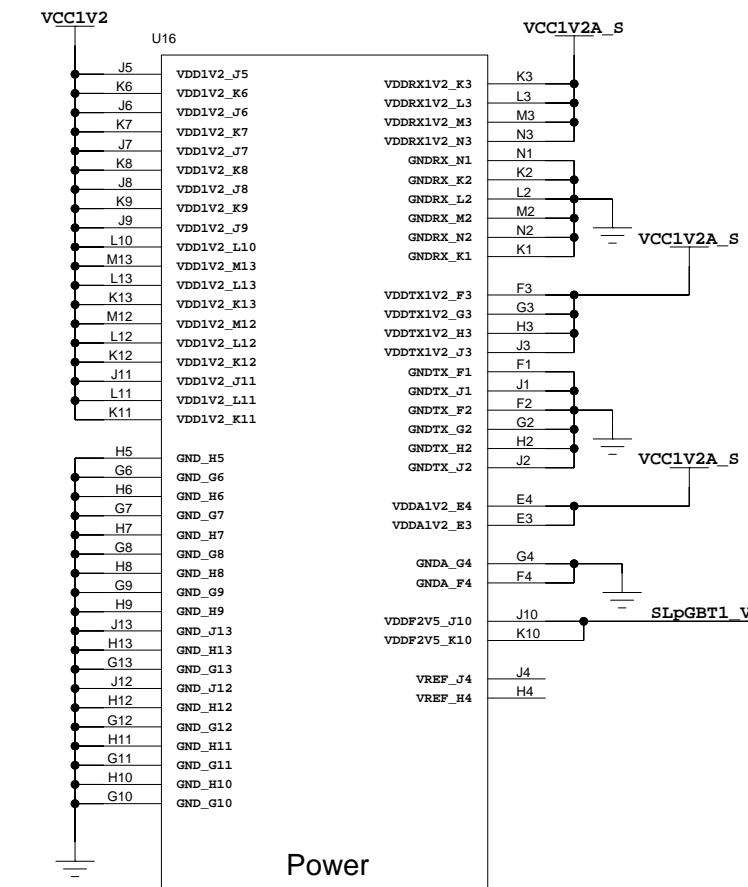
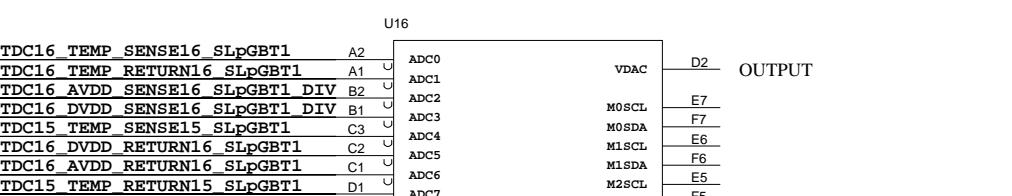
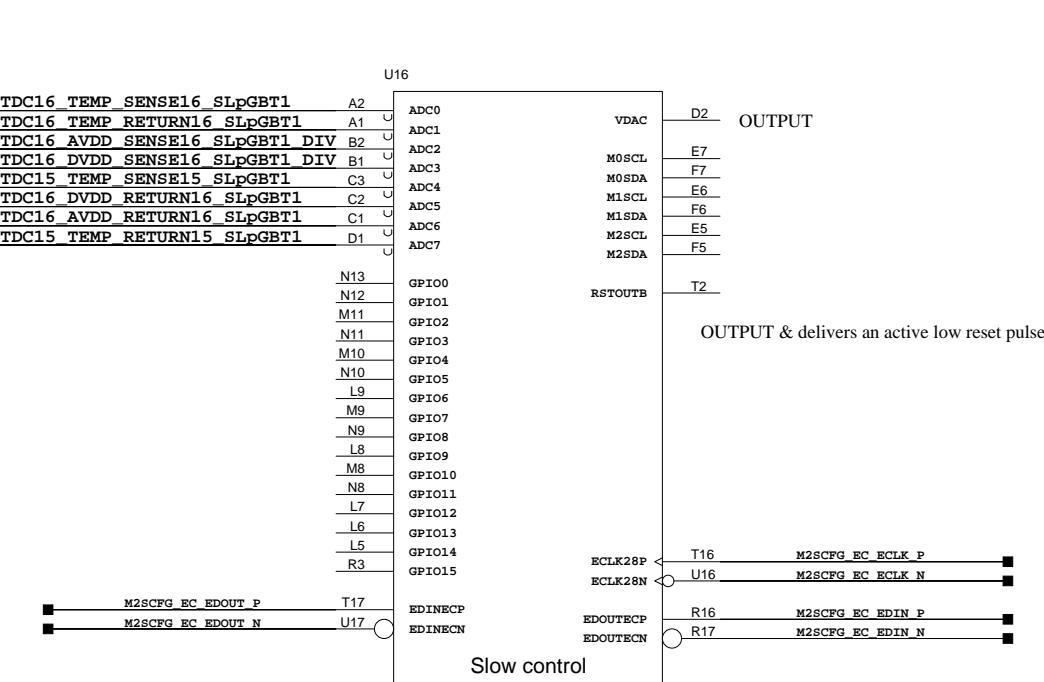
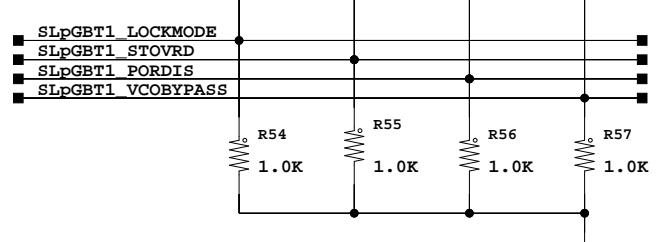
MODE [3:0] 1001: 10Gbps FEC5 SimpleTx



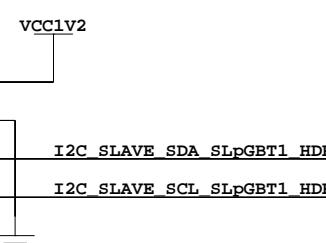
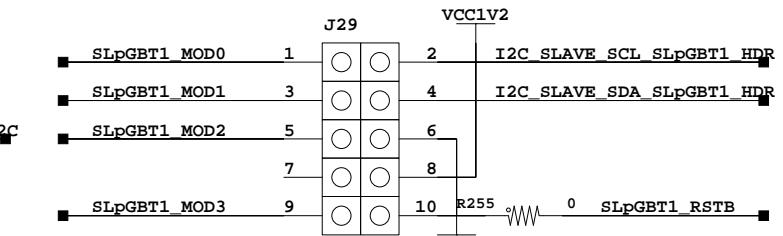
SLpGBT I2C/IC/EC address: 7'h73

*Quick Start:
PORDIS: GND
SC_I2C: GND
ADR3: GND
ADR2: GND
ADR1: GND
ADR0: GND
VCOPYPASS: GND
STATEOVRD: GND

SlpGBT CONTROL



SlpGBT CONFIG FROM RASPBERRY PI



Config LpGBT via USB DONGLE

LpGBT ASIC Chip 1 -- Slave

COMPANY

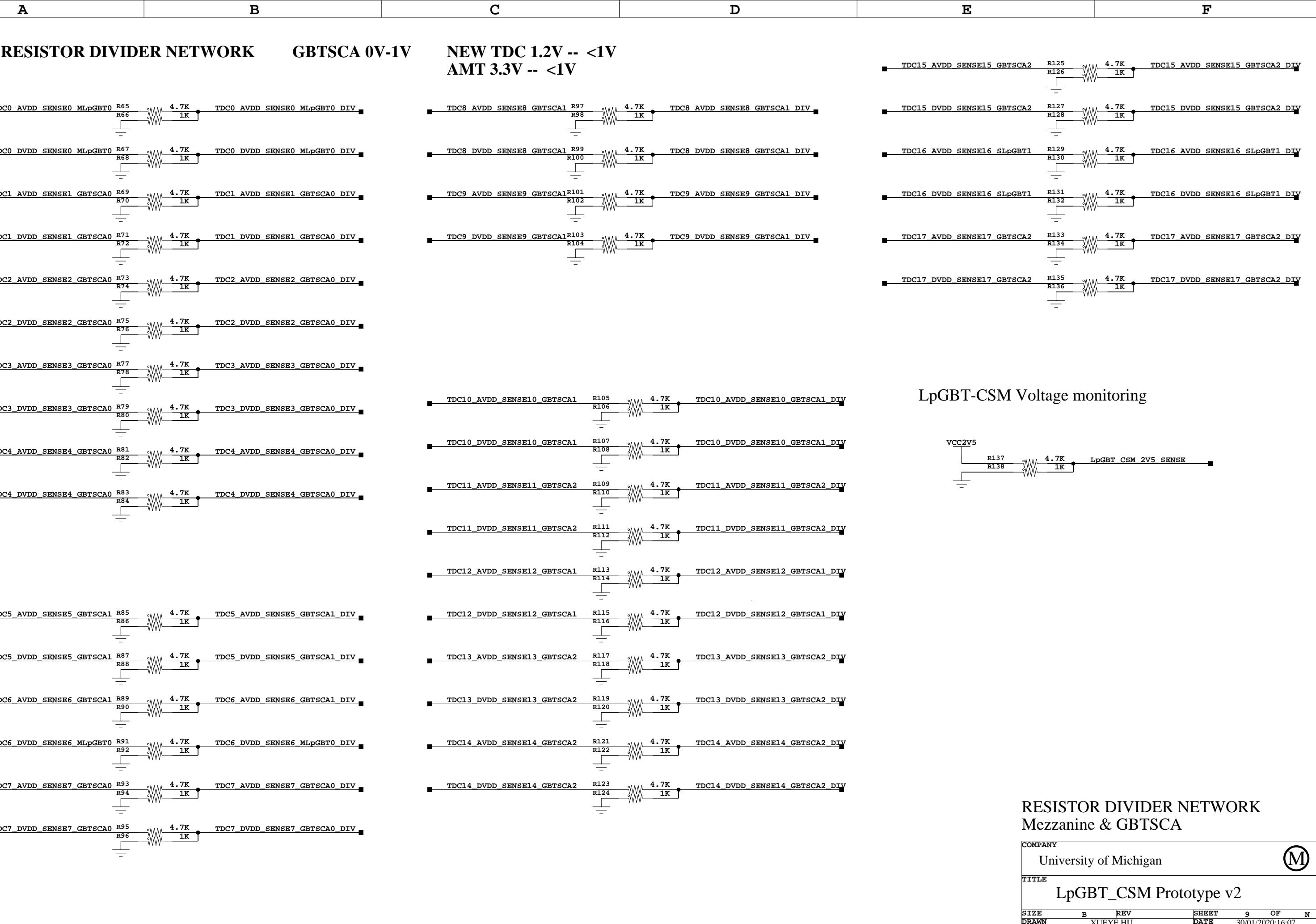
University of Michigan



LpGBT_CSM Prototype v2

SIZE	B	REV	SHEET	8	OF	N
DRAWN	XUEYE HU		DATE	06/06/2020:21:36		

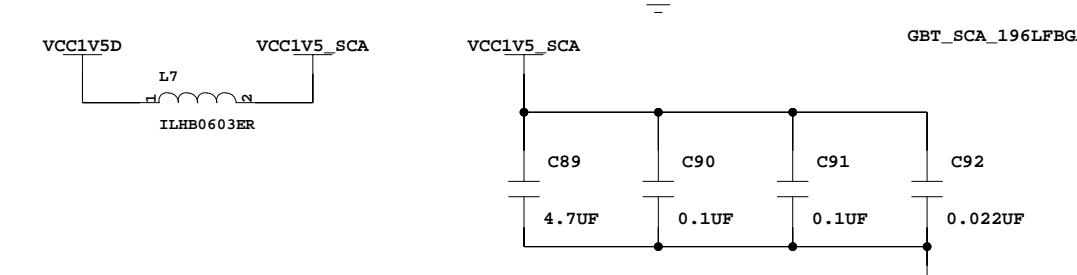
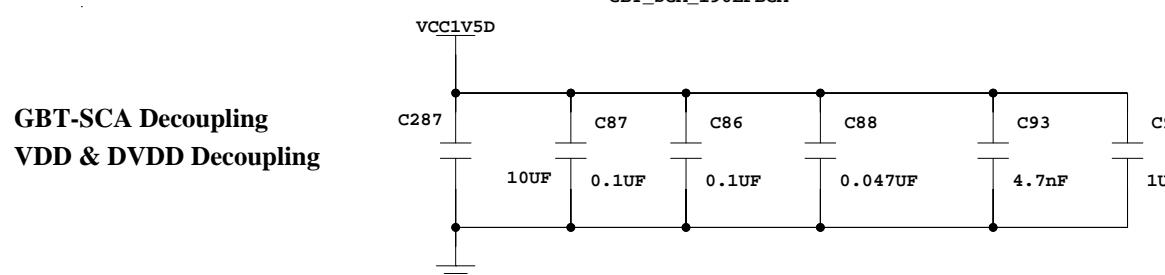
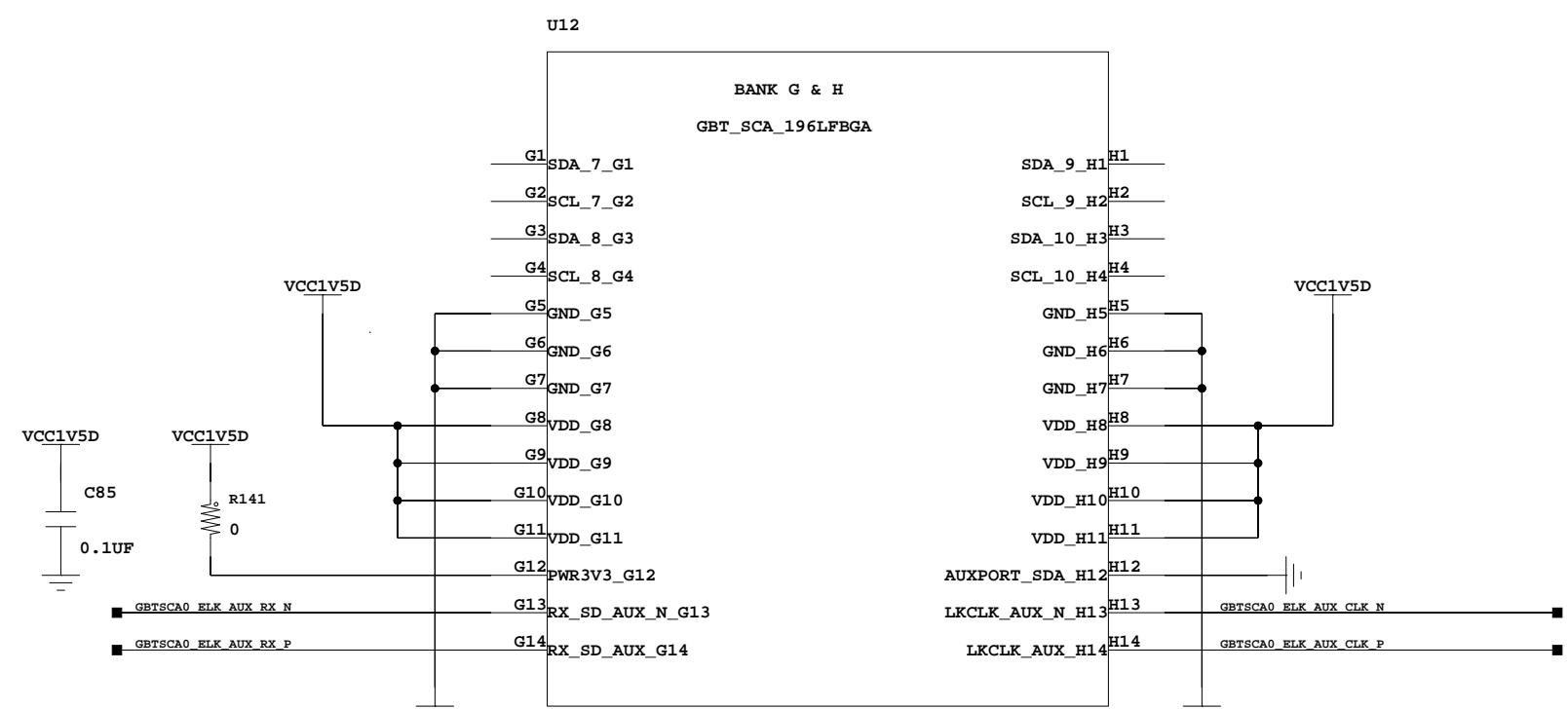
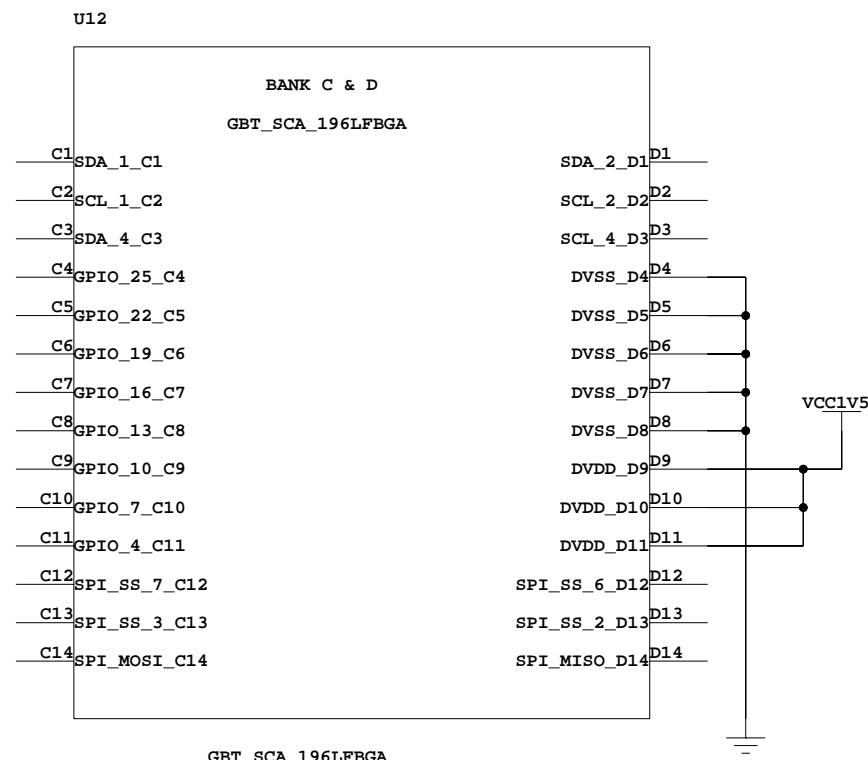
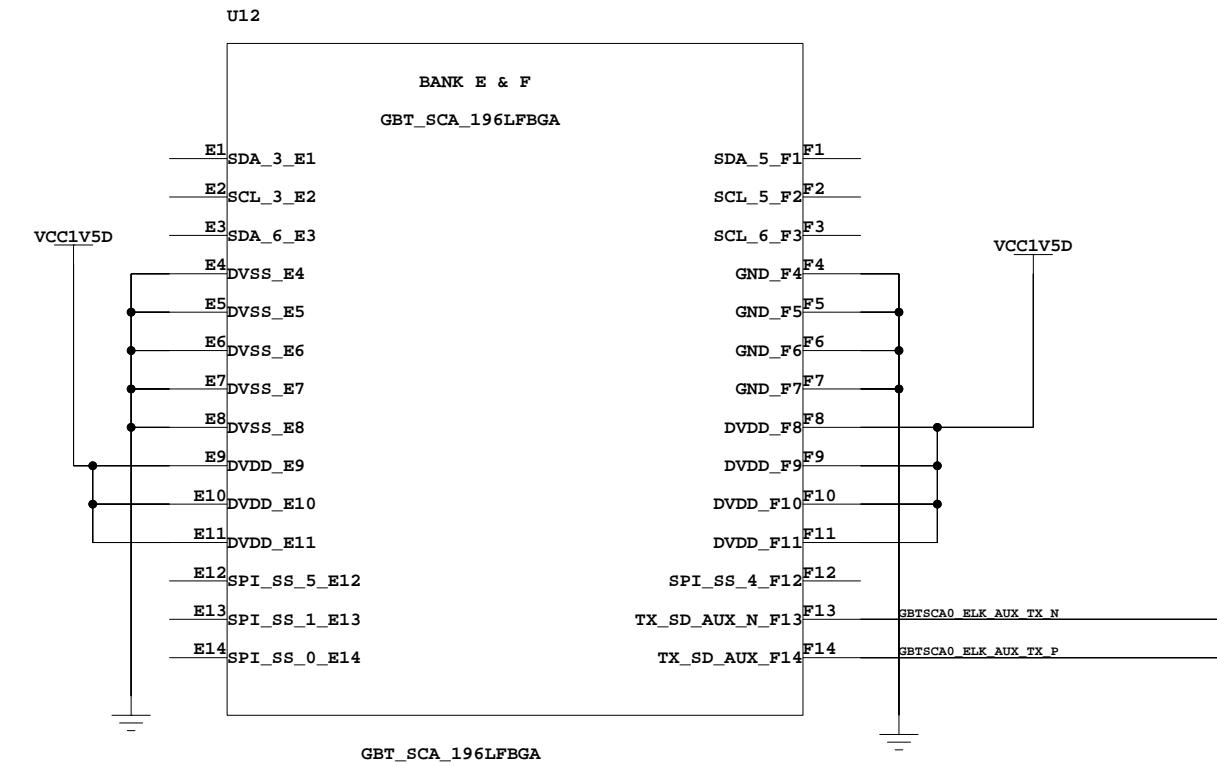
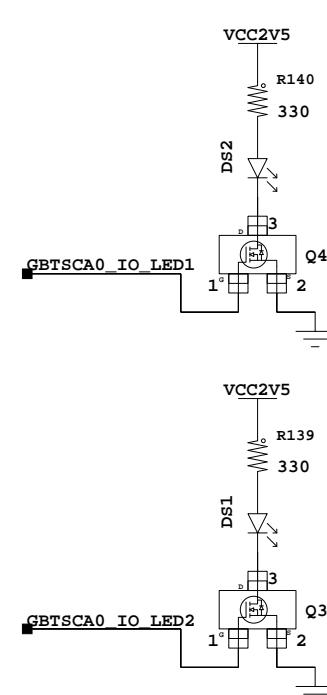
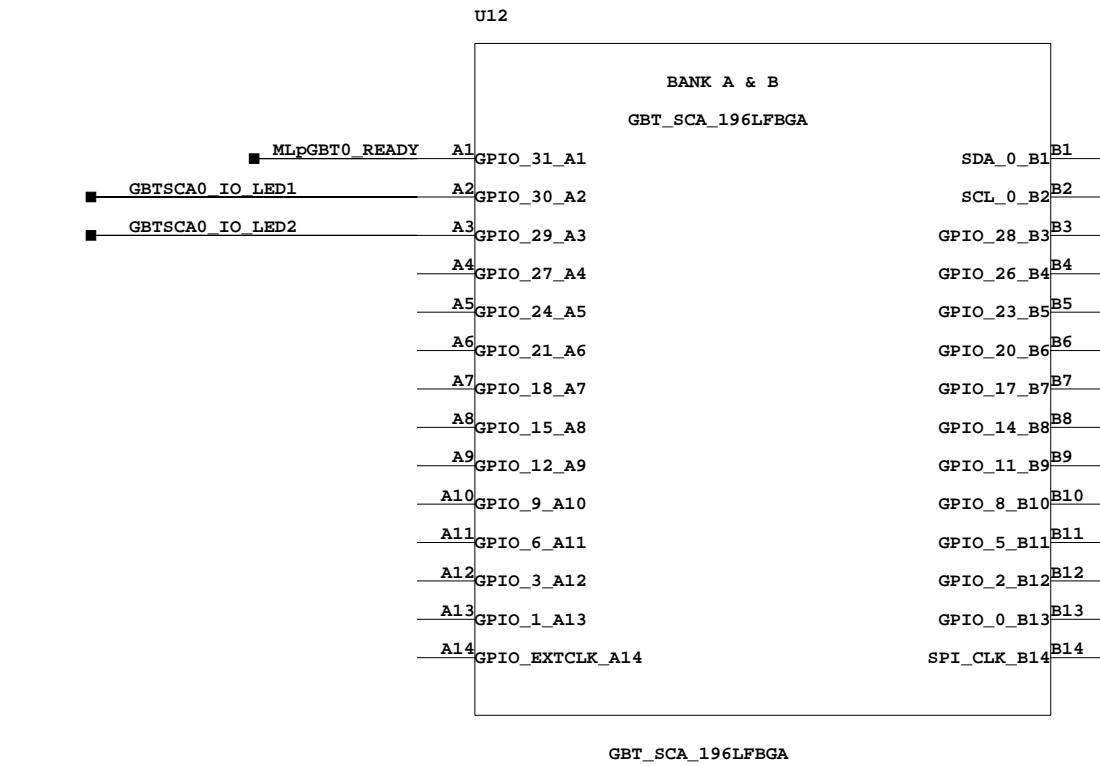
A**B****C****D****E****F**



Note: AGND=GND; DVSS=GND; DVDD=1V5D; AVDD=1V5_SCA; VDD=1V5D

GBT-SCA IO PAD: 0-DVDD

GBT-SCA BANK A-H

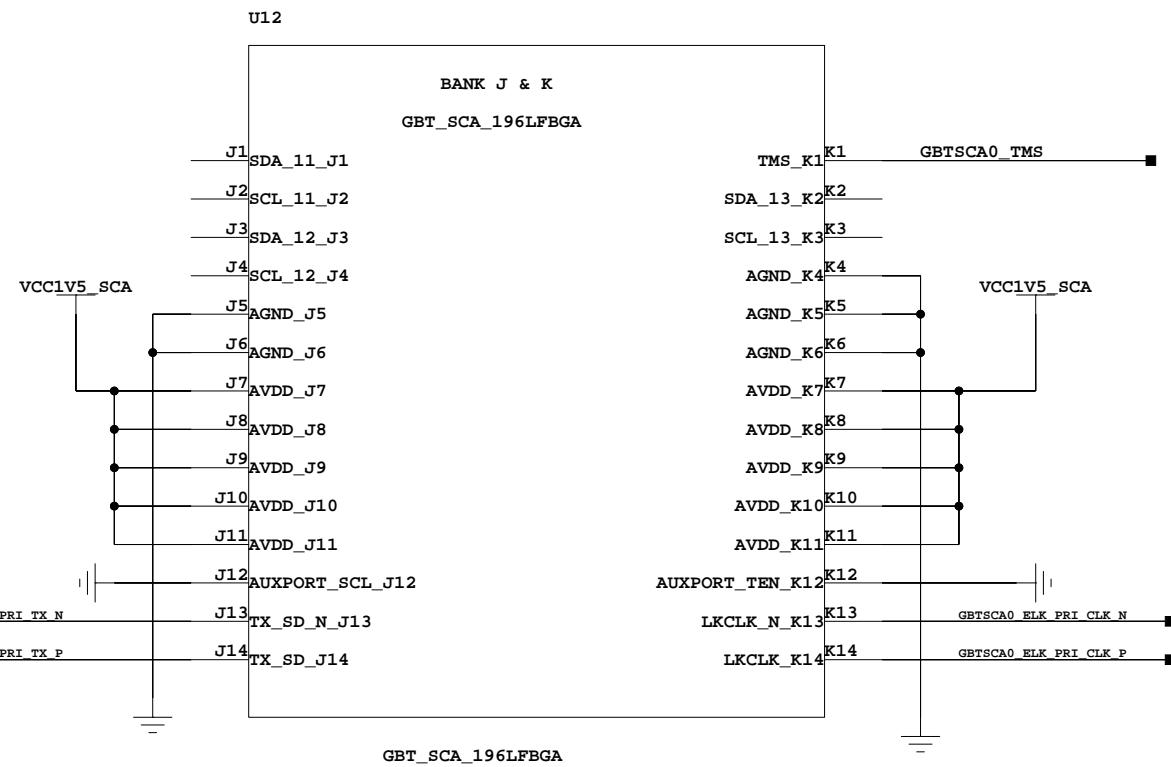


GBT-SCA 0
COMPANY: University of Michigan
TITLE: LpGBT_CSM Prototype v2
SIZE: B REV: 10 OF N
DRAWN: XUEYE HU DATE: 29/05/2020:22:05

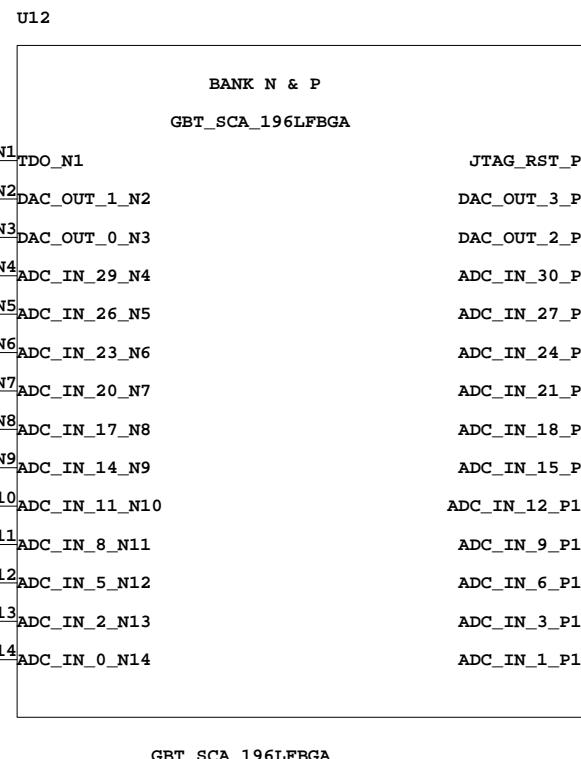


A

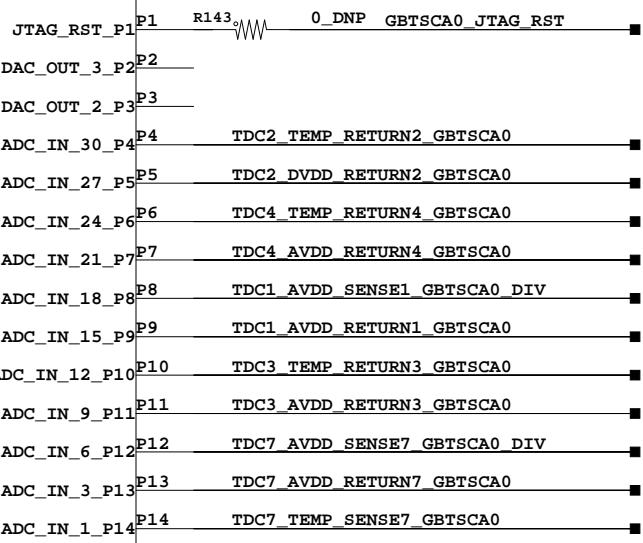
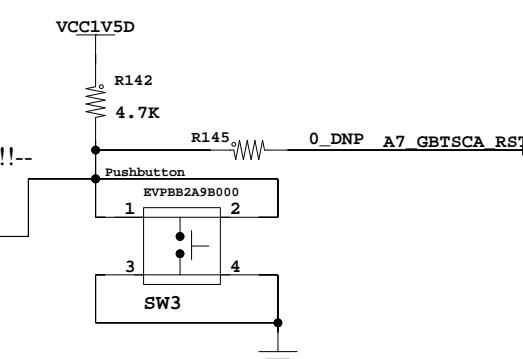
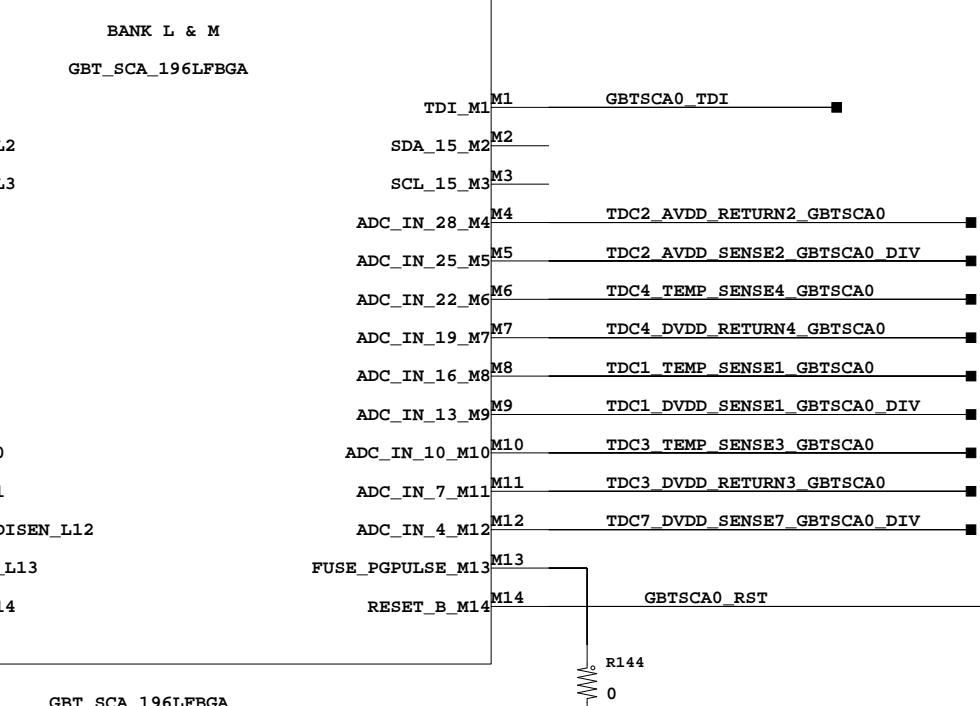
Aux I2C port:
bypassing the e-link ports & used for debugging purposes

**C****D**

GBT-SCA BANK J-P

**E**

GBT-SCA JTAG RESET

**U12**

GBT-SCA fusing not allowed

rx_sd/rx_sd_n : IN

EDOUTECP/N:OUT

GBT-SCA 0

COMPANY
University of Michigan



TITLE
LpGBT_CSM Prototype v2

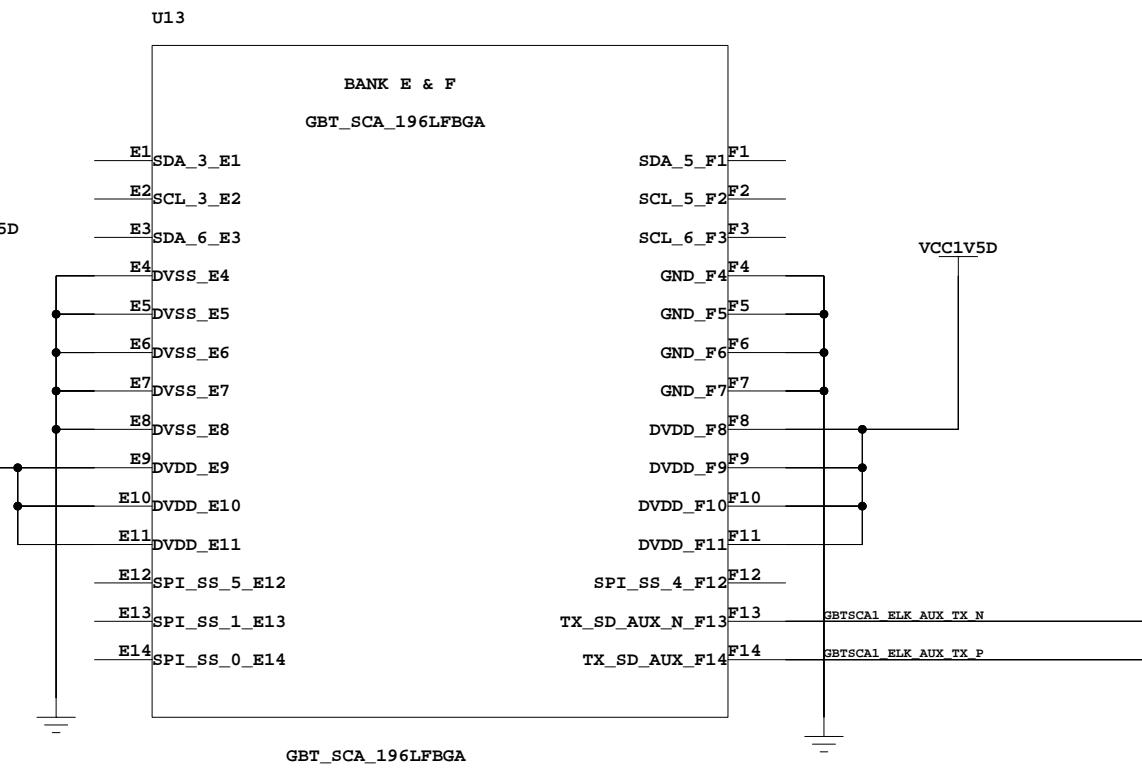
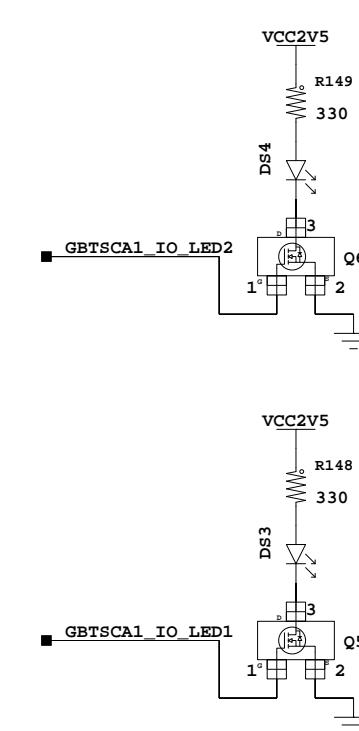
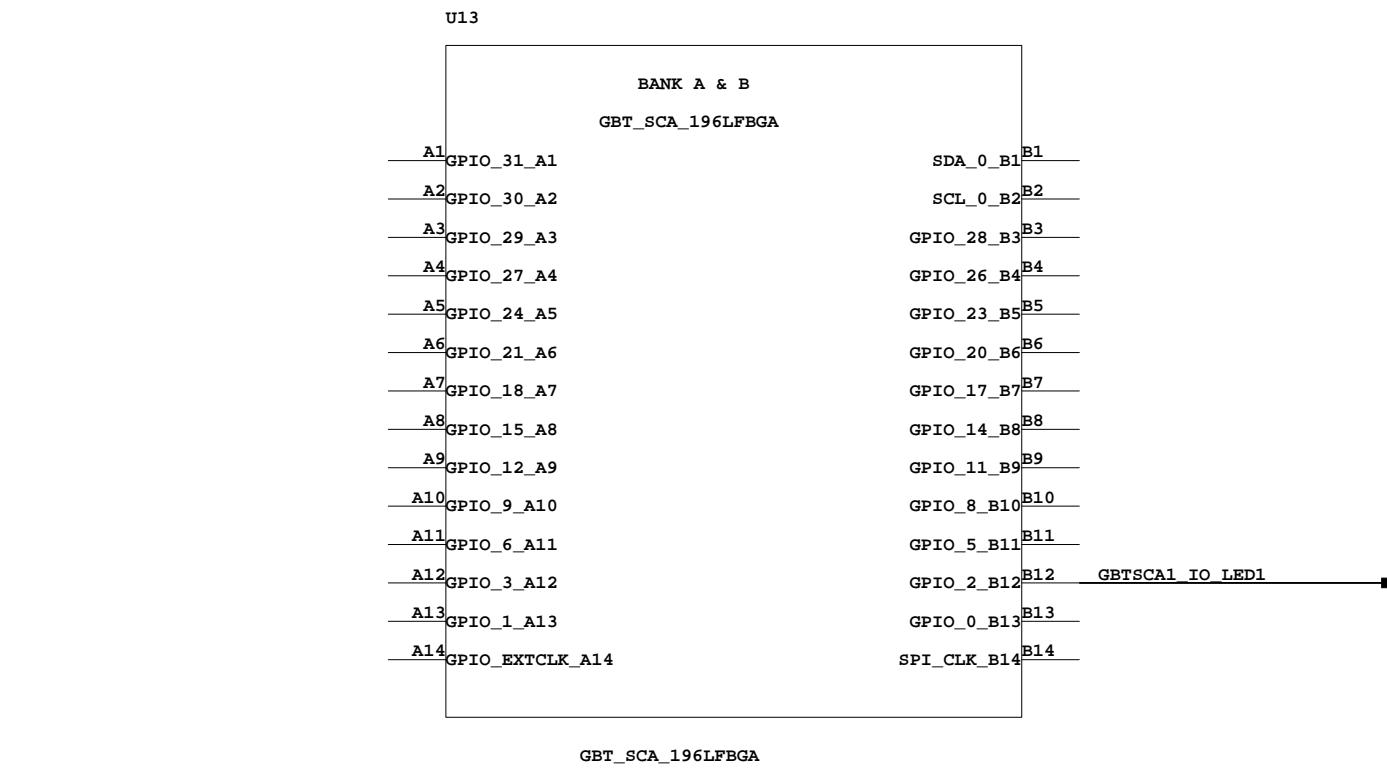
SIZE B REV SHEET 11 OF N
DRAWN XUEYE HU DATE 12/06/2020:13:59

A**B****C****D****E****F**

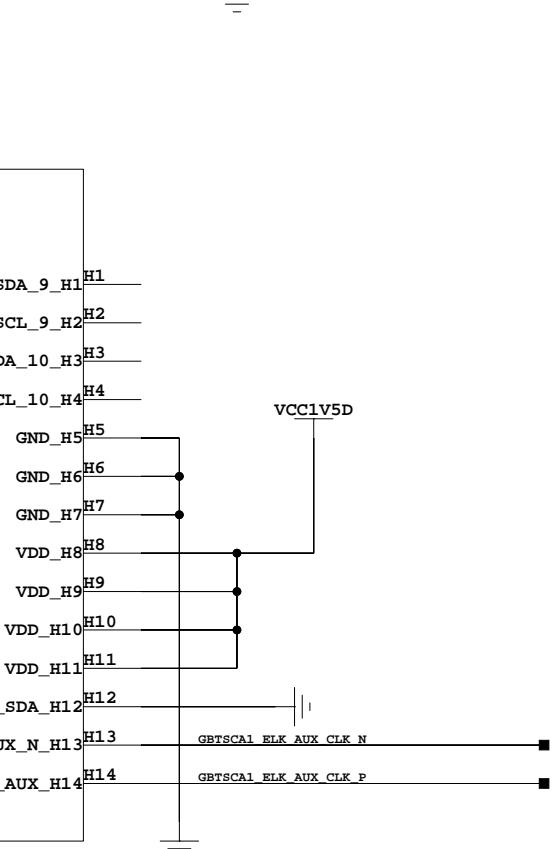
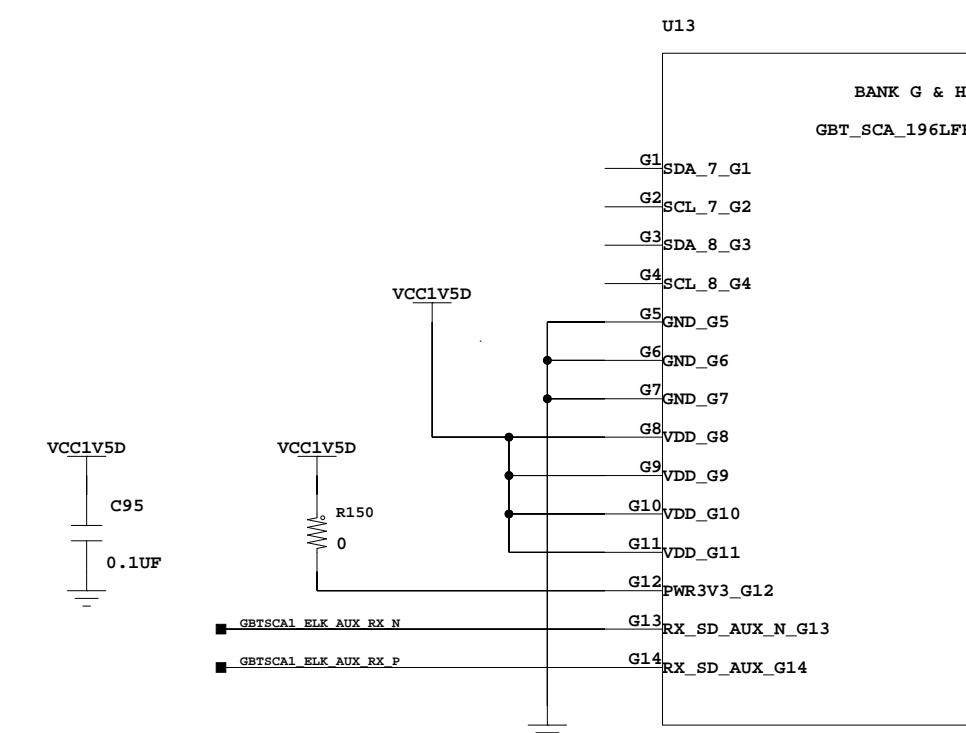
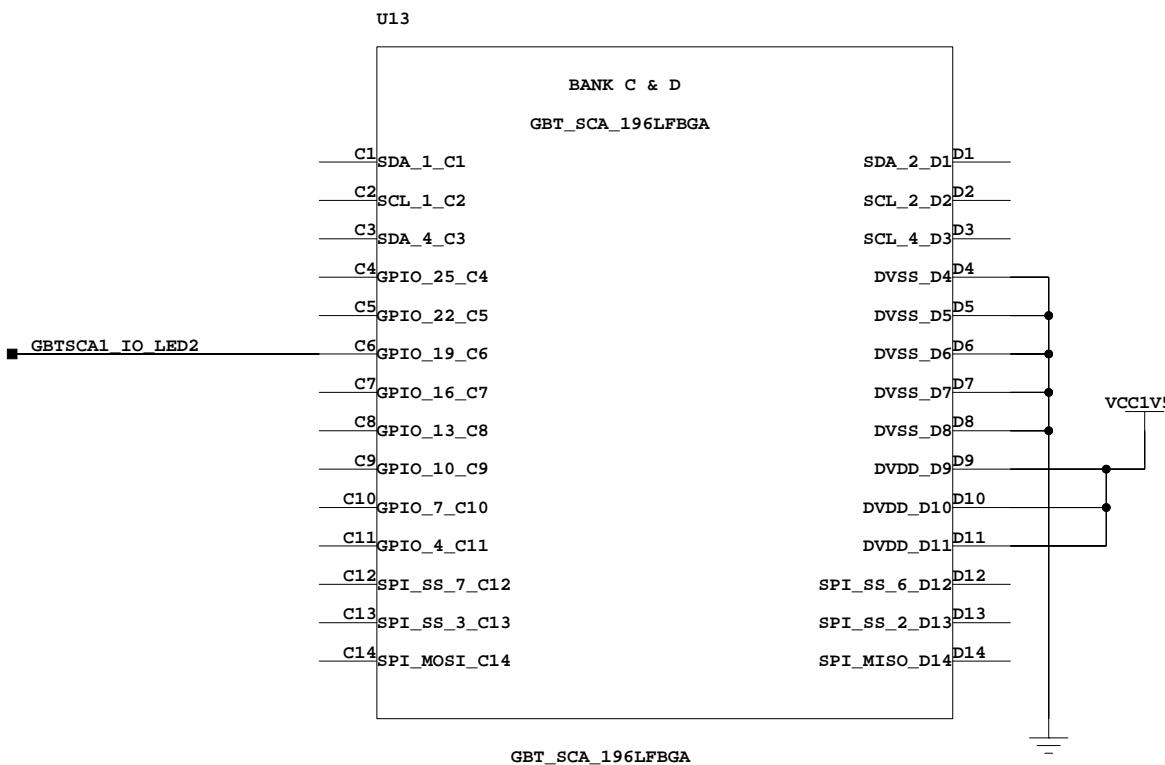
A Note: AGND=GND; DVSS=GND; DVDD=1V5D; AVDD=1V5_SCA; VDD=1V5D

GBT-SCA IO PAD: 0-DVDD

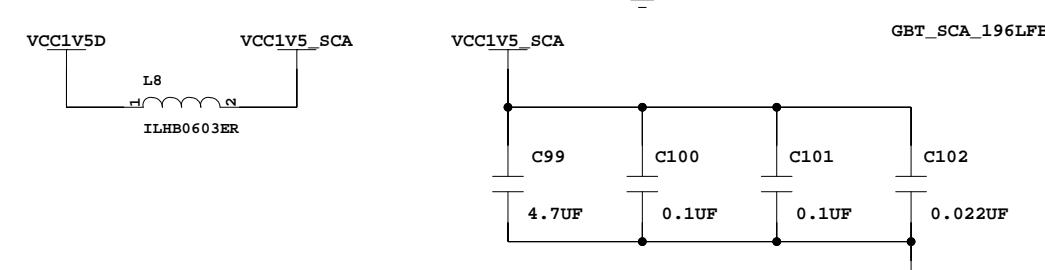
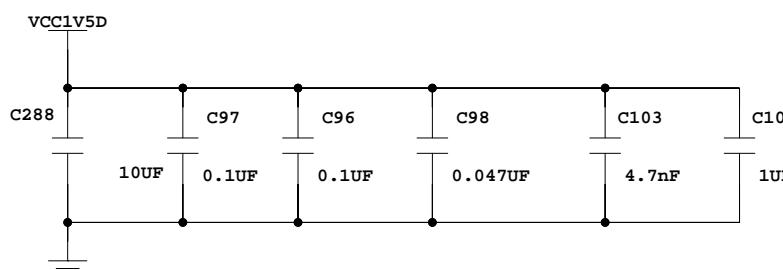
GBT-SCA BANK A-H



GBT_SCA_196LFBGA



**GBT-SCA Decoupling
VDD & DVDD Decoupling**



COMPANY
University of Michigan

TITLE
LpGBT_CSM Prototype v2
SIZE B REV N
DRAWN XUEYE HU DATE 04/06/2020:16:54



A

B

C

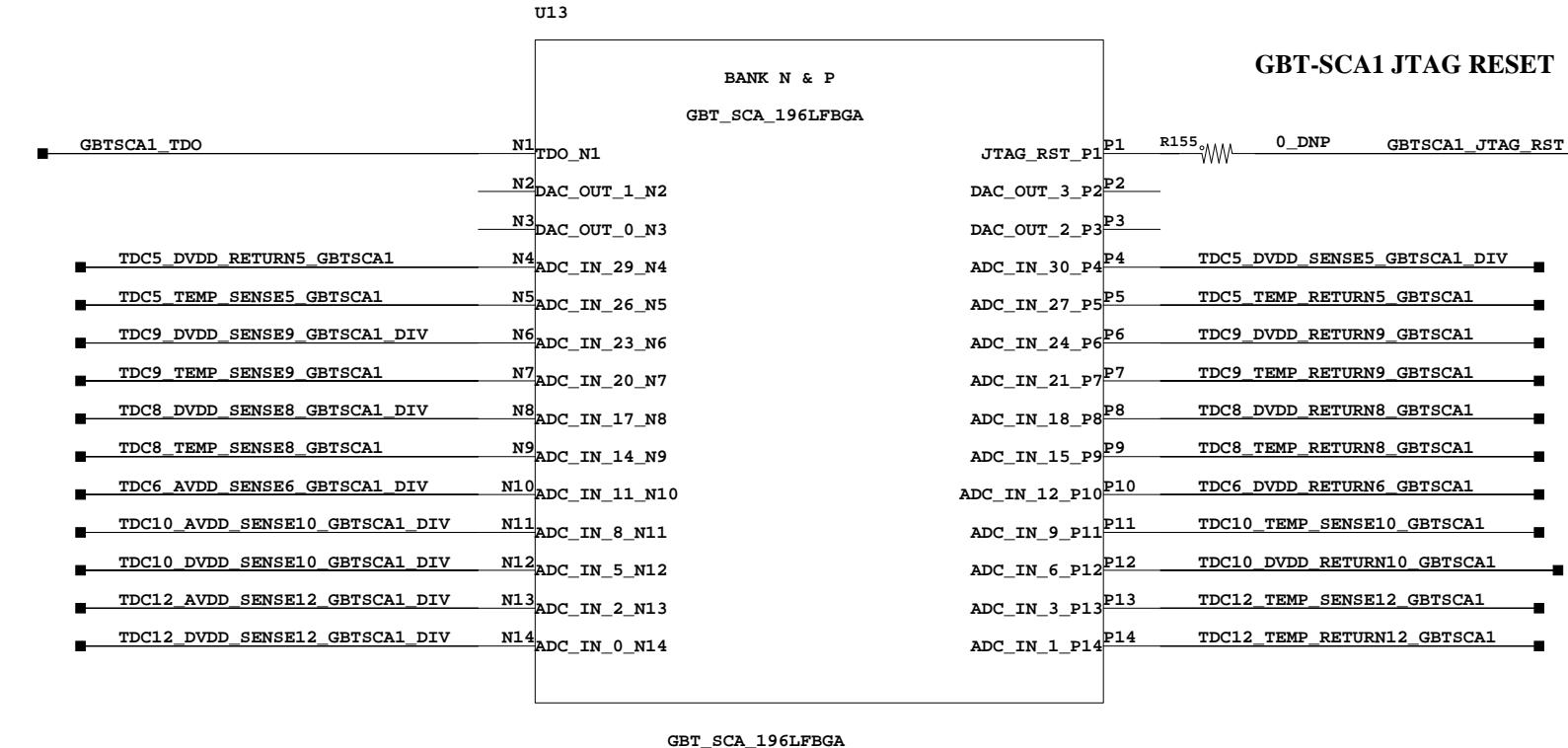
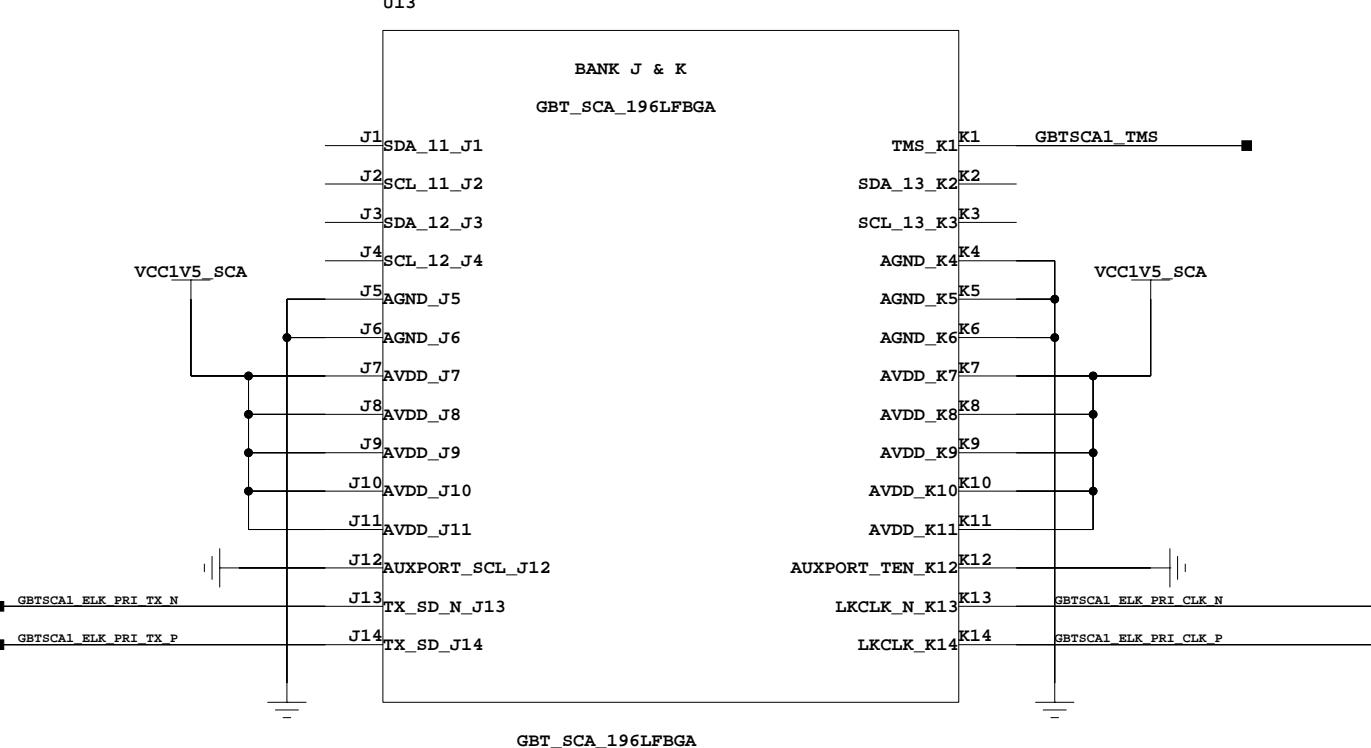
D

E

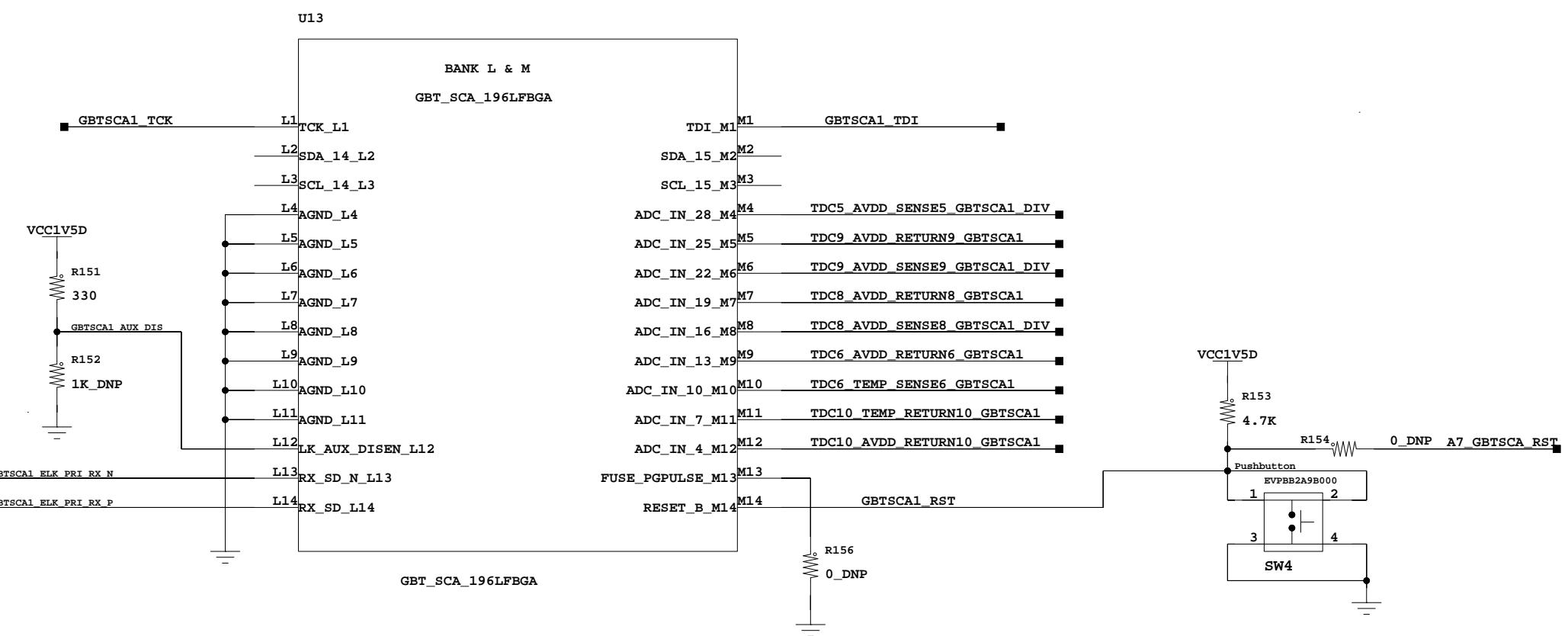
F

GBT-SCA BANK J-P

Aux I2C port:
bypassing the e-link ports & used for debugging purposes



GBTSCA1 JTAG MASTER -- A7 JTAG 1.5V/3.3V compatible ISSUE



GBT SCA 1

COMPANY

TITLE

LpGBT_CSM Prototype v2

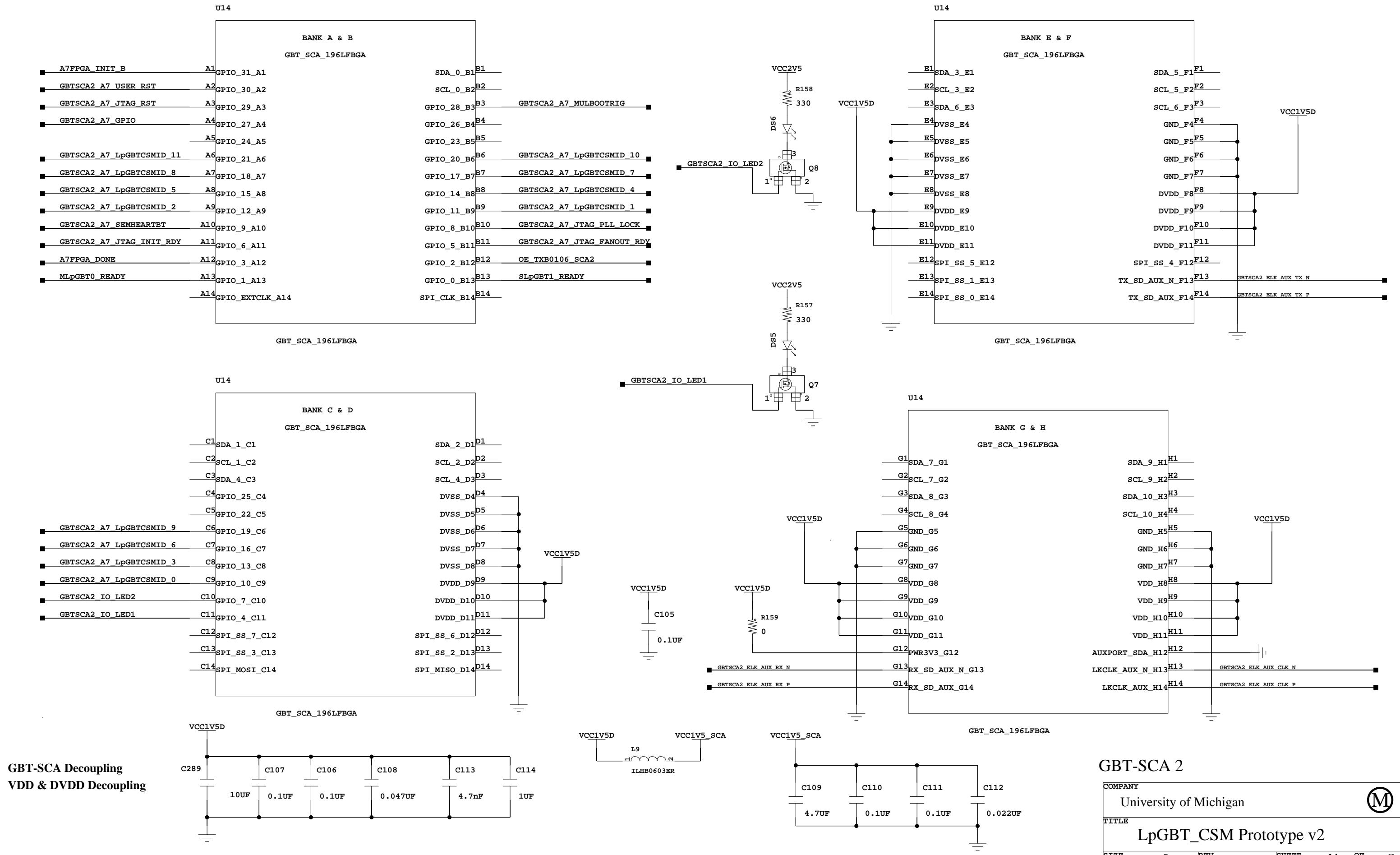
SIZE B REV SHEET 13 OF N
 DRAWN XUEYE HU DATE 04/06/2020:16:54

A **B** **C** **D** **E** **F**

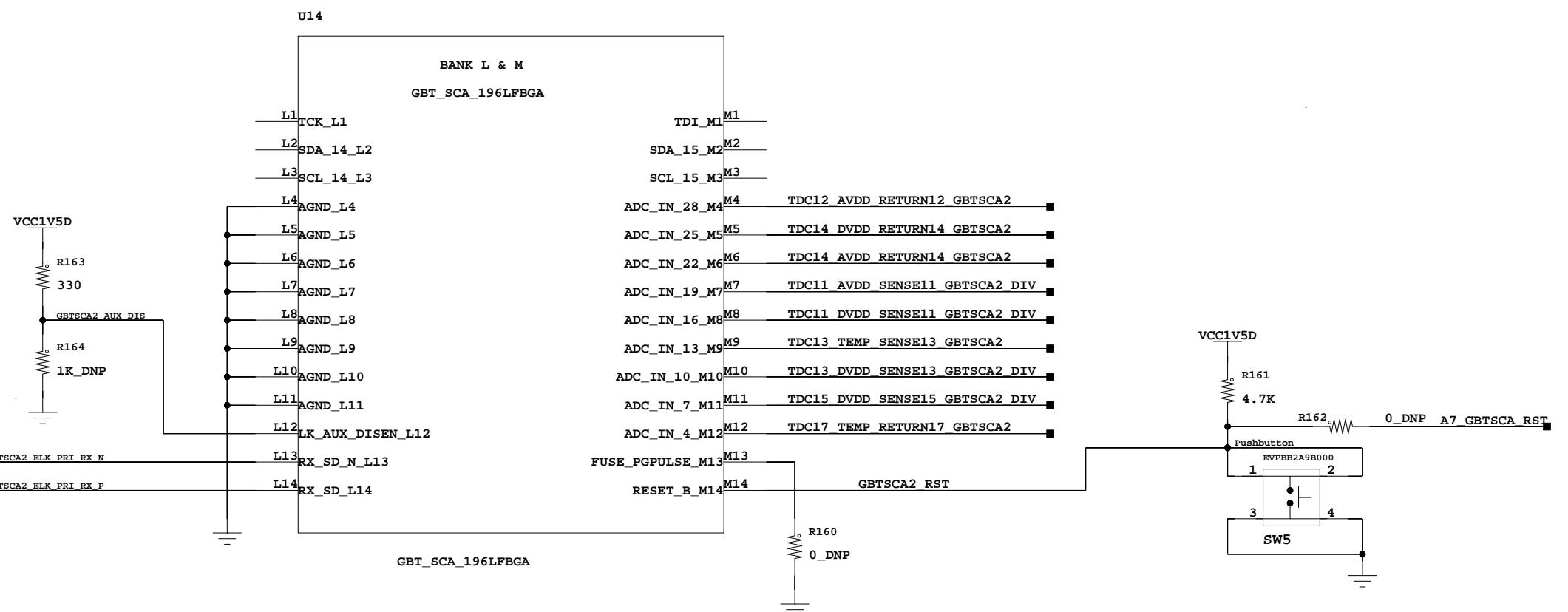
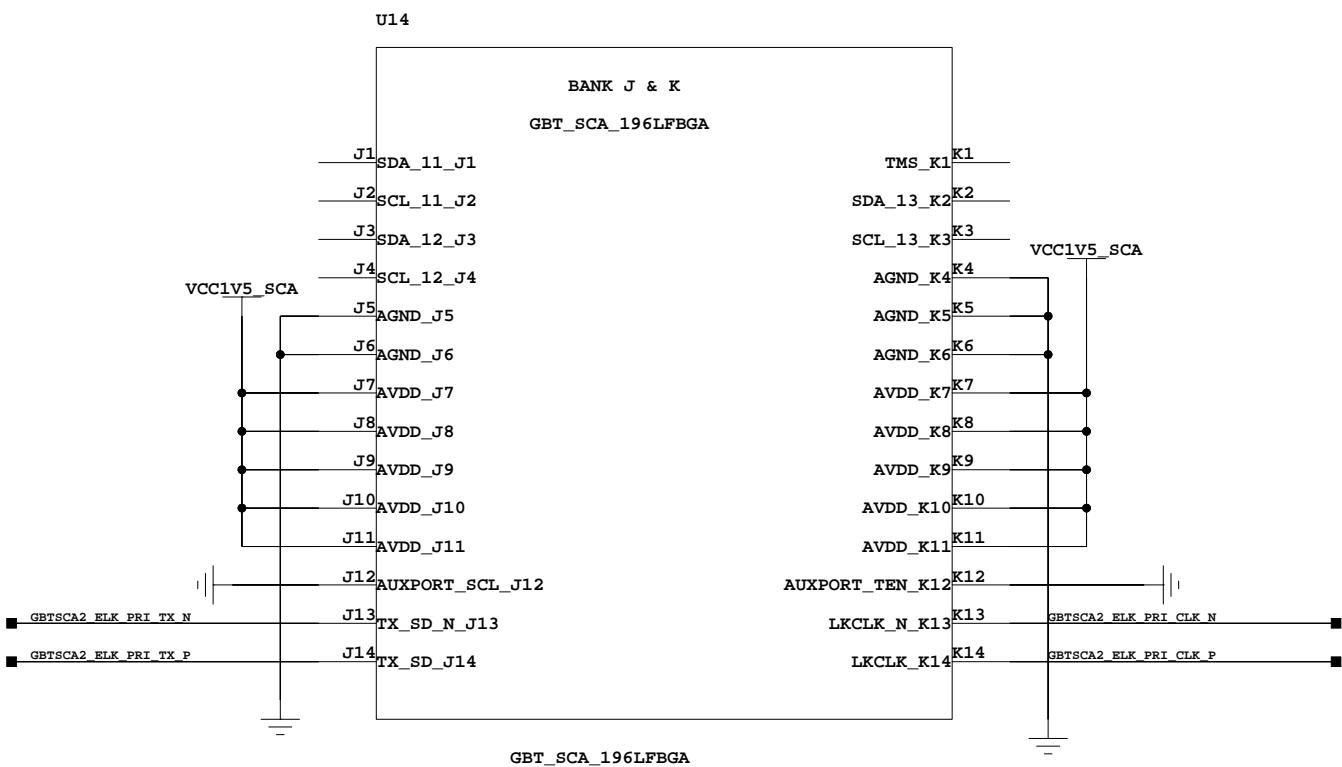
Note: AGND=GND; DVSS=GND; DVDD=1V5D; AVDD=1V5_SCA; VDD=1V5D

GBT-SCA IO PAD: 0-DVDD

GBT-SCA BANK A-H

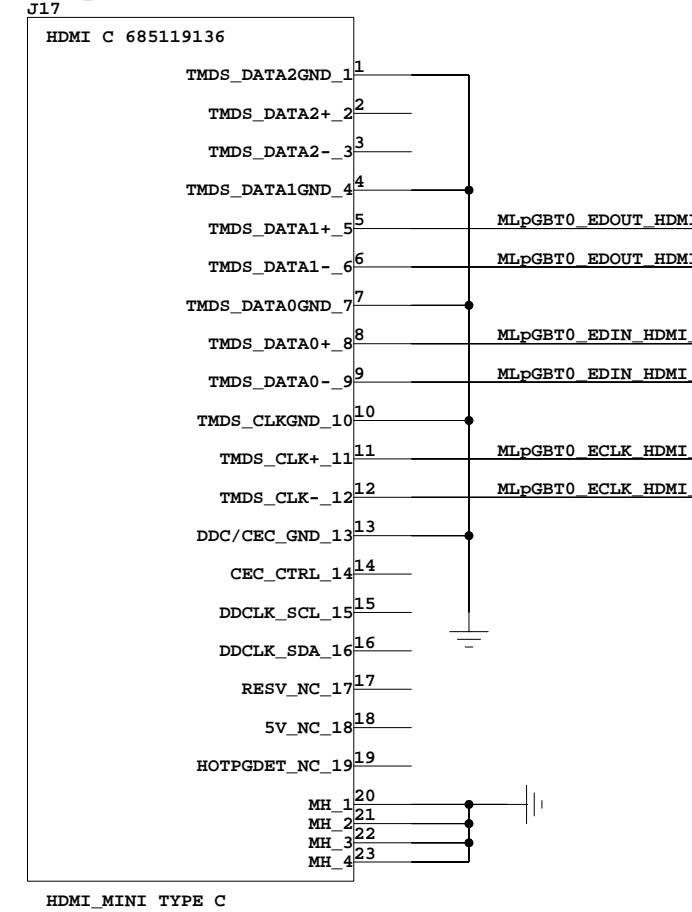


GBT-SCA BANK J-P

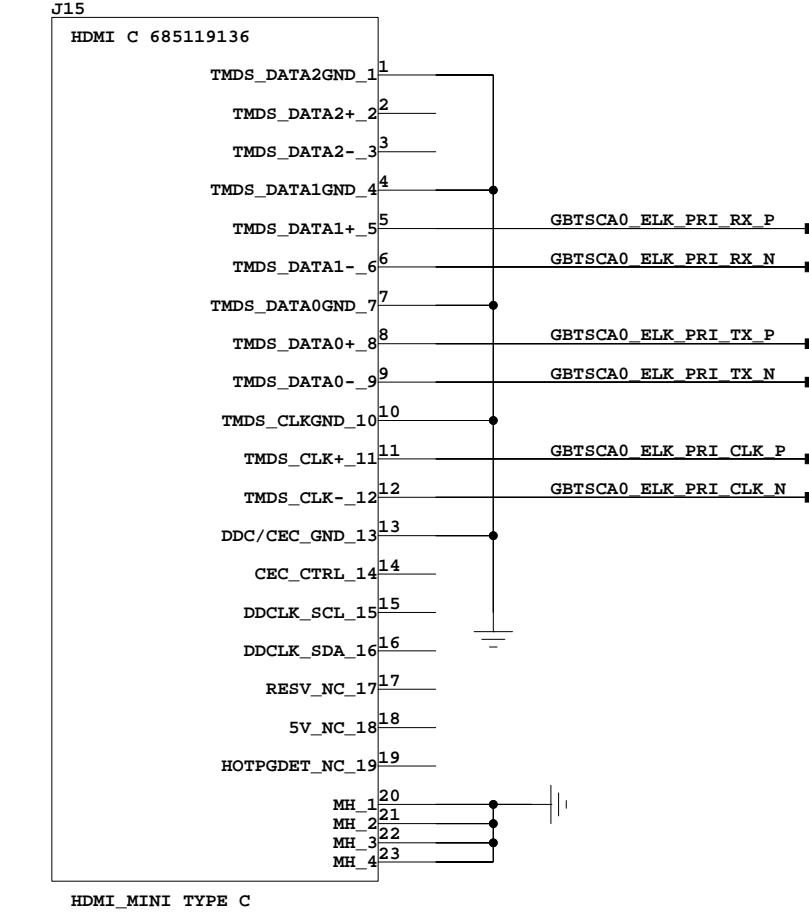


4

MLpGBT0 ELINK TEST PORT



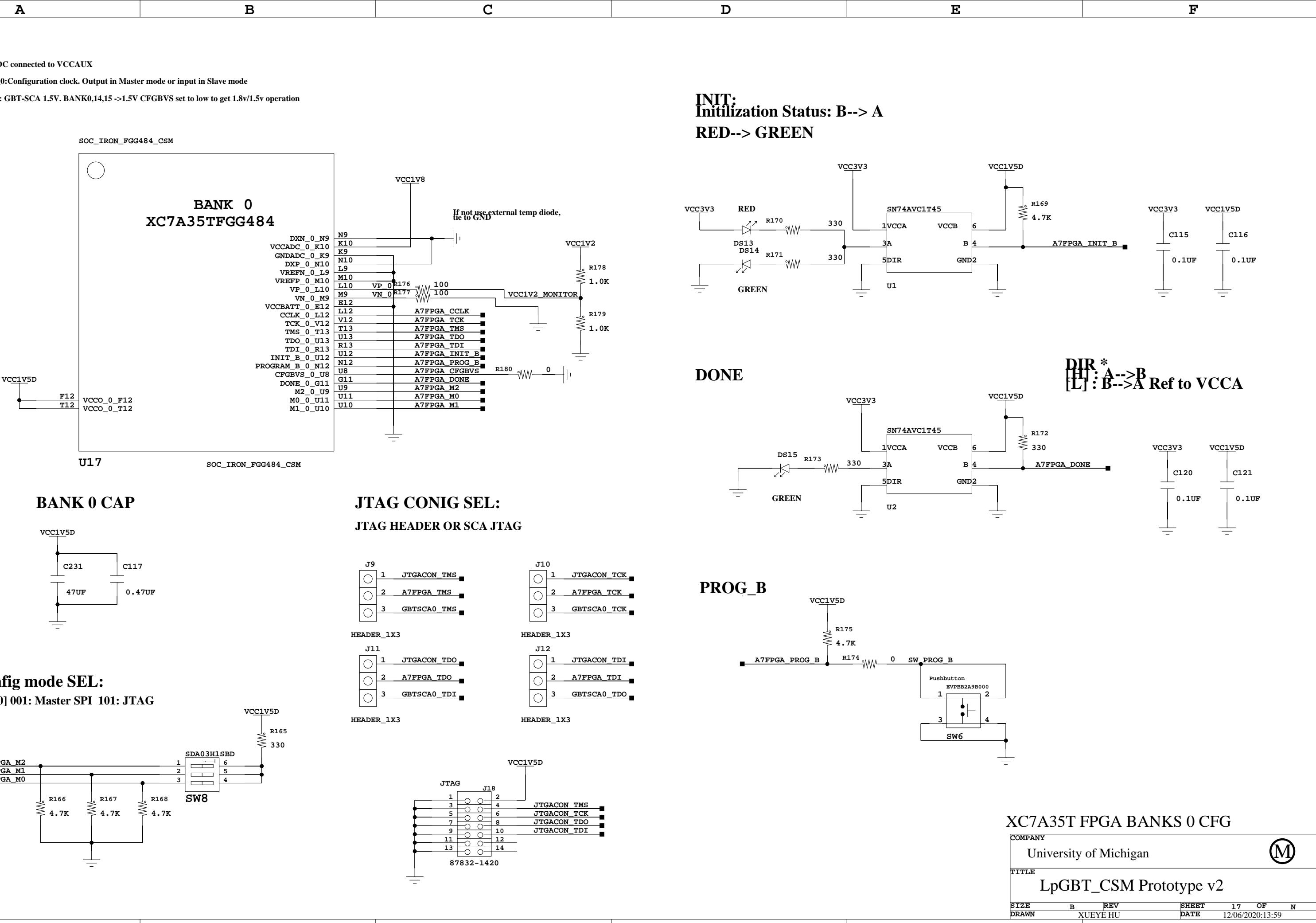
GBTSCA0 PRI SCA E-PORT



LpGBT & SCA ELINK HDMI

COMPANY	University of Michigan	(M)
TITLE		
	LpGBT_CSM Prototype v2	
SIZE DRAWN	B REV XUEYE HU	SHEET 16 OF N DATE 12/05/2020:17:18

4

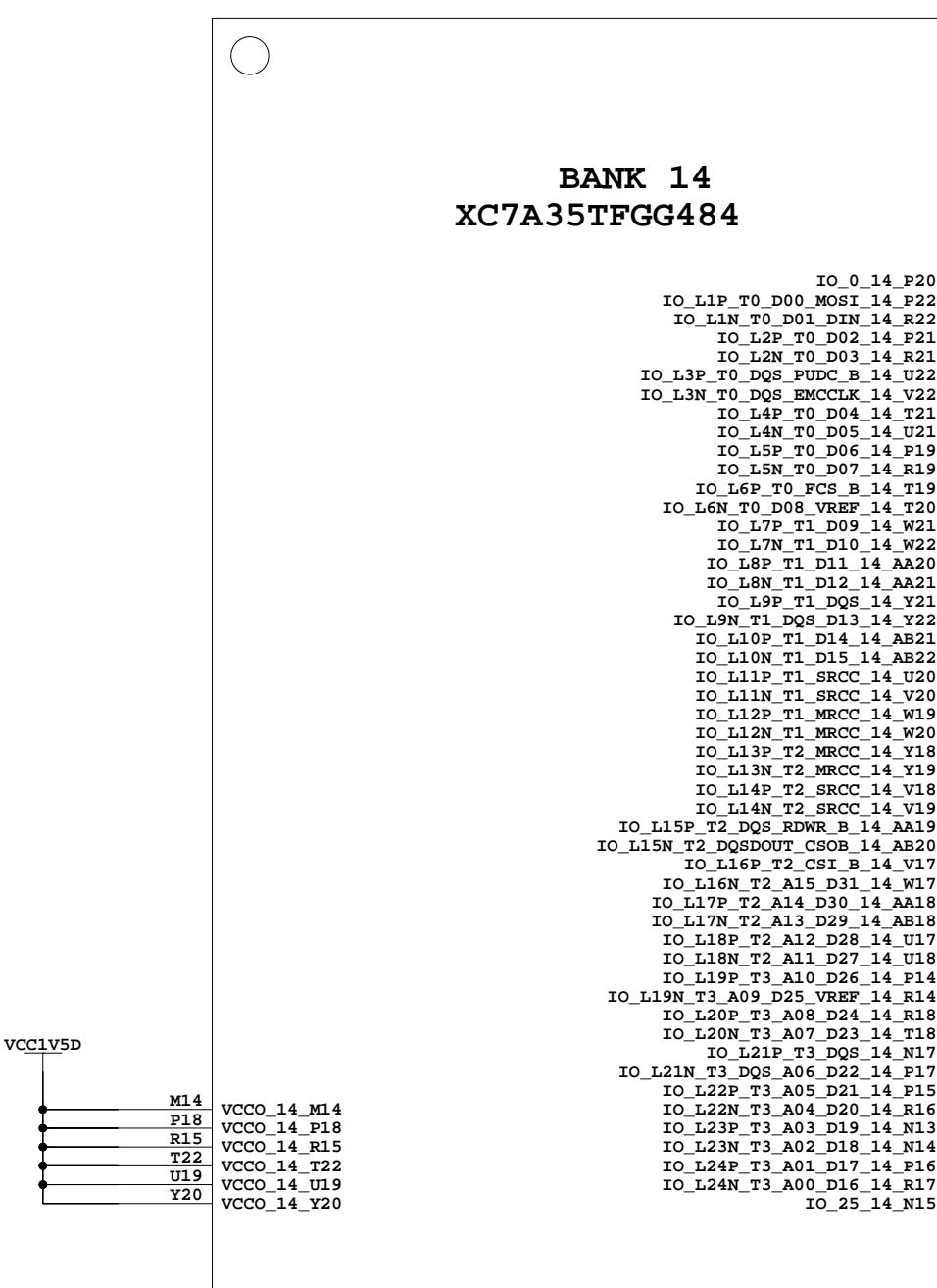


A B C D E F

Configuration BANKs 0/ 14/ 15 share same voltage level

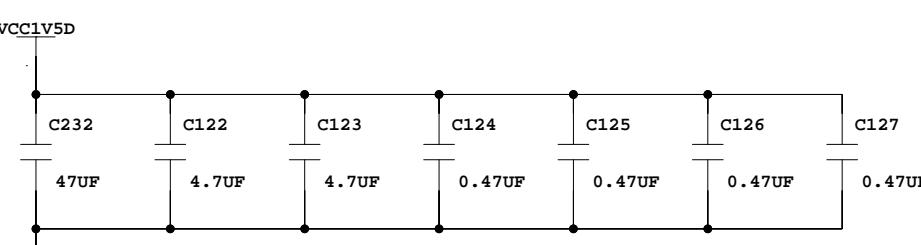
DIFF_SSTL15 FOR ALL DIFF. PAIRS

SOC_IRON_FGG484_CSM



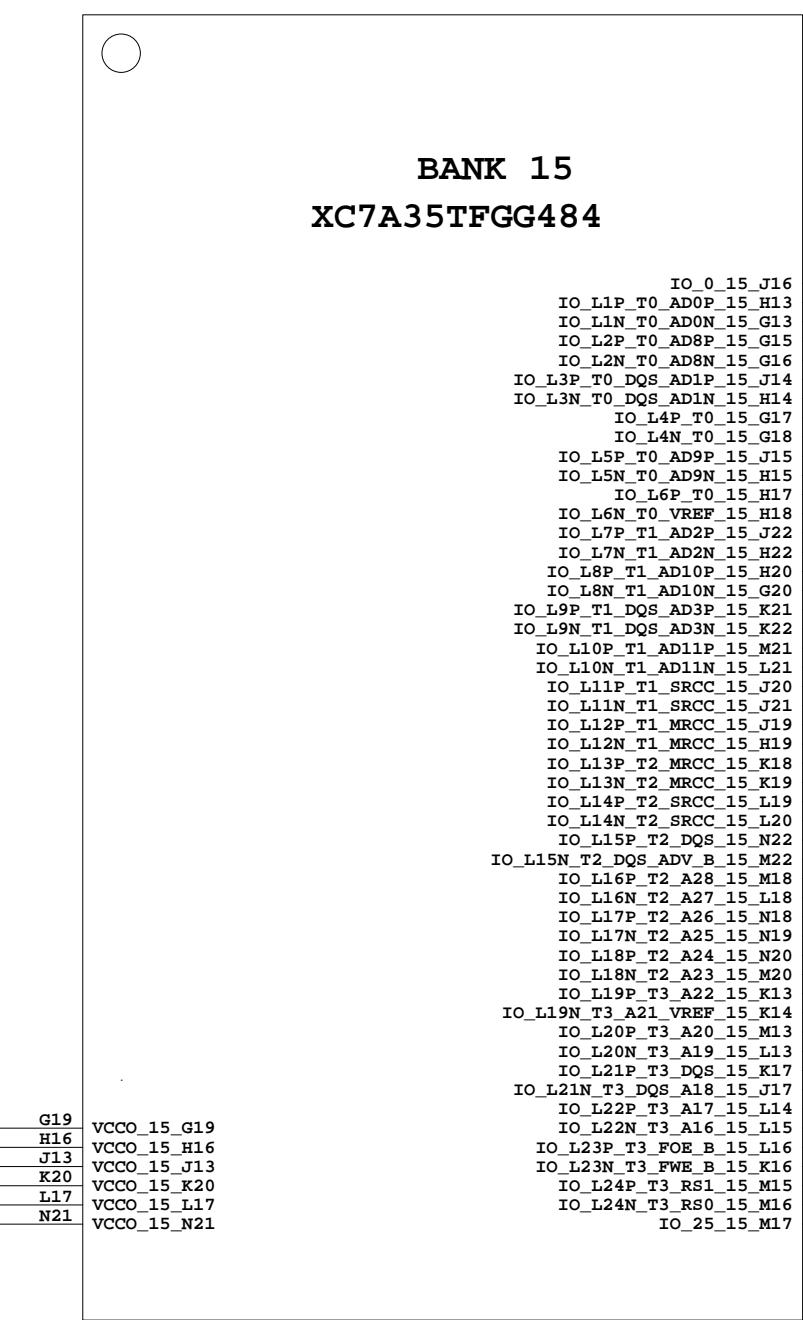
U17

SOC_IRON_FGG484_CSM



XC7A35T VCCO 1*47UF (shared upto 4 banks) /2*4.7UF /4*0.47UF

SOC_IRON_FGG484_CSM

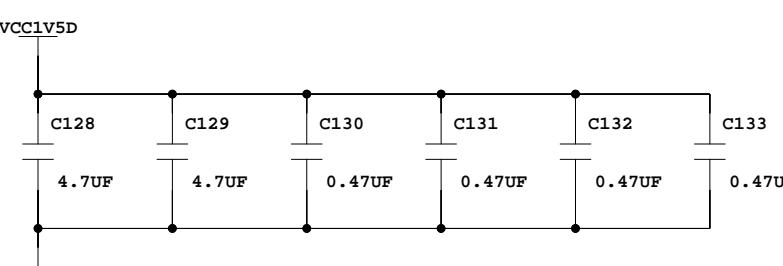


U17

SOC_IRON_FGG484_CSM

FE MEZZ. JTAG SOURCE
GBTSCA1

NEED CHANGE SIGNAL NAME!!



XC7A35T FPGA BANKS 14, 15

COMPANY
University of MichiganTITLE
LpGBT_CSM Prototype v2SIZE B REV SHEET 18 OF N
DRAWN XUEYE HU DATE 05/06/2020:15:56

A

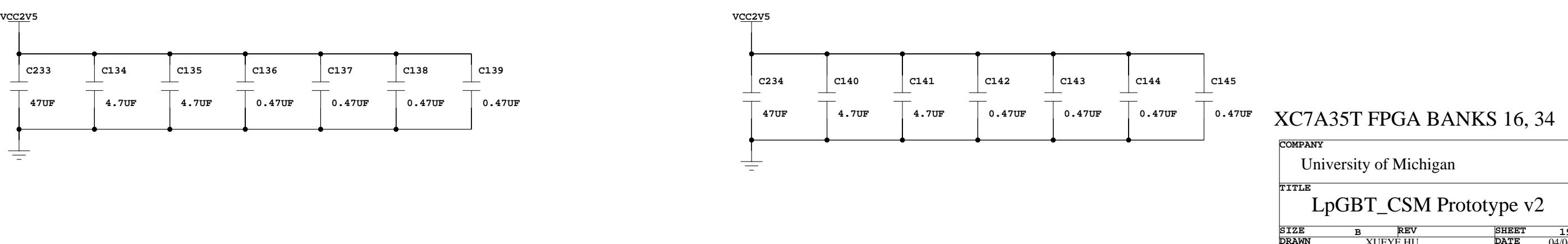
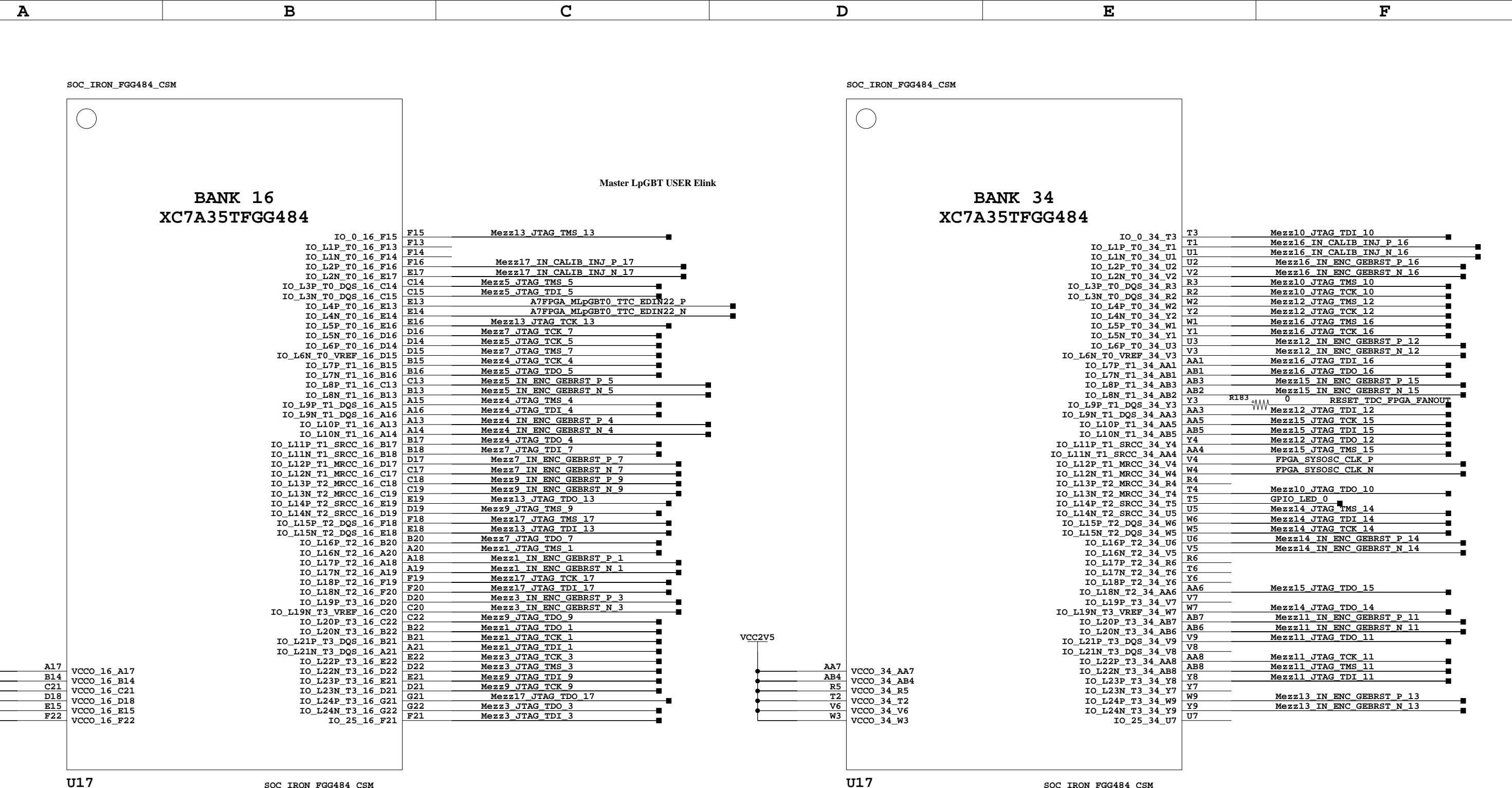
B

C

D

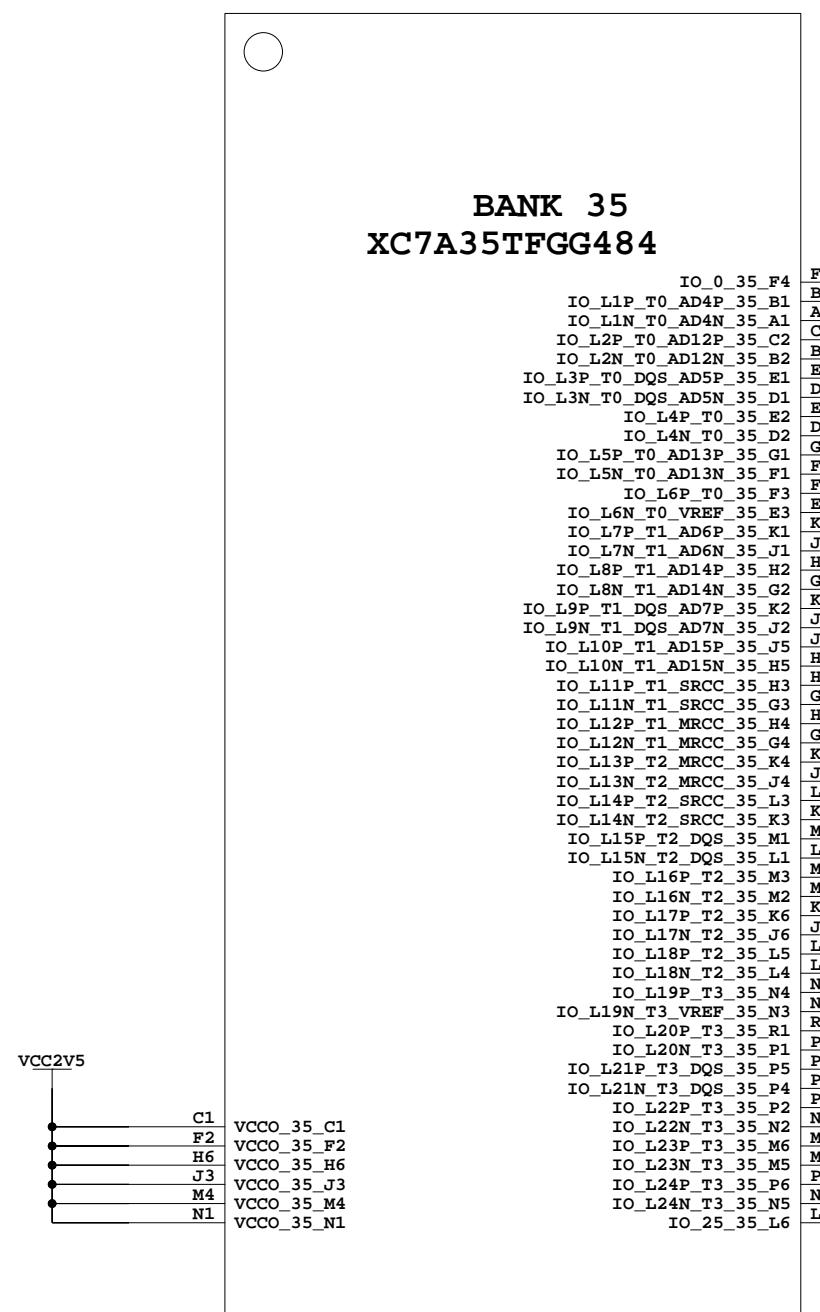
E

F



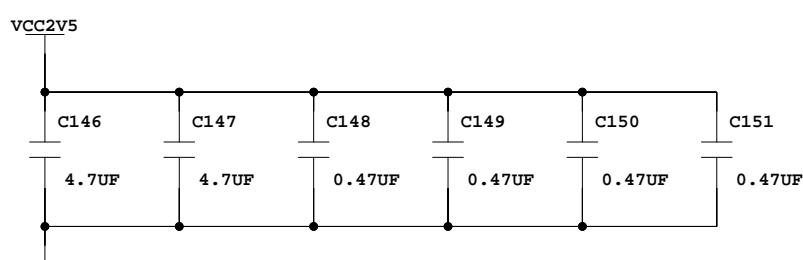
A B C D E F

SOC_IRON_FGG484_CSM

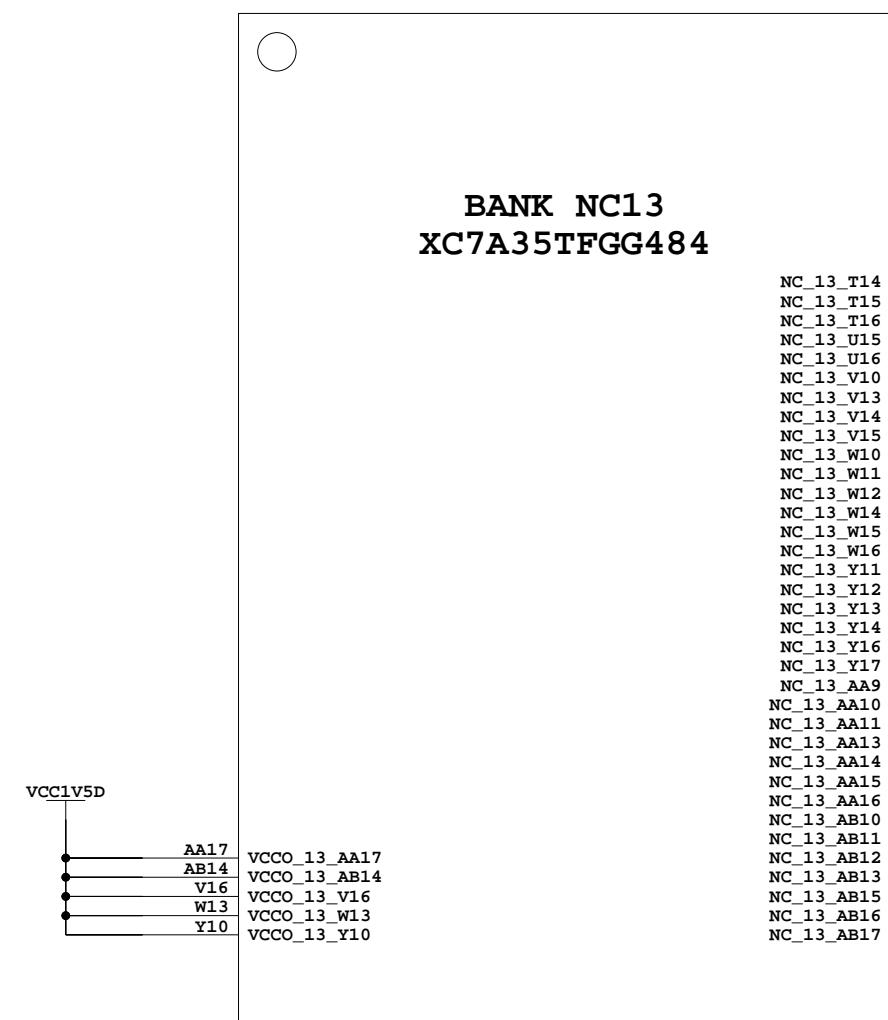


U17

SOC_IRON_FGG484_CSM

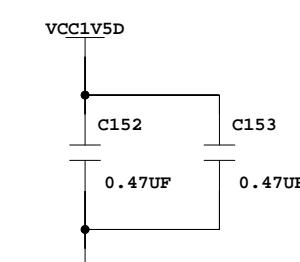


SOC_IRON_FGG484_CSM



U17

SOC_IRON_FGG484_CSM



XC7A35T FPGA BANKS 35, NC13

COMPANY
University of Michigan



TITLE
LpGBT_CSM Prototype v2

SIZE B REV SHEET 20 OF N
DRAWN XUEYE HU DATE 04/06/2020:14:19

A

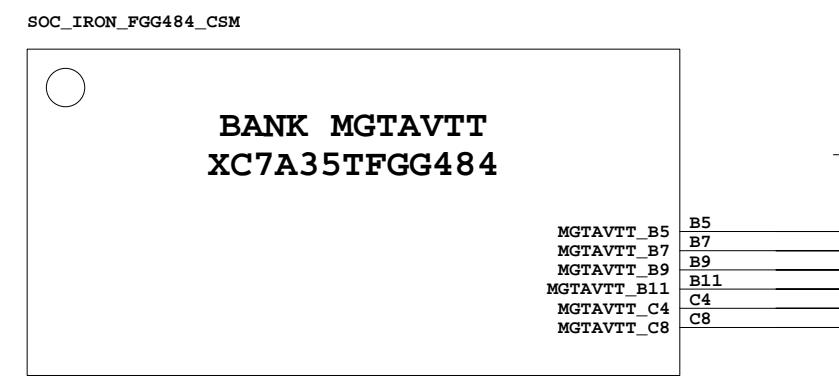
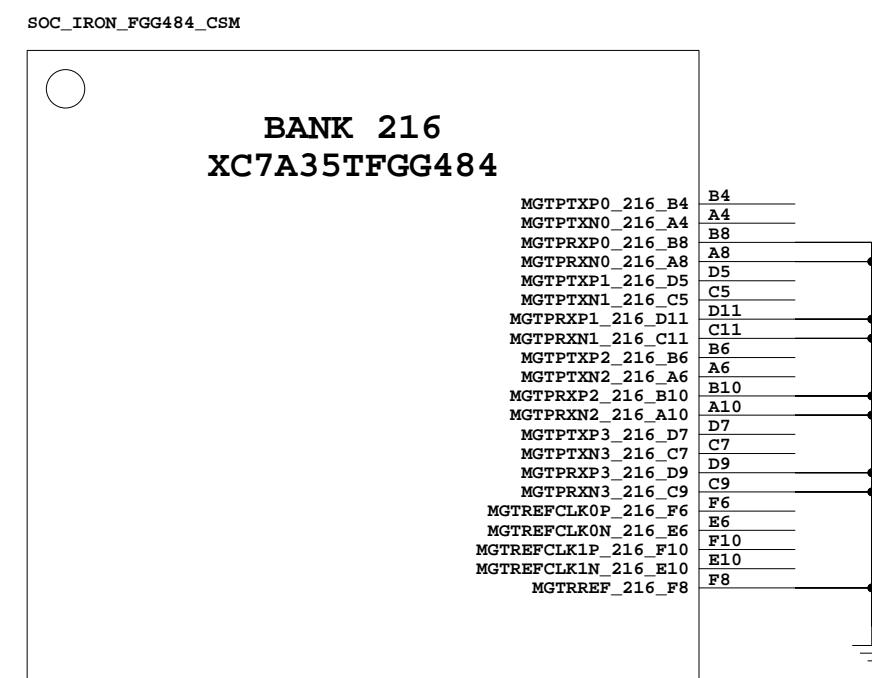
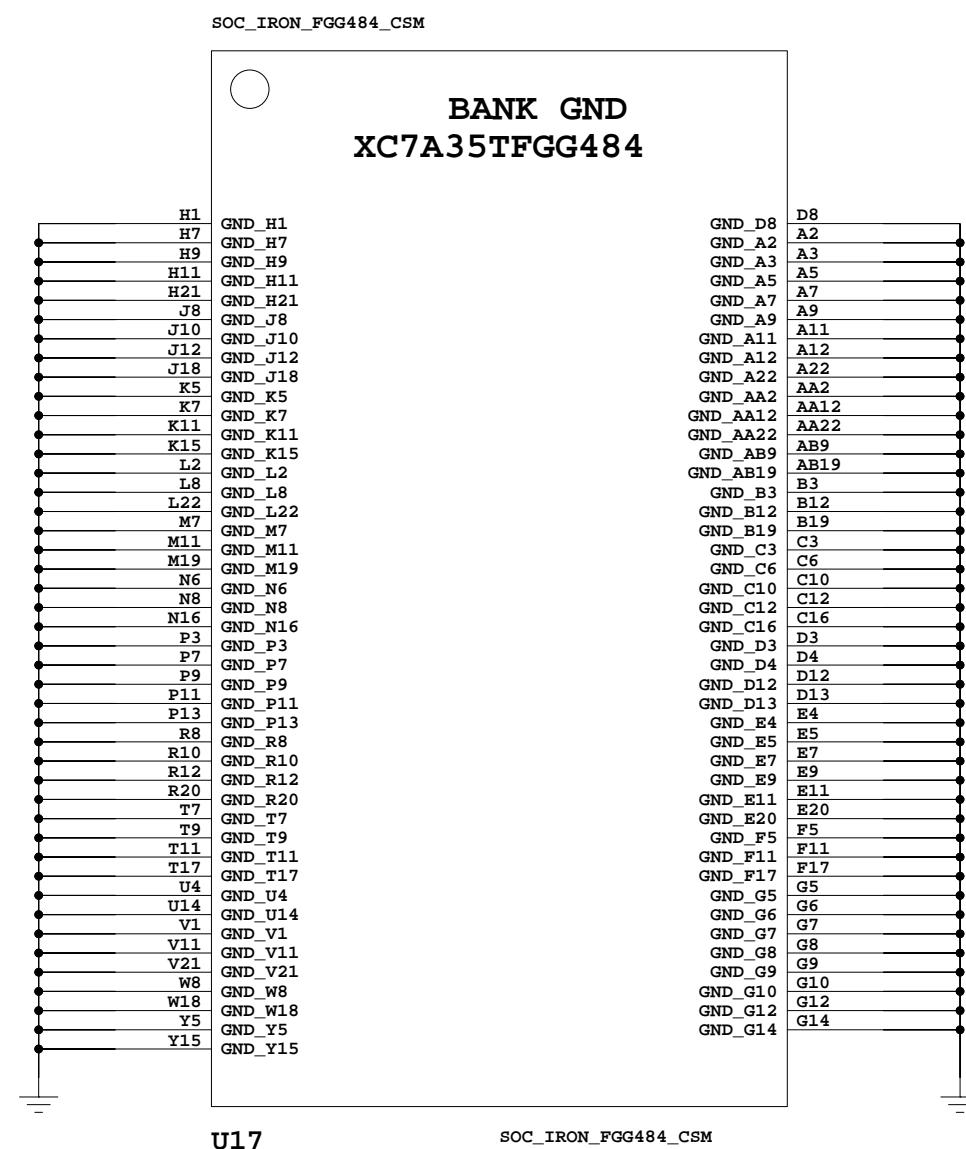
B

C

D

E

F

A**B****C****D****E****F**

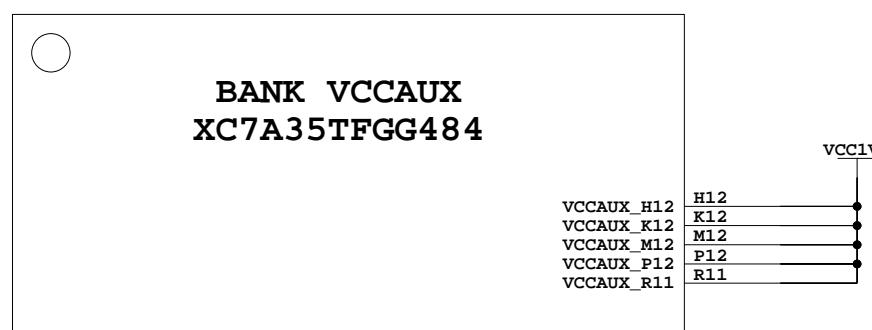
MGTVCC, MGTVTT: GND
MGTREFCLK: FLOAT
MGTRX: GND
MGTTX: FLOAT
MGTRREF: GND

A B C D E F

XC7A35T FPGA VCCAUX Filter CAPs

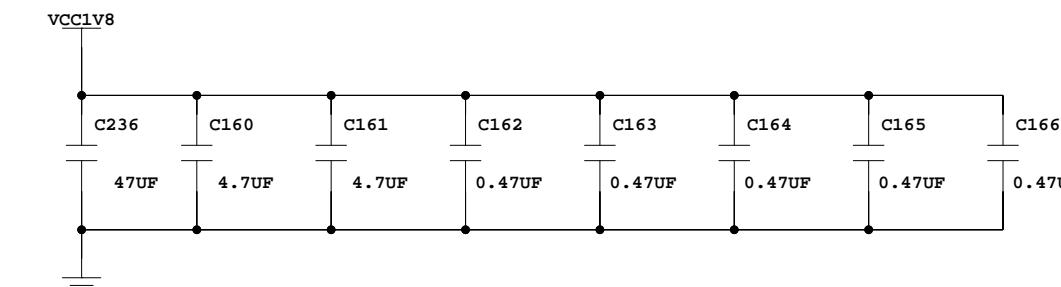
47UF 1/4.7UF 2/0.47UF 5

SOC_IRON_FGG484_CSM



U17

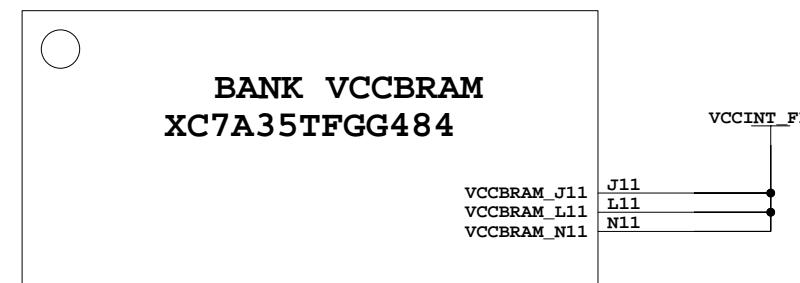
SOC_IRON_FGG484_CSM



XC7A35T FPGA VCCBRAM Filter CAPs

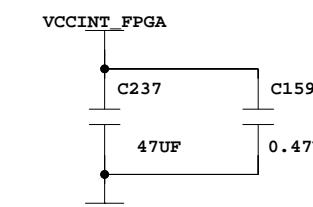
47UF 1/0.47UF 1

SOC_IRON_FGG484_CSM



U17

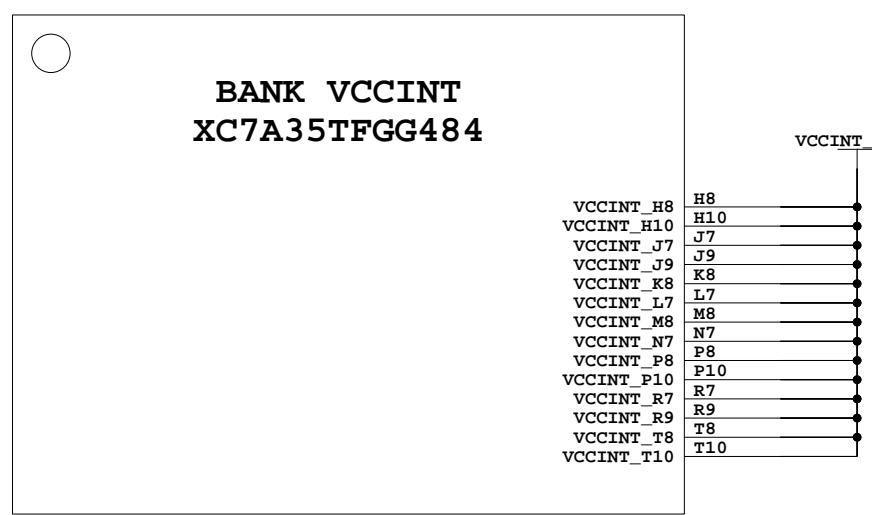
SOC_IRON_FGG484_CSM



XC7A35T EPGA VCCINT Filter CAPs

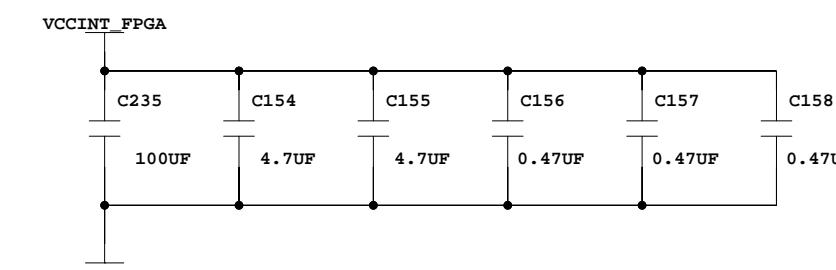
100UF 1/4.7UF 2/0.47UF 3

SOC_IRON_FGG484_CSM



U17

SOC_IRON_FGG484_CSM



XC7A35T FPGA POWER BANKS

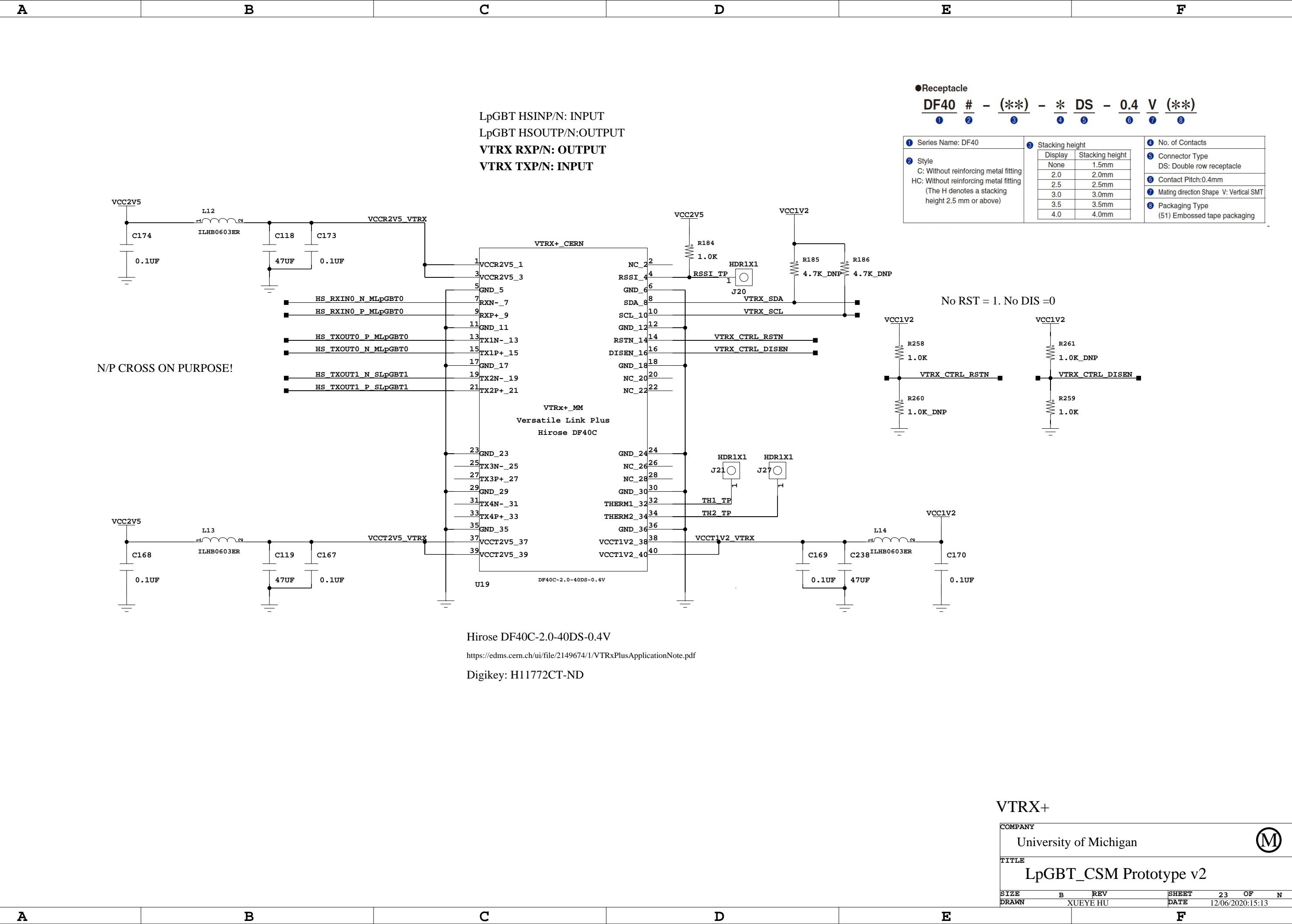
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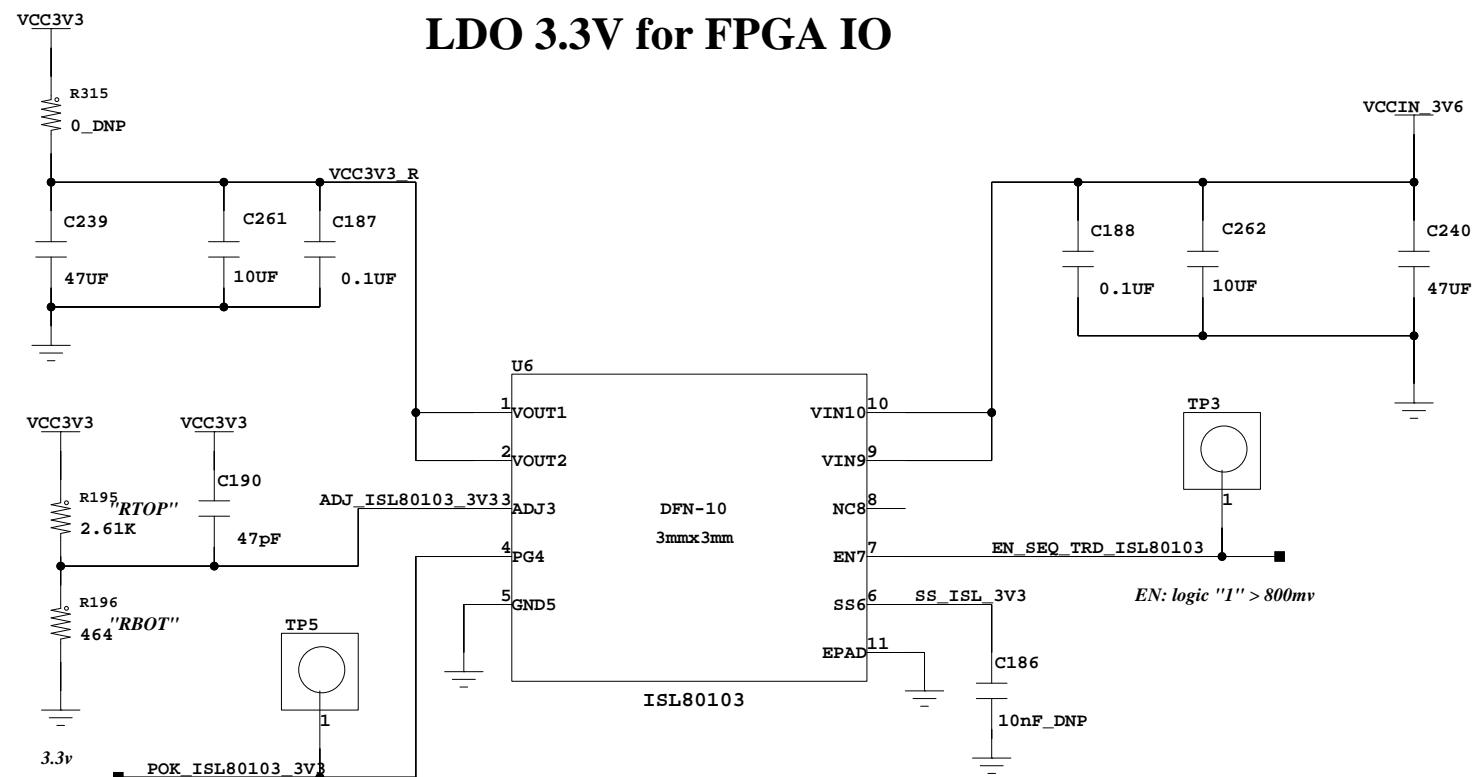


TITLE
LpGBT_CSM Prototype v2

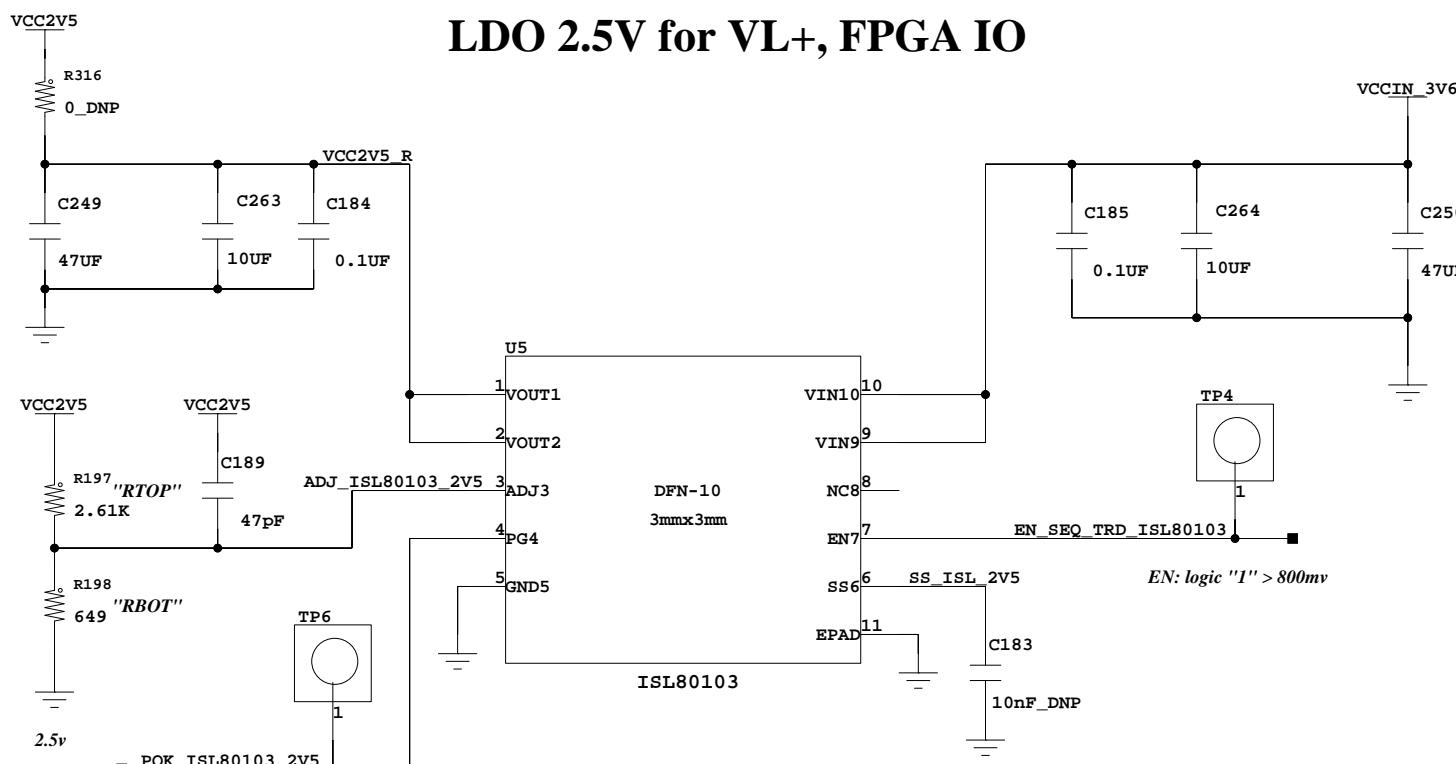
SIZE B REV SHEET 22 OF N
DRAWN XUEYE HU DATE 12/05/2020:22:45

A B C D E F

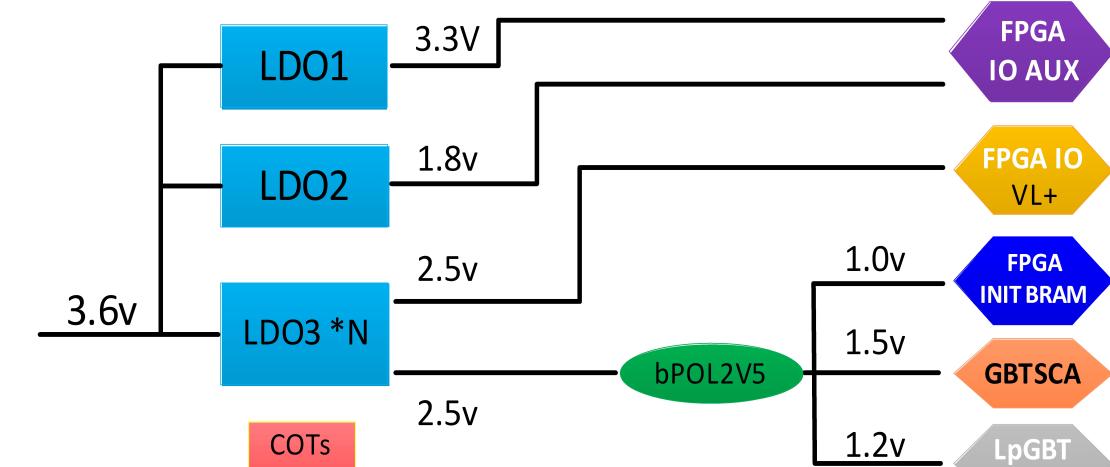




PULL-UP RES ON POWER-ON SEQ. Page



PULL-UP RES ON POWER-ON SEQ. Page



1. VIN Range 2.2V to 6.0V
 2. To ensure adequate thermal relief for 4A operation,
a 2 x 2 grid of vias to GND MUST be placed under U1
 3. C4 and C5 must have orientation as shown to cancel EM
 4. R8 and C9 form an RC circuit to allow
PWR-FN to be active 40 μ S after VIN reaches 11V

$$V_{out} = 0.5V \cdot (RT / RB + 1)$$

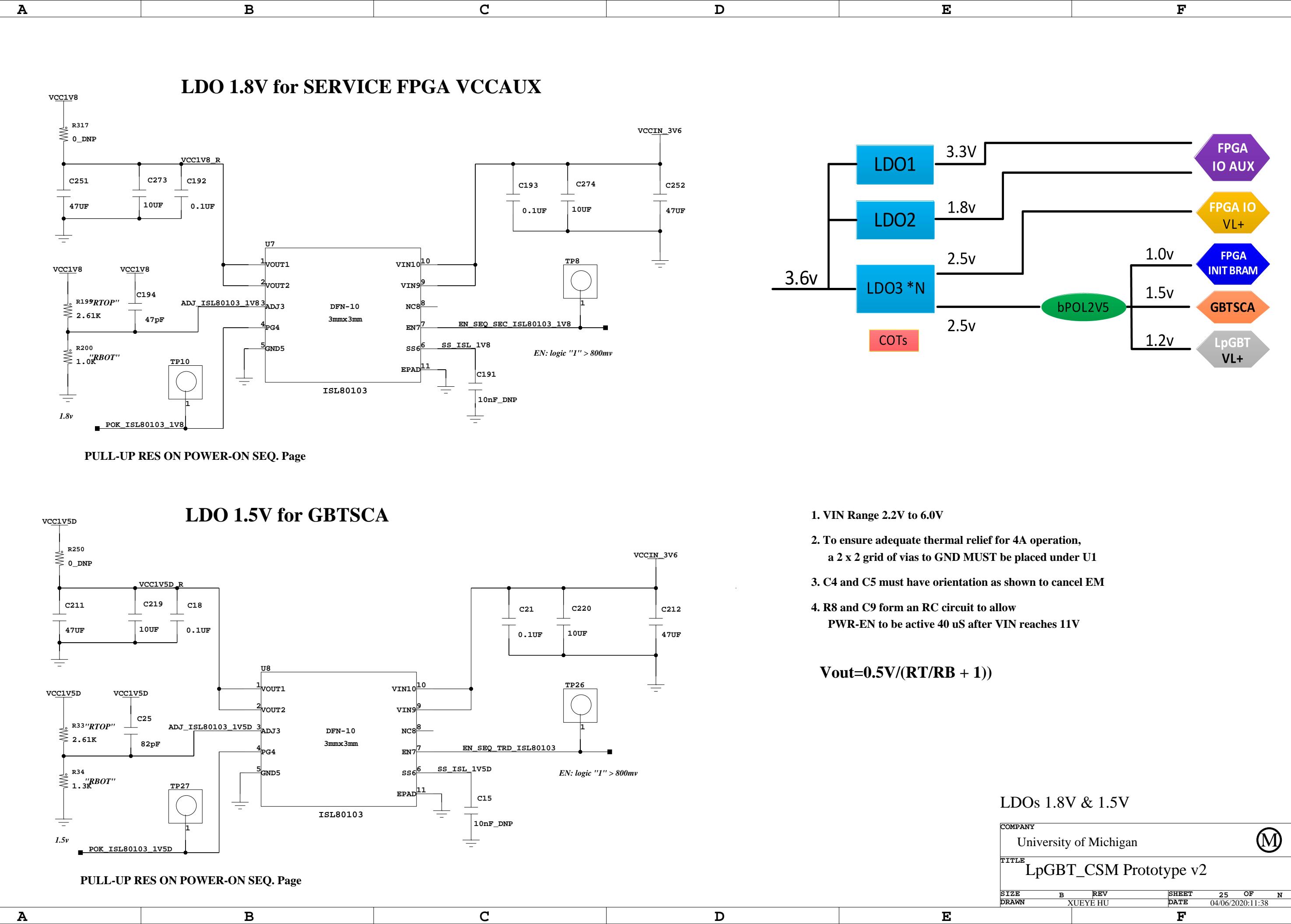
LDOS 3.3V & 2.5V

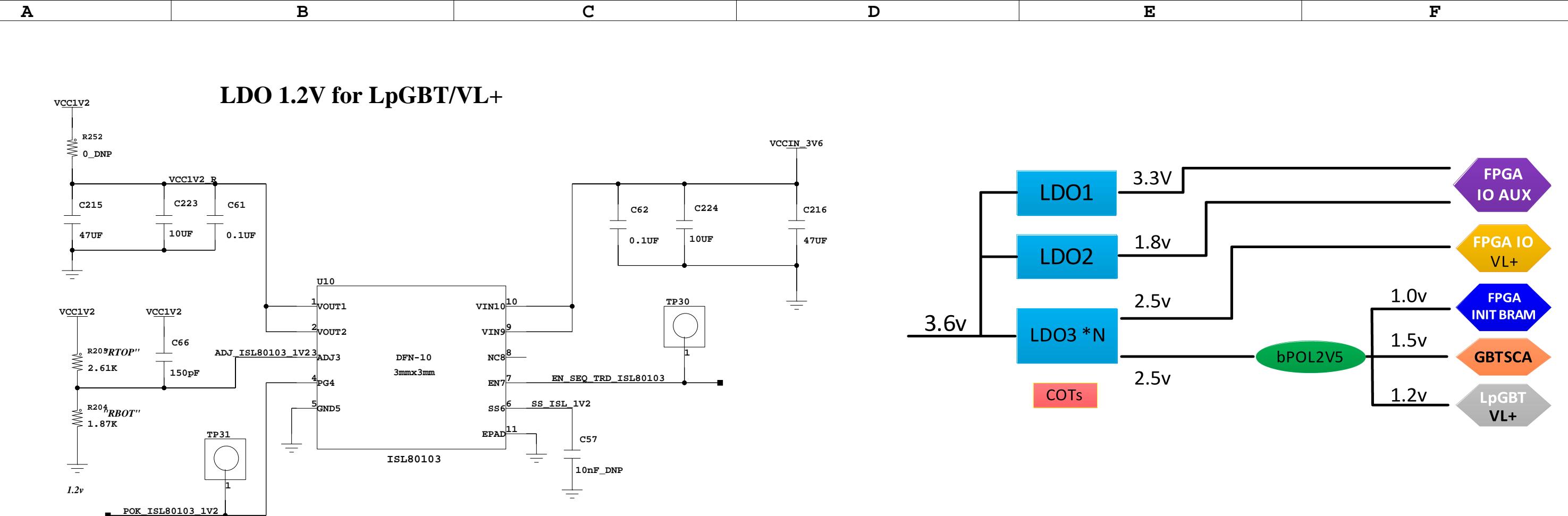
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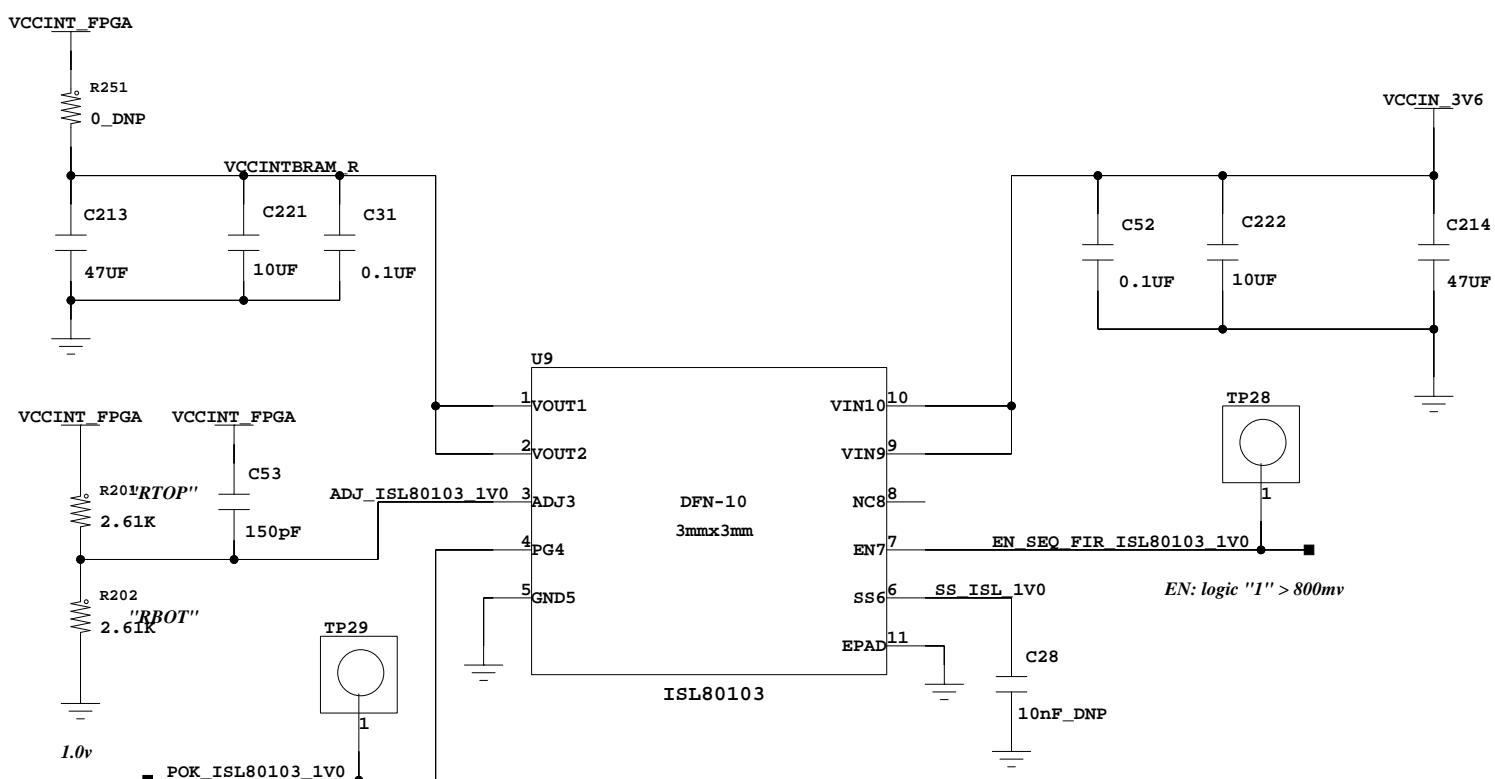
LpGBT_CSM Prototype v2

SIZE	B	REV	SHEET	24	OF	N
DRAWN	XUEYE HU		DATE	30/05/2020:12:26		





LDO 1.0V for SERVICE FPGA VCCINTBRAM



PULL-UP RES ON POWER-ON SEQ. Page

1. VIN Range 2.2V to 6.0V
2. To ensure adequate thermal relief for 4A operation,
a 2 x 2 grid of vias to GND MUST be placed under U1
3. C4 and C5 must have orientation as shown to cancel EM
4. R8 and C9 form an RC circuit to allow
PWR-EN to be active 40 uS after VIN reaches 11V

$$V_{out} = 0.5V / (R_T / R_B + 1)$$

LDOS 1.2V & 1.0V

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TITLE
LpGBT_CSM Prototype v2

SIZE B REV SHEET 26 OF N
DRAWN XUEYE HU DATE 12/05/2020:16:32

A B C D E F

FPGA Power-on Sequence

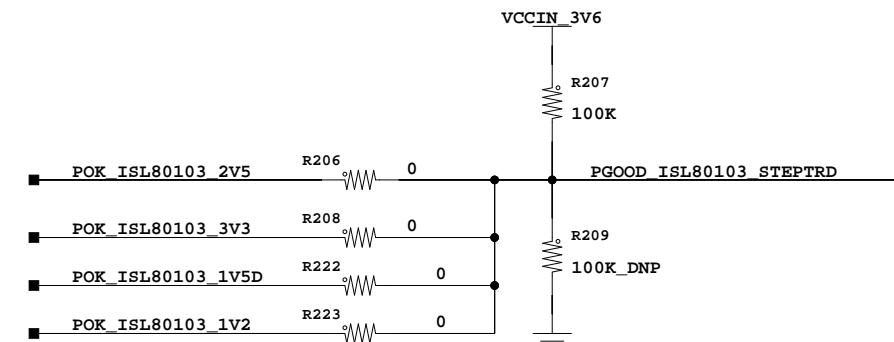
LDO ISL80103: PGOOD, En: 0V-6V
EN TH 800mV

BPOL2V5: PGOOD, En: 0V-2.5V
EN TH 850mV

Pre-stage: Always ON LDO 2.5V FOR BPOL INPUT

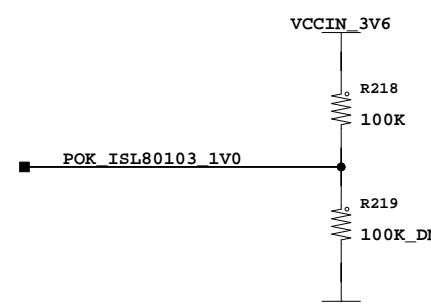
First Stage

EN 1V0 VCCINT VCCBRAM



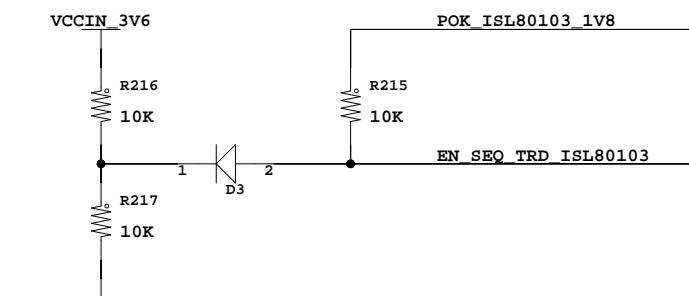
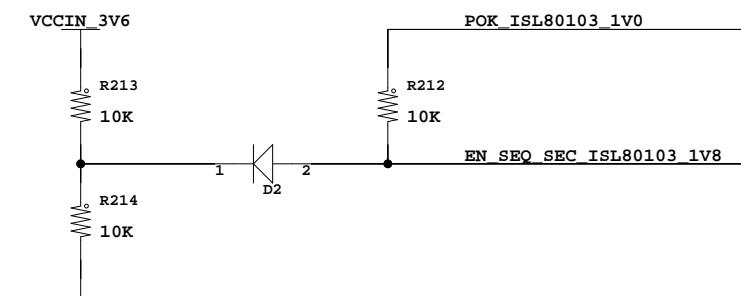
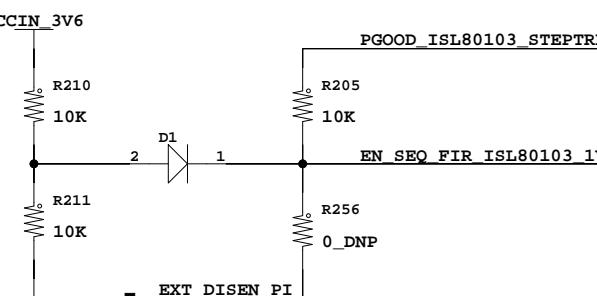
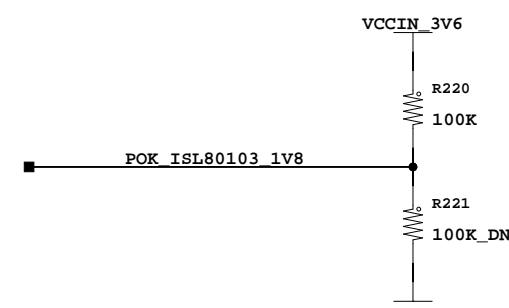
Second Stage

EN 1V8 VCCAUX

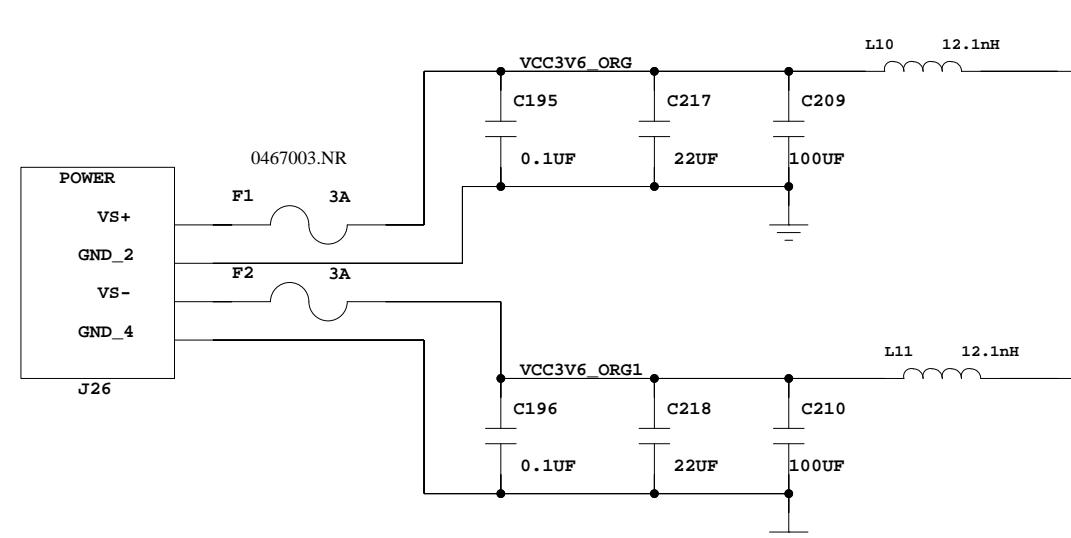


Third Stage

EN 1V2, 1V5D, 2V5, 3V3



Power connector



L29, L30 need to be removed when attached to CSM Mother board
3.6V POWER will get from there

POWER ON SEQ. & CONNECTOR

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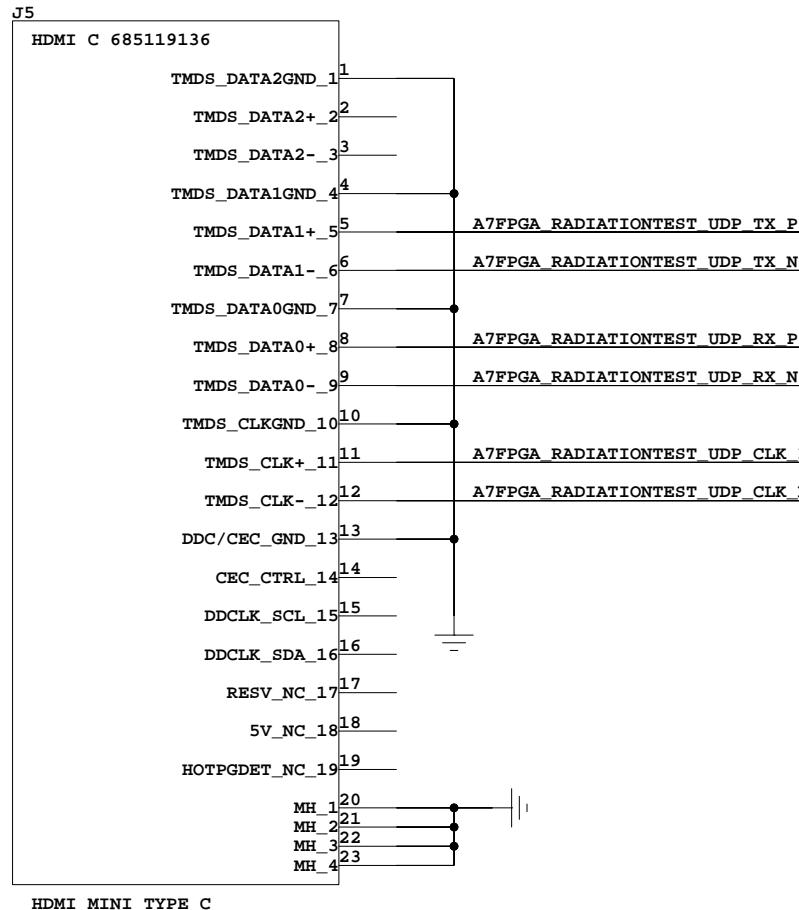
TITLE
LpGBT_CSM Prototype v2

SIZE B REV 27 OF N
DRAWN XUEYE HU DATE 12/05/2020:16:33

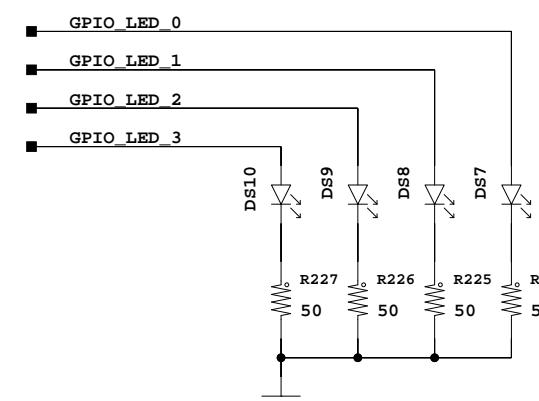
A B C D E F

A**B****C****D****E****F**

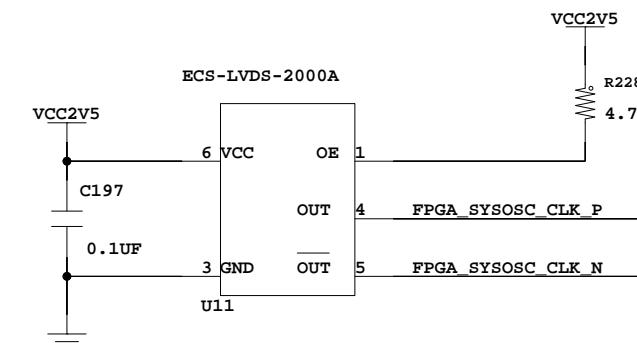
FPGA ELINK TEST PORT



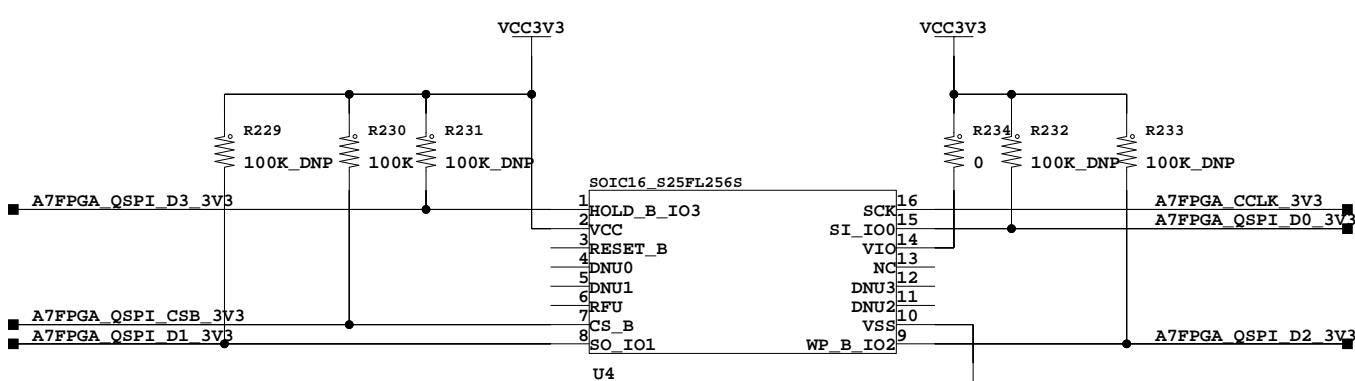
LED INDICATION FOR A7



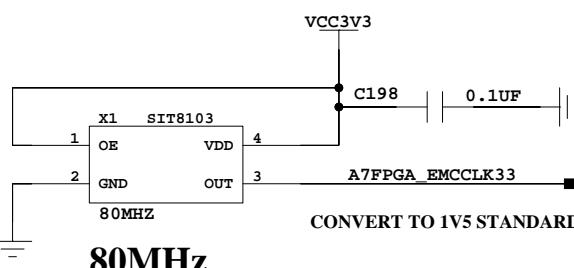
200MHz OSC FOR A7



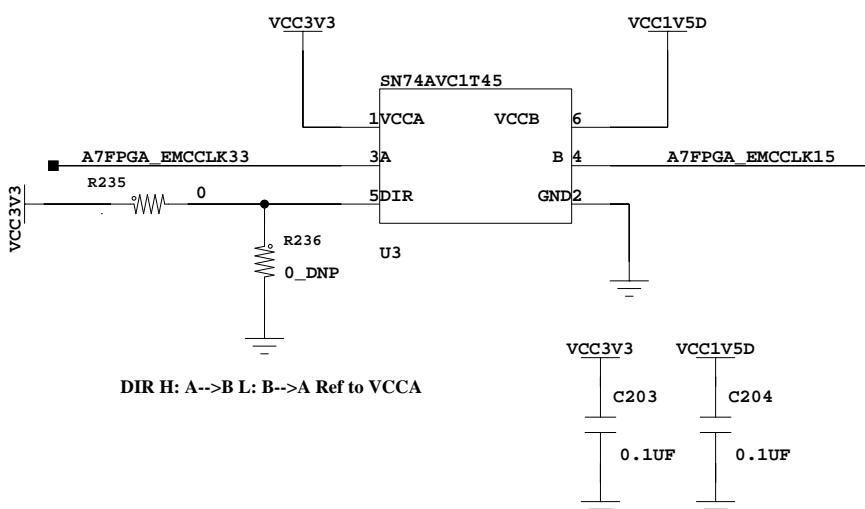
SPI FLASH



OSC FOR CONFIG



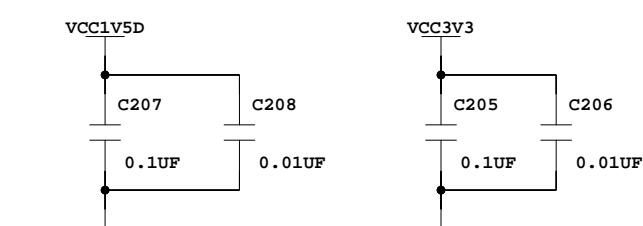
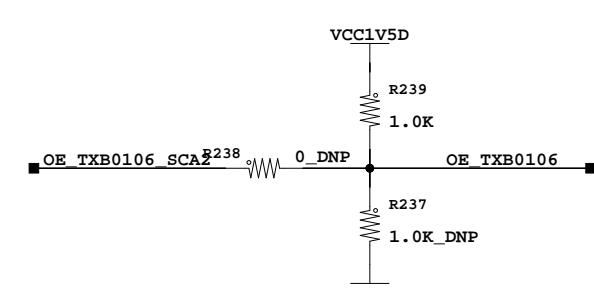
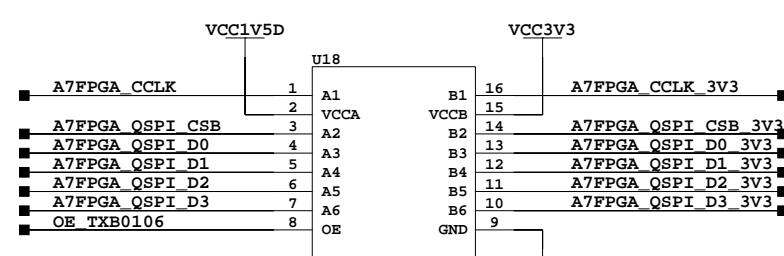
80MHz



DIR H: A-->B L: B-->A Ref to VCCA

CLK Data Trace Length Difference +150mil

NEED AUTO BI-DIR VOLT TRANSLATOR: TXB0104/LSF0204D



FPGA TEST FLASH, OSC, ELINK

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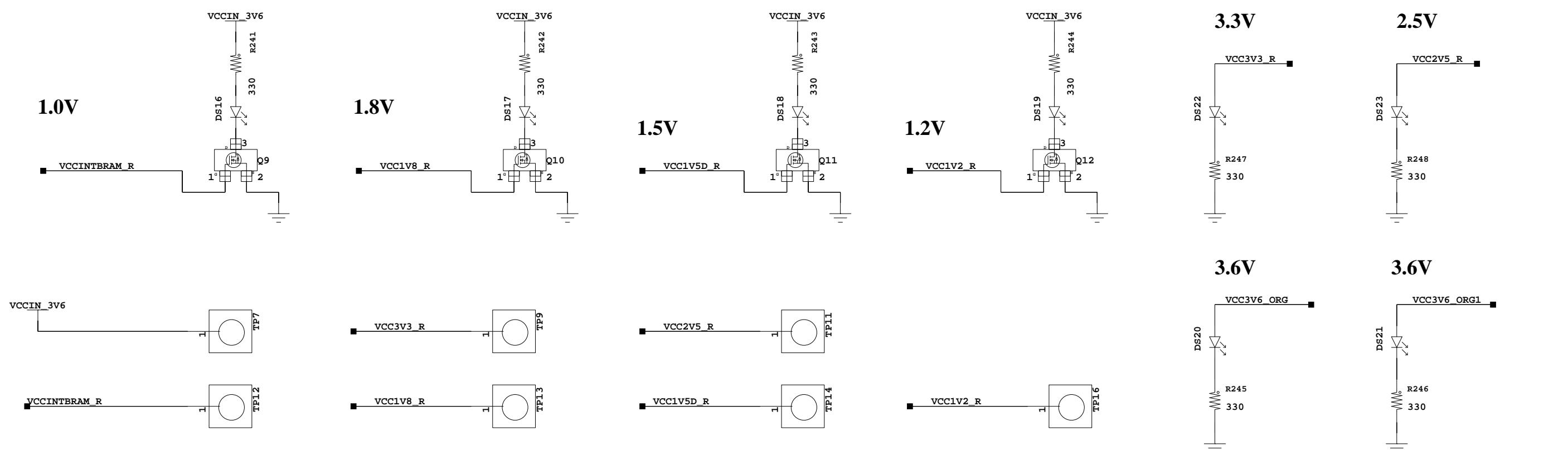


TITLE
LpGBT_CSM Prototype v2

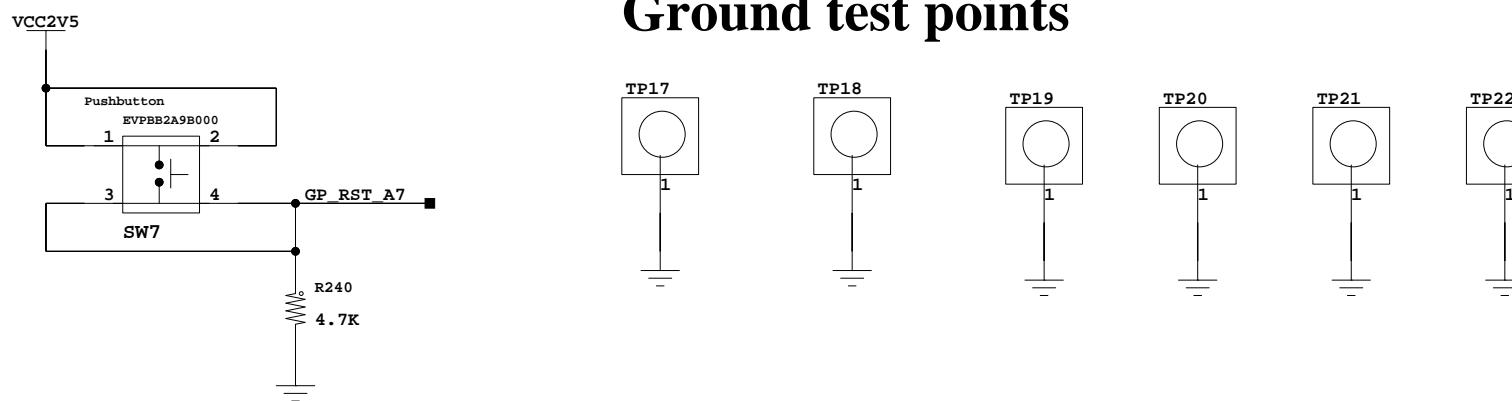
SIZE B REV SHEET 28 OF N
DRAWN XUEYE HU DATE 01/06/2020:22:35

A**B****C****D****E****F**

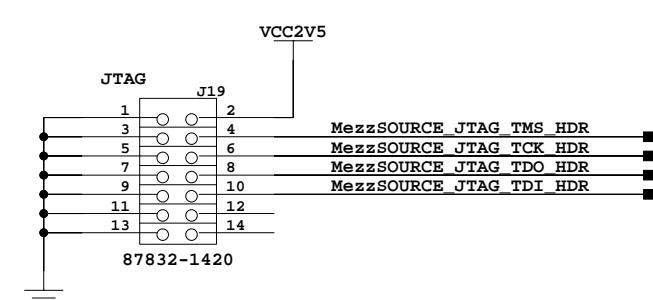
Voltage Indication



Ground test points



JTAG CONN. FOR MEZZ JTAG SOURCE



FPGA TEST POINTS

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TITLE
LpGBT_CSM Prototype v2

SIZE B REV E SHEET 29 OF N
DRAWN XUEYE HU DATE 17/05/2020:15:09