**Project Title**

# Implementation of 12 Hour clock with AM/PM indicator


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**Problem Statement**

Design a set of counters suitable for a 12-hour clock system with an AM/PM indicator. These counters will be driven by a high-frequency clock signal (clk) and will be incremented by one every time a pulse is received on the 'ena' input, indicating a one-second interval. A 'reset' input will be used to set the clock to 12:00 AM. The 'pm' signal will be 0 for AM and 1 for PM. The counters include 'hh' for hours, 'mm' for minutes, and 'ss' for seconds, each represented by two Binary-Coded Decimal (BCD) digits. It's important to note that the reset operation takes precedence over the enable operation and can occur even when the enable signal is not active.

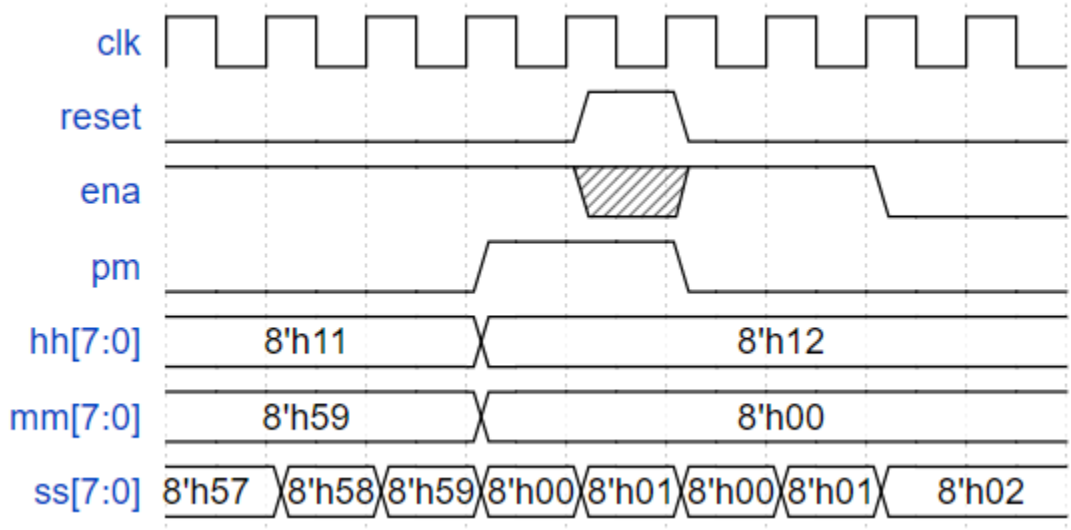
To provide clarity on the operation, consider the following timing diagram which illustrates the transition from 11:59:59 AM to 12:00:00 PM, as well as the behavior of synchronous reset and enable signals.

# Module Declaration

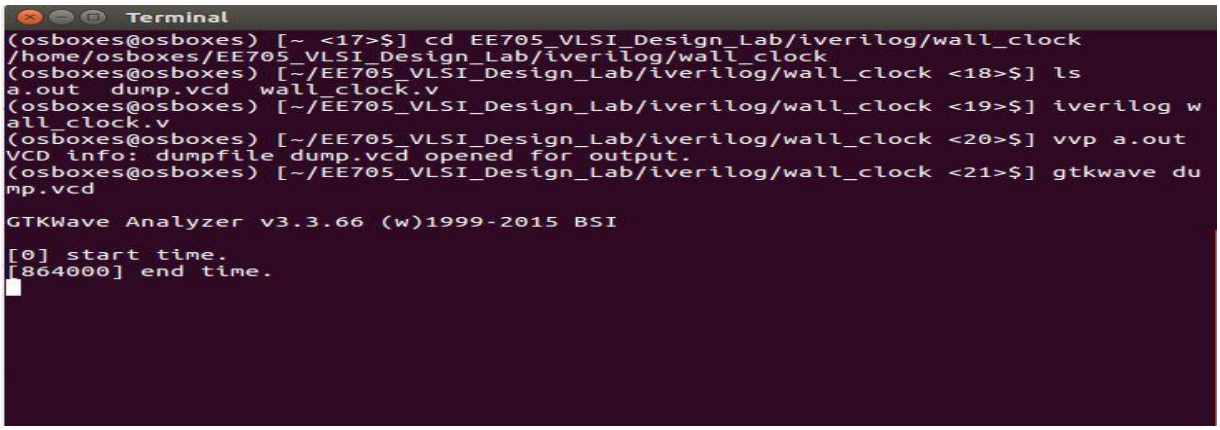
```
module top_module(

    input clk,

    input reset,

    input ena,

    output pm,

    output [7:0] hh,

    output [7:0] mm,

    output [7:0] ss);
```

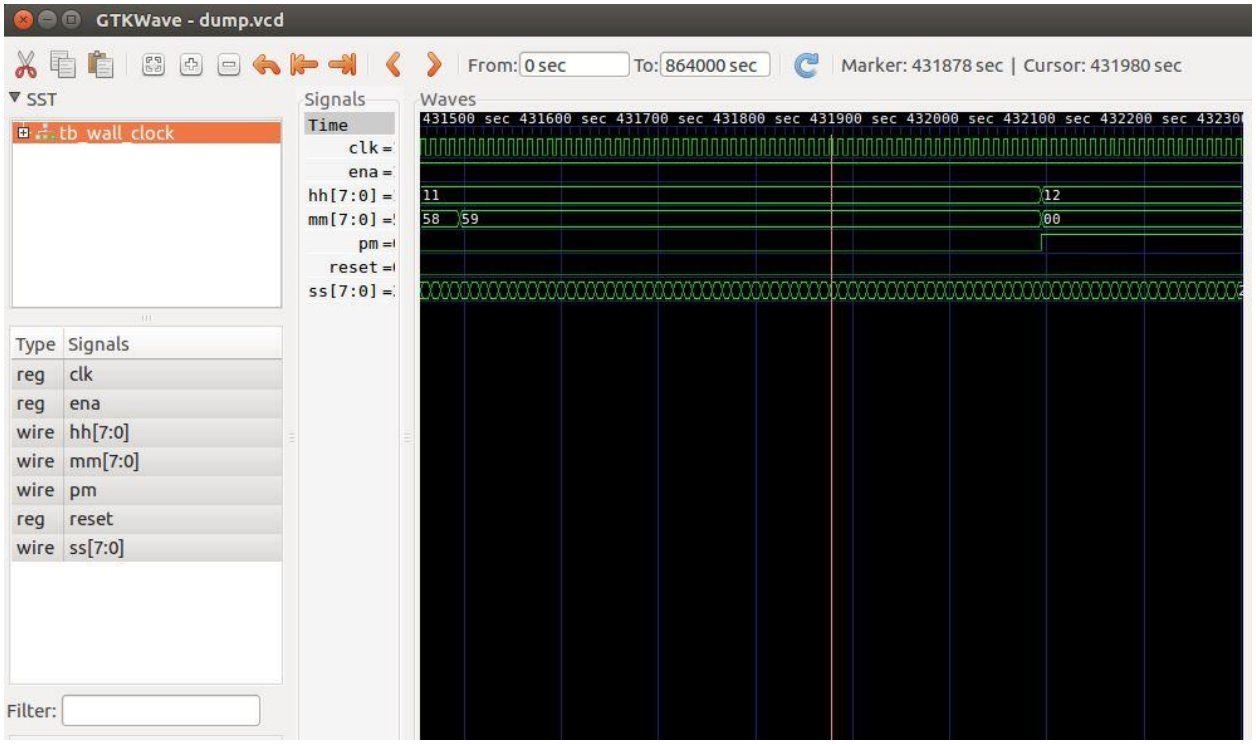
**Note:**

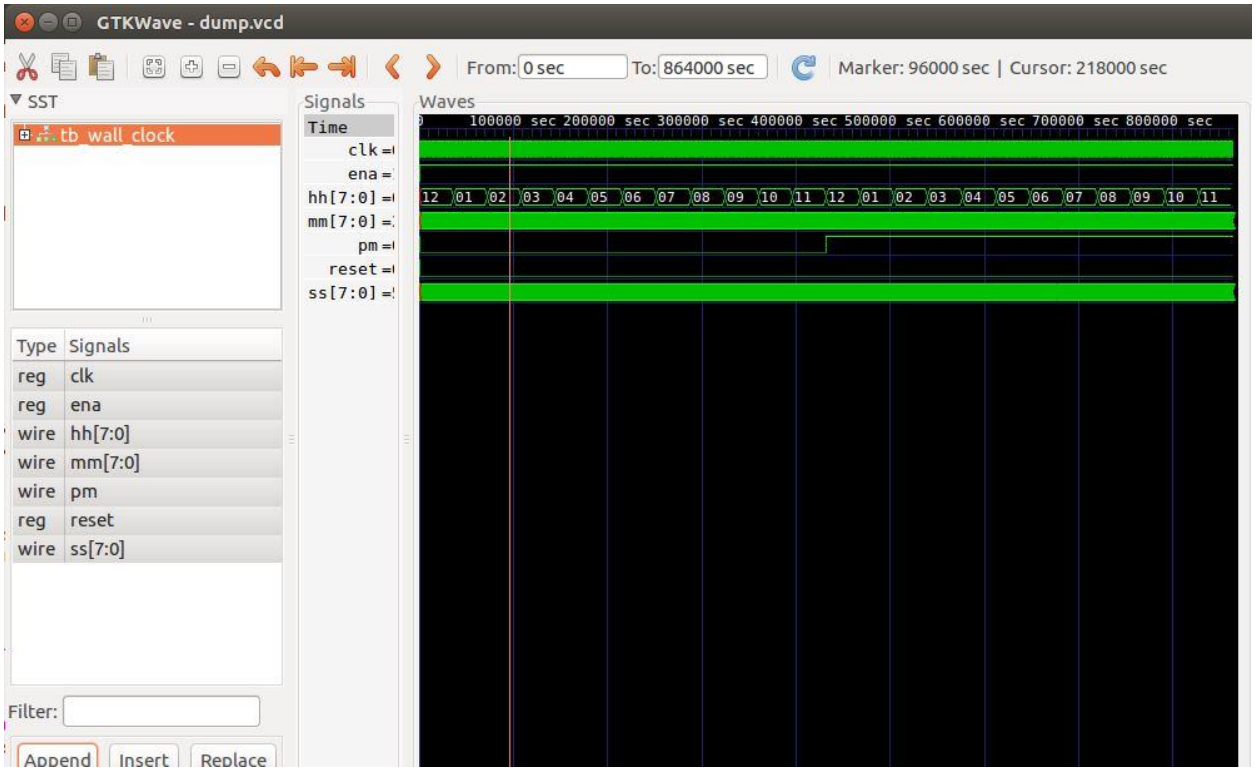
In this clock system, the transition from 11:59:59 PM should result in advancing to 12:00:00 AM, and similarly, the transition from 12:59:59 PM should result in advancing to 01:00:00 PM. There is no representation for 00:00:00 in this context.

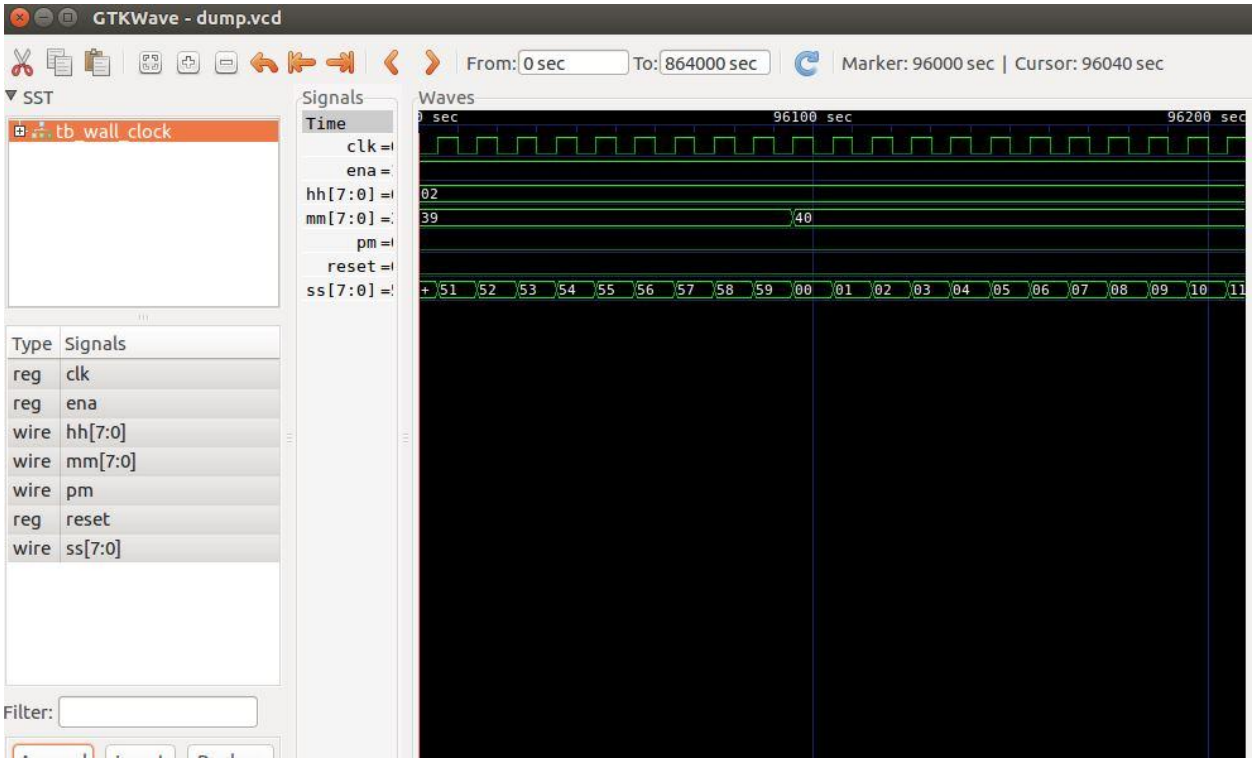


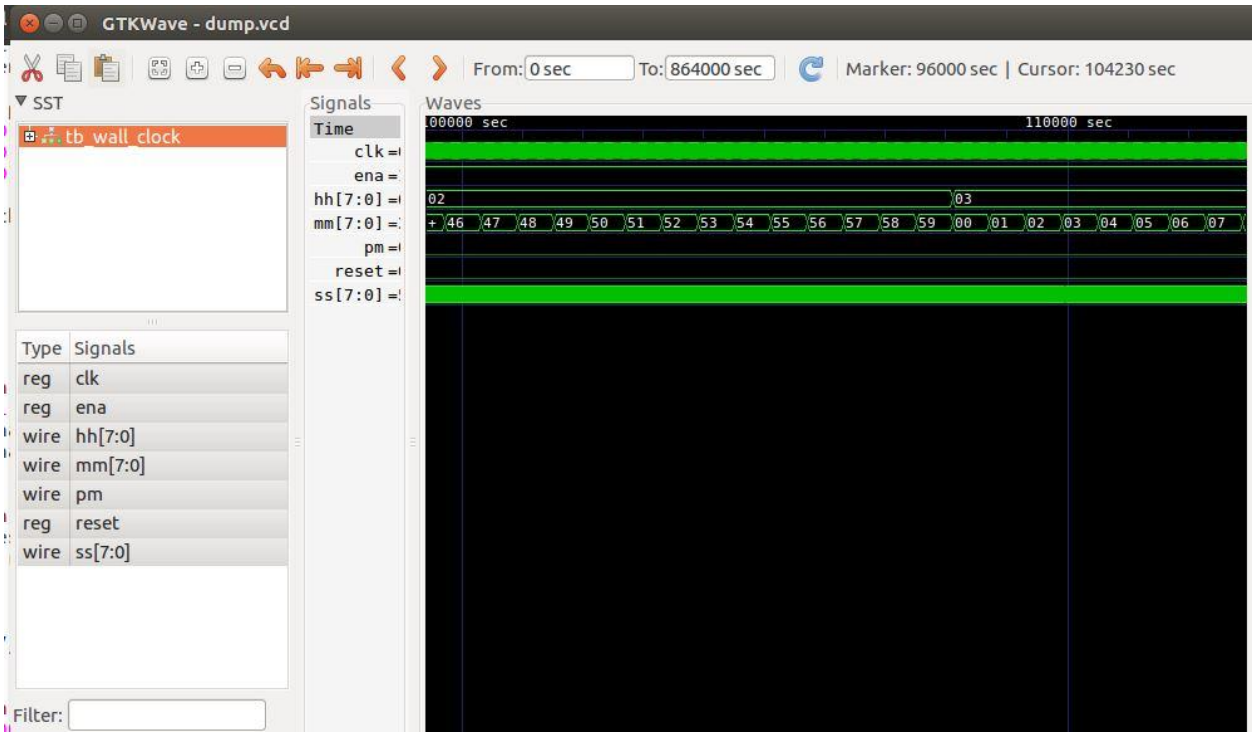

# RESULTS




GTKWave - dump.vcd
From: 0 sec
To: 864000 sec
Marker: 431878 sec | Cursor: 431980 sec
SST
tb_wall_clock
Signals
Time
clk
ena
hh[7:0]
mm[7:0]
pm
reset
ss[7:0]
Waves
431500 sec 431600 sec 431700 sec 431800 sec 431900 sec 432000 sec 432100 sec 432200 sec
11
12
58
59
00
Type Signals
reg clk
reg ena
wire hh[7:0]
wire mm[7:0]
wire pm
reg reset
wire ss[7:0]
Filter:


GTKWave - dump.vcd
From: 0 sec
To: 864000 sec
Marker: 96000 sec | Cursor: 218000 sec
SST
tb_wall_clock
Signals
Time
clk
ena
hh[7:0]
mm[7:0]
pm
reset
ss[7:0]
Waves
100000 sec 200000 sec 300000 sec 400000 sec 500000 sec 600000 sec 700000 sec 800000 sec
12 01 02 03 04 05 06 07 08 09 10 11 12 01 02 03 04 05 06 07 08 09 10 11
Type Signals
reg clk
reg ena
wire hh[7:0]
wire mm[7:0]
wire pm
reg reset
wire ss[7:0]
Filter:
Append
Insert
Replace


GTKWave - dump.vcd
From: 0 sec
To: 864000 sec
Marker: 96000 sec | Cursor: 96040 sec
SST
tb_wall_clock
Signals
Time
clk
ena
hh[7:0]
mm[7:0]
pm
reset
ss[7:0]
Waves
96100 sec
96200 sec
02
39
40
51 52 53 54 55 56 57 58 59 00 01 02 03 04 05 06 07 08 09 10
Type Signals
reg clk
reg ena
wire hh[7:0]
wire mm[7:0]
wire pm
reg reset
wire ss[7:0]
Filter:


GTKWave - dump.vcd
From: 0 sec
To: 864000 sec
Marker: 96000 sec | Cursor: 104230 sec
SST
tb_wall_clock
Signals
Time
clk
ena
hh[7:0]
mm[7:0]
pm
reset
ss[7:0]
Waves
110000 sec
02
03
46 47 48 49 50 51 52 53 54 55 56 57 58 59 00 01 02 03 04 05 06 07
Type Signals
reg clk
reg ena
wire hh[7:0]
wire mm[7:0]
wire pm
reg reset
wire ss[7:0]
Filter: