Single Chip Wi-Fi & Bluetooth Receiver

George Moustakos, Gabriel Ronan

University of Michigan - Ann Arbor, College of Engineering

EECS 411 F20: Microwave Circuits I

Dr. Amir Mortazawi, Wenhao Peng, Suhyun Nam

Submission Date: 12/18/2020

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Introduction

In our modern world, we require fast and reliable communication standards, and we need communication engineers to be intimately familiar with them. This will allow us to achieve better reliability and to develop faster protocols to handle an ever increasing amount of information being sent and received. However, this would all be for nought if the hardware designed for receiving and sending these signals through the electromagnetic spectrum is not custom built for this purpose. Fortunately, receivers everywhere are not scraped together from leftover parts, but are rigorously designed and tested for the fastest and most efficient receiving and transmission of signals. It is for this reason that we decided to make our final project for our Microwave Circuits class a dual Wi-Fi and Bluetooth receiver, as to make us familiarized with the hardware requirements for each of these communications schemes. We also chose these two protocols specifically to share the same chip space, since we discovered that the lower Wi-Fi architecture and the Bluetooth architecture actually operate at the same frequency of 2.4 GHz, and by designing a chip to receive both of these signals, we can learn how the different encryption of these signals can vary drastically and how important it is to build the individual components of each architecture specifically for the communication scheme at hand. We also picked these two standards, since they are the most utilized in modern communication systems. Bluetooth boasts the ability to remove wires for nearby objects, such as computer peripherals and audio devices, and thus has a much lower effective range as a result. Wi-Fi offers a much higher range and much higher data rates than Bluetooth, but has a higher production cost and energy usage.

Requirements

As stated earlier, even though the two wireless standards operate at the same frequency, they actually have quite different requirements, and need components individually designed for each. For Bluetooth we will use a data rate 1 Mbit/s, and for Wi-Fi we will use the 11 Mbit/s data rate. This is important, as the data rate utilized affects the required signal and noise requirements. The most important characteristics when designing front end radio frequency components are the noise generated by the system, the sensitivity of the receiver, and the ability of the components to reject harmonic signals generated by amplifying the input signal. This last requirement is important because of how signals operate in the frequency domain, as second and third order harmonic frequencies can heavily impact how the final signal is converted from the frequency domain into a digital signal. The noise of the system is categorized as the Noise Figure (NF) of the system, a term that incorporates all the noise generated by the subcomponents into one easy value, that can be them compared to other receiver designs. NF is calculated as noise figure is calculated as $NF_{system} = Minimum\ Sensitivity\ + 174\ dBm/Hz\ -\ SNR_{min} - 10log(BW)$, where SNR represents the Signal to Noise Ratio and BW refers to the bandwidth of the filter used to reject other incoming signals. For Bluetooth, the minimum sensitivity required is -70 dBm, and for Wi-Fi the minimum sensitivity is -76 dBm. Thus, the required system NF of Bluetooth is 21 dB and for Wi-Fi the system NF is 10.6 dBm. Finally, the Input Third Order Intercept Point (IIP3) can be calculated as $IIP3 = P_{int} + (P_{int} - P_{Sig} + SNR_{req} + M)/2$, where M refers to the system margin, P_{int} refers to interferer power, and P_{sig} is the power of the desired signal. Thus, we get an IIP3 of -17.5 dBm for Bluetooth and -22.5 dBm for Wi-Fi. All of the required values are tabulated before in Table 1.

	Bluetooth	Wifi - 2.4 GHz
Frequency Range	2.4-2.43835 GHz	2.4-2.4835 GHz
Bandwidth (BW)	1 MHz	22 MHz
Channel Spacing	1 MHz	5 MHz
Number of Channels	79	13
Modulation	GFSK	DBSK, DQPSK, QPSK (depending on Mbps)
Minimum Sensitivity	-70 dBm	≥-76 dBm
Maximum Sensitivity	-20 dBm	-10 dBm
Quality of Service	Bit Error Rate = 10^-4 = 0.1%	Frame Error Rate = 8*10^-2, (BER = 10^-3)
Input Noise	-114 dBm	-100.6 dBm
Input SNR	44 dB	24.6 dB
Required SNR	23 dB	14 dB (11 Mbps)
System Noise Figure	21 dB	10.6 dB (11 Mbps)
IIP3	-17.5 dBm	-22.5 dBm (11 Mbps)
IIP2	12 dBm	10.5 dBm (11 Mbps)

Table 1. Total Wi-Fi and Bluetooth Requirements of Dual Receiver.

Architecture

The three most common receiver architectures are super heterodyne, low-intermediate frequency (Low-IF), and direct conversion receiver. The most commonly implemented architecture is super heterodyne receivers, as they provide very good noise and selectivity parameters for designers to choose to base their model around. However, to implement this architecture, it would be required to have many more mixers and filters on the chip, greatly increasing the sources of noise and the overall complexity of the system. The low-IF receiver architecture has the special advantage of using a low frequency intermediate frequency (usually around 1-2 MHz), which allows for much less complex filters and amplifiers, and the low frequency greatly reduces the noise generated by the secondary components. The direct conversion receiver is a very simple design, and doesn't require the image reject filters that a super heterodyne receiver would require, but it is prone to leakage of the local oscillator into the incoming signal, and has issues related to the noise generated by its components.

Since Bluetooth and Wi-Fi standards are on the same frequency spectrum, we assume that we can share the same receiving antenna for both ports, lowering complexity and the need to learn how to calibrate for two different frequencies. The difficulties lie in the fact that Bluetooth and Wi-Fi have different bandwidths and thus different blocks needed to decode the signal. For the Wi-Fi receiver, we are implementing Direct Conversion Receiver Architecture. For the Bluetooth implementation, we will be using Low-IF Architecture. After researching both implementations, we saw that we can implement a Low-IF Receiver Architecture or DCR Architecture for both, but the benefits of implementing DCR for Bluetooth wouldn't be worth the trouble of designing more stringent and precise components.

The signal diagram of our receiver is shown below in Figure 1, to show how the signal is propagated from the incoming antenna to the analog to digital converter.

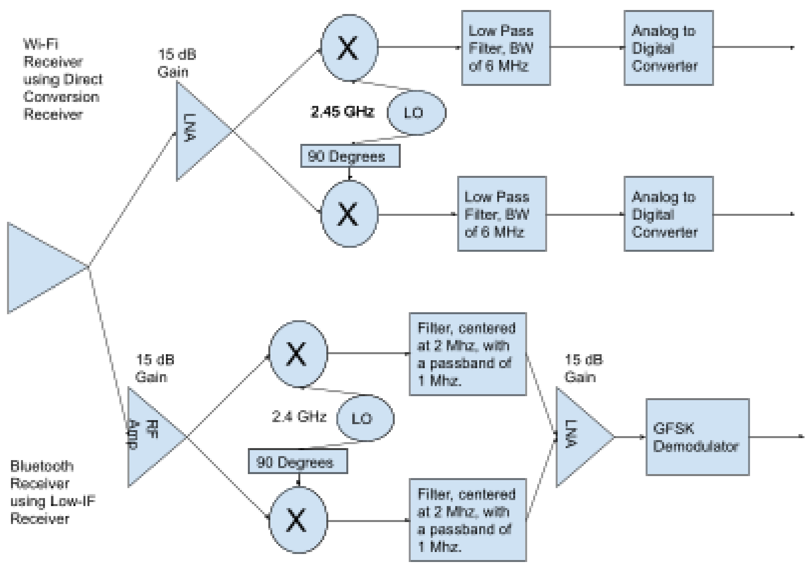

Figure 1. Block diagram of Dual Wi-Fi/Bluetooth Receiver.

Circuit Design

Low Noise Amplifier

Each receiver half of the dual receiver requires an RF amplifier before mixing takes place, as the input signals will be subjected to the subsequent filter and further conversion to digital signals, each having a loss associated with them. Thus, it was decided in the design phase to use amplifiers each with a gain of 15 or more dB at the frequency of 2.4 GHz as to offset any further loss, and to create a stronger signal at the desired signal frequency. Due to the nature of Wi-Fi and Bluetooth having the same frequency, the same RF Amplifier could be used in both portions, saving time and complexity of the system.

The amplifier design starts with a transistor with good scattering parameters at the frequency 2.4 GHz, which is followed by tests for stability, and ending with the design of a matching circuit to increase the gain to a favorable amount. For our design, we used ADS to simulate the S-Parameters of transistors archived in ADS, under the S-Parameter Vendor Kit folder. There are hundreds of transistors in this library, and after researching a good deal of them, we chose to use the HMF0300 MESFET device, which has S11 < 1 and S12 < 1, both of which are required for certain assumptions in the microwave amplifier design steps, as outlined in Chapter 12 of Pozar. We then calculated the K, delta, and mu stability values of this transistor, as well as using ADS to simulate them for us, and found them all to be within the specified range required for a stable amplifier. After obtaining the Γ_S and Γ_L of the transistor based off of its S-Parameters, we plotted each one on an impedance/admittance Smith Chart, as well as plotting the stability circles and made sure no reflection coefficient was within the unstable zone. After doing so, we found the requisite transmission line lengths for the shunt and series components on each side of the device to create the matching network that would increase overall gain and lower overall reflections back to the source from the load, making sure all available power was delivered. These values were found, and imported into ADS, where from we used the LineCalc tool to transform the transmission lines into microwave strip lines that expressed the same behavior at 2.4 GHz. The substrate chosen has the properties of height (H) = 30 mil, dielectric constant (E_r) = 3.5, conductivity (cond) = 5.8e7, conductor thickness (T) = 0.67 mil, dielectric loss tangent (TanD) = 0.0016. The subsequent design of MLIN's of various widths and heights was simulated to have a gain of 13 dB, lower than the required design gain. However, when simulating the transistor in ADS, we used a tool called Max Available Gain (MAG) and found the HMF0300 MESFET had a MAG value of 18 dB. Knowing this, we used the optimization tool found in ADS and used the four variables of the MLIN lengths as variables to be swept over to obtain a gain of at least 15 dB at 2.4 GHz. The final values of the microstrip lines of the LNA were found and the gain of the RF LNA was calculated to be 16.566 dB at 2.4 GHz. As stated earlier, noise was a big consideration when choosing the architecture to be implemented for each standard, and as such we designed the amplifier to have a relatively low noise level. Due to the close incoming frequency of the Wi-Fi and Bluetooth branches, we decided to use the same RF LNA for both portions.

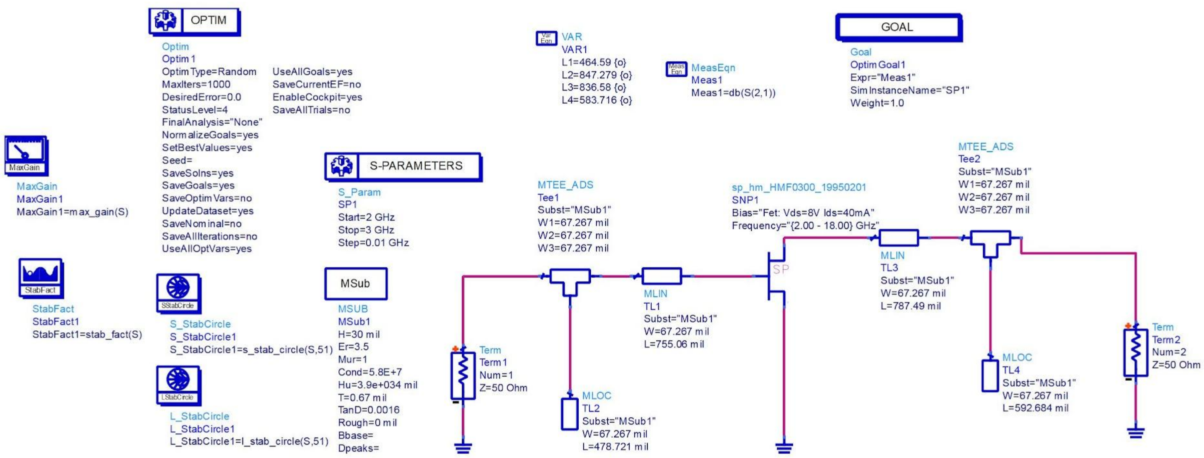

Figure 2. Schematic of RF LNA on ADS with Microstrip Components.

As shown in Figure 2, we have microstrip lines instead of generic transmission lines, as to provide the requisite impedance at the incoming frequency of amplification. We also relied on the ADS simulation tools to show us how the amplifier's stability, noise, and gain would be impacted by any change in impedance, frequency, or power.

Phase Shifter

The quadrature hybrid, or the branch line hybrid in microstrip form, is a 3 dB directional coupler that produces a 90º phase difference between output signals of the through and coupled arms. With all ports matched, the power entering port 1 is evenly divided between ports 2 and 3. There is no power coupled to port 4 as it is isolated. This is ideal for creating the required 90º phase differences for our f_{LO} signals. For both Wifi and Bluetooth architectures, each f_{LO} signal must be split to be used as input to four separate mixers (two for Wifi, two for Bluetooth). To design the quadrature hybrid, we followed the geometry detailed in section 7.5 of Pozar, using f = 2.45 GHz. This design is used for both the Wifi and Bluetooth branches of the receiver, and its ADS design is shown below in Figure 3.

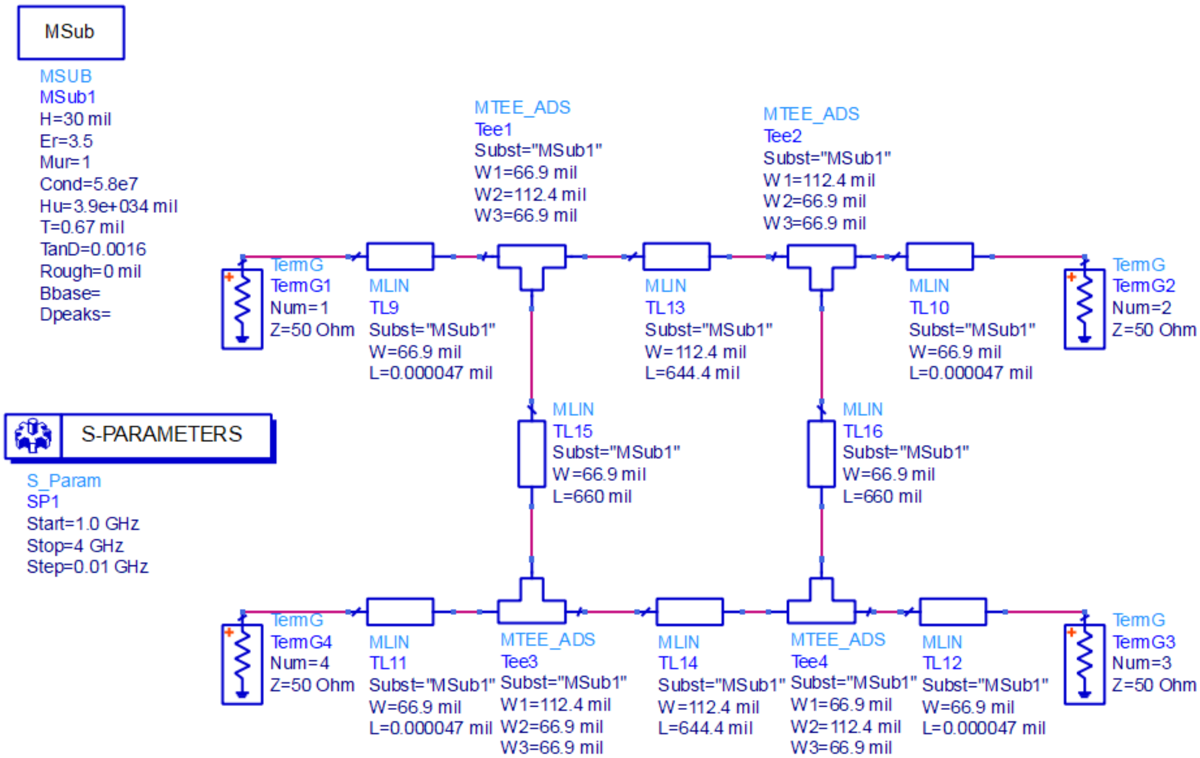

Figure 3. Schematic of Quadrature Hybrid Coupler on ADS with Microstrip Components.

Mixer

A single-ended double-balanced FET wideband mixer was chosen for its simplicity as well as ease of implementation and noise figure analysis.There are two input ports, one for the RF signal and one for the LO signal, and one output port for the RF signal. In our case, we want to down convert the RF signal to a low frequency of 2 MHz for both the Wifi and Bluetooth branches of the network. The Wifi and Bluetooth branches operate at frequencies of 2.45 GHz and 2.40 GHz, respectively, and so the LO signal input must be 2.448 GHz and 2.398 GHz. Any frequency components that lie outside the range of 2 MHz are attenuated by the low pass filter for the Wifi branch and the band pass filter for the Bluetooth branch. The final design of this mixer in ADS is shown below in Figure 4, where the variables Vgg and W1 were set to be 0.5 V and 2 mm respectively. The BSIM3 MOSFET (NMOS) model in ADS was used to create this mixer, and its default specifications are detailed in [1].

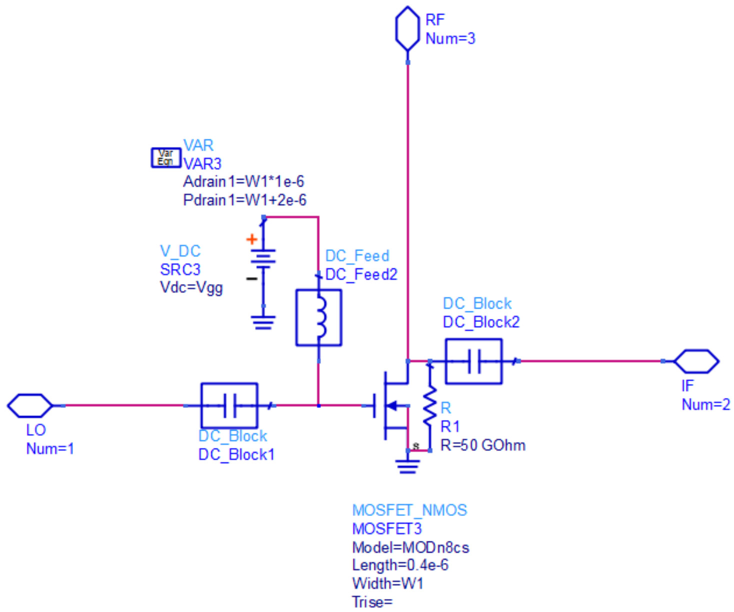

Figure 4. Schematic of Single-Ended FET Mixer in ADS.

Low Pass Filter

A 0.5 dB equal-ripple Chebyshev stepped-impedance low pass filter was designed with a cutoff frequency of 3 MHz and attenuation of at least 30 dB at 4 MHz. This allows us to select the desired channels for the Wi-Fi portion of the device. We chose to implement the filter using Cauer topology with N = 7 elements to comfortably reach 30 dB of attenuation and to allow more flexibility for optimization. We used Table 8.4 and Figure 8.27 of Pozar to achieve preliminary circuit results in ADS, and then further optimized inductor and capacitor values to reach our desired specifications more closely. The base equations we used to find capacitor and inductor values were $L_K^{'} = \frac{L_K Z_0}{\omega_c}$ and $C_K^{'} = \frac{C_K}{Z_0 \omega_c}$ respectively. This design of the Low Pass Filter is shown below in Figure 5, with shunt capacitors and series inductors.

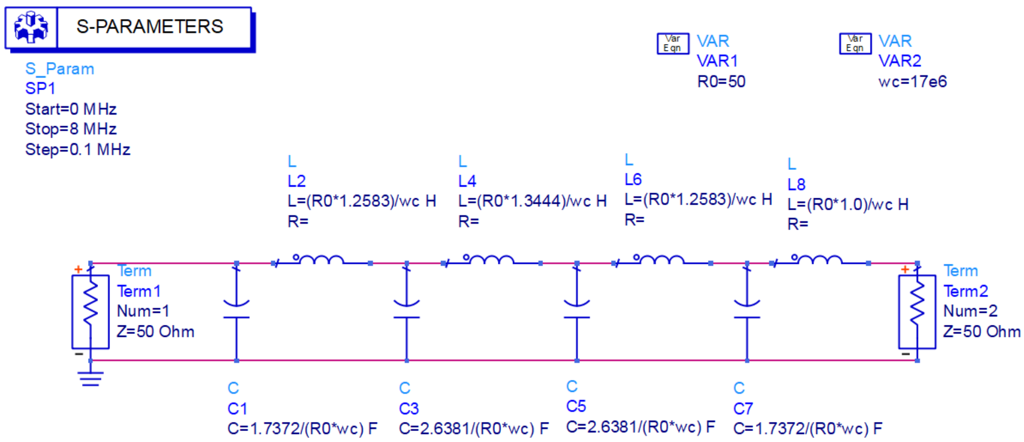

Figure 5. Circuit Diagram of Low Pass Filter utilized in Wifi Architecture.

Band Pass Filter

Due to our decision to implement a Low-IF receiver architecture for our Bluetooth portion, we need to design and test a band-pass filter to pass signals at f_0= 2 MHz, and reject out of band and image frequency signals. For this project, we used cascaded ladder networks of discrete elements of capacitors and inductors, due to the fact that we operate at low frequencies (less than 100 MHz) and thus don't experience the same parasitics that a microwave filter that uses the same elements would experience. We use this network to create the 0.5 equal ripple Chebyshev filter. To design this band pass filter, first we go through the design steps of the low pass filter, finding the out of band blocking decibel level, and then transforming the series inductance into a series LC circuit and the shunt capacitance is transformed into a shunt LC circuit. The equations we use for this are the series LC values $L_K^{'} = \frac{\Delta L_K Z_0}{\omega_0}$ and $C_K^{'} = \frac{1}{\Delta L_K Z_0 \omega_0}$for the series inductance L_K, and the shunt LC values $L_K^{'} = \frac{Z_0}{\omega_0 \Delta C_K}$ and $C_K^{'} = \frac{C_K}{\Delta Z_0 \omega_0}$for the shunt capacitance C_K, all centered at the frequency ω_0. We then simulate the circuit on ADS, changing the order of the network to see how the frequency response of the circuit changes. We do this to obtain the best response for the lowest order, as a higher order has more elements and thus more sources of noise. After all these steps were done, we obtained an N = 4, with the specific series LC and shunt LC circuit parameters shown below in Figure 6. This circuit has a designed center frequency of 2 MHz, and an effective bandwidth of 1 MHz.

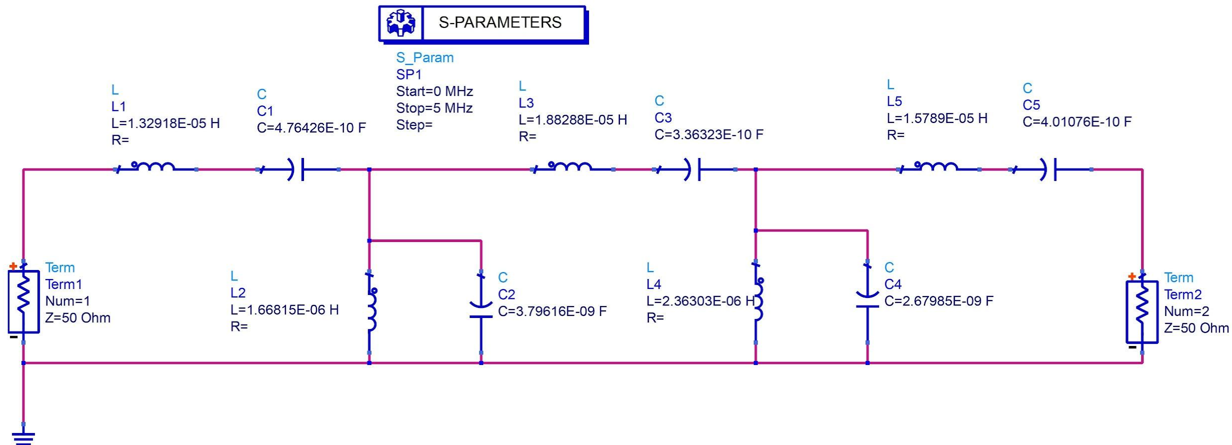

Figure 6. Circuit Diagram of Band Pass Filter utilized in Bluetooth Architecture.

Simulation Results

Low Noise Amplifier Simulation

The Gain and Noise Figure of the RF LNA used in the Bluetooth Architecture is shown in Figure 7. We can see that the gain at the incoming 2.4 GHz frequency is 16.5 dB, a little higher than the specified amount in the design proposal. We can also see that the noise figure of the LNA is extremely low, only at 0.073 dB, which means that the subsequent circuit components have a little more leeway to be less rigorously designed with consideration to noise generated.

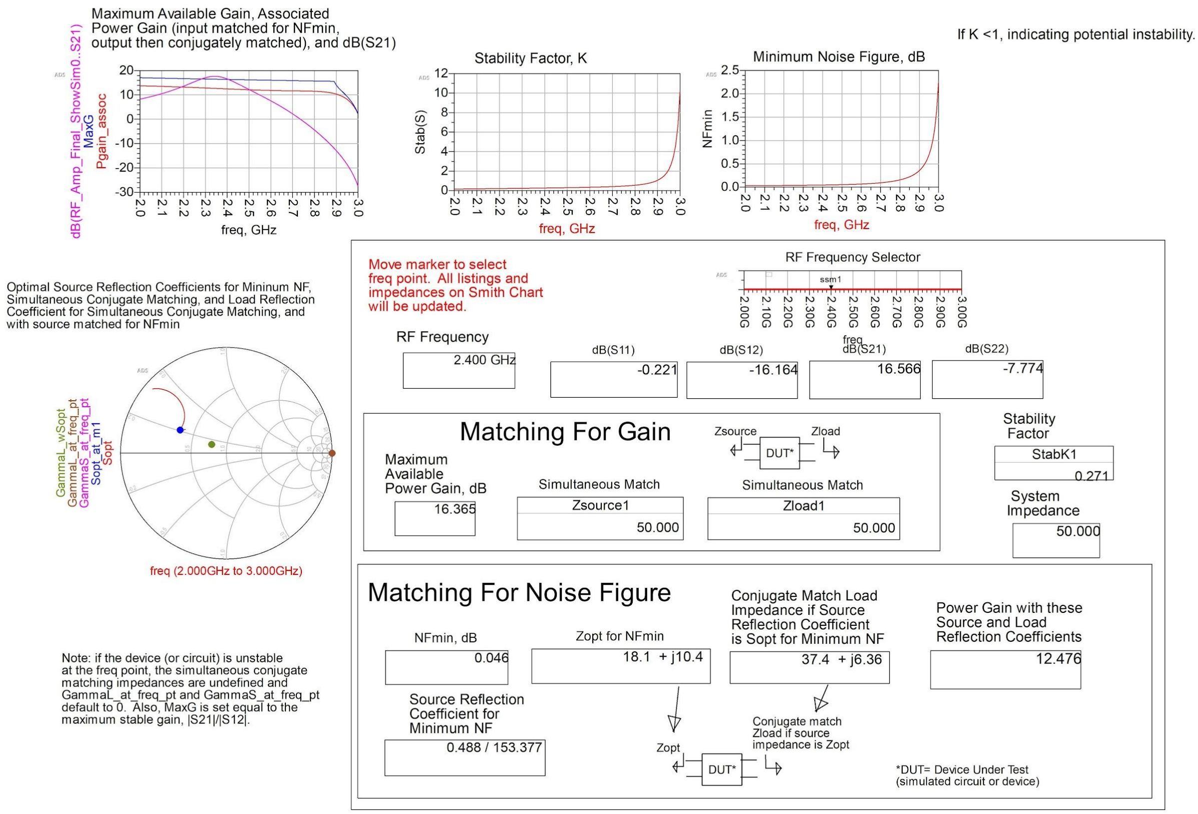

Figure 7. RF 2.4 GHz LNA Gain (Left) and Noise Figure (Right) Plot utilized in Bluetooth Architecture.

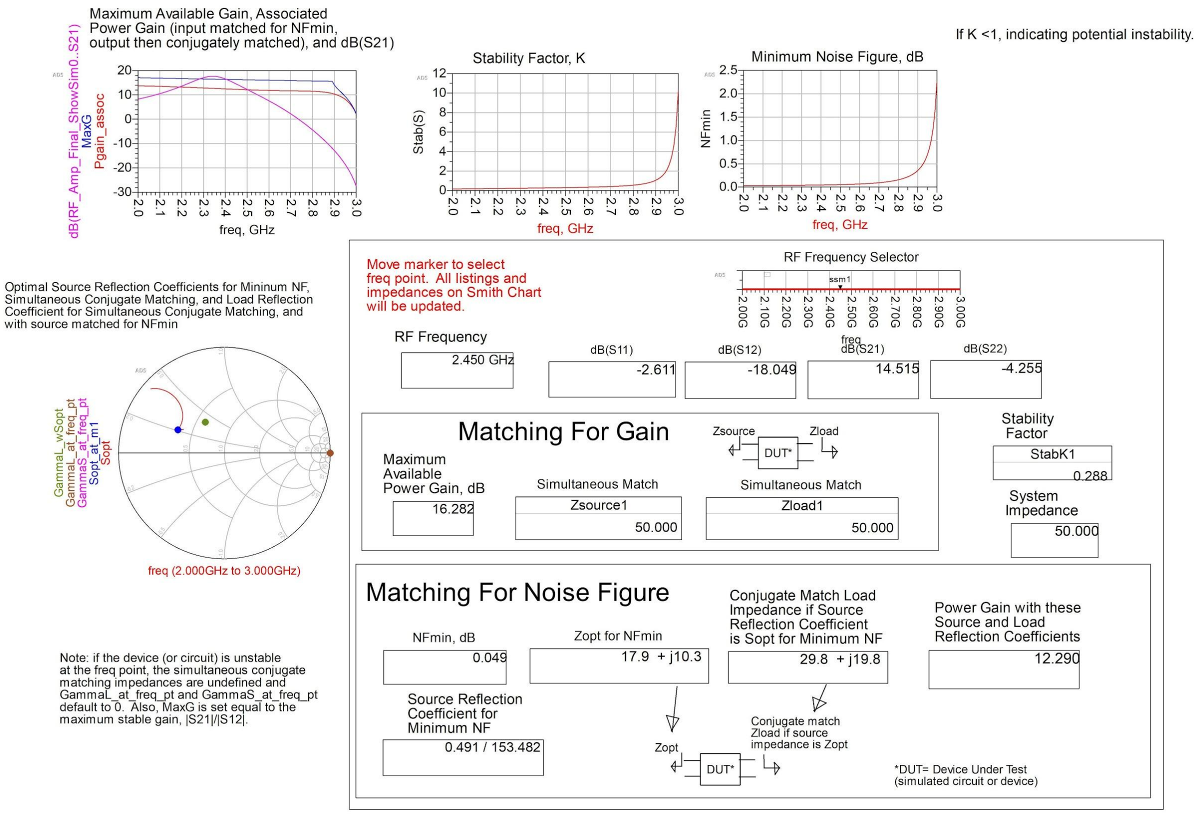

Figure 8. RF 2.45 GHz LNA Gain (Left) and Noise Figure (Right) Plot utilized in Wifi Architecture.

Due to the frequency of Bluetooth and Wi-Fi being only 0.05 GHz in difference, we were able to use the same RF LNA for both branches, with no changes necessary to the circuit matching networks. As shown in Figure 8, the amplifier that operates at 2.45 GHz has almost the exact same parameters as when it operates at 2.4 GHz, showing how our decision to use the same components is already paying off in lowering design and no need for optimization at a new frequency.

Phase Shifter Simulation

Figure 9 shows that an f_{LO} signal near either 2.400 GHz or 2.450 GHz can be effectively split into two separate output signals with a near 90º phase difference. Therefore this implementation can be used in both the Wifi and Bluetooth architectures.

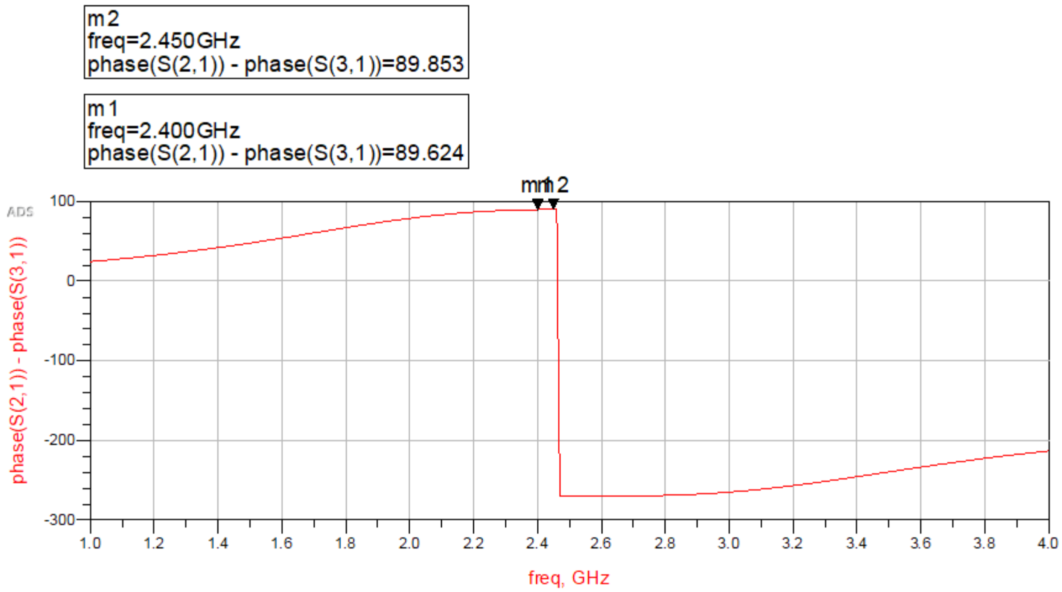

Figure 9. Phase Difference of Split Output Signals for Quadrature Hybrid Coupler.

Mixer Simulation

The mixer is thoroughly tested in ADS to analyze input and output spectrums, conversion gain, port-to-port Isolation, port impedances, reflection coefficients, all-sideband noise figure. We believed that this depth of analysis would allow us to tune our final design more precisely if the required specifications were not met. Notable results include a down conversion gain of -17.464 dB for an RF input of 2.45 GHz for the Wifi branch and a down conversion gain of -17.259 dB for an RF input of 2.40 GHz for the Bluetooth branch. Both of these results are reasonable for our purposes. Down conversion is what allows us to obtain the intended 2 MHz IF signal for both the Wifi and Bluetooth branches. The all-sideband noise figures for the Wifi and Bluetooth RF signals were 12.001 dB and 11.845 dB, respectively. These values are also reasonable for our purposes. The rest of the results are shown in Figures 11, 12, 14, and 15, while the ADS schematic setups are shown in figures 10 and 13. Note that the conversion gains shown in Figures 14 and 15 are the all-sideband conversion gains, and will be lower than their counterparts in Figures 11 and 12.

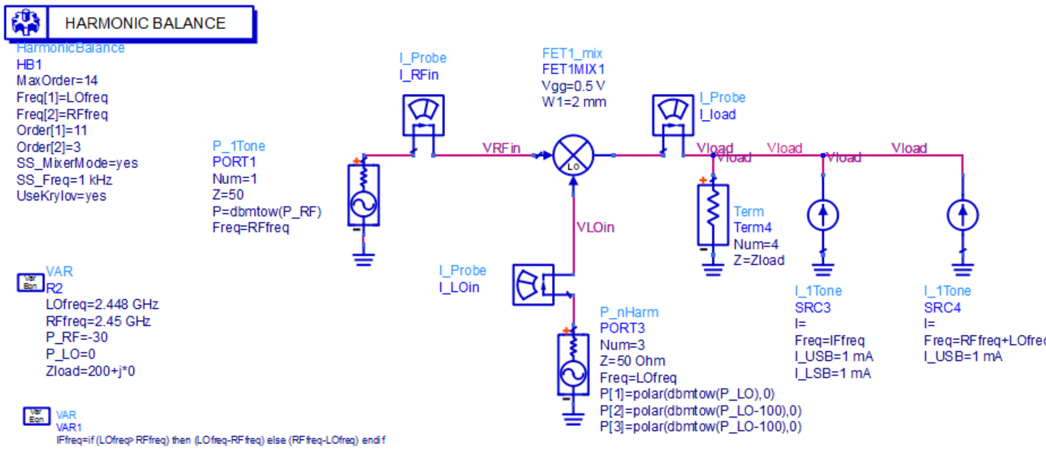

Figure 10. Circuit Diagram of Single Ended FET Mixer Spectral Test Setup.

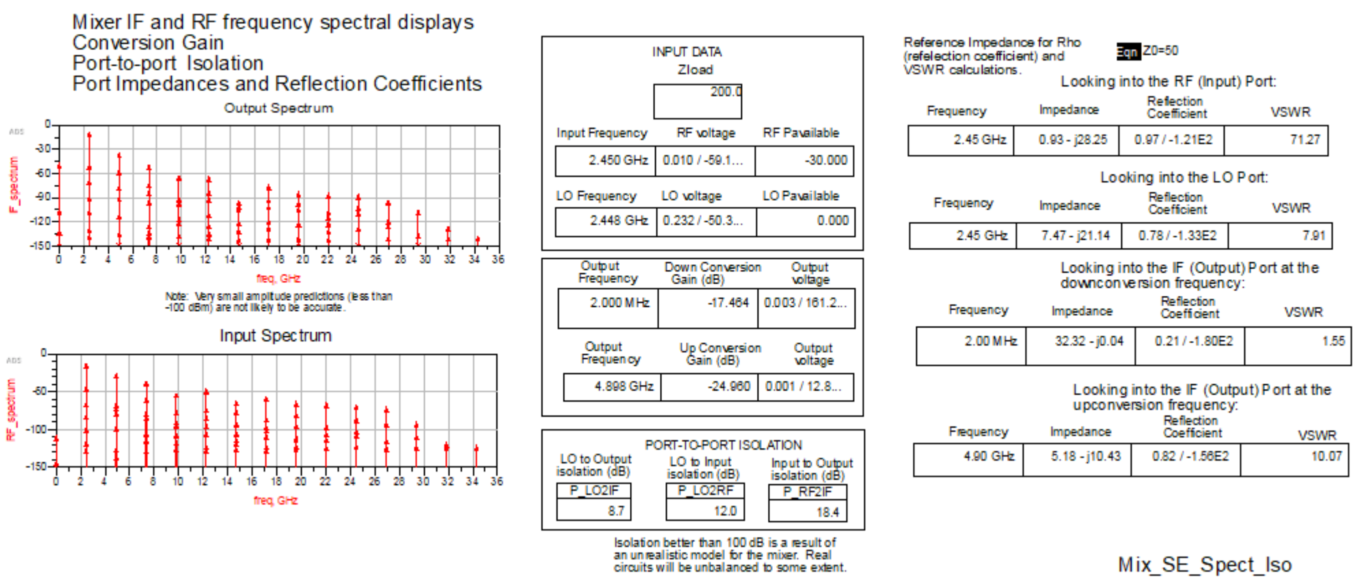

Figure 11. RF, IF Spectral Displays, Conversion Gain, Port-to-Port Isolation, Port Impedances and Reflection Coefficients for Single Ended FET Mixer at f_{RF} = 2.450 GHz and f_{LO} = 2.448 GHz.

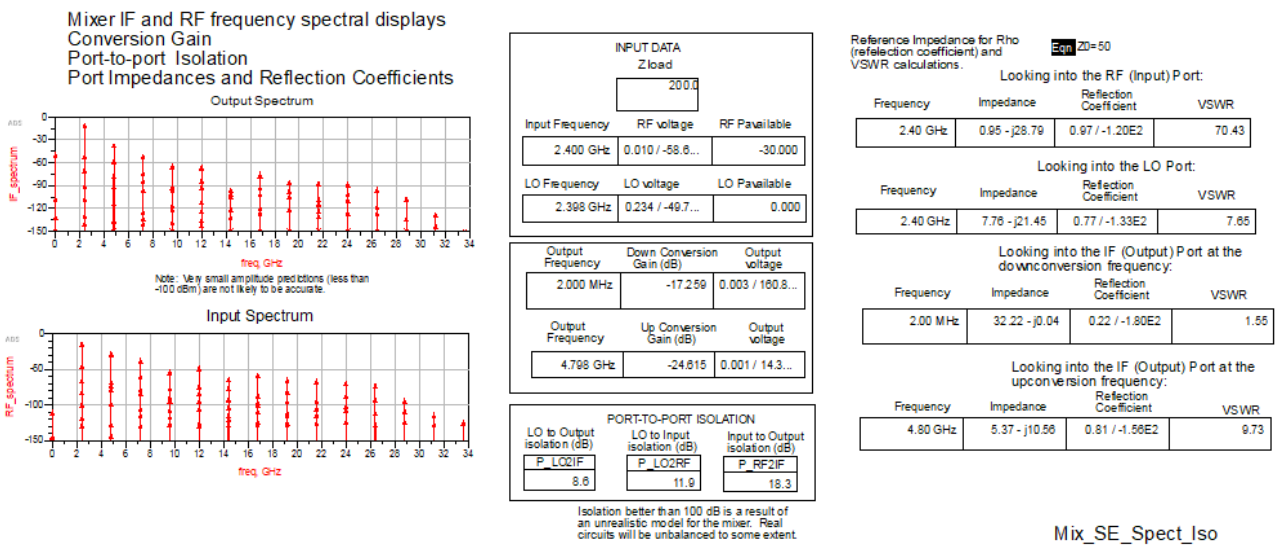

Figure 12. RF, IF Spectral Displays, Conversion Gain, Port-to-Port Isolation, Port Impedances and Reflection Coefficients for Single Ended FET Mixer at f_{RF} = 2.400 GHz and f_{LO} = 2.398 GHz.

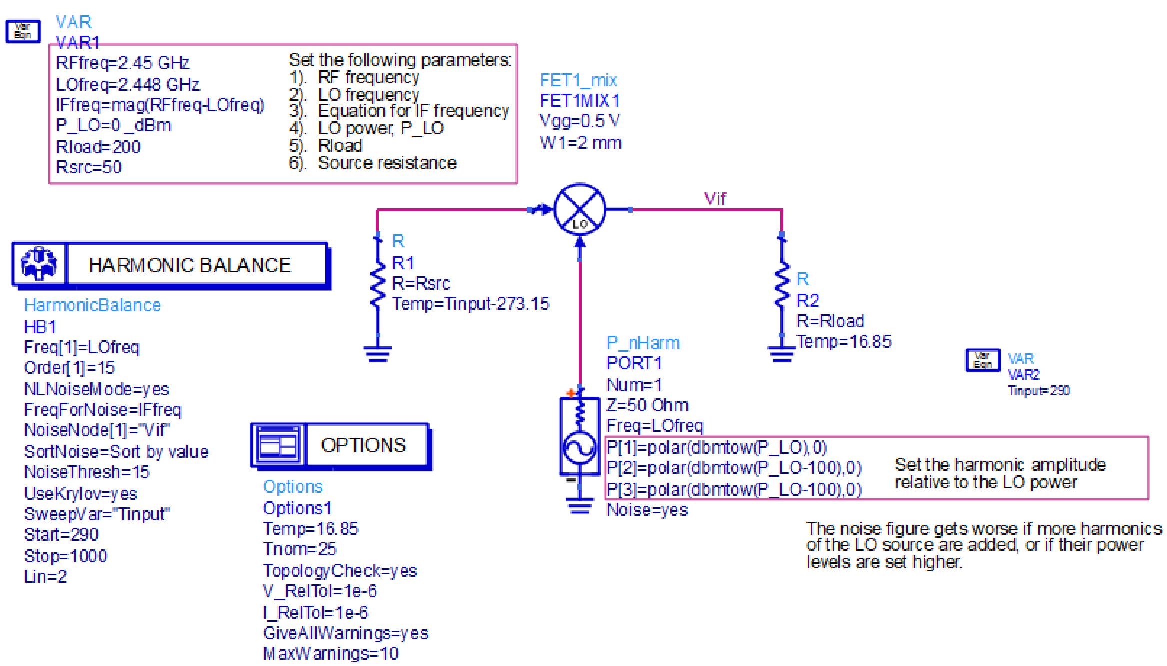

Figure 13: Circuit Diagram of Single Ended FET Mixer Noise Figure Test Setup.

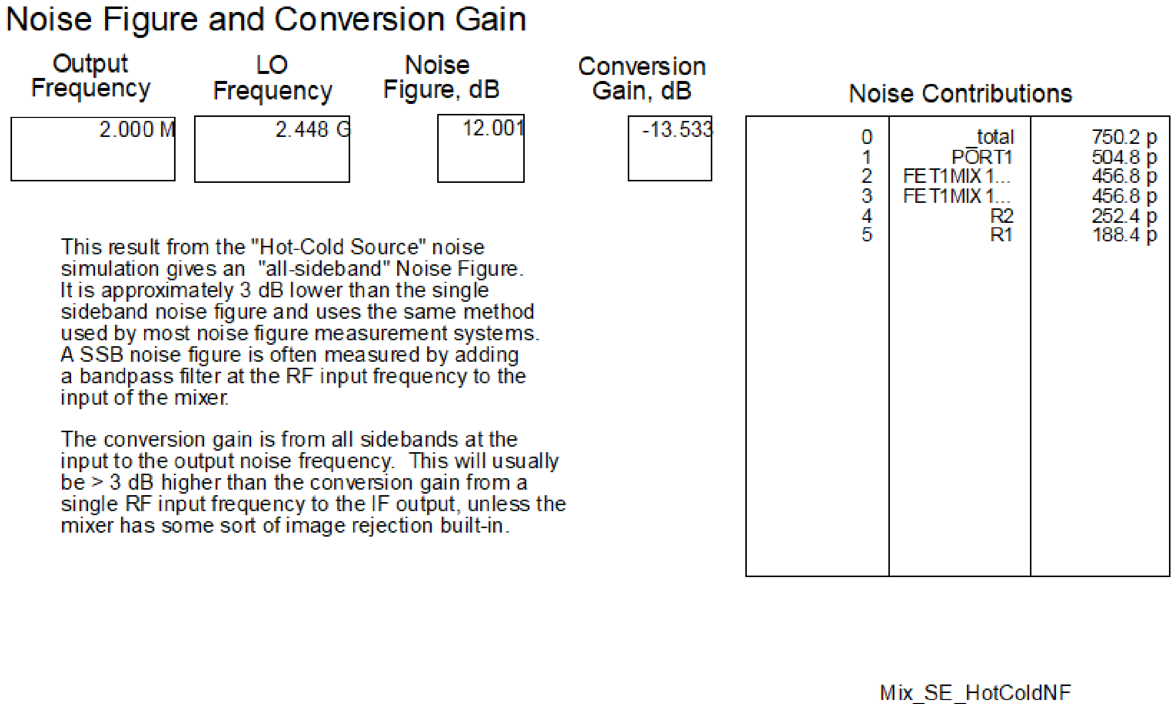

Figure 14: All-Sideband Noise Figure and Conversion Gain for Single Ended FET Mixer with f_{RF} = 2.450 GHz and f_{LO} = 2.448 GHz.

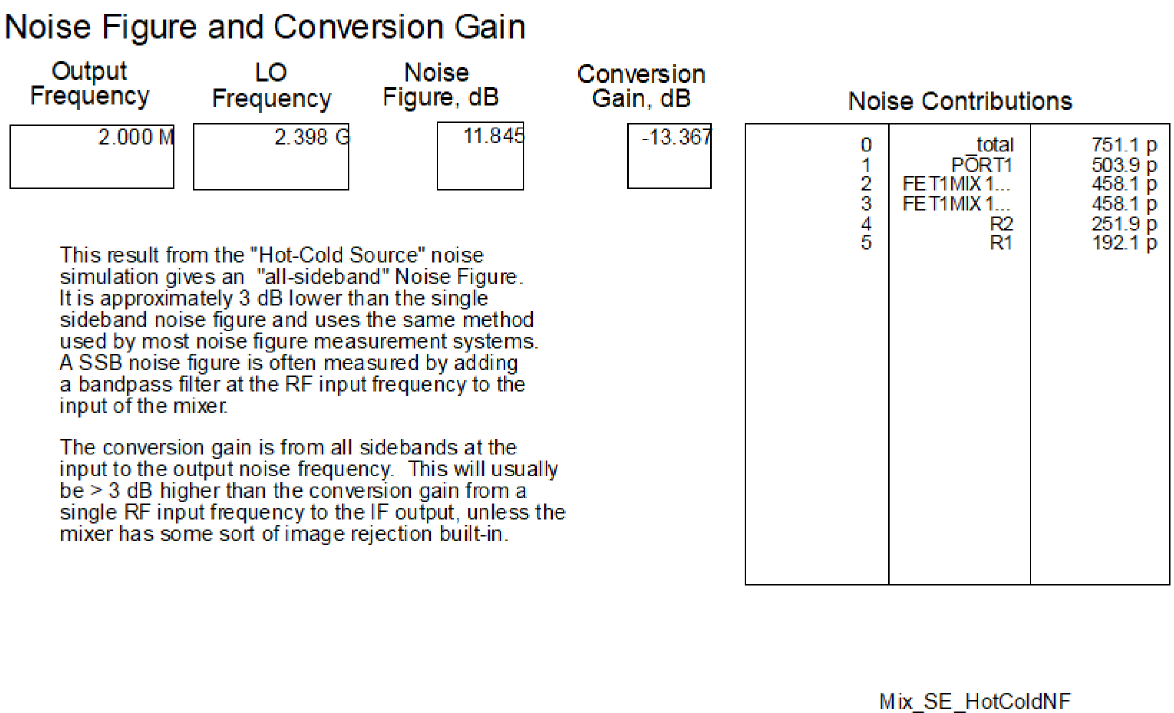

Figure 15. All-Sideband Noise Figure and Conversion Gain for Single Ended FET Mixer with f_{RF} = 2.400 GHz and f_{LO} = 2.398 GHz.

Low Pass Filter Simulation

The low pass filter shown in figure 16 shows that we have met our original specifications for the design. The cut-off frequency is located at 3 MHz, the correct frequency. Marker m2 shows that we also achieve attenuation that is lower than our 40 dB goal at 4.0 MHz. We obtain a result of -43.966 dB at this frequency. Marker m1 shows the approximate minimum value within the pass band, with a value of -0.879 dB. This means that desired signals within the passband will not experience more than 1 dB of attenuation. This variation within the passband is a consequence of the choice of a 0.5 dB equal-ripple Chebyshev stepped-impedance design. Rejected signals are attenuated below -90 dB for all frequencies greater than 7.0 MHz.

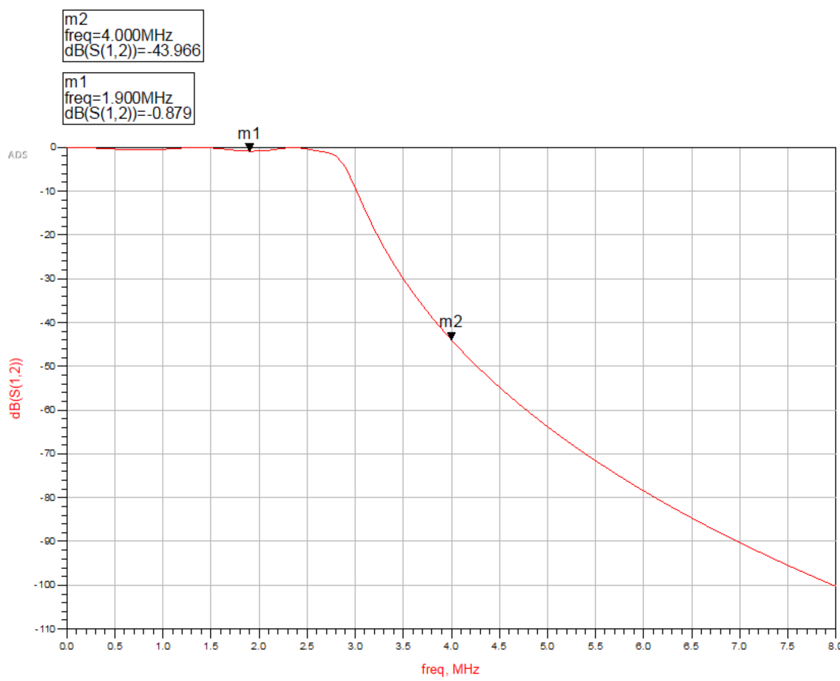

Figure 16. LPF Frequency Response.

Band Pass Filter Simulation

As we can see in Figure 17, the band pass filter fulfills all of the design requirements we set for it. The center frequency is $\omega_0 = \sqrt{\omega_1 \omega_2} = \sqrt{1.5 * 2.6} = 1.97$, where ω_1 and ω_2 are the corner frequencies of the filter, as defined by the markers on m2 and m4. The 3 dB bandwidth is defined as the frequency range on which the filter intersects the 3 dB line. As shown in Figure

17, the left intersection is somewhere between 1.45 and 1.5 MHz and the right intersection is somewhere between 2.6 and 2.7 MHz, meaning our 3 dB bandwidth is right below 1.15 MHz. This is extremely close to our designed bandwidth of 1 MHz. The filter also has great passband attenuation, as the signals that pass through the filter will lose less than 1 dB of the incoming signal strength. The rejected signals also lose nearly 100 dB of their incoming strength, meaning all signals except the ones specified in the bandwidth will be picked up by later electrical components. As shown in Figure 12, the second output frequency of the upconversion mixer has 4.98 GHz, well beyond the pass band of the band pass filter, effectively making it no longer exist.

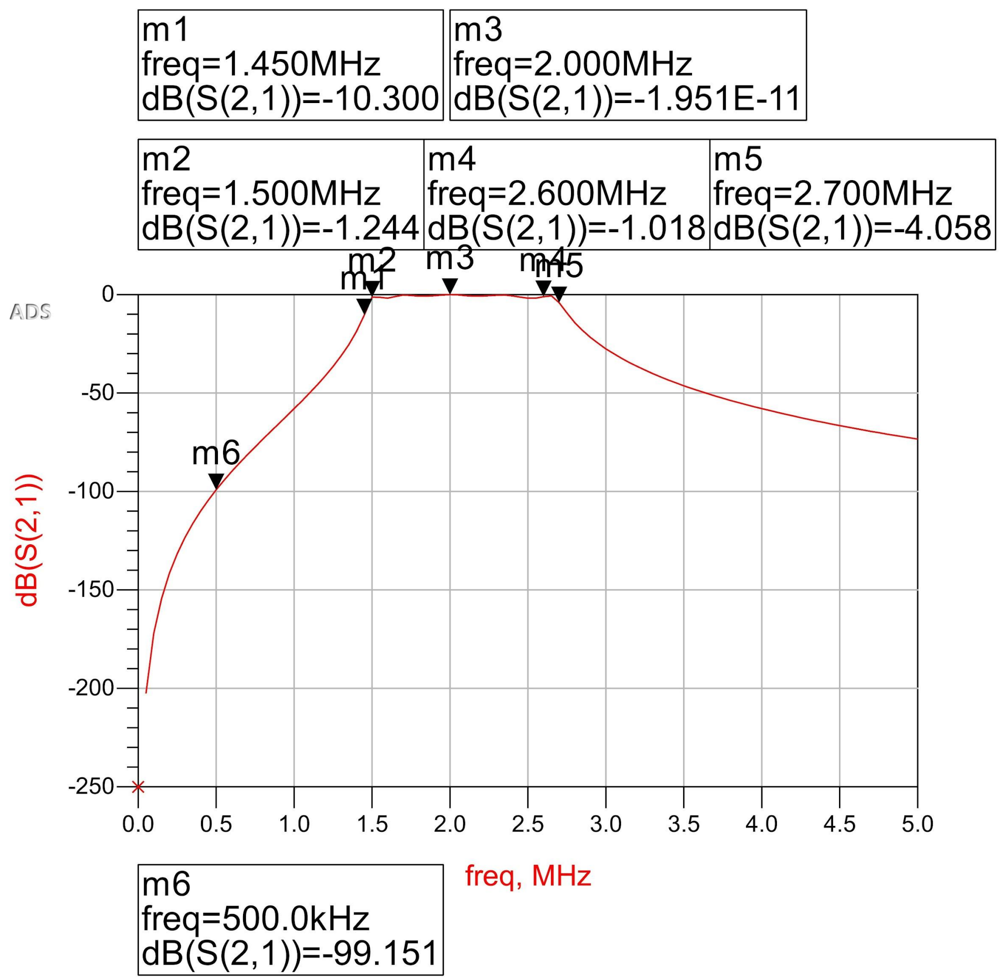

Figure 17. BPF Frequency Response.

Bluetooth Branch Simulation

We started the total bluetooth simulation by using the “Create Hierarchy” function of ADS, as to create functional and easy to use two and three port devices, that were based on the circuit design elaborated on in the earlier sections of this report. We tested our design by only putting one LNA in series with one mixer and one BPF. This setup gave us a total gain of -50 dB and a noise figure of 40 dB. Both of these values were way beyond the designed specifications, and can be attributed to the loss and noise generated by the mixer, due to the concerns of LO leakage and proper mixing performance which were prioritized over low loss. Interestingly, both of these problems were fixed by using the same technique: putting more amplifiers in series before mixing took place. This had the benefit of increasing the incoming signal strength, which increases the total gain of the circuit, which further increased the output Signal to Noise Ratio, which is used in the equation to calculate Noise Figure. This problem and solution are elaborated on further in the Conclusion section of this report.

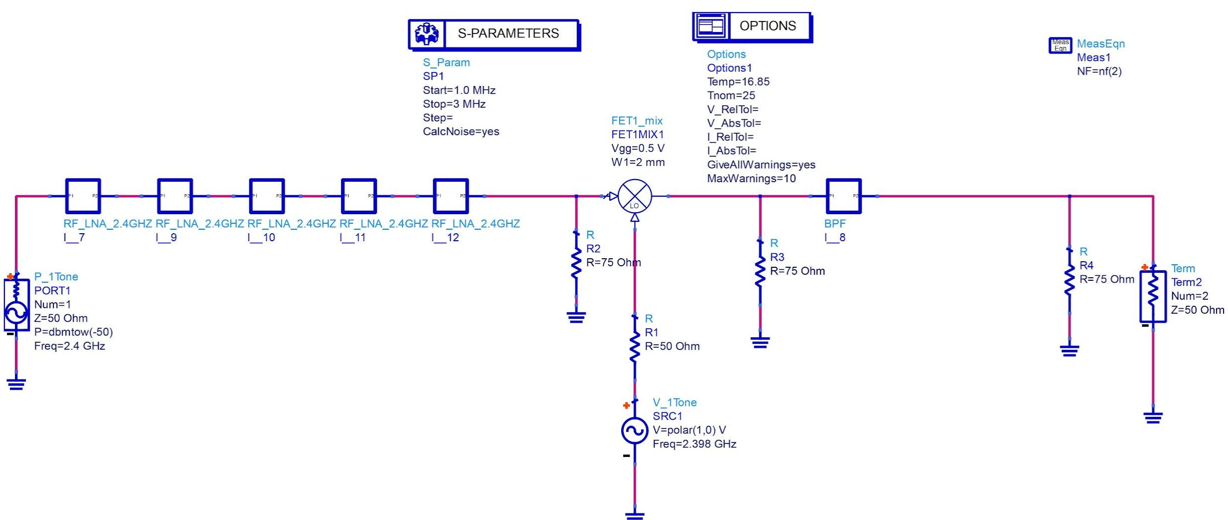

Figure 18. Final Circuit Diagram of Bluetooth Branch of Receiver.

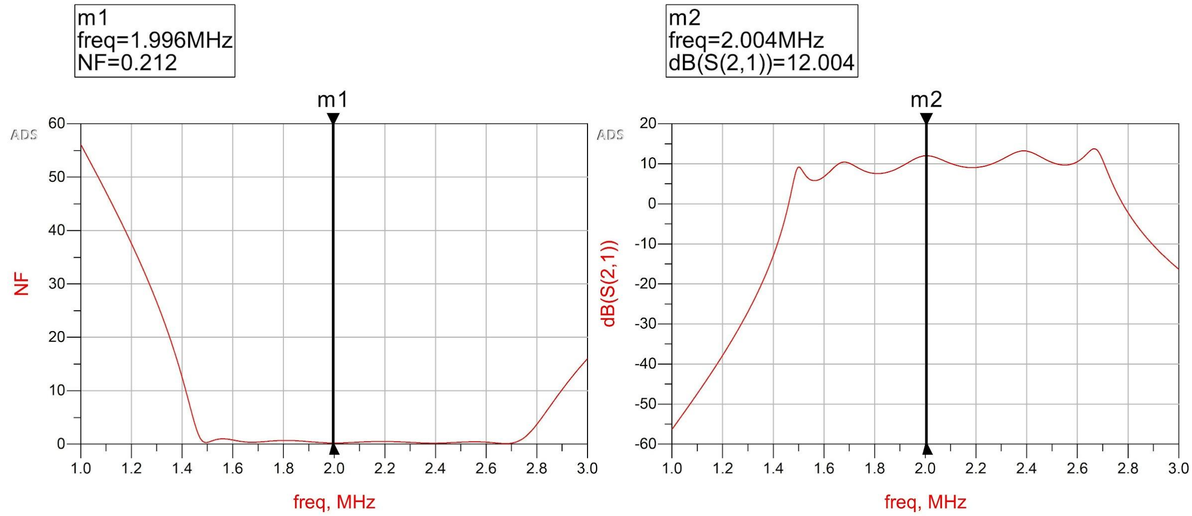

Figure 19. Circuit Simulation of Bluetooth Branch of Receiver.

As shown in Figure 18, the final circuit actually utilizes five consecutive RF LNA to properly boost the signal to required levels, which are above 0 dB. This was possible due to the extremely low noise generated by each amplifier, allowing for as many as needed to be used. The final circuit design also includes three resistors, labeled R1, R2, R3 as shown in Figure 18, which are used to increase the matching performance of the continuous circuit. Since the circuit components were designed in piecemeal fashion, in which the performance of each individual component was prioritized to meet specific requirements, the need to create match the output impedance to the input impedance of the next component was not something that could be overlooked. This needs to be done as to increase the gain, as mismatched circuits is a source of loss, and detracts from the maximum available gain of the design. This culminates in Figure 19, in which the gain and noise factor of the Bluetooth branch are shown at the output frequency of the circuit of 2 MHz. The total gain is 12 dB and the total noise is 0.212, both of which are well within the specifications outlined in Table 1.

Wi-Fi Branch Simulation

The same approach to reducing the noise figure was taken when constructing the Wifi branch of the receiver. The RF signal (f_{RF} = 2.45 GHz) is fed into a cascade of five amplifiers connected in series. Next, the amplified signal is then mixed with an LO signal (f_{LO} = 2.448 GHz). The low pass filter is then used to extract the downconverted signal (f_{IF} = 2 MHz). The resulting noise figure and gain of this network are shown in Figure 21, with a total noise figure of 0.165 and total gain of 13.914, well within the specifications of the project. The component with the largest noise figure is the mixer, with around 12 dB. It is notable that the equation for the noise figure of cascaded elements is $F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots$, and so by pushing back the mixer to the sixth element, its noise contribution is $\frac{F_6 - 1}{G_1 G_2 G_3 G_4 G_5}$, where $G_1 = G_2 = \ldots = G_5$ are the gains of the amplifiers and F_6 is the noise figure of the mixer . We effectively nullify the noise contribution of the mixer this way, and from the cascaded equation we see that the noise figure of the amplifier dominates the system.

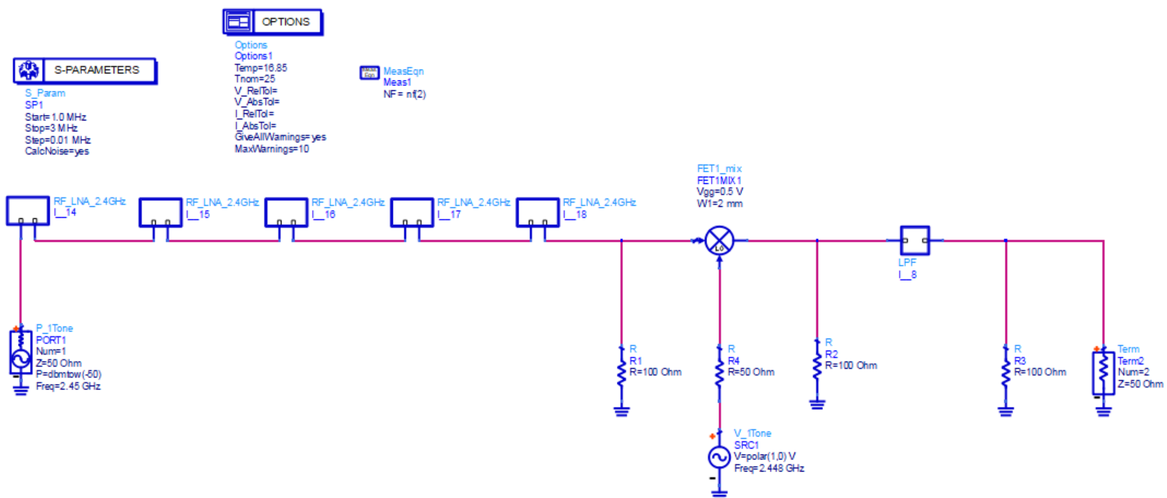

Figure 20. Final Circuit Diagram of Wifi Branch of Receiver.

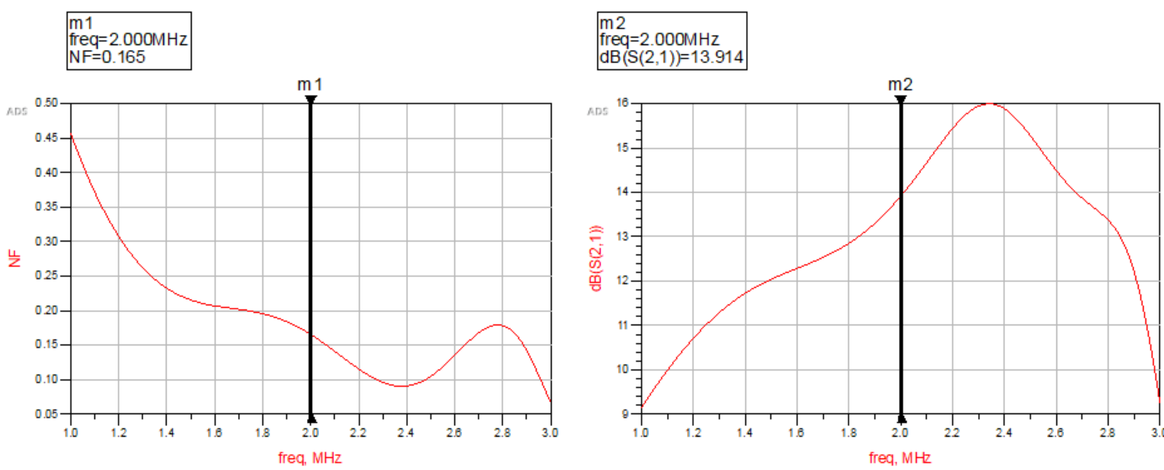

Figure 21. Circuit Simulation of Wifi Branch of Receiver.

We believe that the peak at 2.4 MHz in the gain plot of S(2,1) is a result of the rippling of the Chebyshev lowpass filter passband. In Figure 16, we see that S(2,1) at 2 MHz is roughly 1 dB down from S(2,1) at 2.4 MHz. In figure 21 we see similarities; S(2,1) at MHz is roughly 2 dB down from S(2,1) at 2.4 MHz.

Conclusion

This final project for our Microwave Circuits class is the culmination of years of study of electronics, and has taught us how to effectively use our knowledge and experience in circuit design to create an overall circuit system that conforms to a given set of requirements that we had to research for ourselves. Over the course of this project, we used not only the resources at our disposal in terms of access to computer design systems and help from our professor and his assistants, but our own ability to read and comprehend other project reports and our ability to grasp and decipher technical documents for various electronic devices. We also learned how to create various microwave components, in terms of amplifiers for a given gain and noise value, filters for low pass and band pass purposes that require a certain attenuation in their pass and reject bands, and mixers that operate in the linear region and don't degrade the incoming signal too harshly. We also learned how to simulate the early design versions of these devices and use the results of these simulations to refine our final design and create components that adhere to the requirements presented by us.

However, the entire process was not without its hardships and challenges. It was not easy to find and implement transistors in our amplifier design that actually conformed to the design requirements, and it was only after many trials of testing the components packaged in the S-Parameter Vendor Library in ADS that we were satisfied with one of them to use in our project. It was actually this specific problem that made it almost impossible to create a single reliable low frequency amplifier to be used in the Bluetooth branch to amplify the final signal enough. This actually led to a different solution, one that didn't rely on creating a new device, but implementing an already designed device. Another problem we faced was in the fact that the noise figure of the final design was very high due to the noise generated by the mixer, in the range of 40-50 dB in the output port. We actually solved the amplification issue and the noise figure issue in the same solution, whereby we put five RF amplifiers in series with each before mixing took place. This had the double benefit of creating enough amplification before any mixers or filters were applied to the signal so that no second amplifier was needed after filtering, and pushed the mixer deeper into the noise figure equation, with an even bigger denominator created by the five previous amplifiers. The equation in question is $F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ...$, and it is obvious by looking at it that the first iteration that had the mixer as F_2 made it a much higher source of noise, and the final design that had the mixer as F_6 made it so that it could be effectively zero, with G_1 through G_5 each contributing 16 dB of positive gain.

Overall, we are very pleased with our final design, and proud of the fact that we were able to leverage our skills in such a way as to create a device that is capable of not only supporting two distinct communication methods, but utilizes many of the same components for both as to create a simple and reliable dual receiver.

Hardware Specifications

[1] Single-ended FET mixer transistor, BSIM3 MOSFET (NMOS): http://literature.cdn.keysight.com/litweb/pdf/ads2008/ccnld/ads2008/BSIM3_Model_(BSIM3_MOSFET_Model).html

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