2023 Digital IC Design Homework 3

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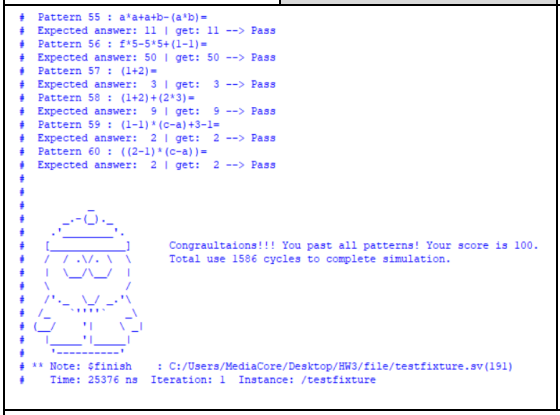
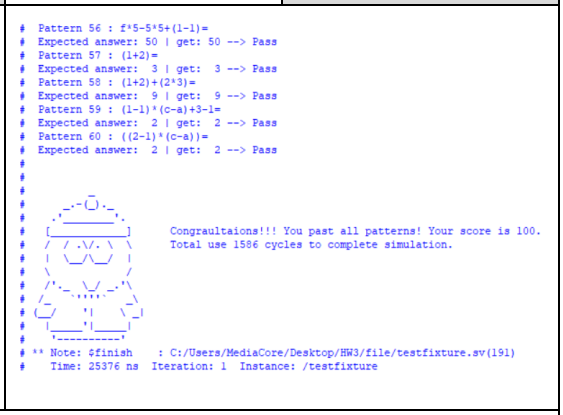
Simulation Result

Functional simulation	100	Gate-level simulation	100





Synthesis Result

Total logic elements	361
Total memory bits	0
Embedded multiplier 9-bit elements	1
Total cycle used	1586
Clock width	16

Flow Summary

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Flow Status	Successful - Fri Apr 21 14:37:32 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	AEC
Top-level Entity Name	AEC
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	361 / 55,856 (< 1 %)
Total registers	155
Total pins	19 / 325 (6 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	1 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

Description of your design
主要使用的演算法：Infix Method，一開始花蠻多時間在理解 Infix to Postfix 演算法，完成 Infix to Postfix 後，發現使用 Infix 可以用更少的 Total logic elements 且 Total cycle used 也更少。 主要分四個狀態：DATA_IN、CAL、DONE、RESET。 DATA_IN: 將題目給的 data 丟給 data_stack，在 CAL 時可利用 data_count 控制時序上的問題。 CAL: 將 number 丟到 value_stack，運算子丟到 ops_stack，再作演算法，亦會判斷乘法與加減的層級關係。 DONE: 將 valid 拉起來，result 即為 value_stack [0]。 RESET: 將各參數作 reset，便進下一筆測資。

*Scoring = Area cost * Timing cost*

*Area cost = Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements*

*Timing cost = Total cycle used * Clock width*

*** Total logic elements must not exceed 1500.**