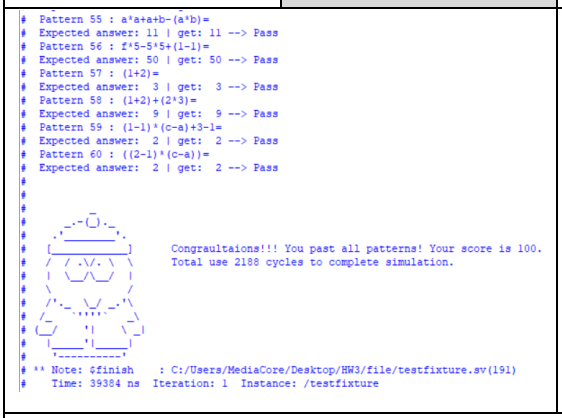
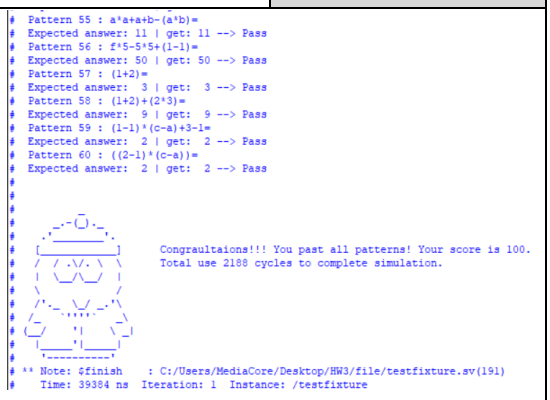
2023 Digital IC Design Homework 3

NAME	林柏戎
Student ID	Q36114239

Simulation Result

Functional simulation	100	Gate-level simulation	100





Synthesis Result

Total logic elements	507
Total memory bits	0
Embedded multiplier 9-bit elements	1
Total cycle used	2188
Clock width	18

Flow Summary

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Flow Status	Successful - Wed Apr 19 11:12:49 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	AEC
Top-level Entity Name	AEC
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	507 / 55,856 (< 1 %)
Total registers	257
Total pins	19 / 325 (6 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	1 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

Description of your design
主要是使用助教提供的演算法：Infix to Postfix Method，一開始花蠻多時間在理解此演算法，後來懂了之後就蠻好寫的了。 主要分五個狀態：DATA_IN、STACK、CAL、DONE、RESET。 DATA_IN: 將題目給的 data 丟給 data_stack，在 STACK 時可利用 num_count 控制時序上的問題。 STACK: 將 number 丟到 output_stack，運算子丟到 oper_stack，並同時作 Infix to Postfix 的演算法，最後 output_stack 即為最後要做 cal 的 stack。 CAL: 將 output_stack 作 cal，output_stack 裡的 number 丟到 cal_stack，output_stack 遇到運算子，則將 cal_stack 最後兩個作運算。 DONE: 將 valid 拉起來，result 即為 cal_stack[0]。 RESET: 將各參數作 reset，便進下一筆測資。

*Scoring = Area cost * Timing cost*

*Area cost = Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements*

*Timing cost = Total cycle used * Clock width*

*** Total logic elements must not exceed 1500.**