Introduction to SoC

Instructor: NCTU

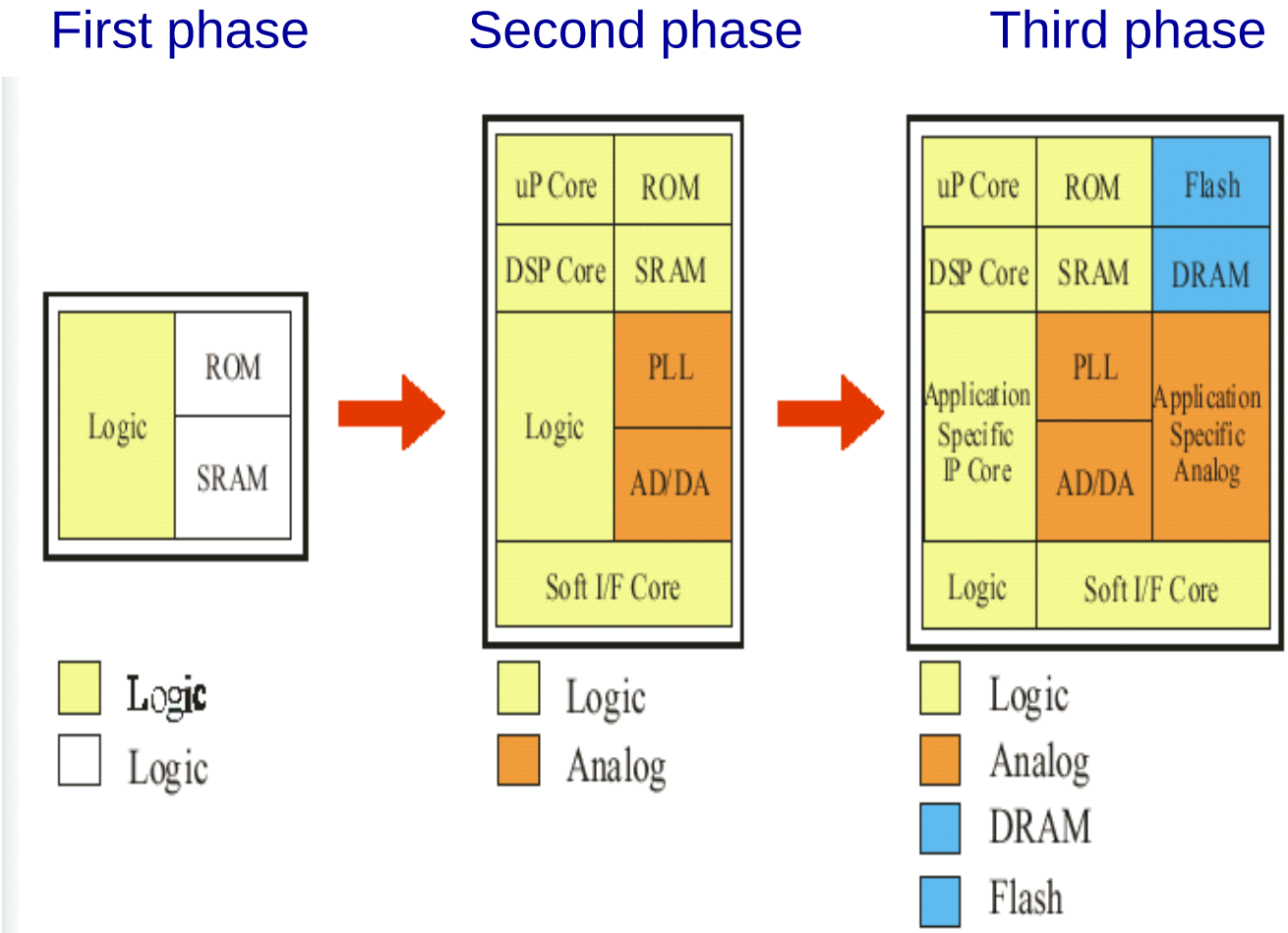
SoC: System on Chip

- **System**

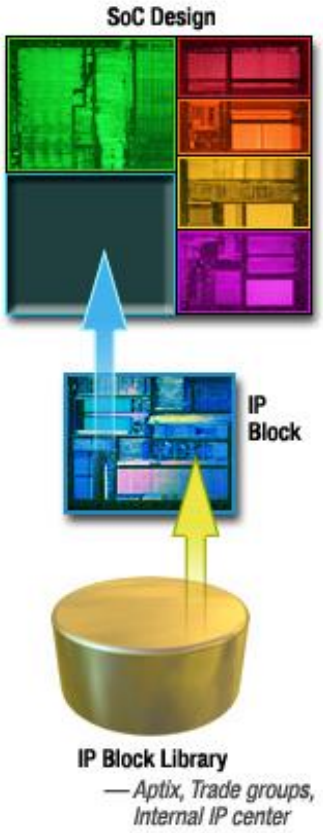
  A collection of all kinds of components and/or subsystems that are appropriately interconnected to perform the specified functions for end users.

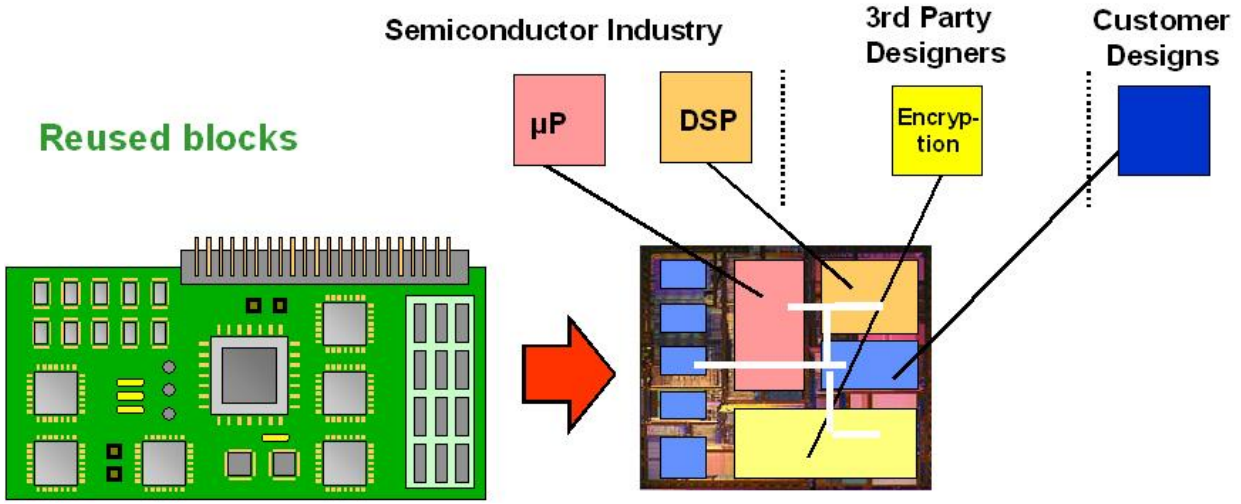
- **A SoC design is a “product creation process” which**
  - Starts at identifying the end-user needs (or system)
    - Hardware
    - Software
  - Ends at delivering a product with enough functional satisfaction to overcome the payment from the end-user

SoC Evolution



What is SoC in your mind?



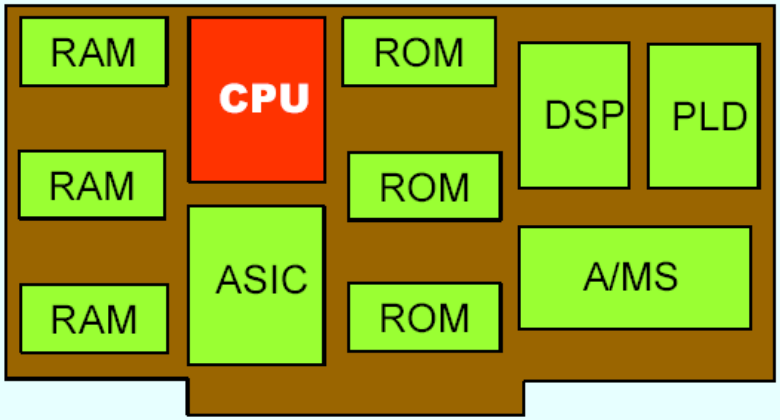


Definition: integration of a complete system onto a single IC

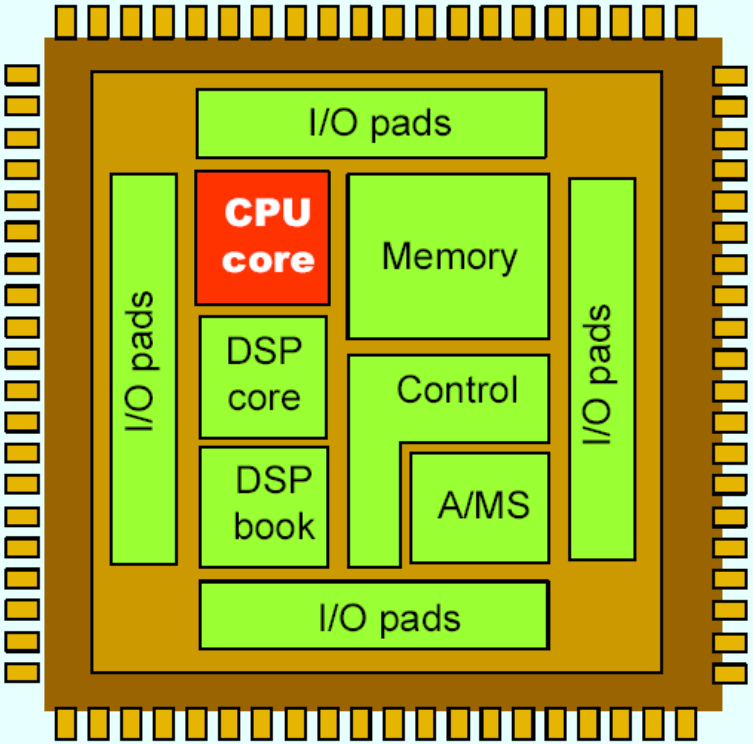
Board to Chip

Is it possible to design a 100-Billion-Transistor SOC in 100 Days?

A/MS=analog/mixed signal
ASIC = application-specific IC
CPU = central processing unit
PLD = programmable logic device

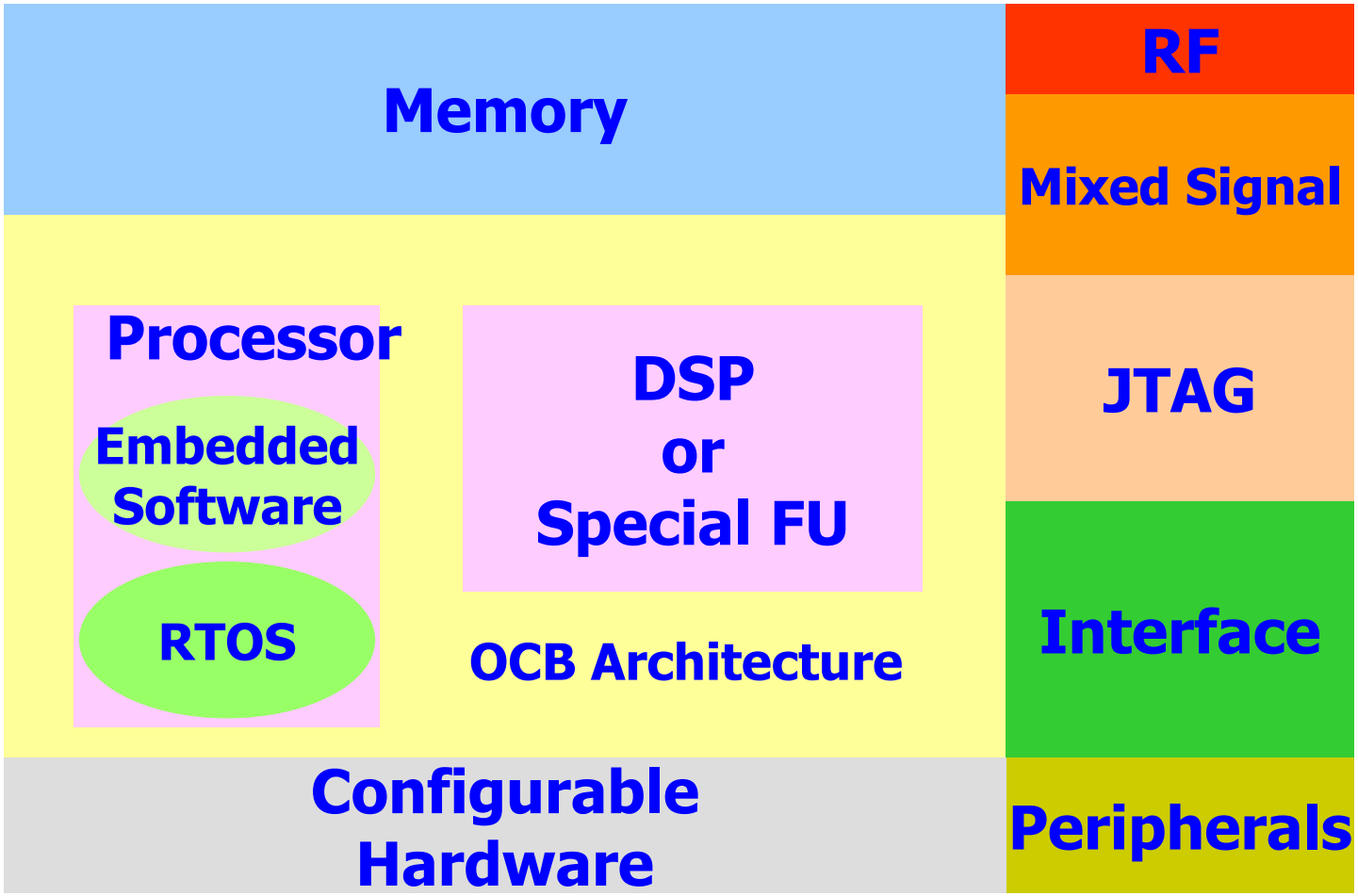


Board components



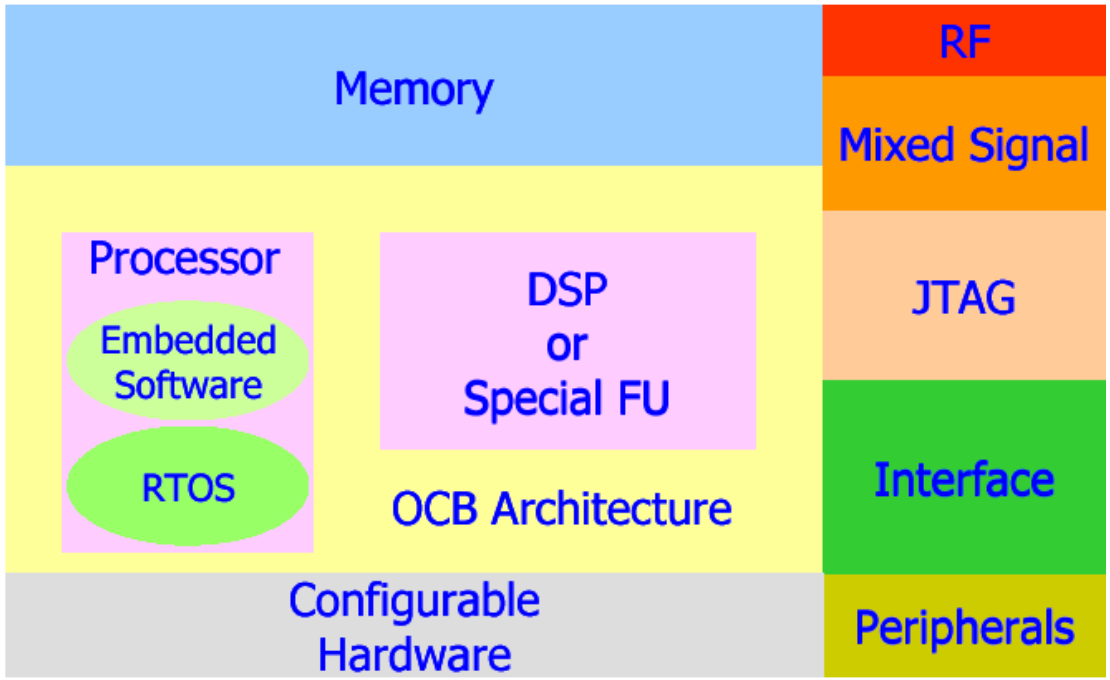
Virtual components

SoC Architecture

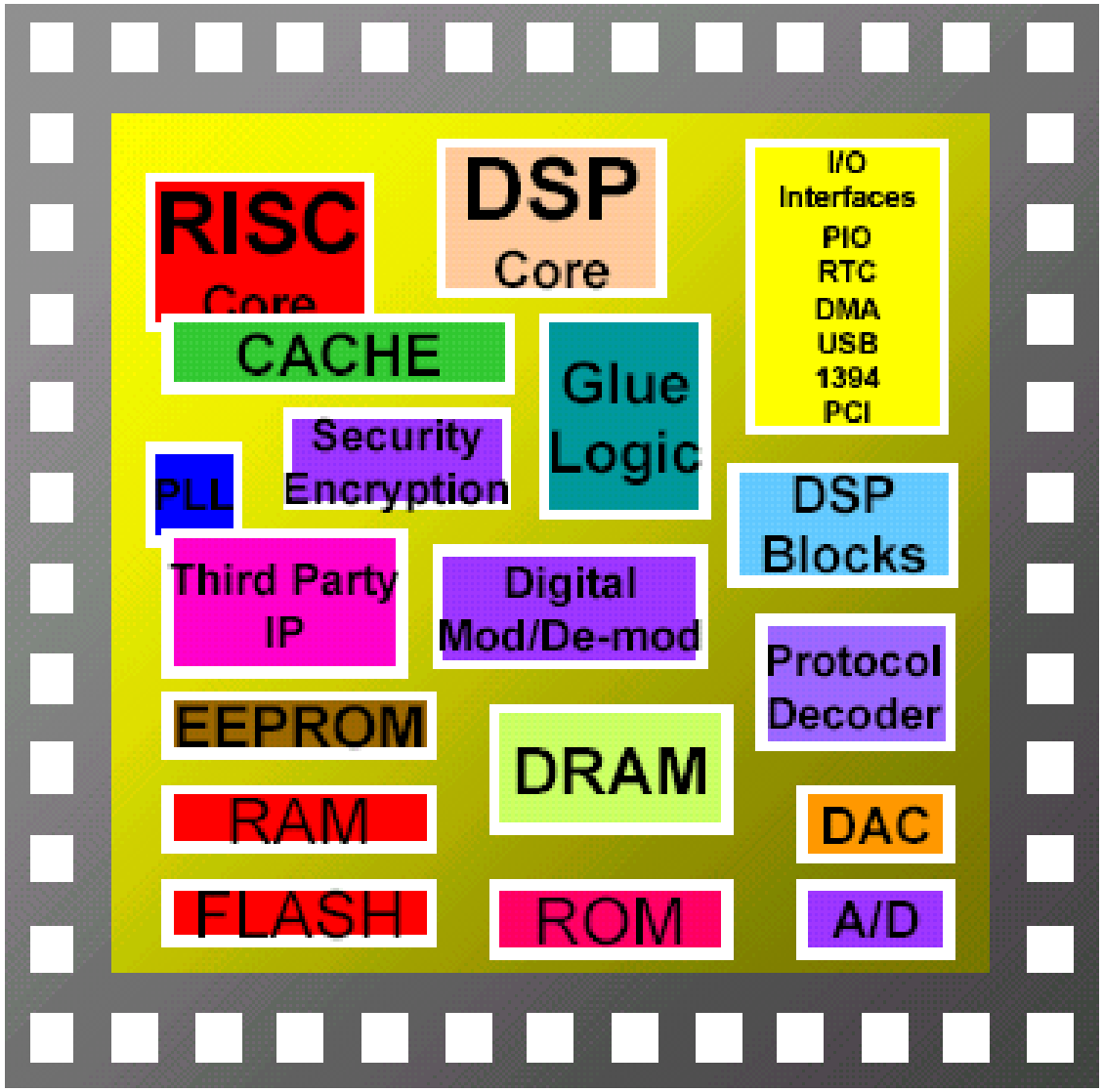


SoC Architecture

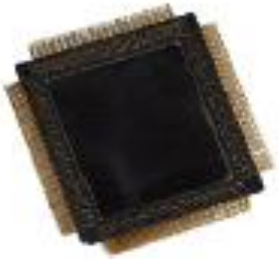
- **Hardware:**
  - Analog: ADC, DAC, PLL, TxRx, RF…etc.
  - Digital: Processor, Interface, Accelerator…etc.
  - Storage: SRAM, DRAM, FLASH, ROM…etc.
- **Software: OS, Application**



System on a Chip



SOC is industry trend



ASIC/ASSP

Today

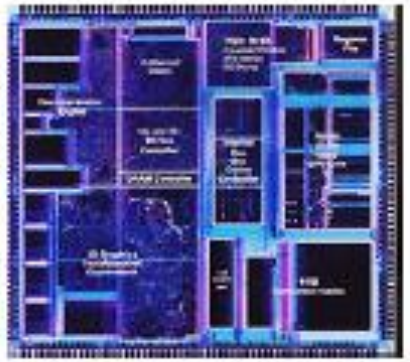
Assembly

System-Board

IP/System-Board

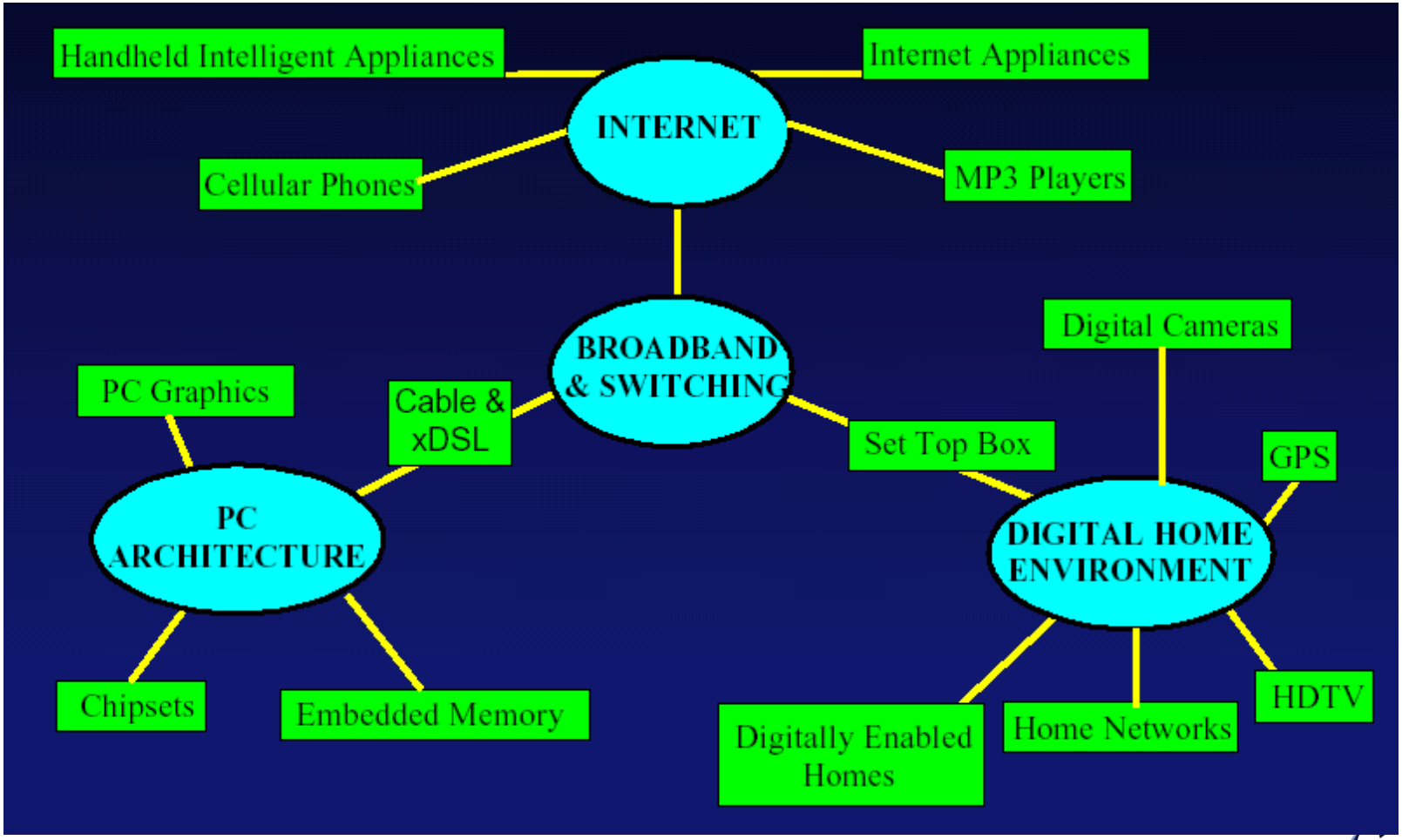
Tomorrow

Integration



SOC

SoC Applications



Source: Semiconductor Research Corp.

Example: Mobile Phone

Yesterday

- Voice only; 2 processors
- 4 year product life cycle
- Short talk time

Today

Single Chip

- 5~8 Processors
- Memory
- Graphics
- Bluetooth
- GPS
- Radio
- WLAN

- Voice, data, video, SMS
- <12 month product life cycle
- Lower power; longer talk time

Source: EI-SONICS

SoC Design Considerations

- Architecture strategy
- Design-for-test strategy
- Validation strategy
- Synthesis and backend strategy
- Integration strategy

Why SoC?

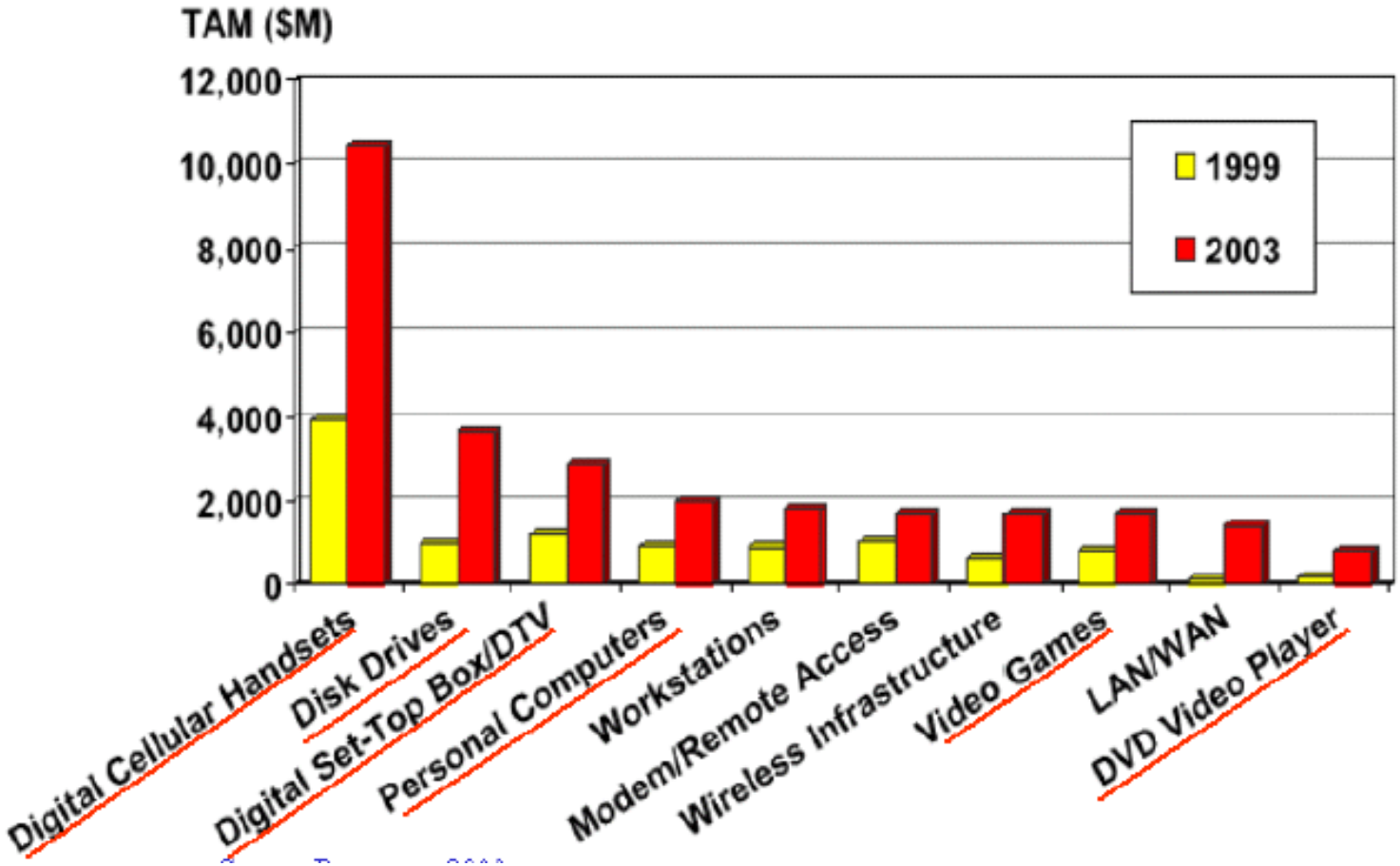
Why?

- **Complex applications**
  - Semiconductor density ↑ 58% per year, but design productivity ↑21% annually.
- **Process technology allows it**
- **High performance**
- **Miniaturization**
- **Battery life**
- **Short market windows**
- **Cost sensitivity**

Characteristics

- **Very large transistor counts on a single IC**
- **Mixed technologies on the same chip**
  - Digital, memory, analog, FPGA
  - Hardware and software
- **Multiple clock frequencies**
- **Hierarchical design with embedded reusable IP cores**

Where SoC Goes To?

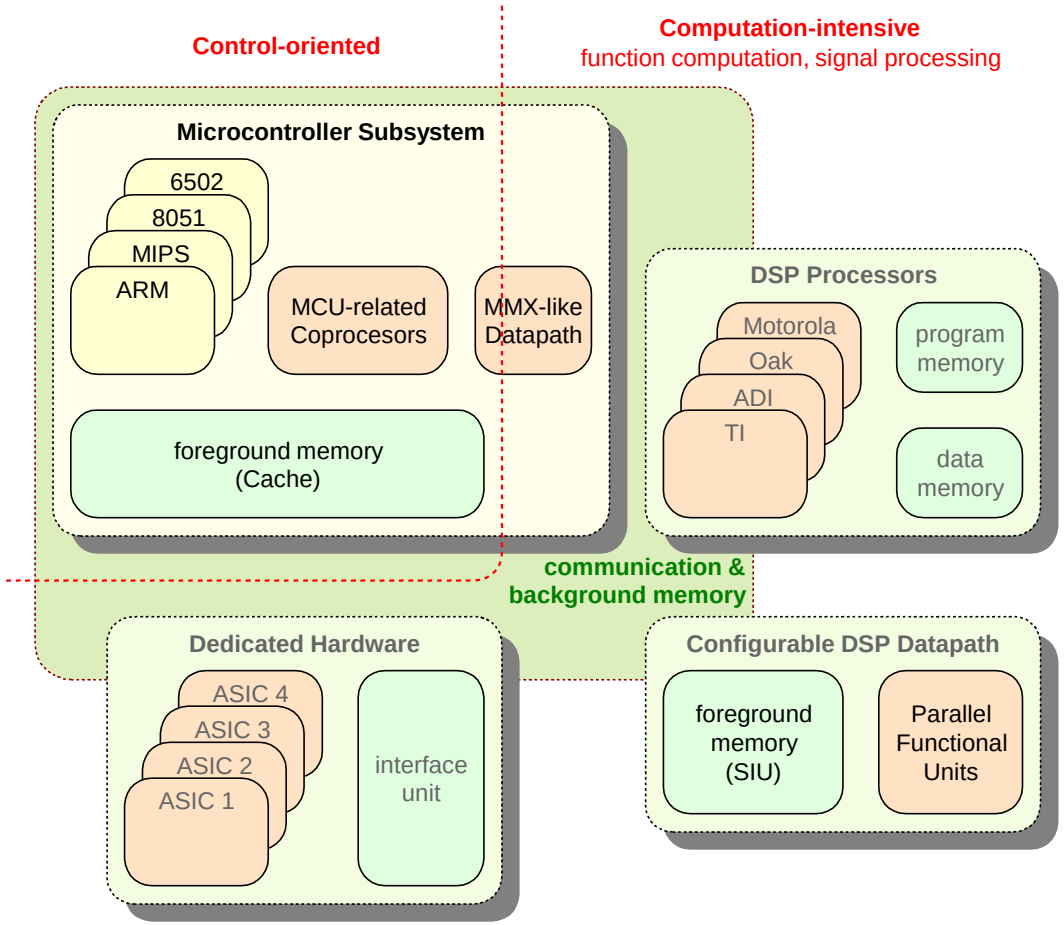


Architecture Strategy

- Central processing core
- DSP cores
- On chip bus
- Easy plug-and-play IPs
- I/O, peripherals
- Platform-based design methodology
  - Parameterization
  - Function partition

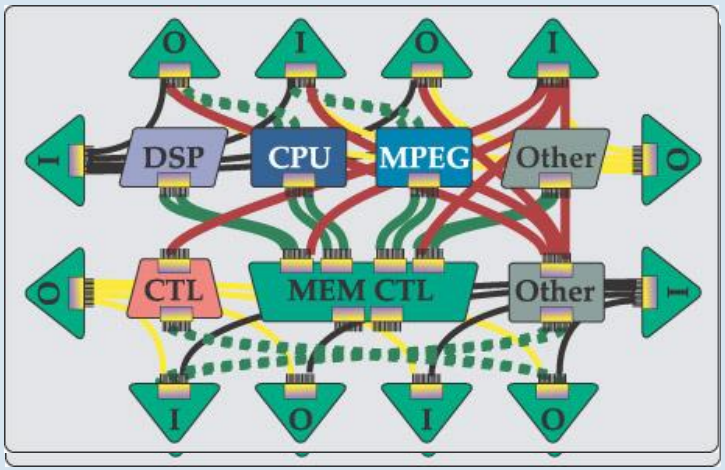
Alternative Computing Subsystem

- Control-dominated subsystem
  - controls & coordinates system tasks
  - performs ***reactive*** tasks (e.g. user interface)
- Data-dominated subsystem
  - regular & predictable ***transformational*** tasks
  - well-defined DSP kernels with high parallelism



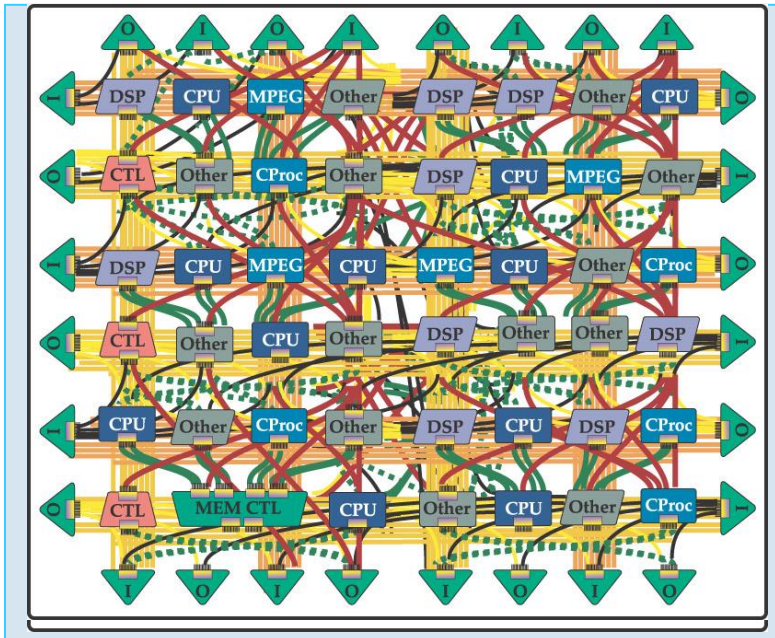
SOC Complexity / Abstraction

Yesterday



- Processor-centric (1 or 2)
- Simple I/O
- Manageable Complexity

Today



- Many processing units
- Large amount of I/O
- Overwhelming Complexity!

Source: EI-SONICS

Conquer the SoC Complexity

- **Use a known real entity**
  - A pre-designed component (IP, VC reuse)
  - A platform (architecture reuse)
- **Partition**
  - Based on functionality
  - Hardware and software
- **Modeling**
  - At different level
  - Consistent and accurate

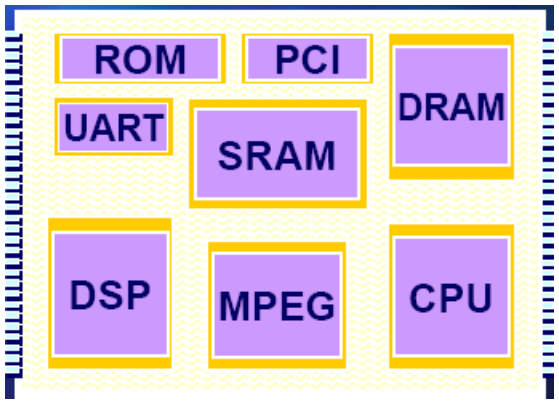
What is IP?

- **Intellectual Property (IP)**
  - Intellectual Property means products, technology, software, etc. that have been protected through patents, copyrights, or trade secrets.
- **Virtual Component (VC)**
  - A block that meets the Virtual Socket Interface Specification and is used as a component in the Virtual Socket design environment. Virtual Components can be of three forms — Soft, Firm, or Hard. (VSIA)
- **Also named mega function, macro block, reusable component**

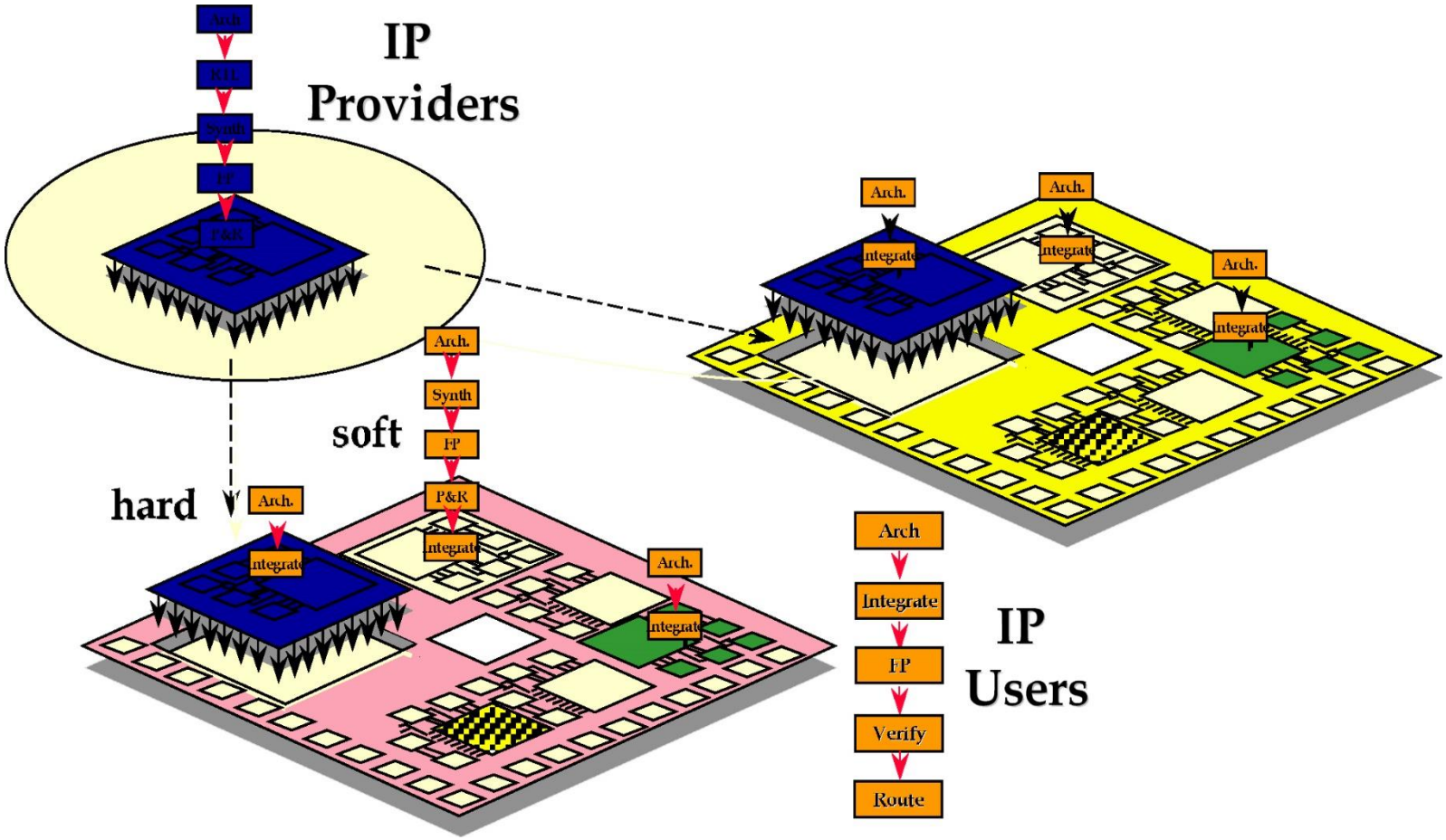
SoC and SIP

- System-on-Chip (SoC)
- Semiconductor Intellectual Property (IP)
  - Also known as cores, virtual components (VCs)
  - Memory, processors, DSPs, I/O, perpherials

- SoC = ∑ IPs ?



Core(IP)-Based Design



IP, VC, PE, FU, …

- Memory controller
- Interrupt controller
- Power management controller
- Internal memories
- Bridges
- Caches
- Other functions

Hard, Soft, Firm IPs

- **Hard core**
  - Large logic circuits
  - An ART
  - E.g. ARM core
- **Soft core**
  - Tiny logic circuits
  - Synthesize layout using standard cells with ASIC flow
  - E.g. IPs
- **Firm core**
  - Medium logic circuits
  - Need tight integration with custom cells
  - Tile-based layout like Hard core
  - E.g. FPGA CAD tools

Types of IP

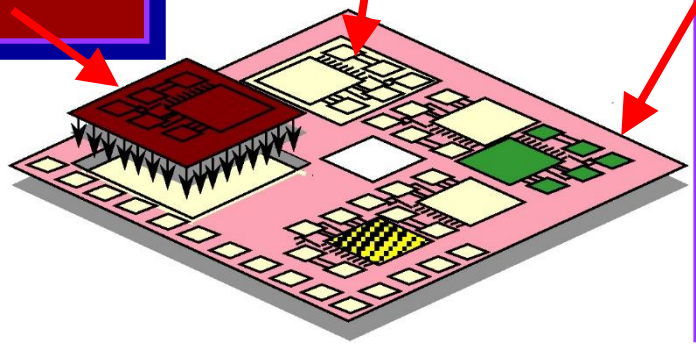
Firm IP:

- gate level or synthesizable RT level data
- Some technology and/or physical constraints
- some flexibility on form & function
- Predictable size and speed

Hard IP:

(“physical”)

- Polygon level data
- Technology specific
- Fixed form & function
- Well characterized



Soft IP: (“Core”)

- RT level or above
- Technology portable
- Flexible form & function
- Estimated size and speed

Differences in Design Between IC and IP

- **Limitation of IC design**
  - Number of I/O pin
  - Design and Implement all the functionality in the silicon
- **Soft IP**
  - No limitation on number of I/O pin
  - Parameterized IP Design: design all the functionality in HDL code but implement desired parts in the silicon
  - IP compiler/Generator: select what you want !!
  - More high level auxiliary tools to verify design
  - More difficult in chip-level verification
- **Hard IP**
  - No limitation on number of I/O pin
  - Provide multiple level abstract model
  - Design and Implement all the functionality in the layout

IP Value

- Foundation IP – Cell, MegaCell
- Star IP – ARM (low power)
- Niche IP – JPEG, MPEGII, TV, Filter
- Standard IP – USB, IEEE1394, ADC, DAC
- ……..

IP Sources

- Legacy IP
  - from previous IC
- New IP
  - specifically designed for reuse
- Licensed IP
  - from IP vendors

Why IP ?

- **Don’t know how to do it**
- **Cannot wait for new in-house development**
- **Standard/Compatibility calls for it**
  - PCI, USB, IEEE1394, Bluetooth
  - Software compatibility
- **Configurable**

Why Configurable?

- All IPs are typically customized to meet specific SoC specification
- Software upgradability
- Short product cycles
- E.g. External memory controller supports
  - memory types (sync. Or async.)
  - Sizes,
  - Widths,
  - Banks,
  - Etc.

SoC: A Finer View

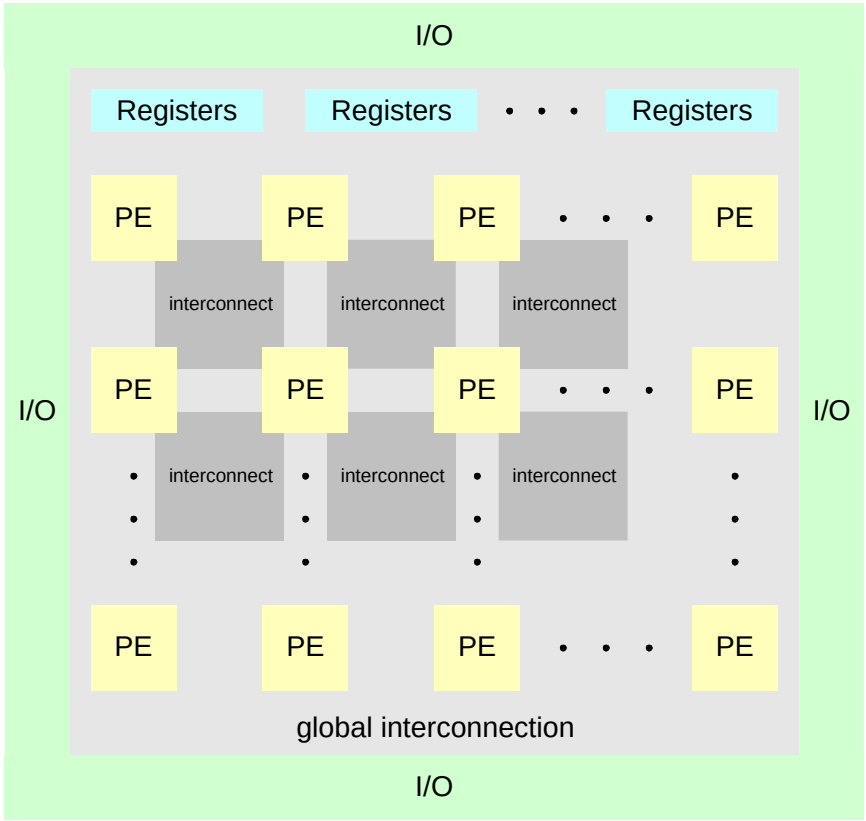
- **SoC = ∫ (IPs + Platform)**

- **Platform, or Semiconductor Infrastructure IP**
  - Interconnect/Inter-block communication
  - Performance optimization
  - Test
  - Diagnosis
  - Repair
  - Power management
  - …

General-Purpose Metamer

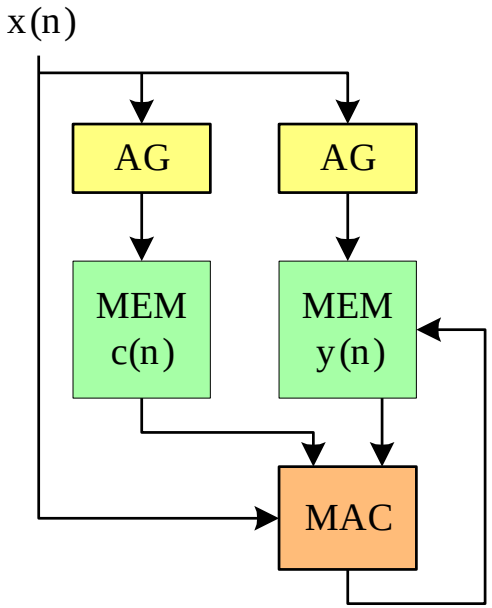
- **PE granularity**

  (usually imply # of functionalities)
- **Interconnection routability**
  - neighbor (1-D) / mesh (2-D)
  - crossbar
  - bus
- **Initialization mechanism**
- **Configuration overhead**

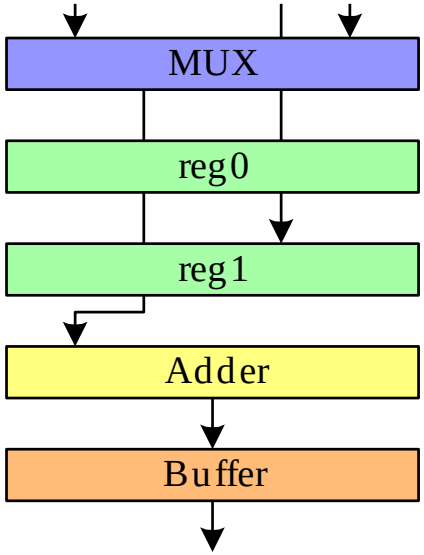


PE Granularity

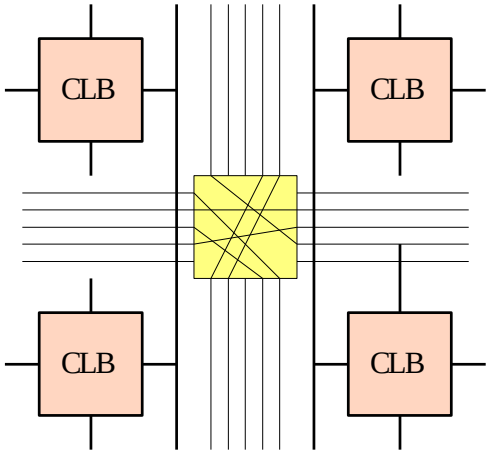
- Smallest unit of the reconfigurable fabric that can be reprogrammed
- tradeoffs between flexibility and reconfiguration overhead



Reconfigurable Dataflow



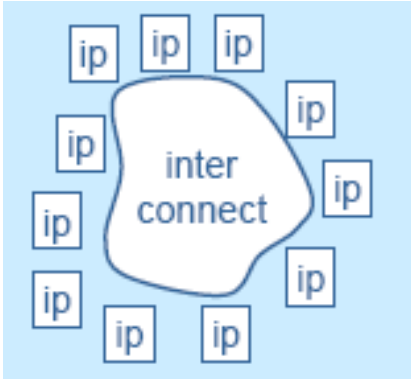
Reconfigurable Datapath

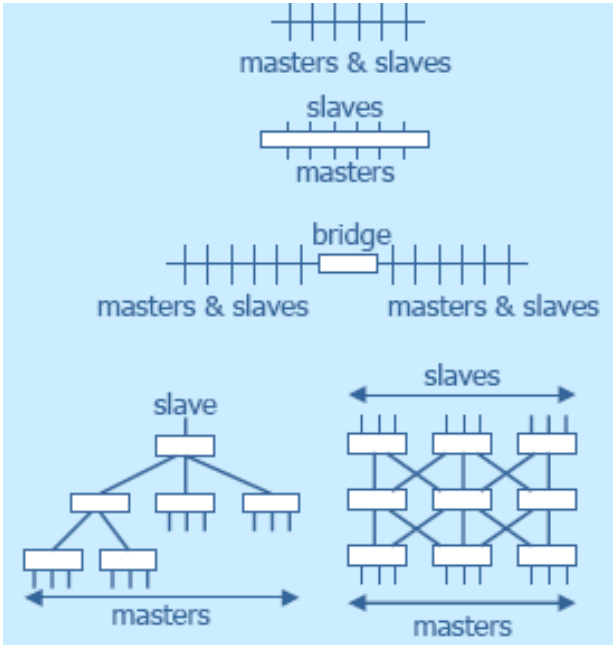


Reconfigurable Logic

On-Chip-Bus, OCB

- **Requirements**
  - Have to connect many local IPs
    - Heterogeneous traffic
    - Scalable capability
    - QoS
- **Types**
  - Wire (zero hop)
  - Bus (single hop)
  - Switch, router (multi-hop)
  - Circuit-switched
  - Packet-switched

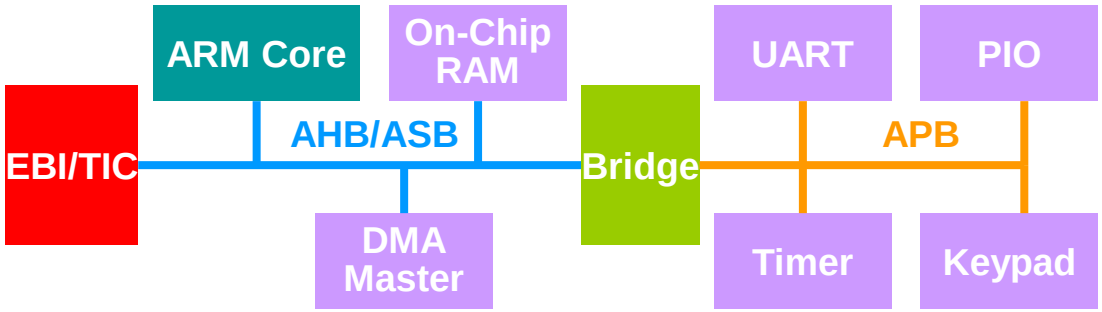




Source: Philips

Example: ARM OCB - AMBA

- Advanced Microcontroller Bus Architecture (AMBA)
- AMBA 2.0 specifies
  - the Advanced High-performance Bus (AHB)
  - the Advanced System Bus (ASB)
  - the Advanced Peripheral Bus (APB)
  - test methodology



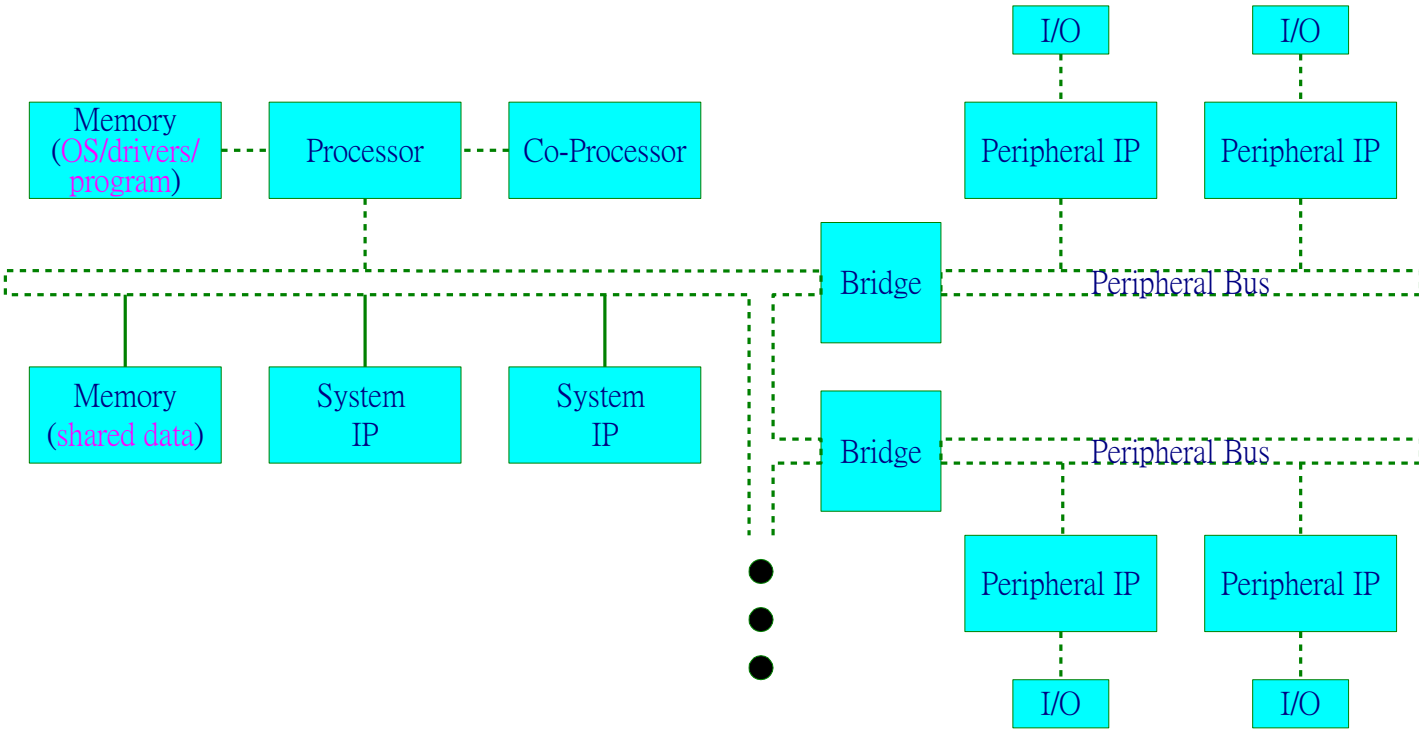
A typical AMBA system

Virtual Component Interface (VCI)

- **What is VCI**
  - A request-response protocol, contents and coding, for the transfer of requests and responses
- **Why VCI**
  - Other IP blocks not available ‘wrapped’ to the on-chip communications may work with IP wrappers. VSI Alliance VCI is the best choice to start with for an adaptation layer
- **VCI specifies**
  - Thee levels of protocol
    - Advanced VCI (AVCI),
    - Basic VCI (BVCI), and
    - Peripheral VCI (PVCI)
  - Transaction language

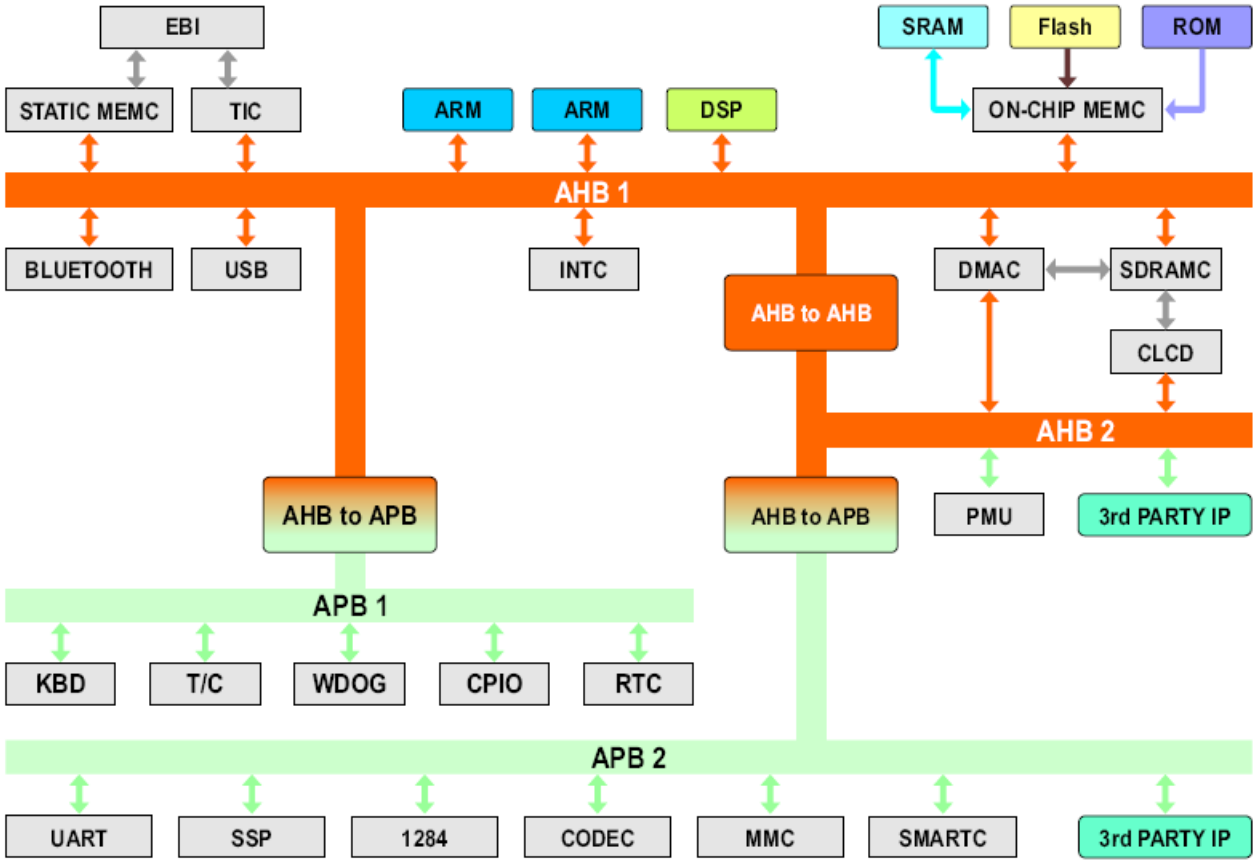
Platform

- **A** platform **is a suite of reusable parts (IP) of many system designs in a limited spectrum of applications**



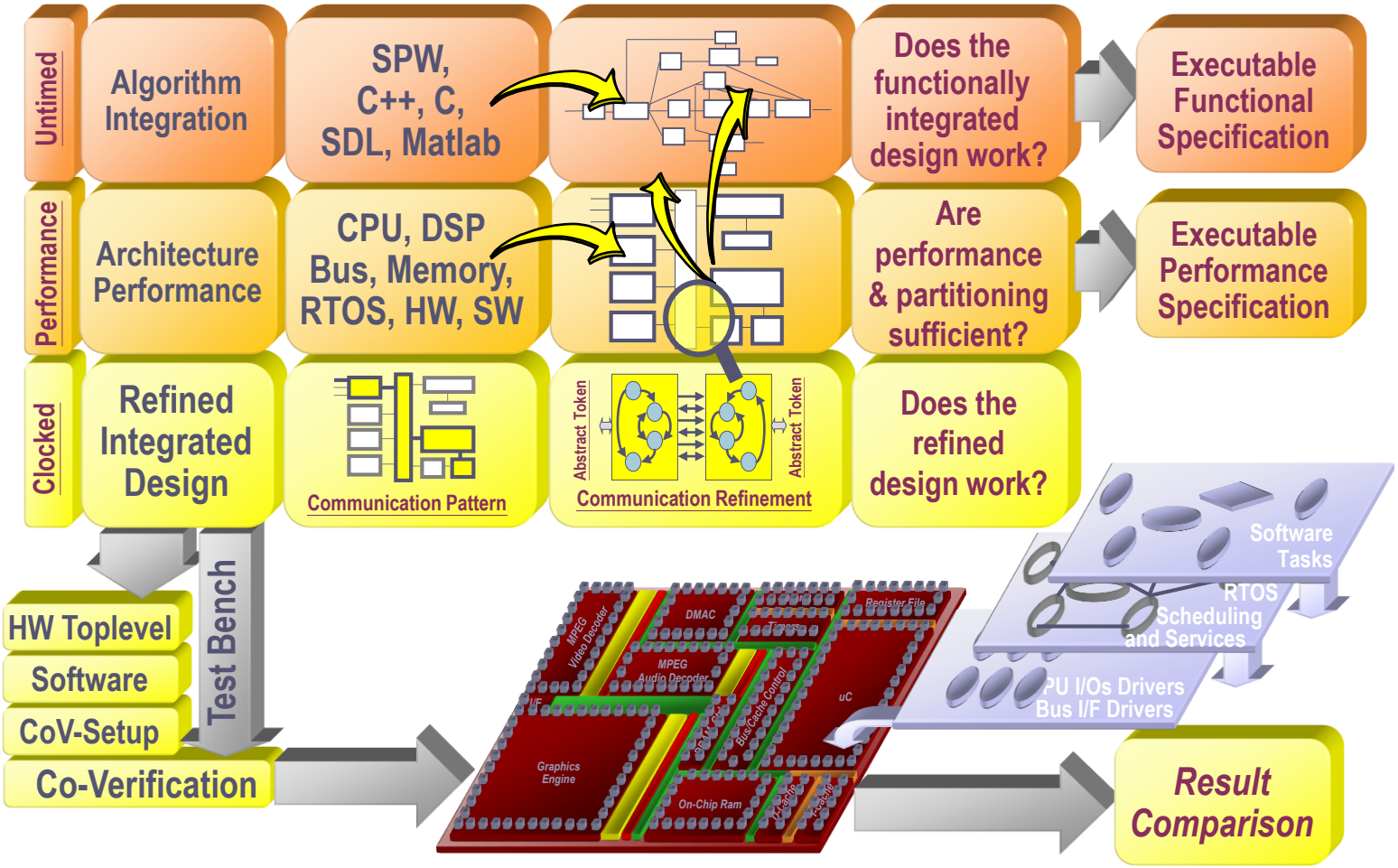
Source: SOC Design Overview /MOE, R.O.C.

Platform Example



Wipro's ARM-based SoC-RapTor Platform

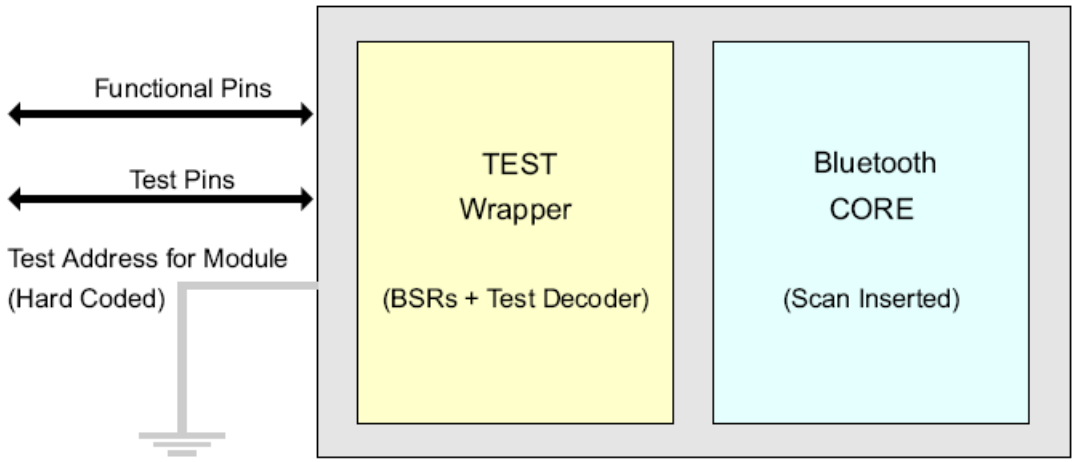
Hardware, Software and Testbench Export



Source: Cadence

DFT Strategy

- DFT is usually implemented using a full scan, muxed flip-flop of scan insertion.
- For embedded memories, Built in Self-test (BIST) and Module Test are best used.

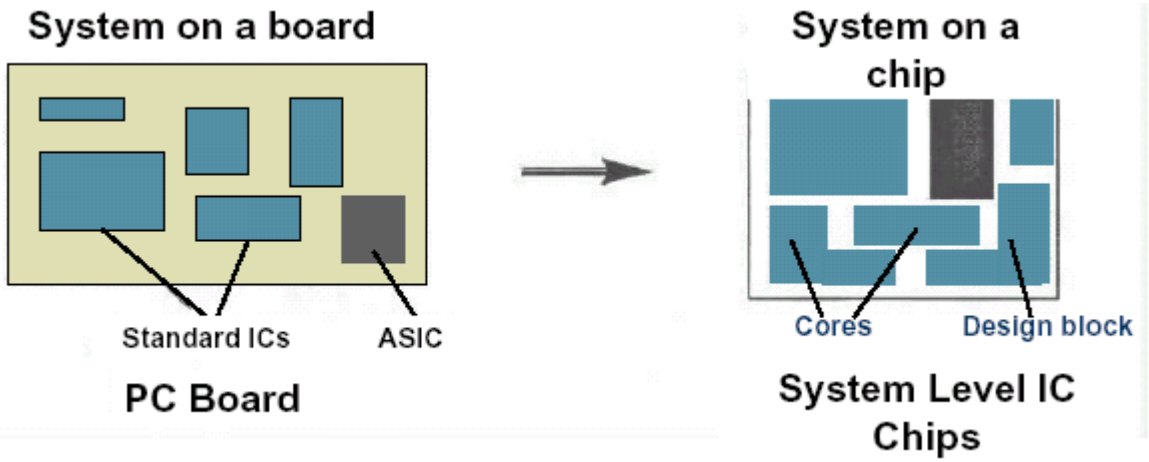


Benefits of Platform-based Design

- **Simplify backbone design:**
  - A platform provides an architecture reference which is proved to be a applicable architecture.
  - Simple modification is enough to be suitable to similar systems.
- **Save repetitive design time:**
  - Existing IPs for the platform can be adopted to accelerate the build up time.
  - Based on existing platform ease the replace of custom design.
- **Ease the verification:**
  - The environment provided by a platform helps to verify the custom modification in each step.
- **Early evaluation:**
  - A virtual prototyping provides early system performance data and H/S partitioning information.

Benefits of Using SoC

- Reduce overall system cost
- Increase performance
- Lower power consumption
- Reduce size



SoC - New Design Era

New design consideration

– Design methodology ◂ Platform-based design ▸

– Functionality implementation

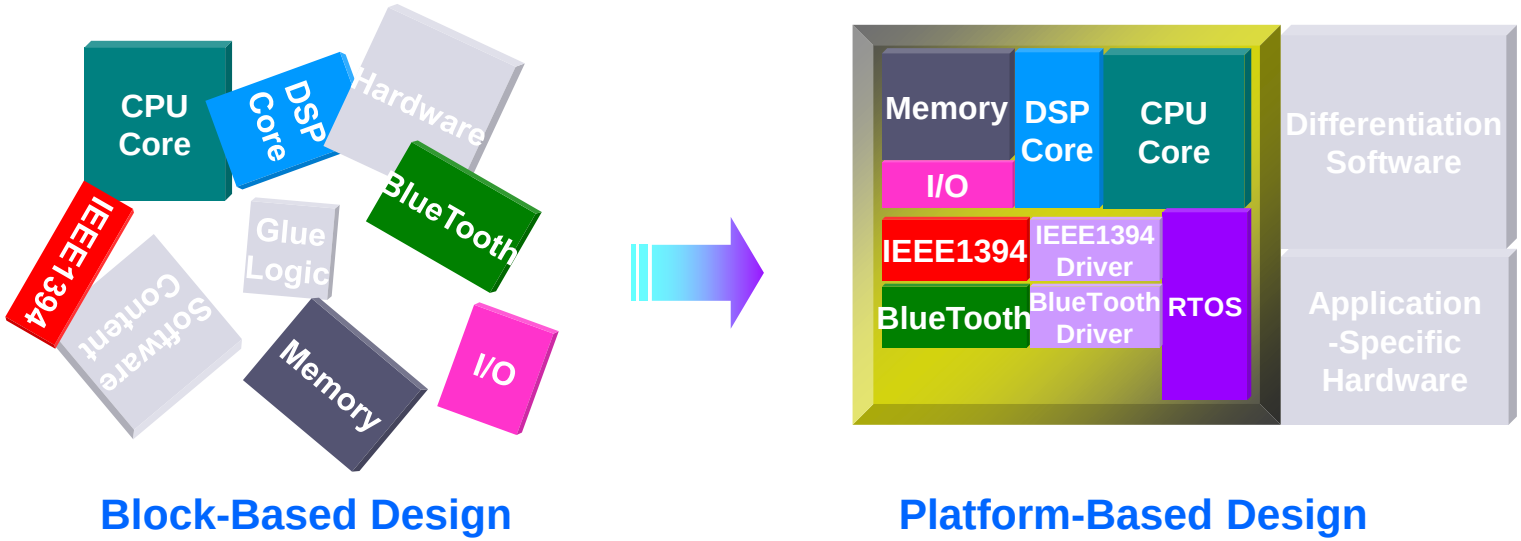
- Personal reuse
- In-house reuse
- IP reuse
- Architecture reuse
- Parameterized and blockwise design
- IP Compiler/Generator

Reuse without redesign

– Multi-level design descriptions

– Physical design consideration/constraint

The New System Design Paradigm



Block-Based Design

Platform-Based Design

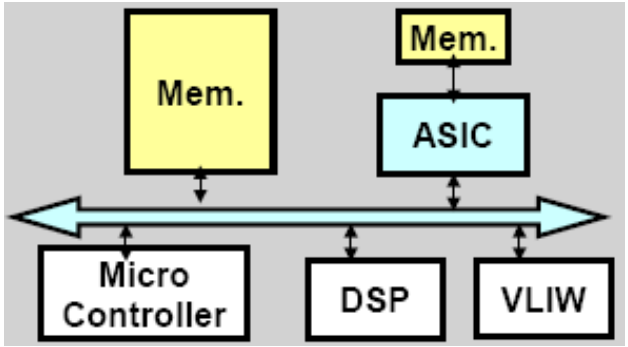
Orthogonalization of concerns: the separation

of function and architecture,

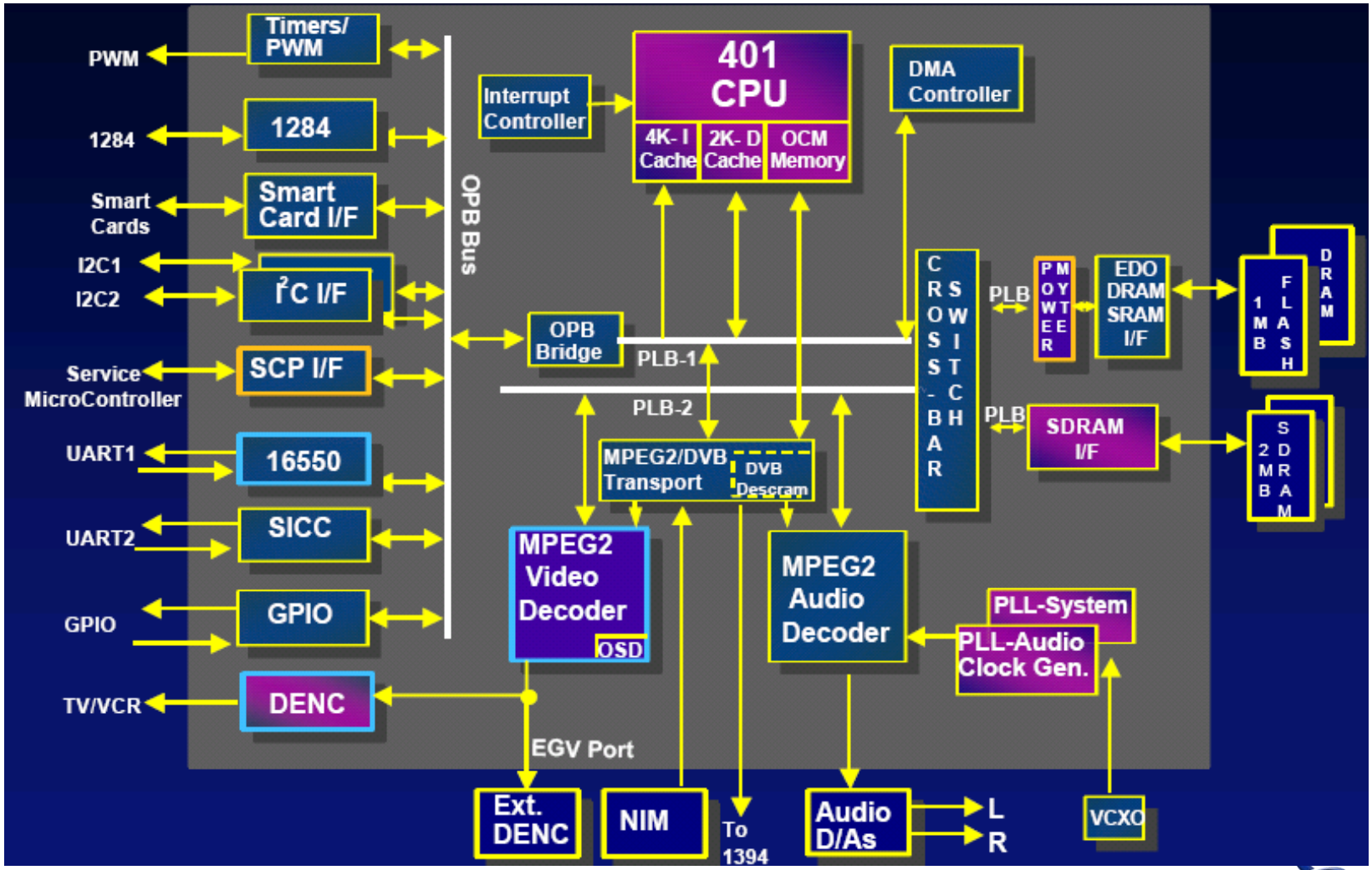
of communication and computation

SoC Current Status

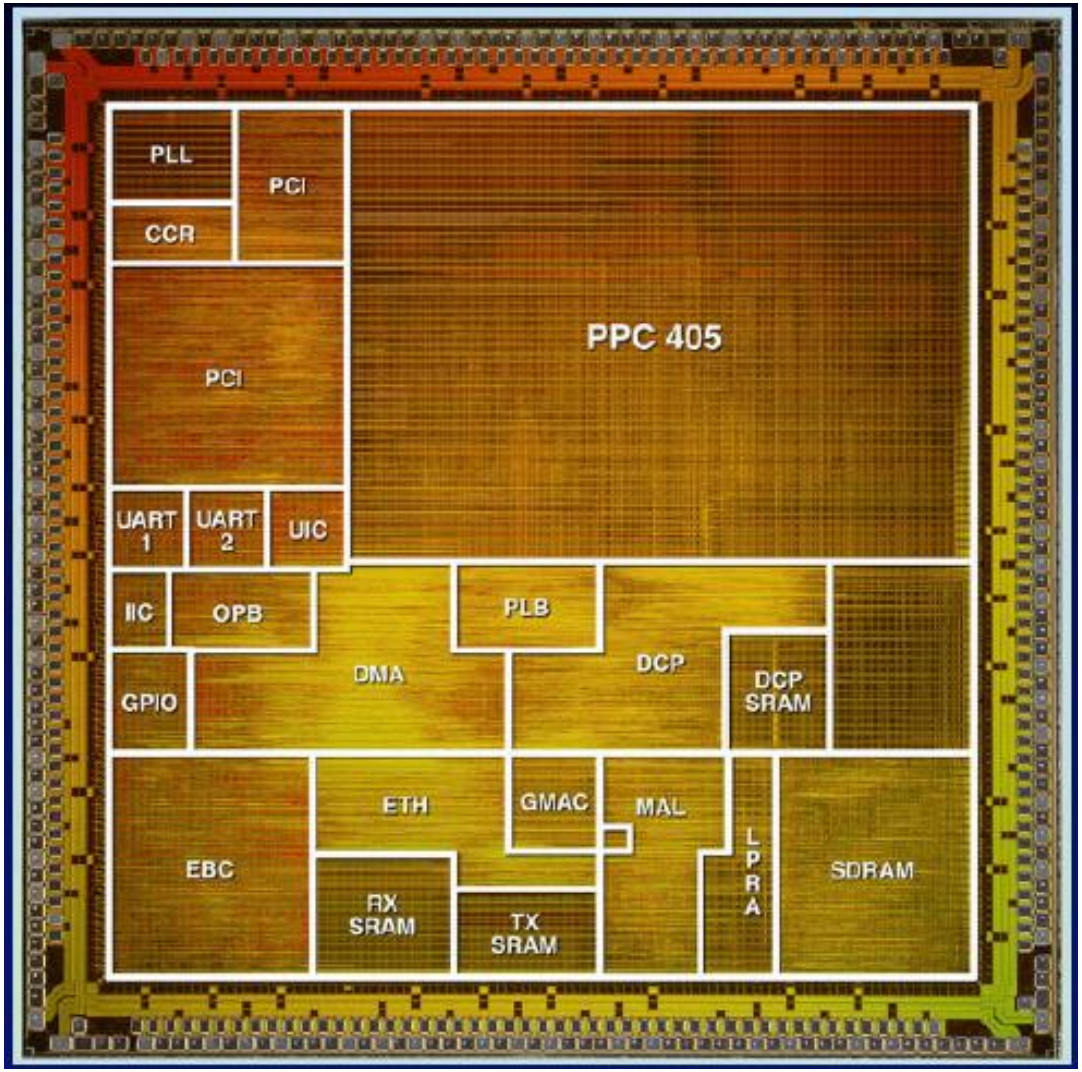
- Time-to-market pressure
- ASIC/ASSP ratio: 80/20 in 2000, but 50/50 now
- In-house ASIC design is down, replaced by off-the-shelf, programmable ASSP
- Heterogeneous multi-processor SoC platform
- Problem is that each system is an ad-hoc solution
  - No effective programming model
  - Poor SW productivity



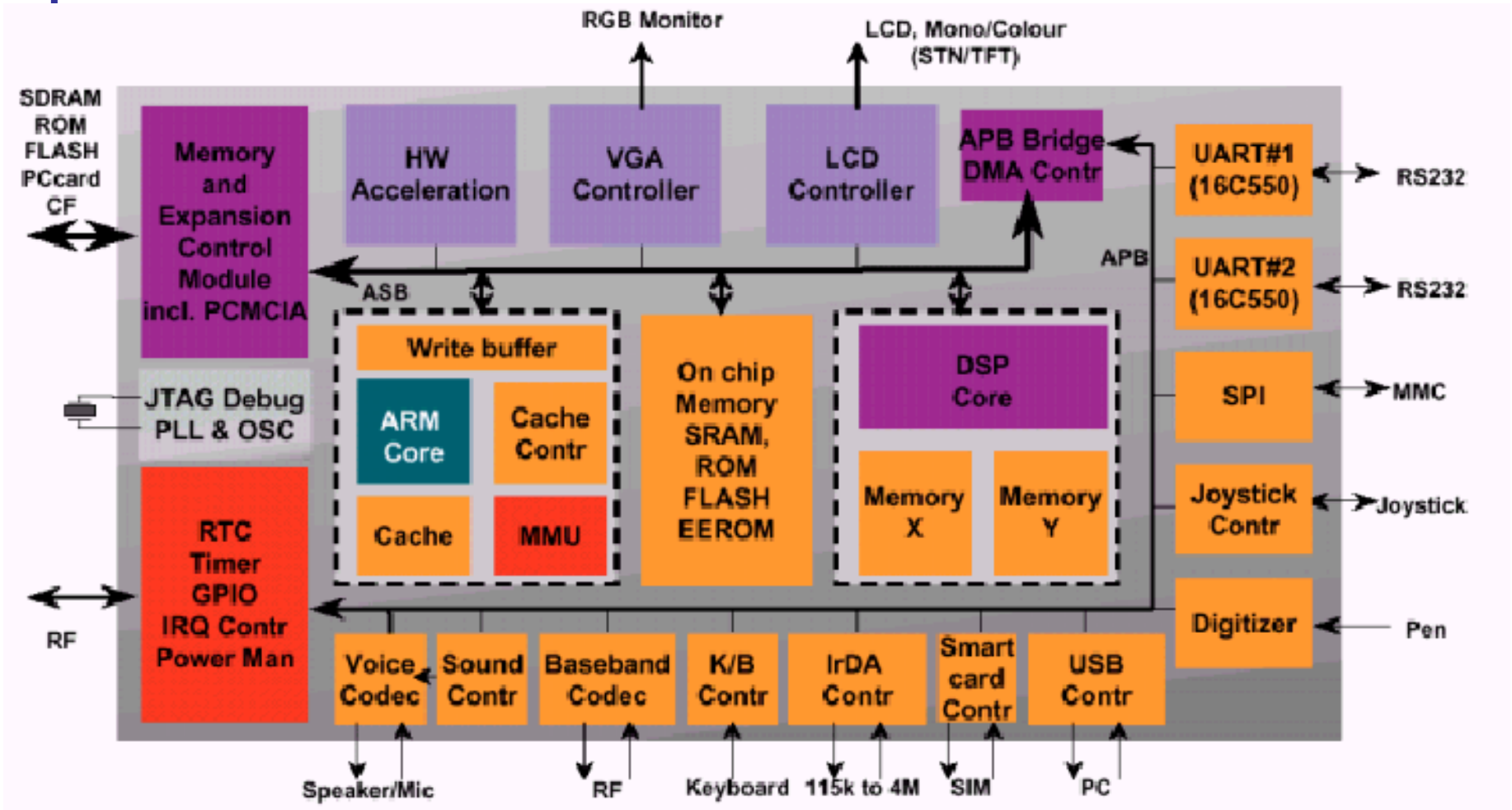
Set Top Box Controller



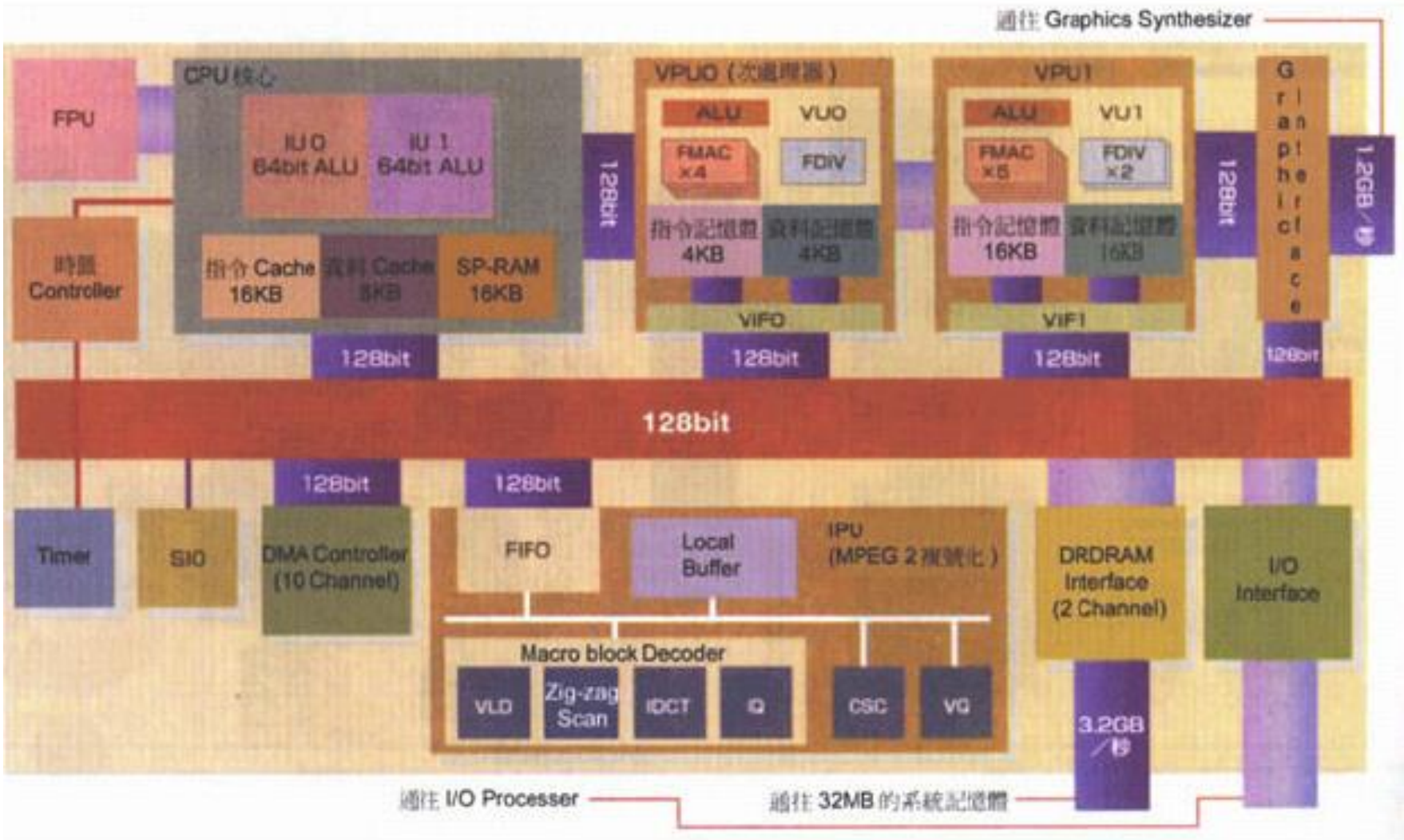
IBM's SoC


PLL
PCI
CCR
PPC 405
PCI
UART 1
UART 2
UIC
IIC
OPB
PLB
DCP
GPIO
DMA
DCP SRAM
ETH
GMAC
MAL
EBC
LPRA
SDRAM
RX SRAM
TX SRAM

Generic Wireless / Computing



Emotion Engine in PS2



Snapshot

- 30mm wafer and Pentium 4™

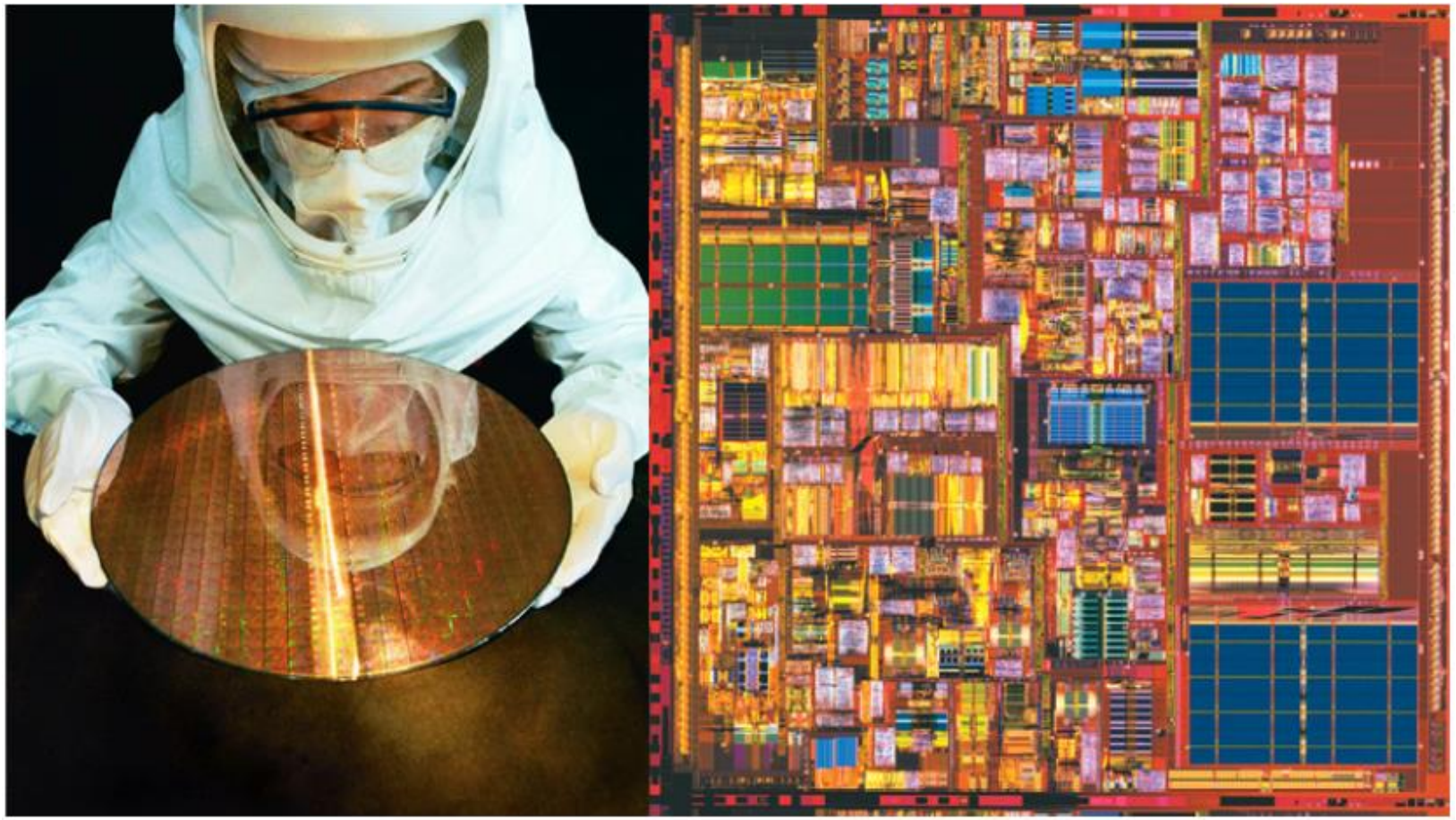
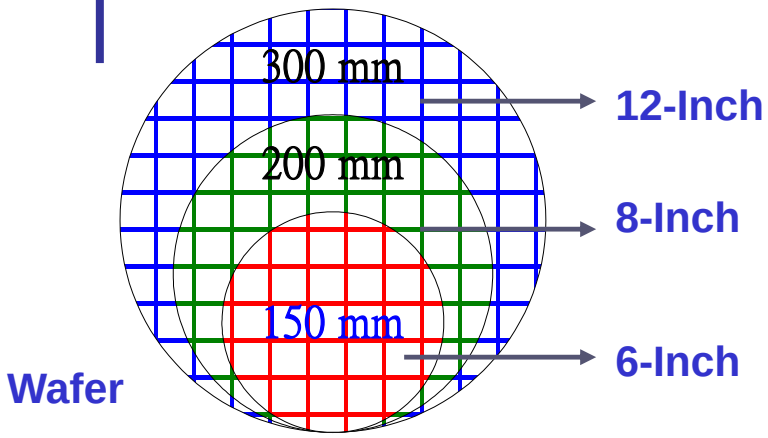
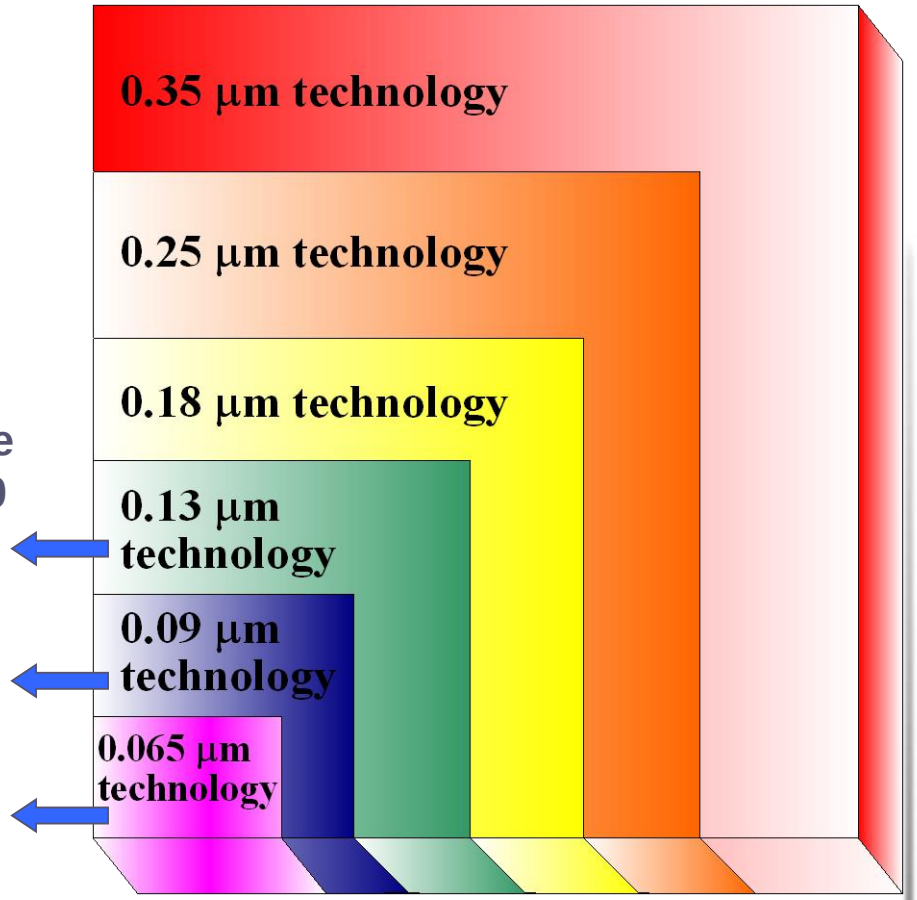


Photo courtesy of Intel

Feature Technology and Size





When compared to the **0.18-micron** process, the new **0.13-micron** process results in less than 60 percent the die size and nearly 70 percent improvement in performance

The **90-nm** process will be manufactured on 300mm wafers

NEC devises low-k film for second-generation **65-nm** process