Introduction to IC

Instructor: NCTU

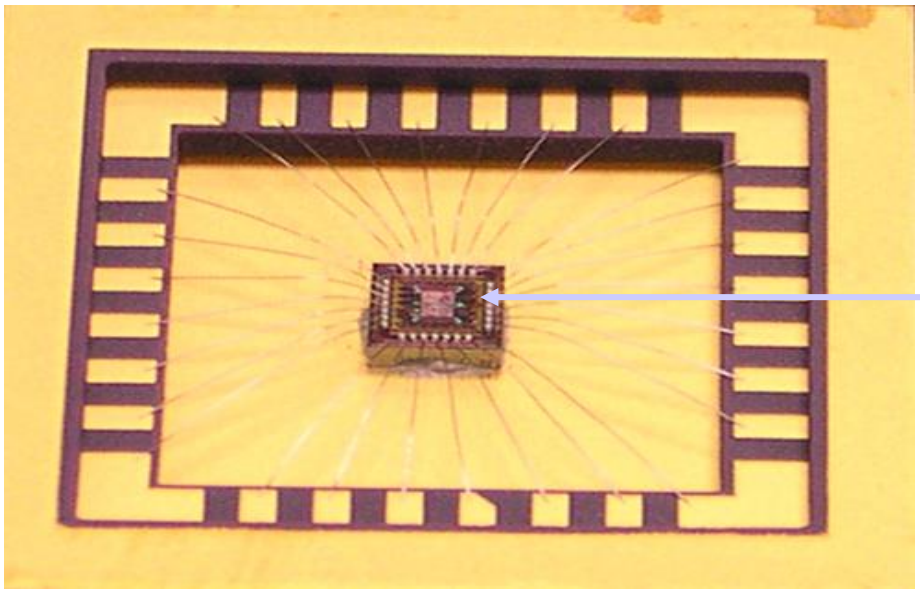
Outline

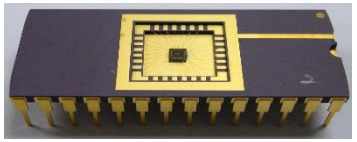
- Introduction to Integrated Circuits (IC or Chip)

Chip Everywhere!

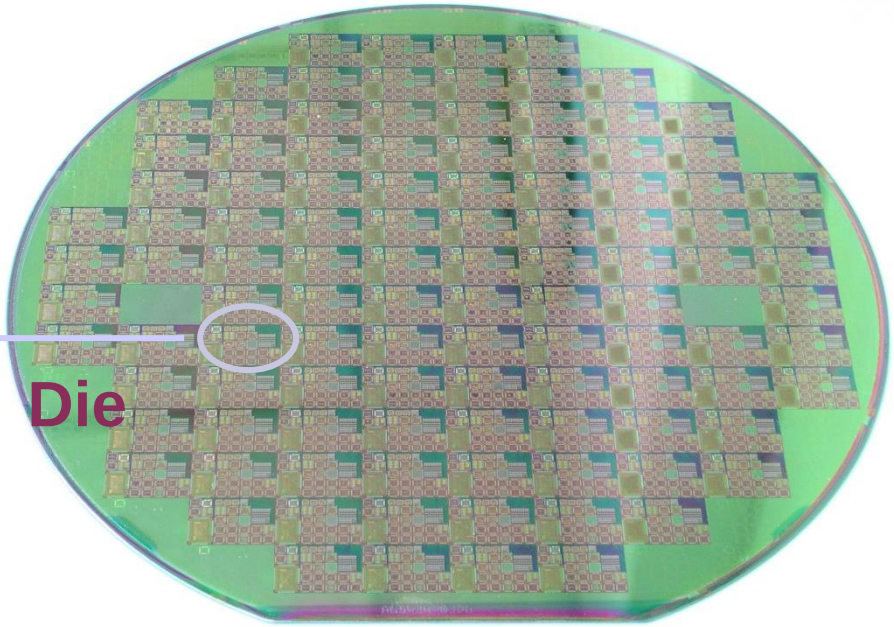
Wafer & Die & Packaging

Assembly/Packaging

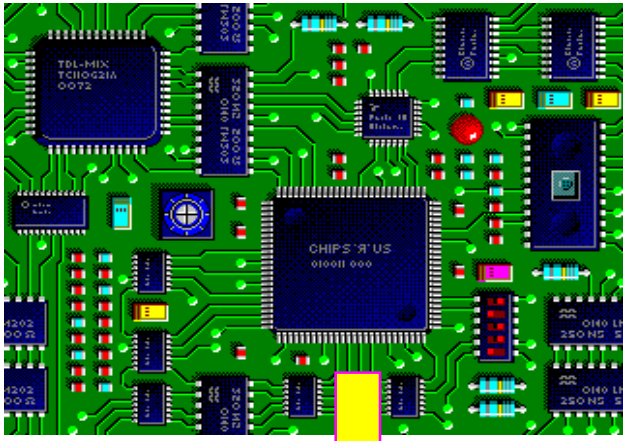


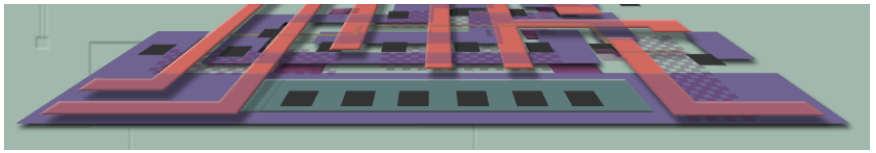


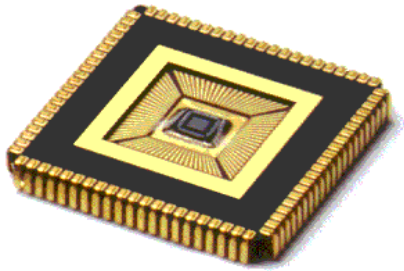
Wafer

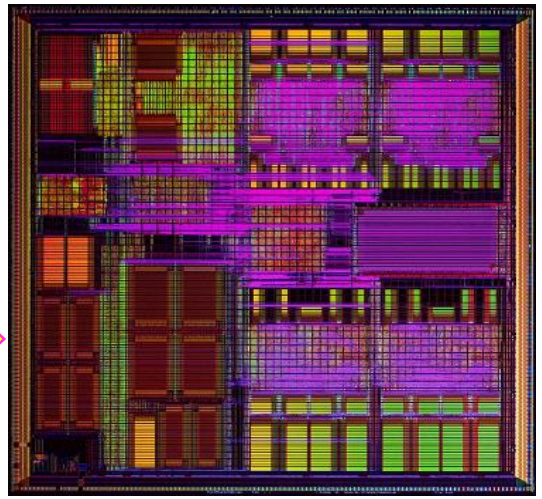


Integrated Circuits (ICs)

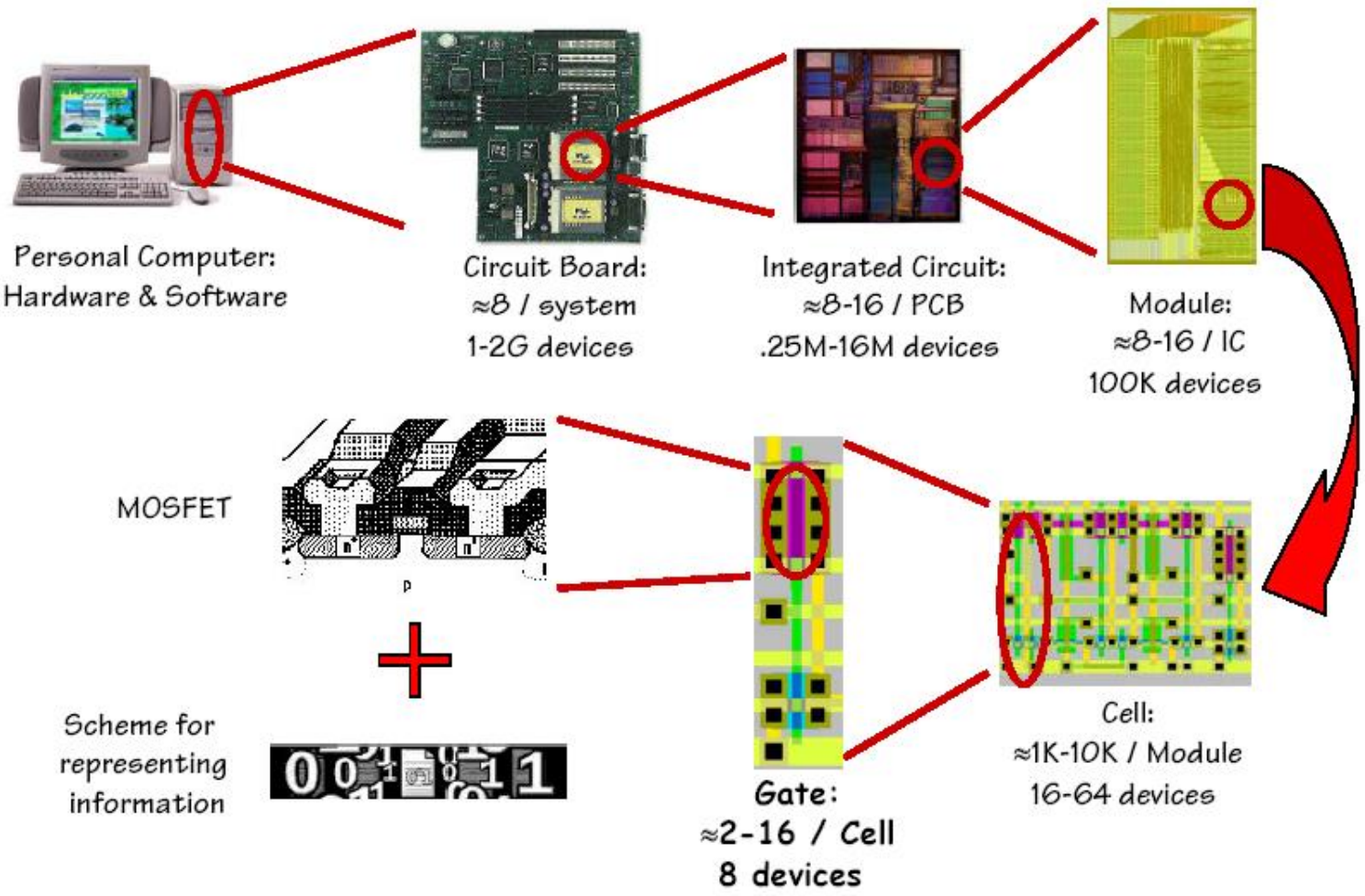








Modern System Engineering

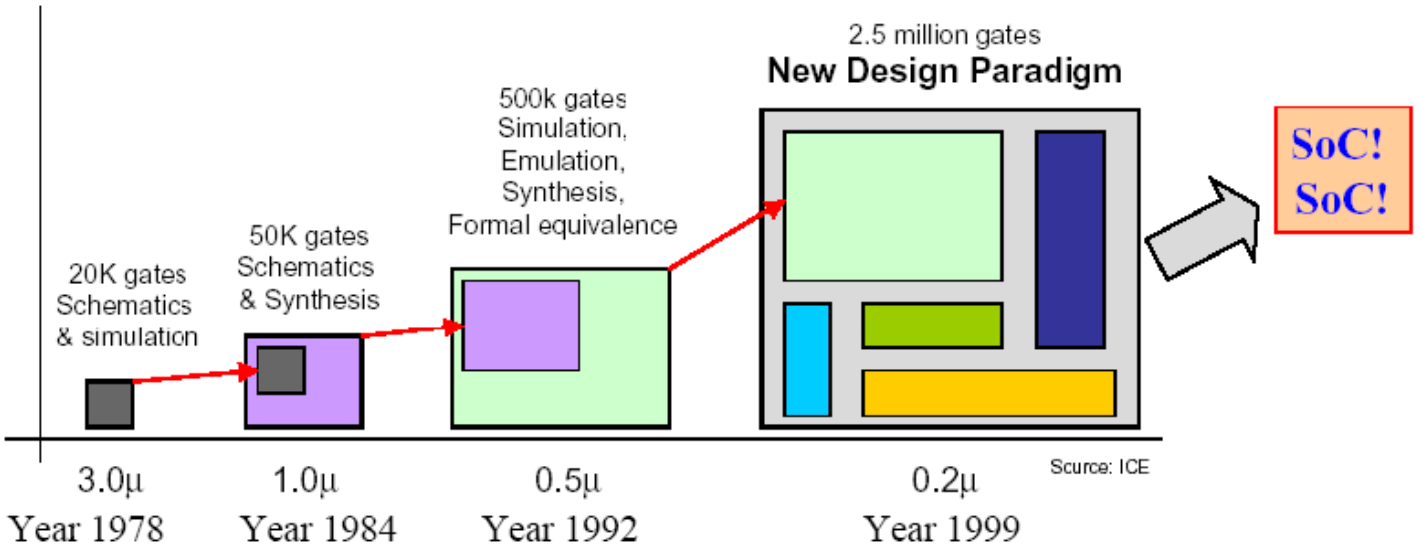


IC Design History

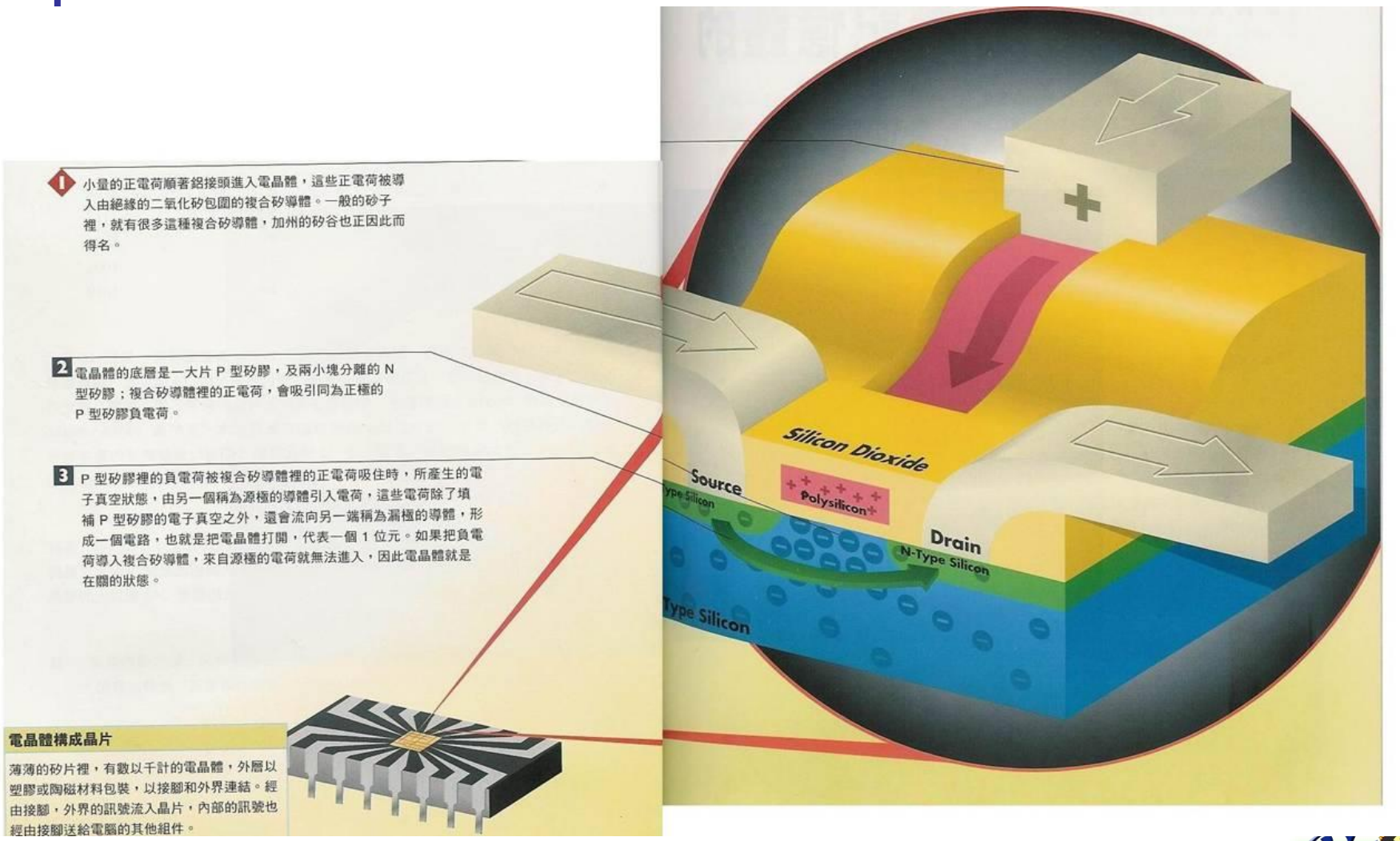
- **In 1970's**
  - The layout was the design
  - IC design was an ART
  - No simulation, no verification
- **In 1980's**
  - Technology CMOS 2.0~1.0
  - Design complexity 30K~400K transistors
  - Daisy, DEC (2MB RAM, .5GB HD, 1MIPS)
  - Logic simulation, Verification, CAD layout
  - ASICs
- **In 1990's**
  - Technology CMOS 1.0~0.18
  - Design complexity 400K~10M gates
  - SUN Sparc, Pentium4 (4GB-16GB, 1 Terabyte HD)
  - Synthesis, P&R
  - ASICs, Processors, Embedded software, FPGA
- **In 2000's**
  - ?

Evolution of Microelectronics

- **Today's Silicon process technology**
  - 0.13μm CMOS
  - ~100 M of devices, 3GHz internal clock
- **Yesterday's chips are today's function blocks**

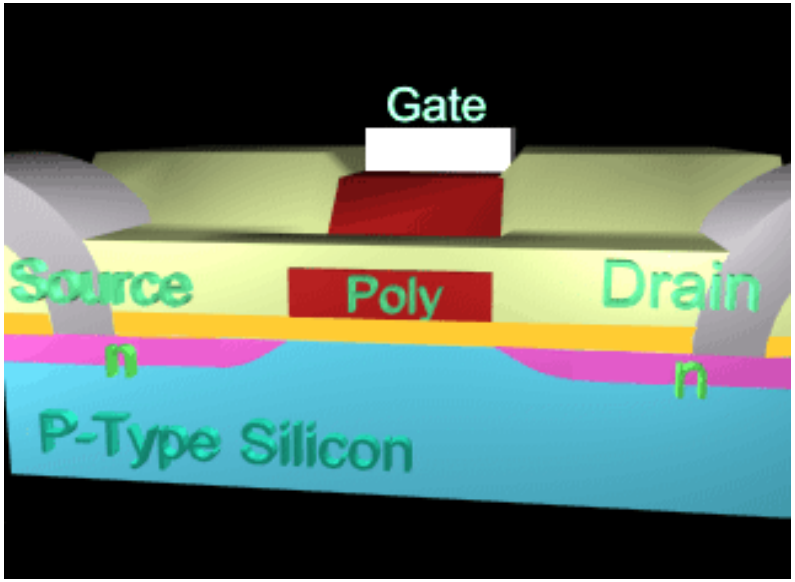


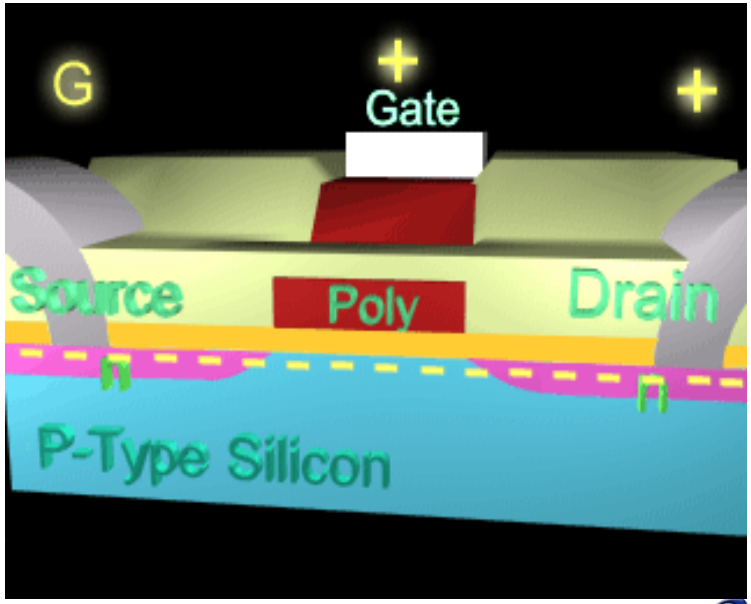
MOS (Metal Oxide Semiconductor)



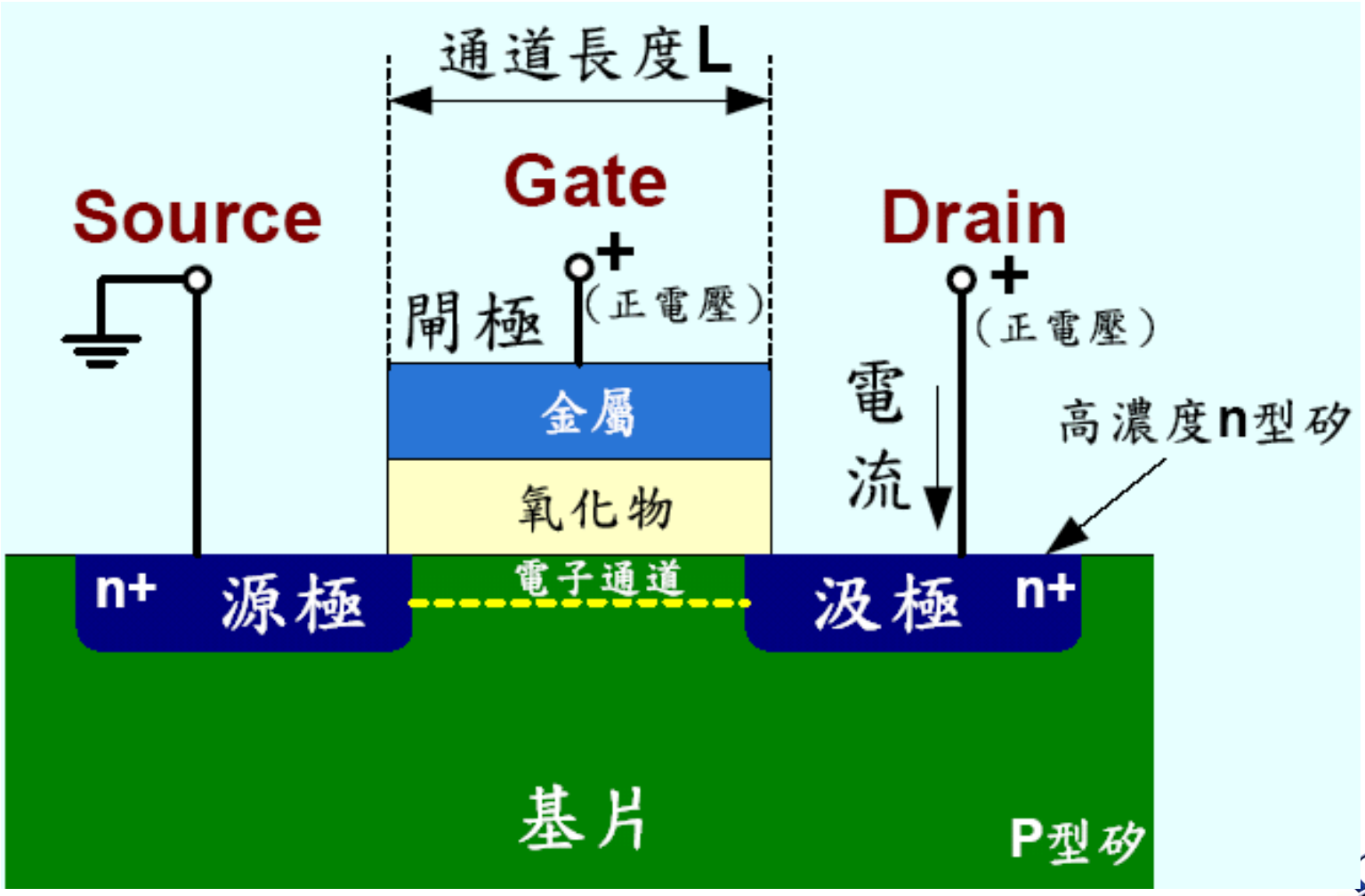
N-channel Metal-Oxide-Semiconductor

- **NMOS**
  - Gate – poly
  - Source, Drain – n-type
  - Substrate – p-type
  - Carrier – electrons





MOS電晶體示意圖


通道長度L
Gate
Source
Drain
閘極
+
(正電壓)
+
(正電壓)
電流
金屬
氧化物
高濃度n型矽
n+
源極
電子通道
汲極
n+
基片
P型矽

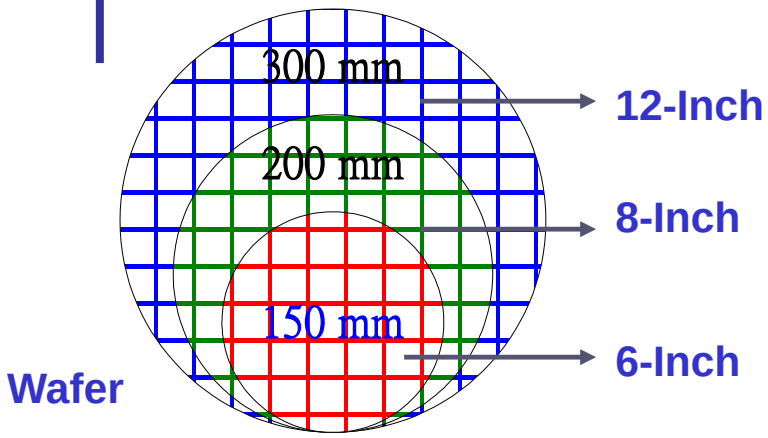
SOC相關技術

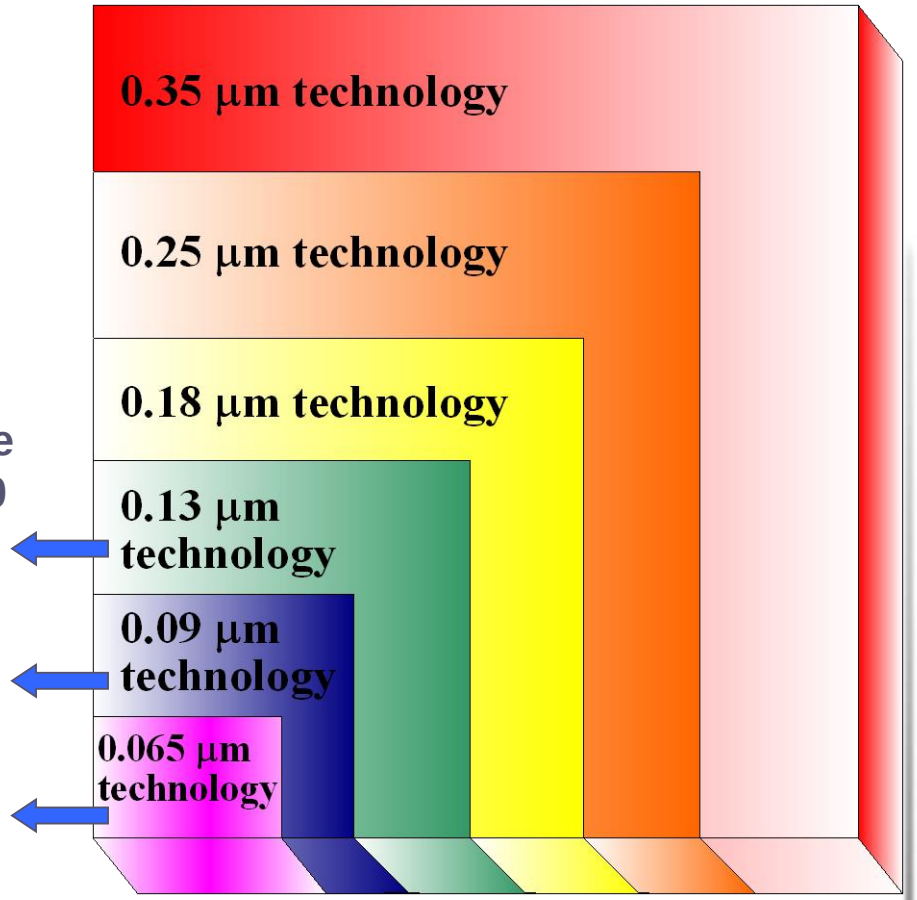
- 製程技術 (Process Technology)
- 設計 (Design)
- 測試 (Testing)
- 封裝 (Packaging)
- 輔助設計工具 (Electronic Design Automation, EDA tools)

VLSI-related Topics

- **VLSI design**
  - Designs of layouts, circuits, logic gates, architectures, or behaviors
- **VLSI technology**
  - Process technology of fabricating transistors in VLSI chips (UMC, TSMC)
- **VLSI testing**
  - 1/3 of total costs, design for testability
- **VLSI CAD**
  - All the related EDA (electronic design automation) tools during VLSI designs

Feature Technology and Size



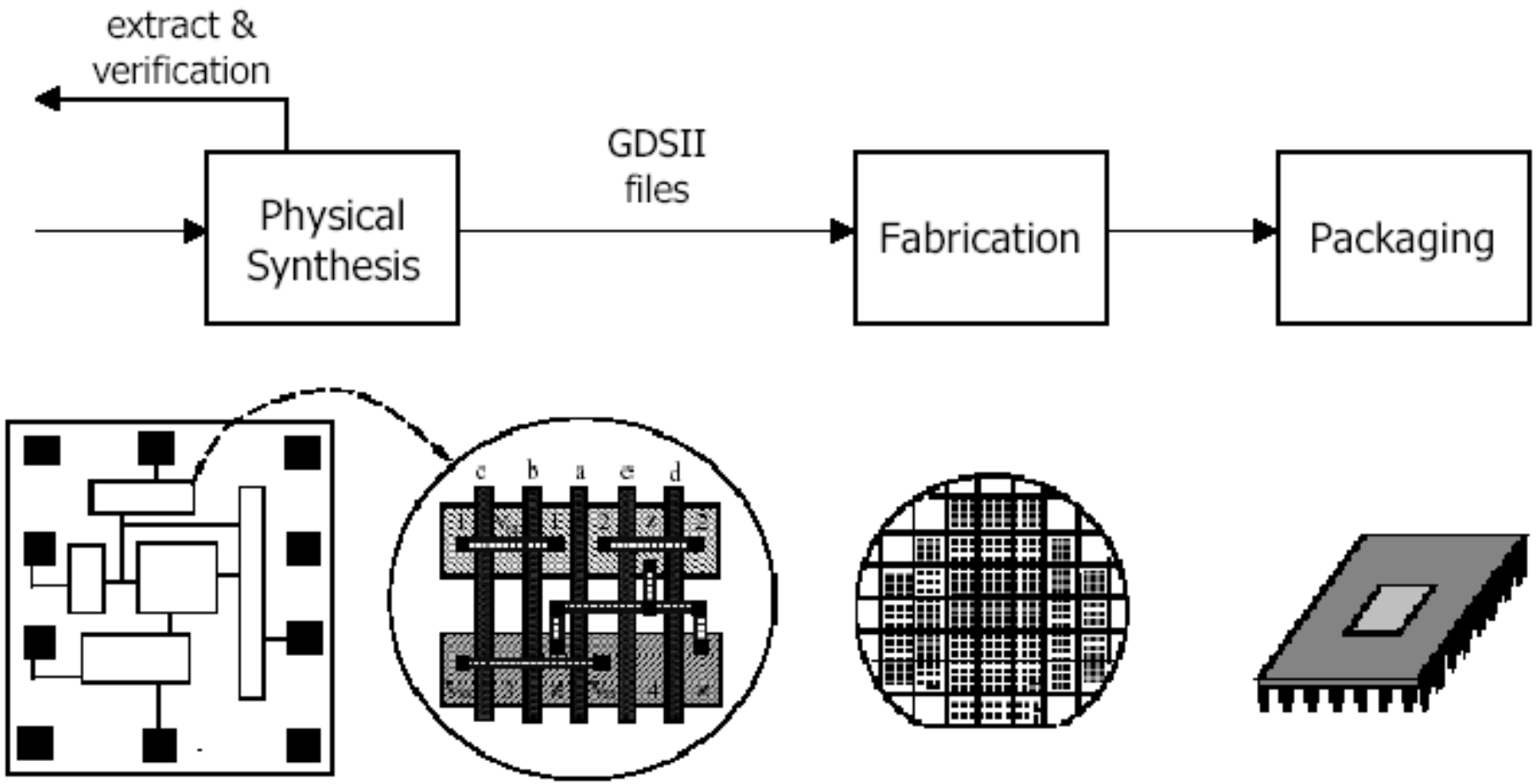


When compared to the **0.18-micron** process, the new **0.13-micron** process results in less than 60 percent the die size and nearly 70 percent improvement in performance

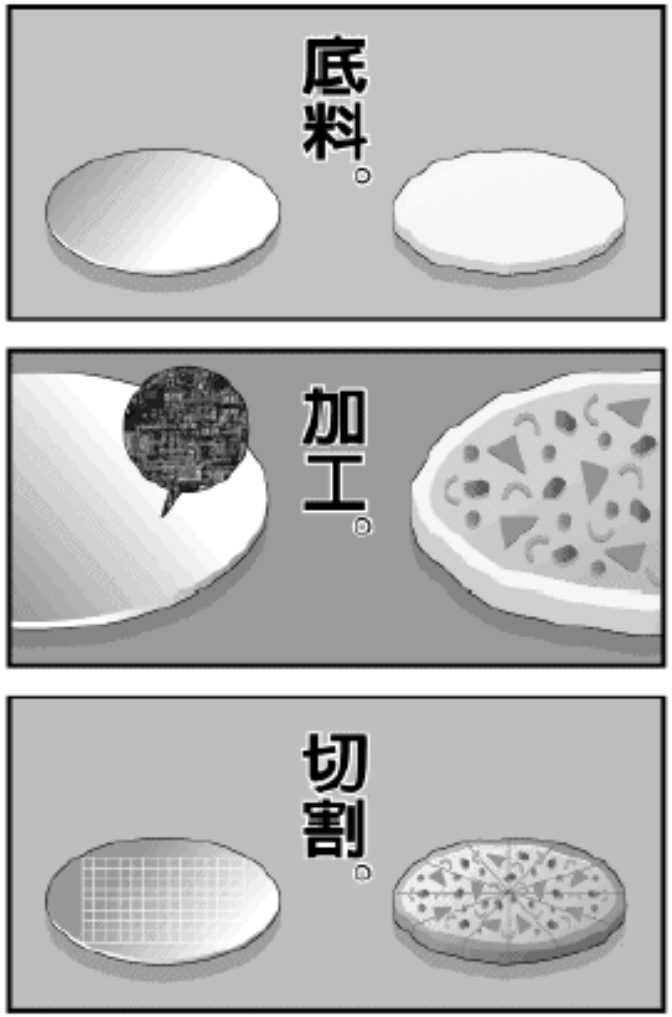
The **90-nm** process will be manufactured on 300mm wafers

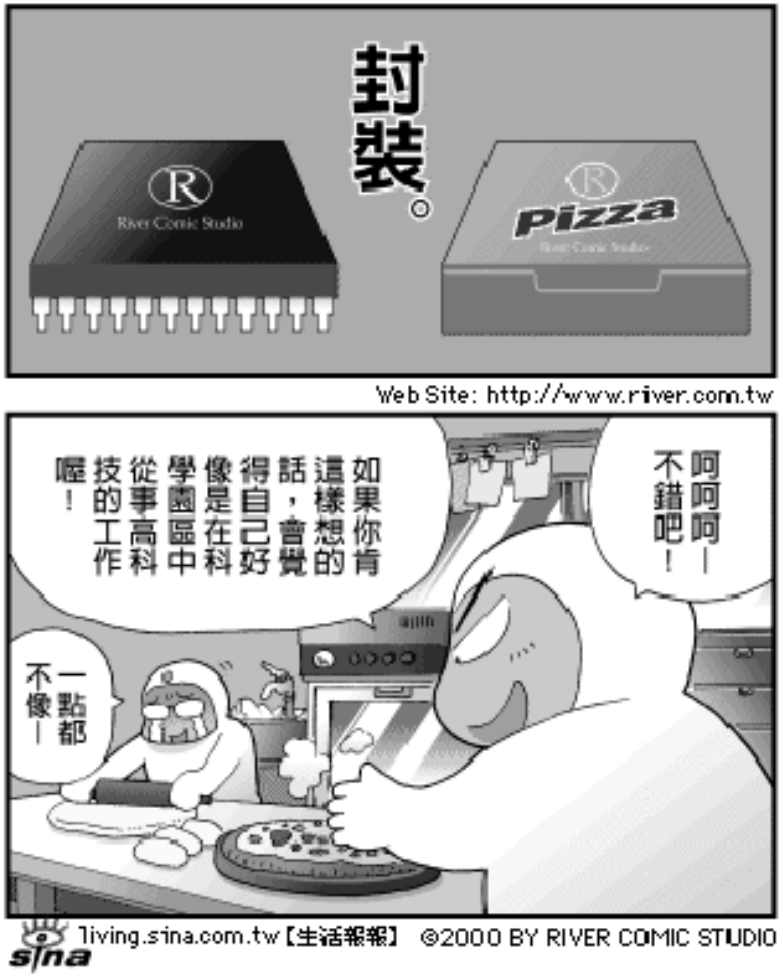
NEC devises low-k film for second-generation **65-nm** process

IC設計與晶圓代工


extract &
verification
Physical
Synthesis
GDSII
files
Fabrication
Packaging
c b a e d

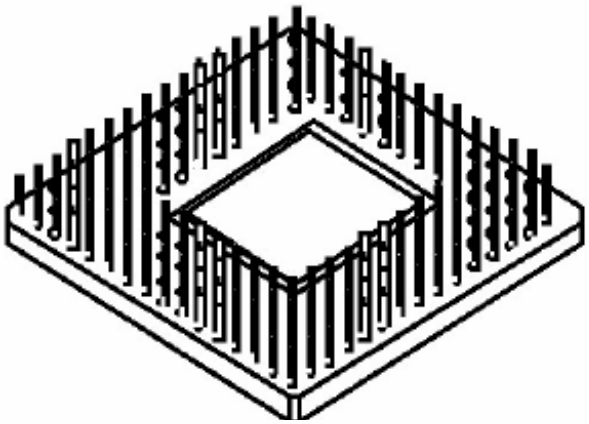
IC Fabrication

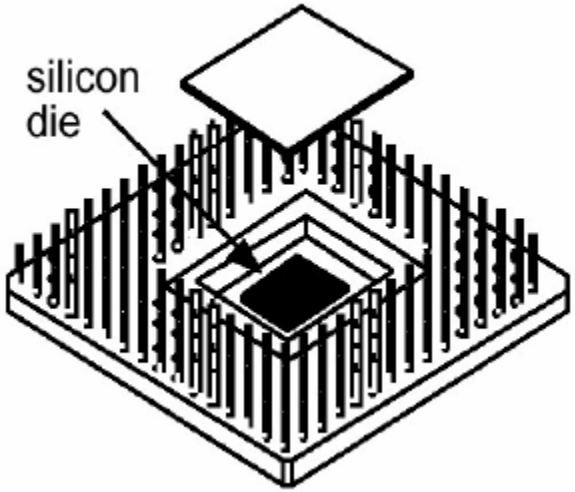


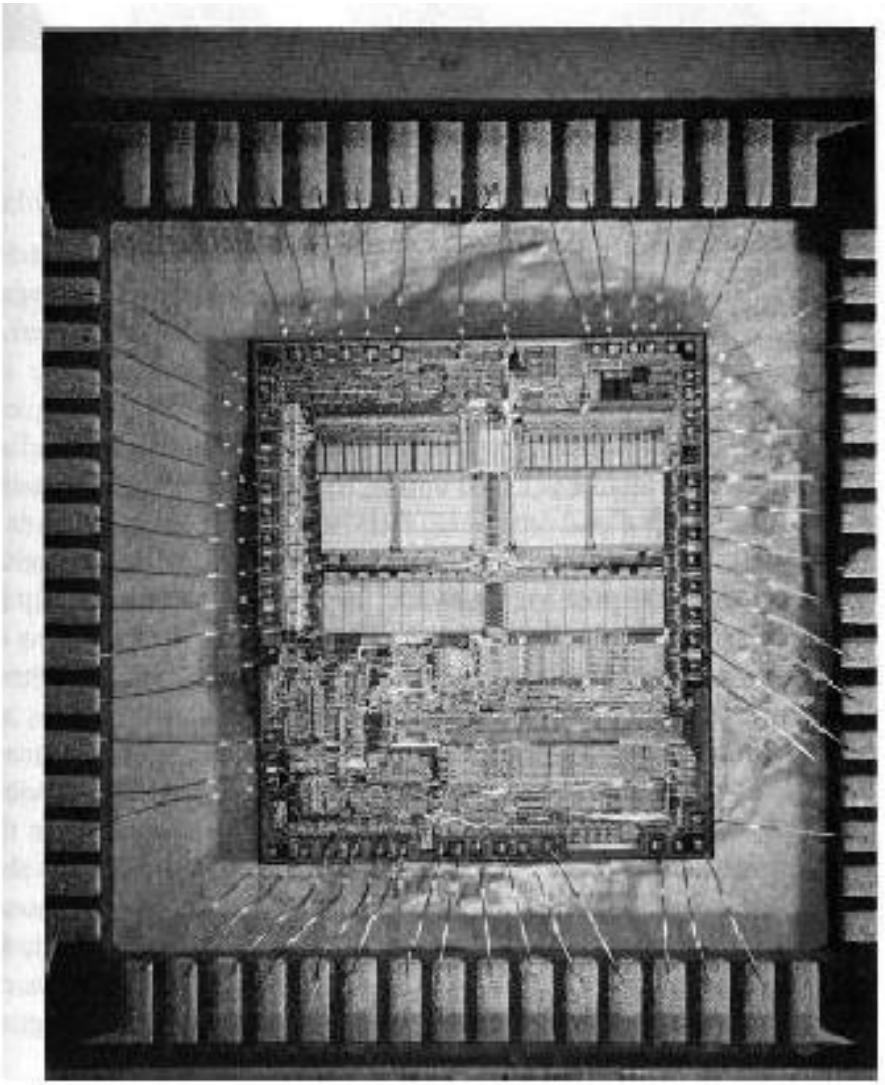


Sawing a Wafer into Chips

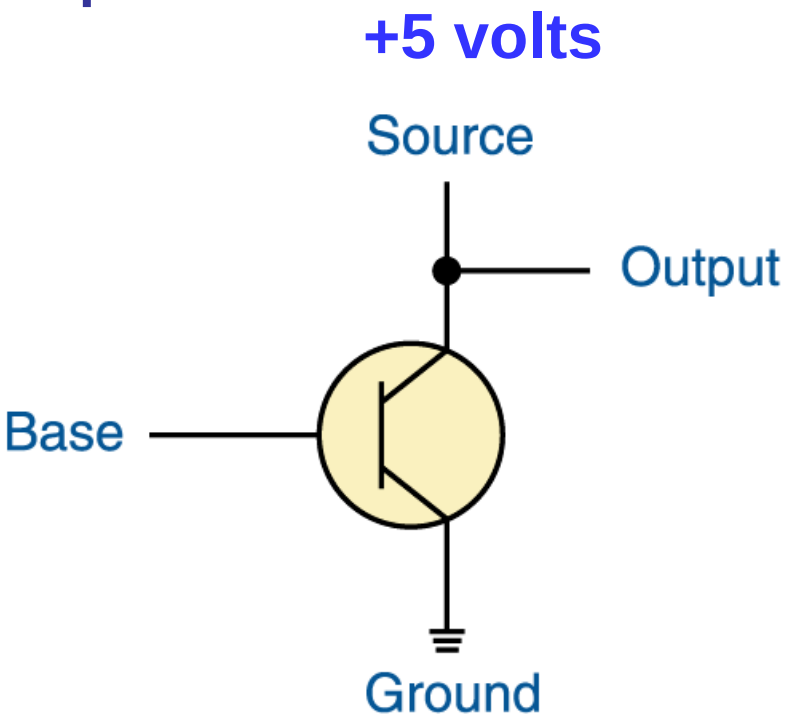
IC and Die







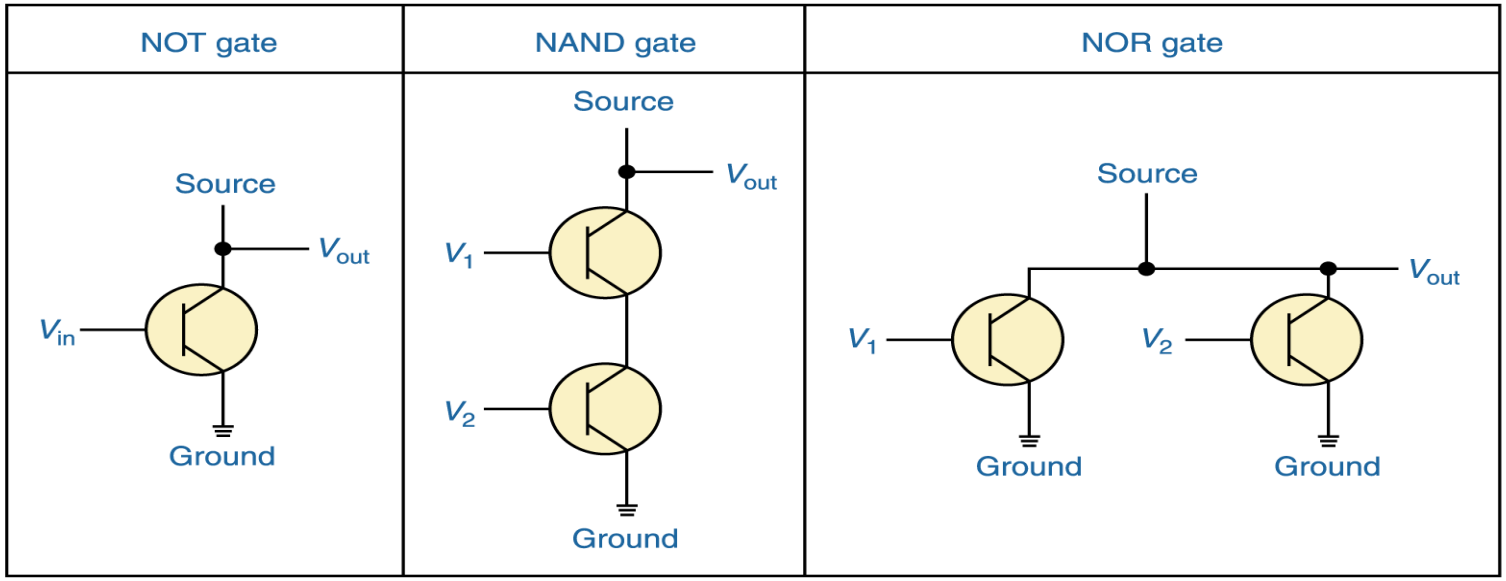
Constructing Gates



- **A transistor has three terminals**
  - A source (feed with 5 volts)
  - A base
  - An emitter, typically connected to a ground wire
- **If the base signal is high (close to +5 volts), the source signal is grounded and the output signal is low (0). If the base signal is low (close to 0 volts), the source signal stays high and the output signal is high (1)**

Constructing Gates

It turns out that, because the way a transistor works, the easiest gates to create are the NOT, NAND, and NOR gates

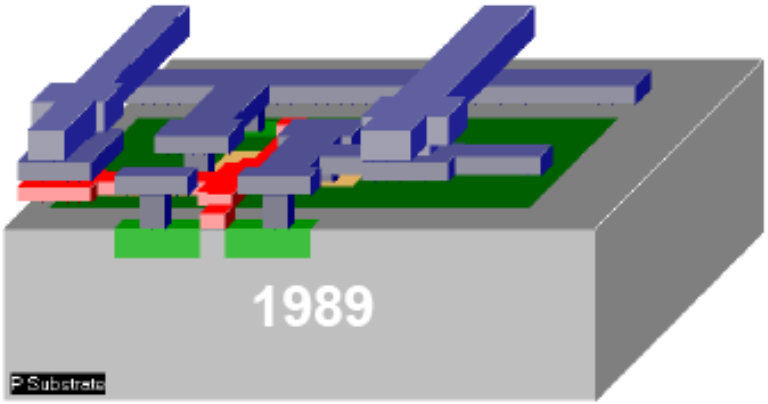


V_{in}	V_{out}
0	1
1	0

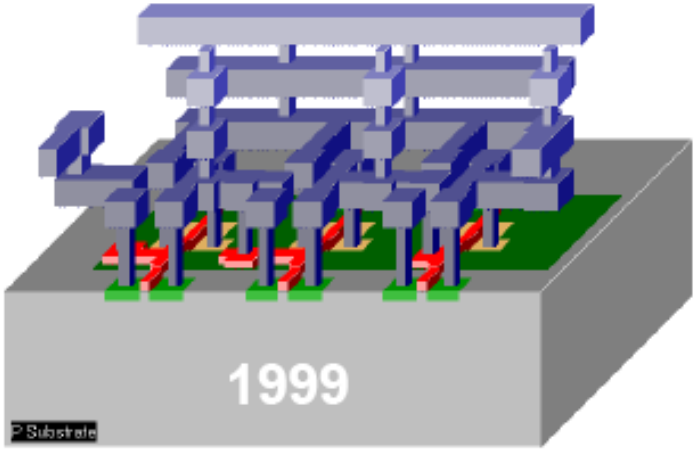
V_1	V_2	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

V_1	V_2	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0

Changes in Real ICs



0.8µm CMOS



0.18µm CMOS

Technology:	0.8µm	0.18µm	0.07µm
# of Metal layers:	2~3	6	8-9
G.W. Aspect ratio (t/w):	~0.8	~1.8	~2.7
Wire length(m/chip):	~130	~1,480	~10,000

Interconnects Start to Dominates Cost and Performance

Interconnect starts to be main design constraints

Source: L.-R. Zheng, KTH

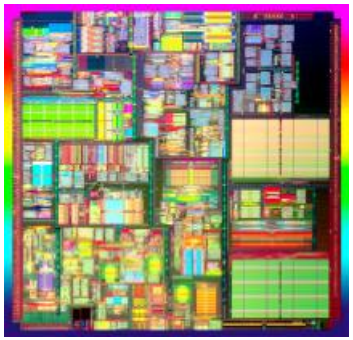
Moore's Law in Action

- **Example:**

  Intel Pentium 4 microprocessor evolution

  - 0.18 micro technology
    - 42M transistors
    - Die size: 217 mm^2

  - 0.13 micro technology
    - 55M transistors
    - Die size: 146 mm^2



Source: Intel

Snapshot

- 30mm wafer and Pentium 4™

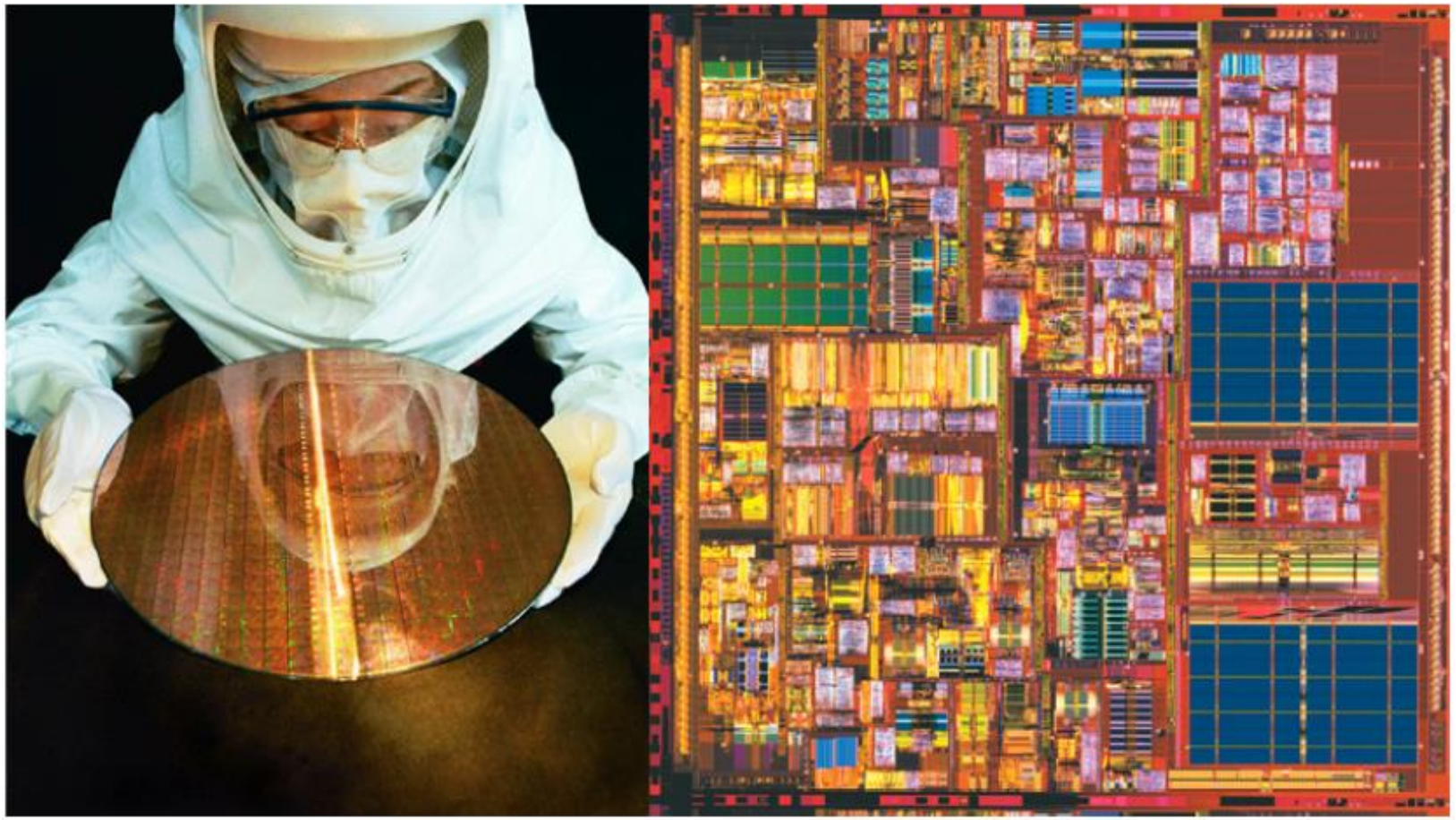
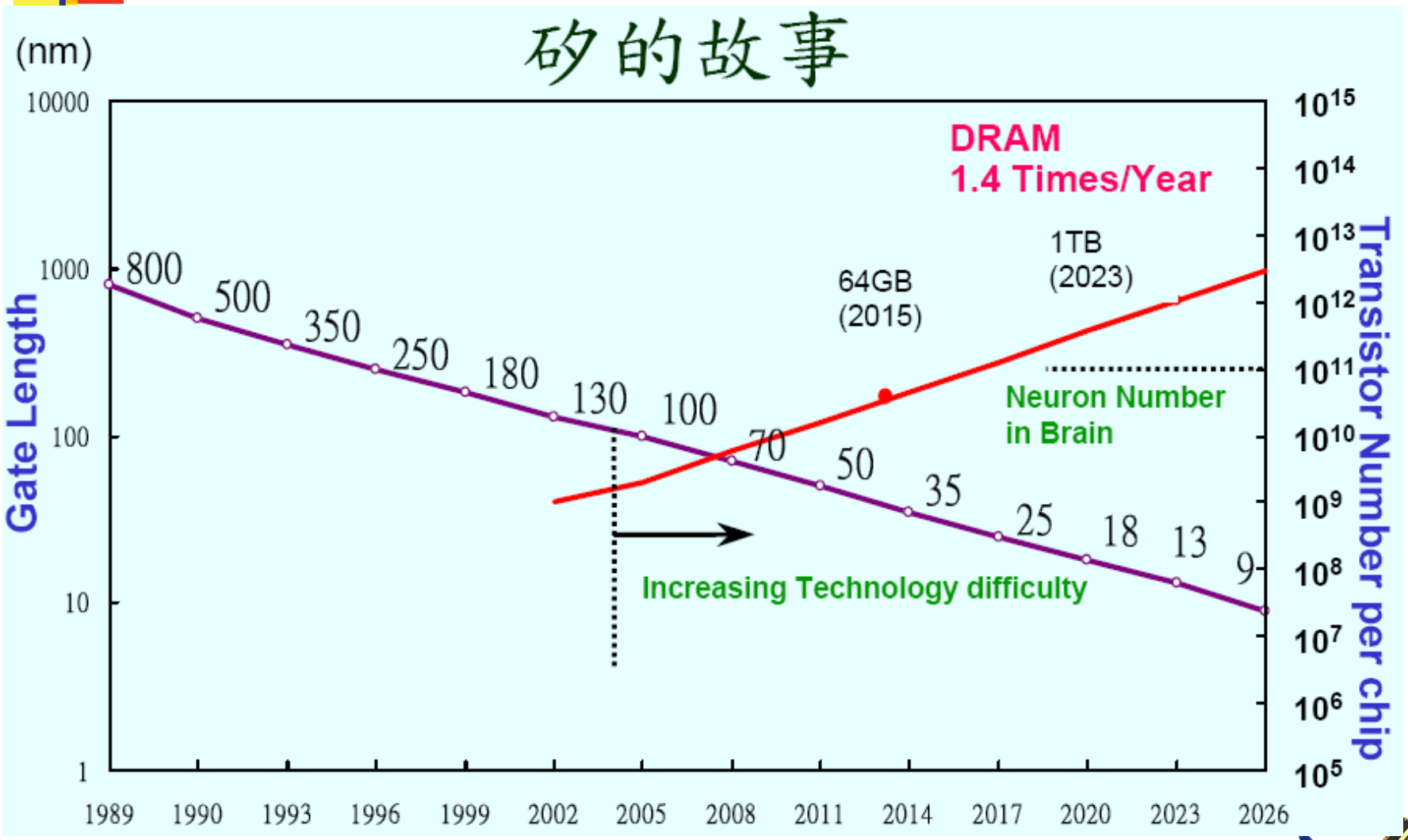


Photo courtesy of Intel

製程技術演進與預測


矽的故事
(nm)
10000
1000
100
10
1
Gate Length
800
500
350
250
180
130
100
70
50
35
25
18
13
9
DRAM
1.4 Times/Year
64GB
(2015)
1TB
(2023)
Neuron Number
in Brain
Increasing Technology difficulty
10^{15}
10^{14}
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
Transistor Number per chip
1989
1990
1993
1996
1999
2002
2005
2008
2011
2014
2017
2020
2023
2026

Expectation By SRC Roadmap

Year of first DRAM shipment	1995	1998	2001	2004	2007	2010
Minimum feature of size (mm)	0.35	0.25	0.18	0.13	0.10	0.07
Memory in bits/chip (DRAM/FLASH)	64M	256M	1G	4G	16G	64G
Microprocessor transistor per chip (2.3 times per generation)	12M	28M	64M	150M	350M	800M
ASIC (gate per chip)	5M	14M	26M	50M	210M	430M
Chip frequency (MHz) for a high-performance on-chip clock	300	450	600	800	1,000	1,100
Maximum number of wiring levels (logic), on chip	4-5	5	5-6	6	6-7	7-8
Power supply voltage (V) for desktop	3.3	2.5	1.8	1.5	1.2	0.9
Maximum power for high performance with heat sink (W)	80	100	120	140	160	180

Source: SIA (Semiconductor Industry Association) road map

System Development Flow

Applications

Specifications

傳輸距離： 100 m
功率消耗：2 W
功能：影像傳輸、
語音傳輸
螢　幕：176 x 220 pixel
65535 色
1.8 吋 TFT
其他

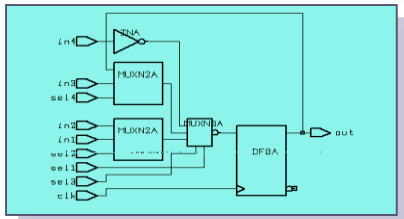
System Design

Hardware:
CPU,
RAM, I/O…

Software:
C,C++

Component Design

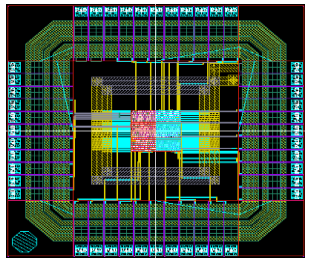
```
always @(posedge clk)
begin
  if (sel1) begin
     out=in1;
  else
     out=in2;
  end
end
```



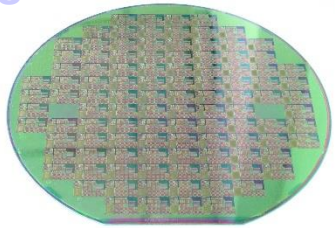
Synthesis

Placement & Routing

Layout

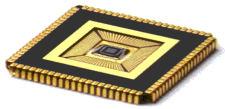


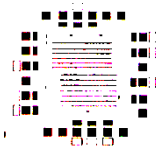
Fabrication



Testing

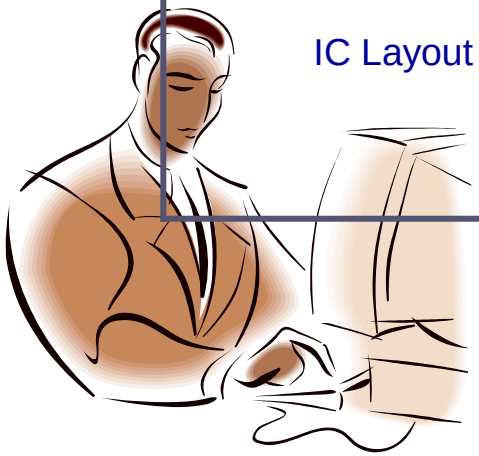
Marketing





IC Designers

Who	What to do
System Design Engineer ASIC Design Engineer IP Design Engineer Circuit Design Engineer CAD Engineer Test Engineer	Specification Definition Behavioral Design and Simulation Register Transfer Level (RTL) Design, Simulation and Testing Gate/Switch/Circuit Level Design, Simulation and Testing
IC Layout Engineer	Physical Layout Layout Verification Post-layout Verification (Simulation)



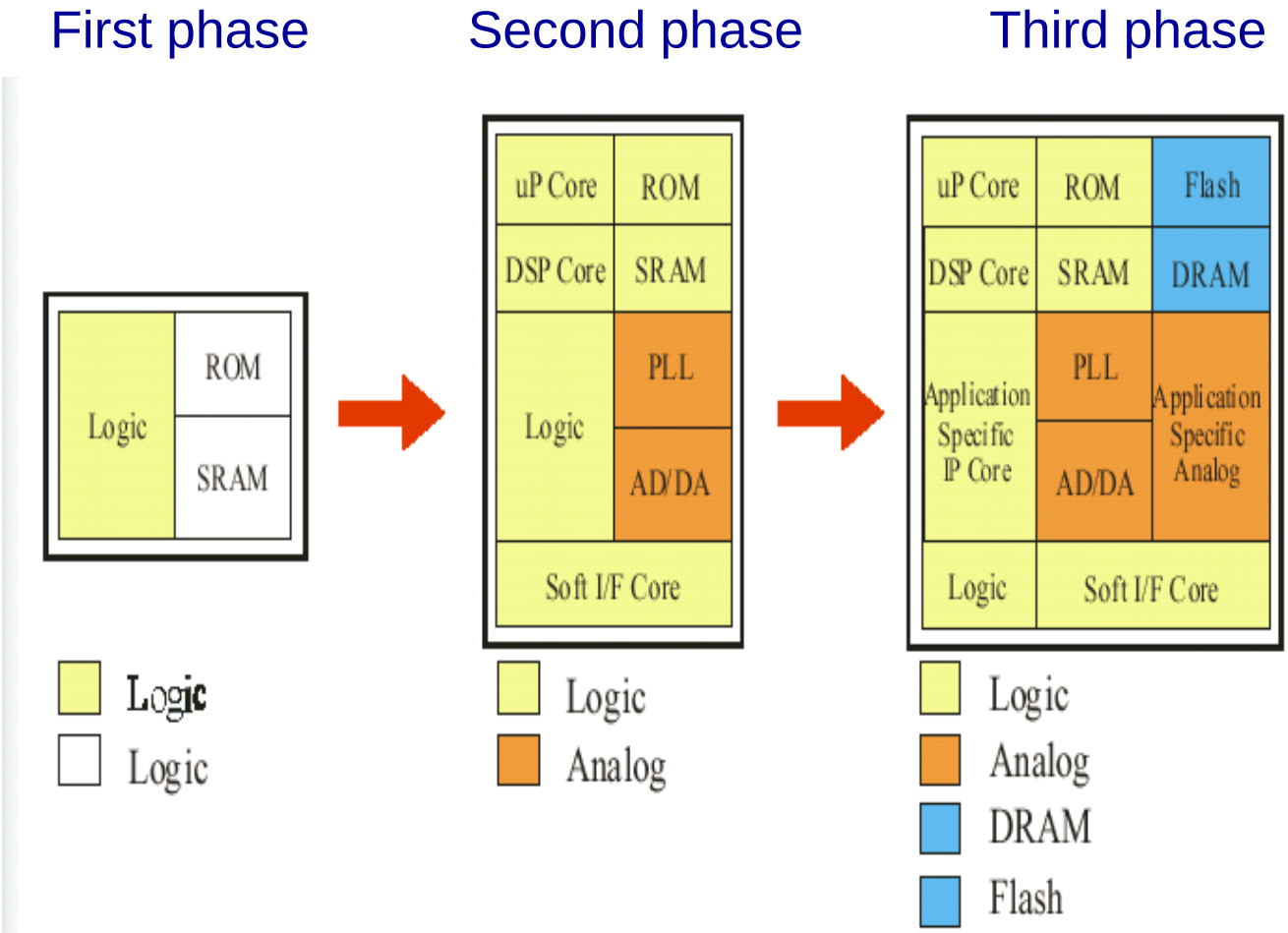
SoC: System on Chip

- **System**

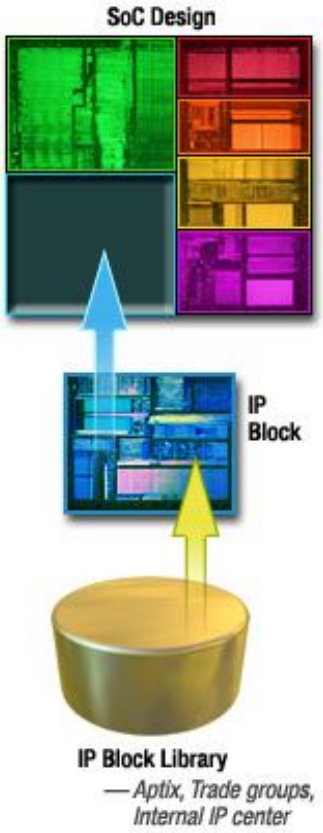
  A collection of all kinds of components and/or subsystems that are appropriately interconnected to perform the specified functions for end users.

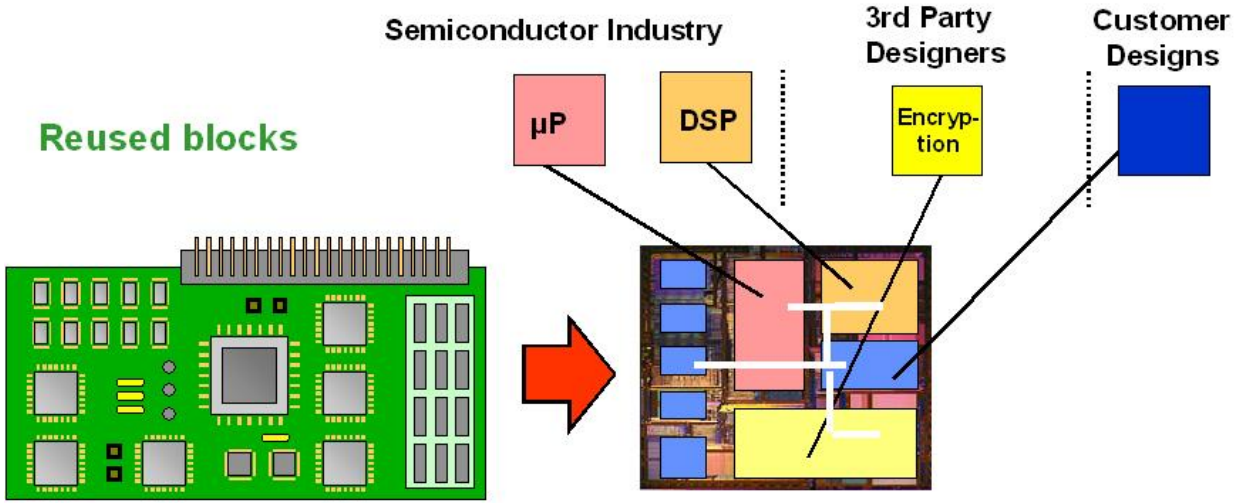
- **A SoC design is a “product creation process” which**
  - Starts at identifying the end-user needs (or system)
    - Hardware
    - Software
  - Ends at delivering a product with enough functional satisfaction to overcome the payment from the end-user

SoC Evolution



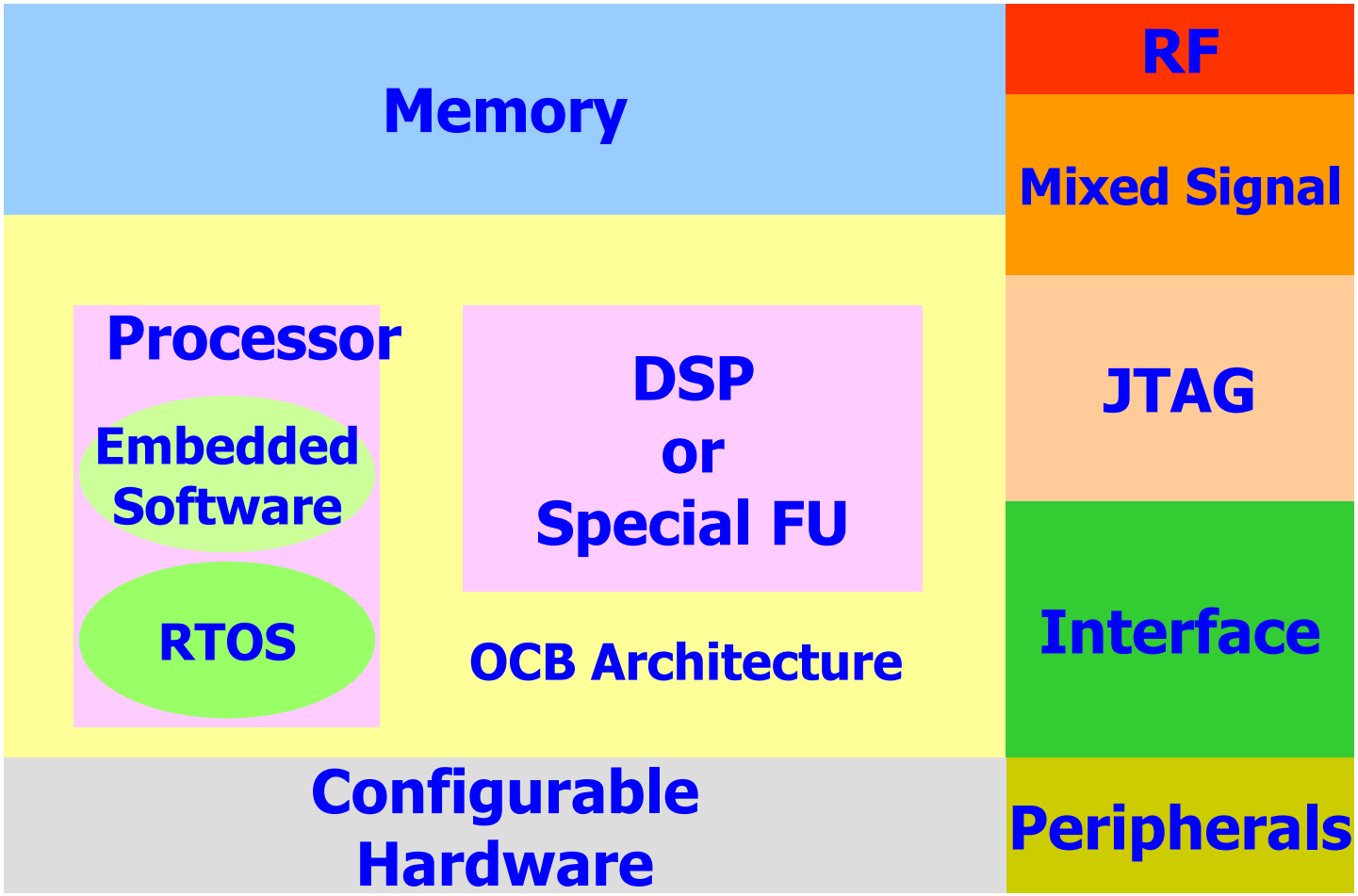
What is SoC in your mind?



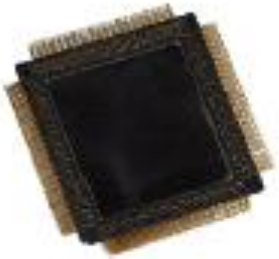


Definition: integration of a complete system onto a single IC

SoC Architecture



SOC is industry trend



ASIC/ASSP

Today

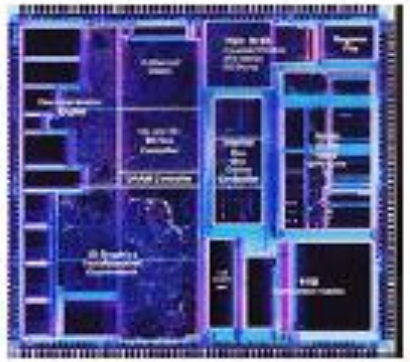
Assembly

System-Board

IP/System-Board

Tomorrow

Integration



SOC

Example: Mobile Phone

Yesterday

- Voice only; 2 processors
- 4 year product life cycle
- Short talk time

Today

Single Chip

- 5~8 Processors
- Memory
- Graphics
- Bluetooth
- GPS
- Radio
- WLAN

- Voice, data, video, SMS
- <12 month product life cycle
- Lower power; longer talk time

Source: EI-SONICS

VLSI Applications

- **Microprocessors or microcontroller**
  - Pentium, ARM, DSP processors
- **Memory**
  - DRAM, SRAM, ROM, ..
- **Special purpose processors**
  - Audio, image or video compression
    - Image: JPEG, JPEG2000
    - Video: MPEG1,2,4,7, H.26x
    - Audio: MP3, AC3,
  - Communication (wired or wireless)
- **Information Appliance (IA)**