


2023 Digital IC Design Homework 4

NAME	林柏戎		
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Simulation Result			
Functional simulation	100	Gate-level simulation	100
<pre>#----- # START!!! Simulation Start #----- # Layer 0 output is correct ! # Layer 1 output is correct! #----- # SUMMARY #----- # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # terminate at 21765 cycle #-----</pre>		<pre>#----- # START!!! Simulation Start #----- # Layer 0 output is correct ! # Layer 1 output is correct! #----- # SUMMARY #----- # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # terminate at 21765 cycle #-----</pre>	
Synthesis Result			
Total logic elements	494		
Total memory bits	0		
Embedded multiplier 9-bit elements	0		
Total cycle used	21765		

Flow Summary



<<Filter>>

Flow Status	Successful - Sat May 06 12:58:18 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	ATCONV
Top-level Entity Name	ATCONV
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	494 / 55,856 (< 1 %)
Total registers	166
Total pins	82 / 325 (25 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	0 / 308 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design
<p>主要使用的演算法:用 mapping 的方式，不要每次做 conv 時都重新抓 data 值，這樣會很花 cycle。一開始只做奇數排，做完一輪後再做偶數排。</p> <p>主要分四個狀態: CONV、LAYER0、LAYER1、DONE。</p> <p>CONV: Mapping 時會將最後兩直排的值記下來，並往前一個直排，這樣只需要花 3 個 cycle 讀下一個 data。</p> <p>LAYER0: 將 conv 完後的值丟到 cdata_wr，caddr_wr 也是對應的值。</p> <p>LAYER1: LAYER0 做完就到 LAYER1，去看 caddr_wr 對應的 cdata_wr 有沒有比當前的 cdata_wr 大，若有，則取代；若無，則維持原值。</p> <p>DONE: 將 busy 拉低，並讓 testfixture 去 check result</p>

*Scoring = (Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements) X Total cycle used*

*** Total logic elements must not exceed 1000.**