數位IC設計

Pei-Yin Chen, 陳培殷
資訊工程系 特聘教授 兼 計算機與網路中心主任

Syllabus (1/2)

- Time and Place
  - Tuesday : 9:10 ~ 12:00　　　測量系 經緯廳
- Contact Information
  - 資訊系11F Rm:65B13 (06-2757575 EXT 62547)
  - E-mail: pychen@mail.ncku.edu.tw
- Office Hour
  - Monday: 8:00~12:00
- Assistants
  - 資訊系10F 數位IC設計實驗室(65A01)
    博士生 陳宥融 lt2es.93039@gmail.com

Syllabus (2/2)

評分方式: 期中上機考(15%); 期末上機考(25%)

作業含Demo(60%)

兩次考試皆為Verilog實作設計，因修課人數較多，

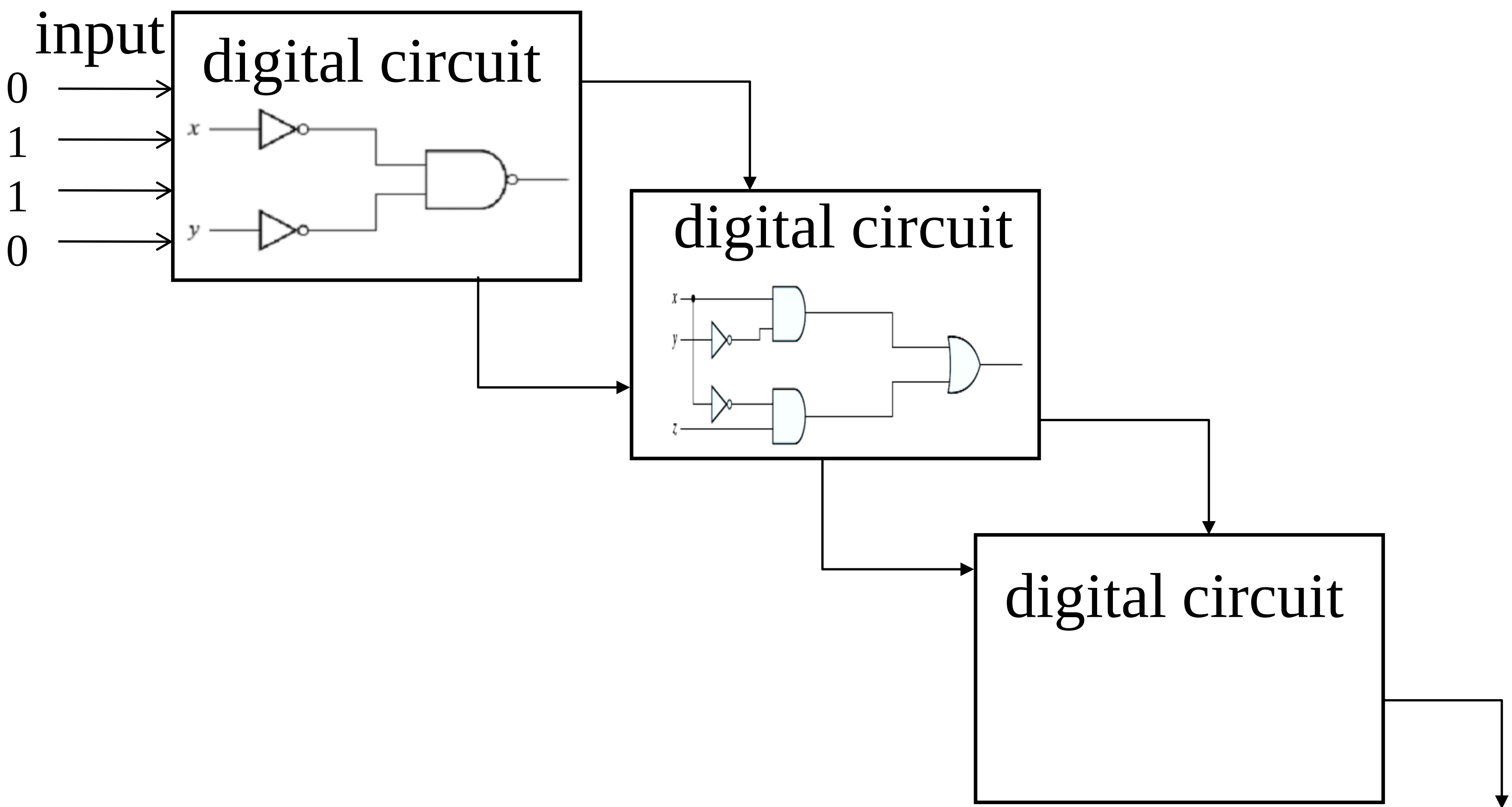
考試與作業皆以pass與fail評分，不會部分給分。

上課1~15週(期末考)，3週非同步線上(於第1週看完)。

參考書目：

1. 教育部P&L聯盟課程講義– FPGA系統設計實務
2. HDL chip design (Douglas J. Smith), Doone Publications
3. Principles of digital design (Daniel D. Gajski), Prentice Hall
4. Modeling, synthesis, and rapid prototyping with the Verilog HDL (Michael. D. Ciletti), Prentice Hall
5. 數位IC設計--Verilog,(陳培殷),滄海書局

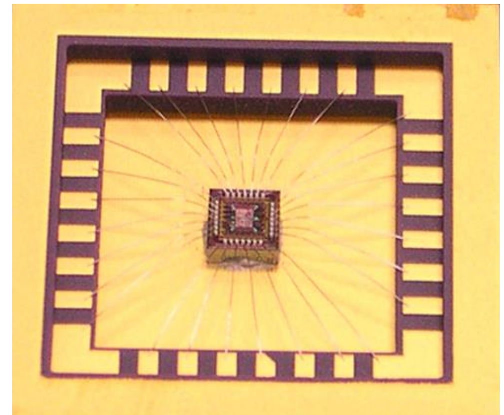
Digital System

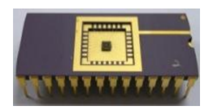


digital circuit === IC (integrated circuit)

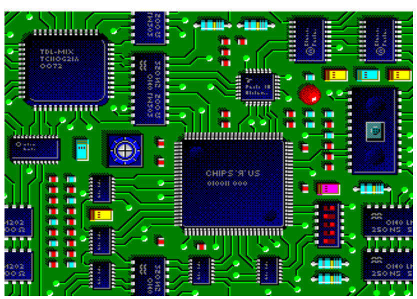
semiconductor

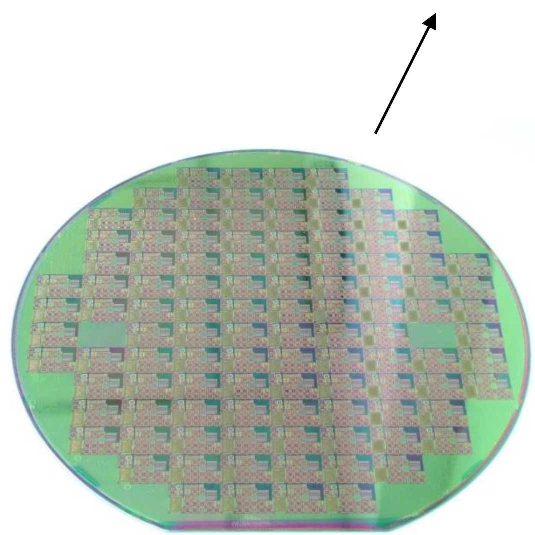
Chip/Circuit Everywhere!

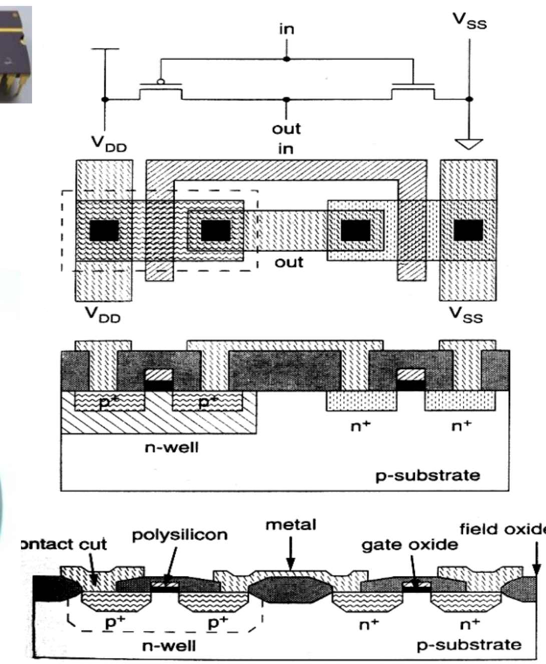




Applications







Circuits

- **Transistor**
- **Gate (1 gate ~= 2~14 transistors)**

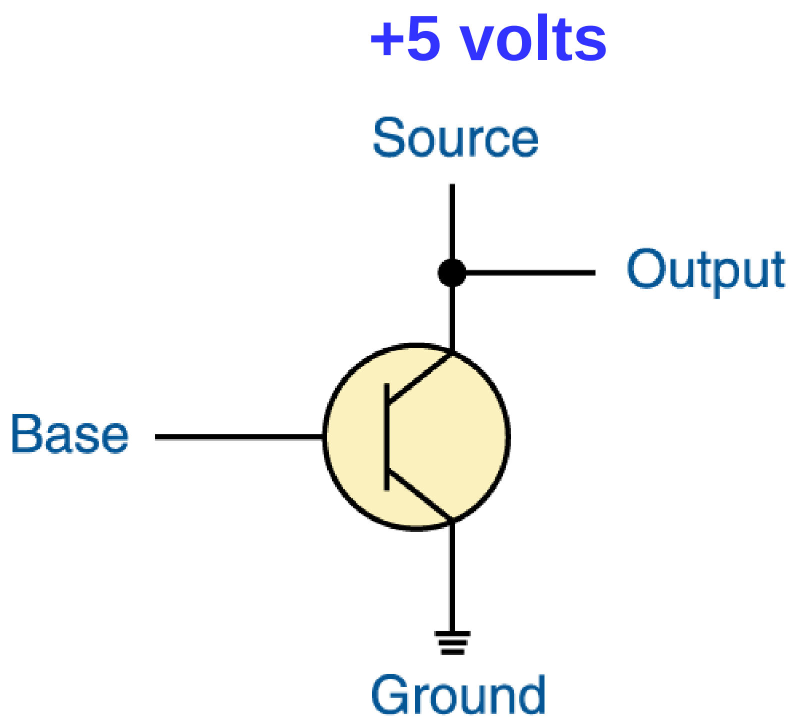
  A combination of interacting transistors

- **Circuit**

  A combination of interacting gates designed to accomplish a specific logical function

- **IC (Integrated Circuit)**
- **System➔ PCB (printed circuit board)**
- **SoC (system on a chip) ➔ How many gates in a chip?**

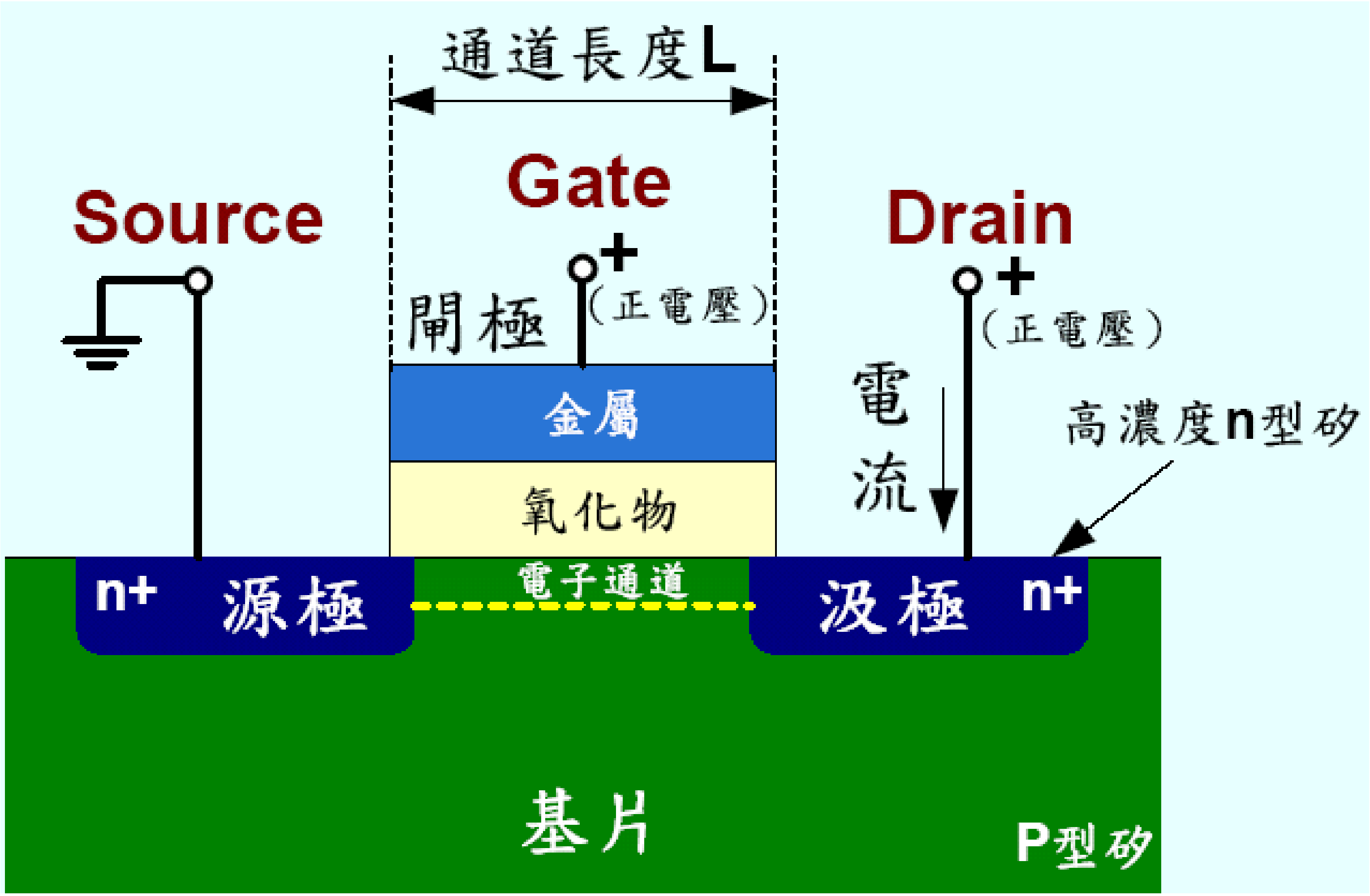
Transistor(電晶體)



- A transistor has three terminals
  - A source (feed with 5 volts)
  - A base
  - An emitter, typically connected to a ground wire
- If the base signal is high (close to +5 volts), the source signal is grounded and the output signal is low (0). If the base signal is low (close to 0 volts), the source signal stays high and the output signal is high (1)

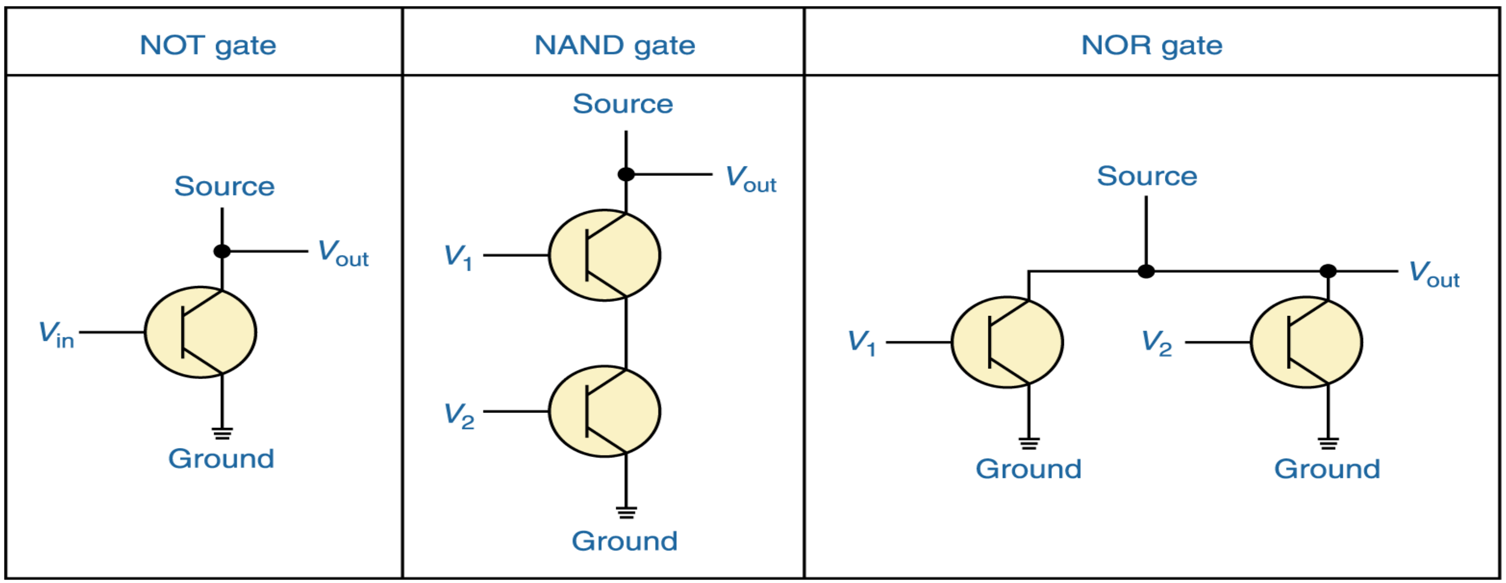
N-channel MOS Transistor

Transistor (電晶體)– Semiconductor(半導體)



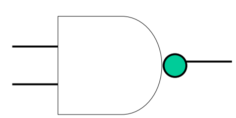
Constructing Gates (semiconductor)

- It turns out that, because the way a transistor works, the easiest gates to create are the NOT, NAND, and NOR gates

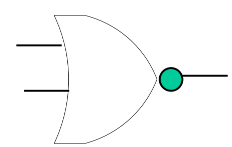


V_{in}	V_{out}
0	1
1	0

V_1	V_2	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

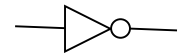


V_1	V_2	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0



IC Design (with CMOS)

CMOS Inverter



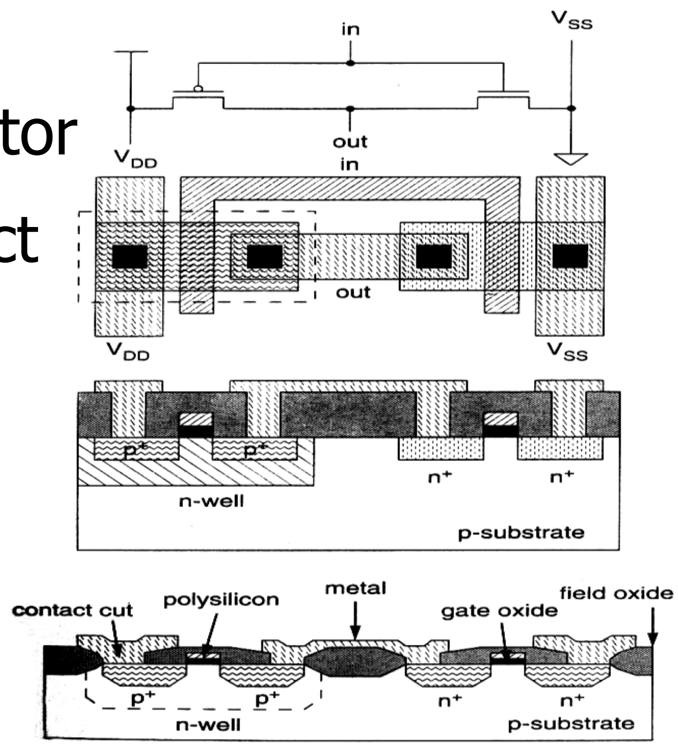
One npn transistor

and one pnp transistor

are used to construct

one inverter.

done by
chip designer

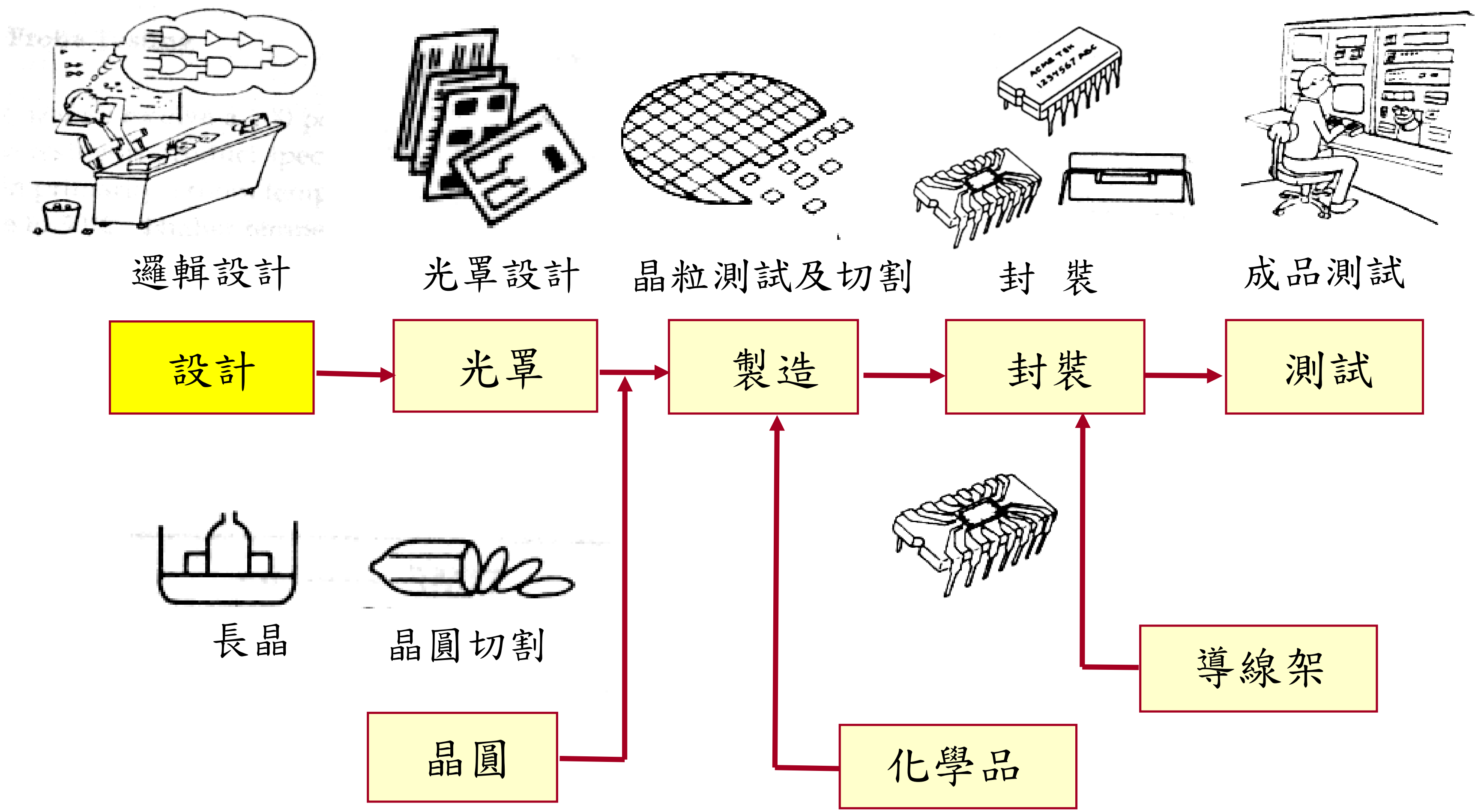


masking

done by
TSMC, UMC

Packing, Testing

IC Industry in Taiwan



IC Design flow

IC design flow

Full Custom

Semi Custom (Cell-Based Design)

ASIC

a. Standard Cells:

TSMC, UMC-cells

b. FPGA or PLD Programmable logic:

Xilinx, Altera, Actel-cells

Full (Fully) Custom Design:

a. For analog circuits and digital circuits requiring custom optimization
b. Gates, transistors and layout are designed and optimized by the engineer

Semi Custom Design:

a. For larger digital circuits
b. Real gates, transistors and layout are synthesized and optimized by related software tools
c. Realization with hardware description language (HDL) such as VHDL and Verilog

Goal of Course

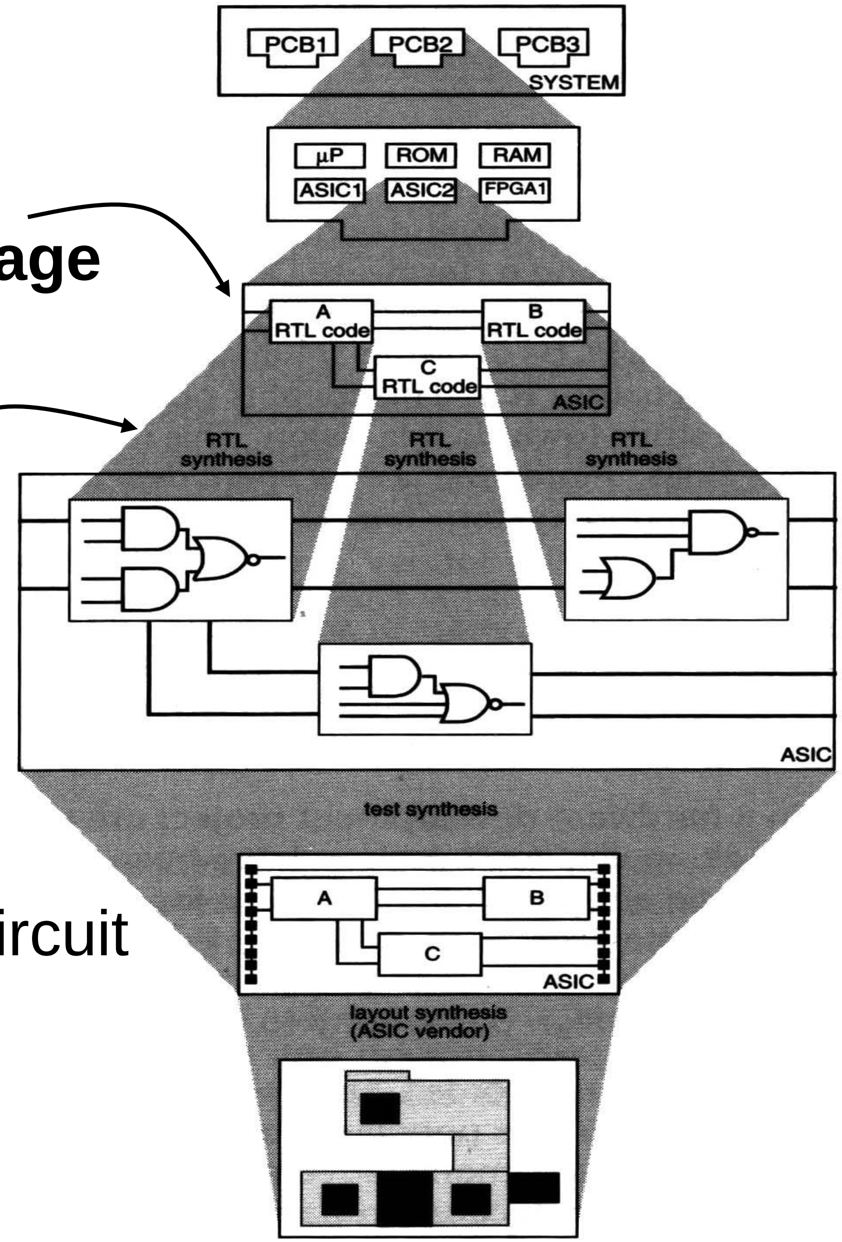
- Digital IC Design
- Cell-Based Design
- Verilog
- PC-based simulation

Hierarchical Components in PCB

1. **Describe the circuits with Hardware Description Language (HDL硬體描述語言)**

2. **Synthesis (合成) the circuits**

   ….



application specific integrated circuit (ASIC晶片)

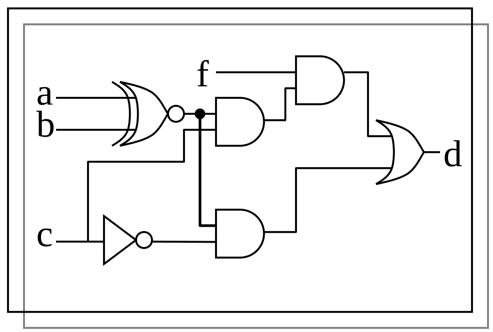
Synthesis

- *Synthesis = Translation+Optimization+Mapping*

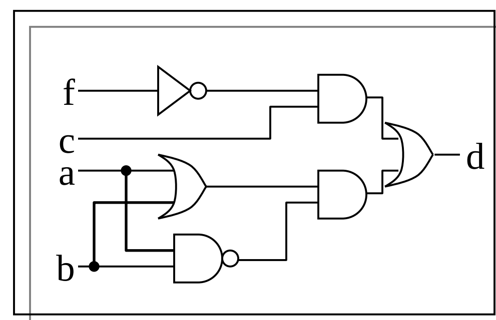
```
always @(…)
    if (a==b)
        if (c==1)
            d=f;
        else
            d=1;
    else
        d=0;
```

HDL Source

Translate into Boolean Representation



Optimize + Map



Target Technology

Process of logic synthesis

2021 Top 10 Fabless IC Suppliers

https://www.electronicsweekly.com/news/business/top-ten-fabless-2021-2022-03/

Table 1: Global Top 10 IC Design Company Revenue, 2021 (Unit: US$1 Million)

	2021 Rank	2020 Rank	Company		2021 Revenue	2020 Revenue	YoY
	1	1	Qualcomm		29,333	19,407	51%
	2	3	NVIDIA		24,885	15,412	61%
	3	2	Broadcom		21,026	17,745	18%
聯發科	★ 4	4	MediaTek	176億	17,619	10,929	61%
	5	5	AMD		16,434	9,763	68%
聯詠	★ 6	8	Novatek	40億	4,836	2,709	79%
	7	7	Marvell		4,281	2,942	46%
瑞昱	★ 8	9	Realtek	37億	3,767	2,635	43%
	9	6	Xilinx		3,677	3,053	20%
奇景	★ 10	-	Himax	15億	1,547	888	74%
	-	10	Dialog		-	1,376	-
	Top 10 Total				127,405	85,971	48%

1. Ranking accounts for top 10 companies before disclosure of financial reports.
2. Qualcomm revenue accounts for QCT division only; NVIDIA revenue not including OEM/IP; Broadcom revenue accounts for semiconductor division only

Source: TrendForce, Mar. 2022

2021年台灣前十大IC設計廠營收排名

2021年排名	公　司	2021年營收(百萬元)	2020年排名	2020年營收(百萬元)	年增率（%）
1	聯 發 科	493,414	1	322,146	53.2
2	聯　詠	135,366	2	79,955	69.3
3	瑞　昱	105,504	3	77.759	35.7
4	奇景光電	43,236	4	26,141	65.4
5	瑞鼎科技	24,834	6	14.425	72.2
6	慧榮科技	23,893	5	13,959	71.2
7	晶豪科技	23,845	7	15,267	56.2
8	矽創電子	22,256	8	13,805	61.2
9	敦泰電子	21,991	9	13.800	59.4
10	群聯電子	11.823	10	10.083	17.3
總和		906,163		587,340	54.3

註：慧榮科技、群聯電子管收僅計算晶片收入，模組產品營收未予計算。
Source:各廠商；TrendForce整理，Mar,2022

Outline

- **Chapter 1**: Introduction
- **Chapter 2**: Semi Custom Design Flow
- **Chapter 3**: RTL Coding-Part I
- **Chapter 4**: RTL Coding-Part II
- **Chapter 5**: Digital System Design
- **Chapter 6**: Control Unit
- **Chapter 7**: Datapath
- **Chapter 8**: Case Study
- **Chapter 9**: System on a Chip
- **Chapter 10**: Low-Power Design