Intel FPGA Software: Quartus Prime

Advisor : Lih-Yih Chiou

Lecturer : David

Date : 2024/04/18

Quartus Prime

EE

LPHPLAB VLSI Design LAB

Outline

- Introduction to FPGA
- Tool Installation
- Quartus Basic GUI
  - Create Project
  - EDA tools Setting
  - Compilation & Synthesis
  - Waveform Simulation
  - Power, Performance and Area

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Introduction to FPGA (1/2)

- The two most popular choices for FPGAs are Xilinx (AMD) and Altera (Intel).
- FPGA Device Family Comparison

Application	AMD-Xilinx Devices	Intel-Altera Devices
Highest performance	Versal* Prime Versal* Premium	Intel® Agilex™ F-Series Intel® Agilex™ I-Series
High performance	Virtex* UltraScale+* Kintex* UltraScale+* Xynq* UltraScale+*	Intel® Agilex™ F-Series Intel® Agilex™ I-Series Intel® Stratix® 10 GX/SX/TX/MX/DX
Mid-range	Virtex* UltraScale* Kintex* UltraScale* Zynq* -7000	Intel® Stratix® 10 GX/SX/TX/MX/DX Intel® Arria® 10 GX/SX
Low cost	Artix* -7	Intel® Cyclone® 10GX

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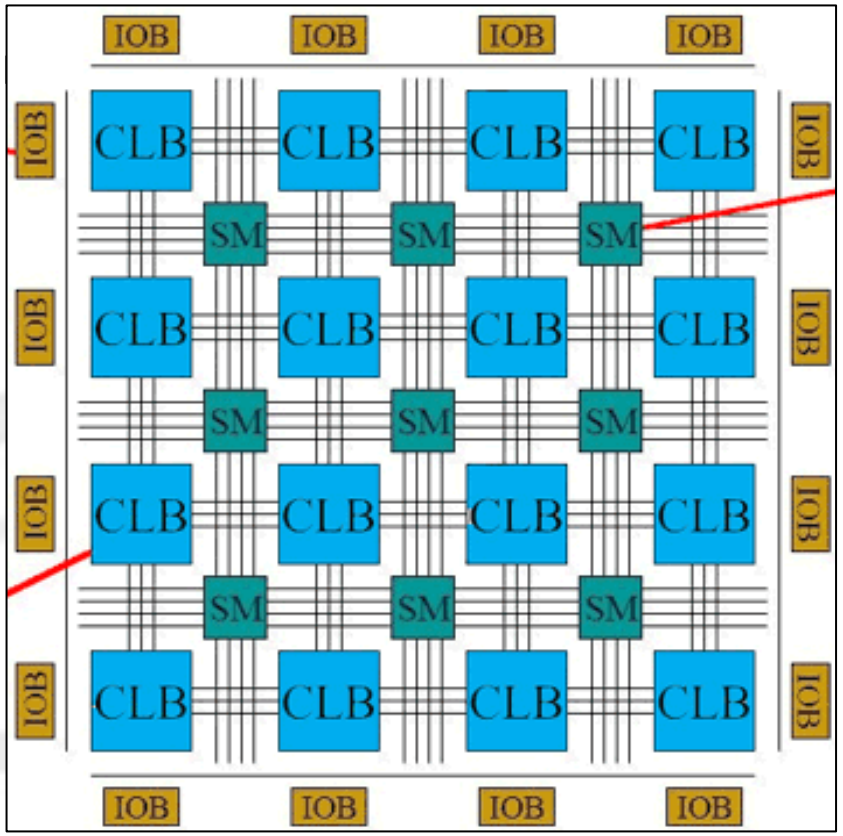
Introduction to FPGA (2/2)

- Logic Blocks
  - General logic blocks
  - Programmable to perform different
- Reconfigurable Interconnect
  - Programmable routing channels
  - Connecting blocks and I/O
- I/O Blocks
  - Connecting the chip to the outside
- Dedicated Hardware
  - Memory (SRAM, BRAM, URAM)
  - DSP (Multiplier)
  - Special function unit

Most of the delay in the FPGA comes from the interconnect



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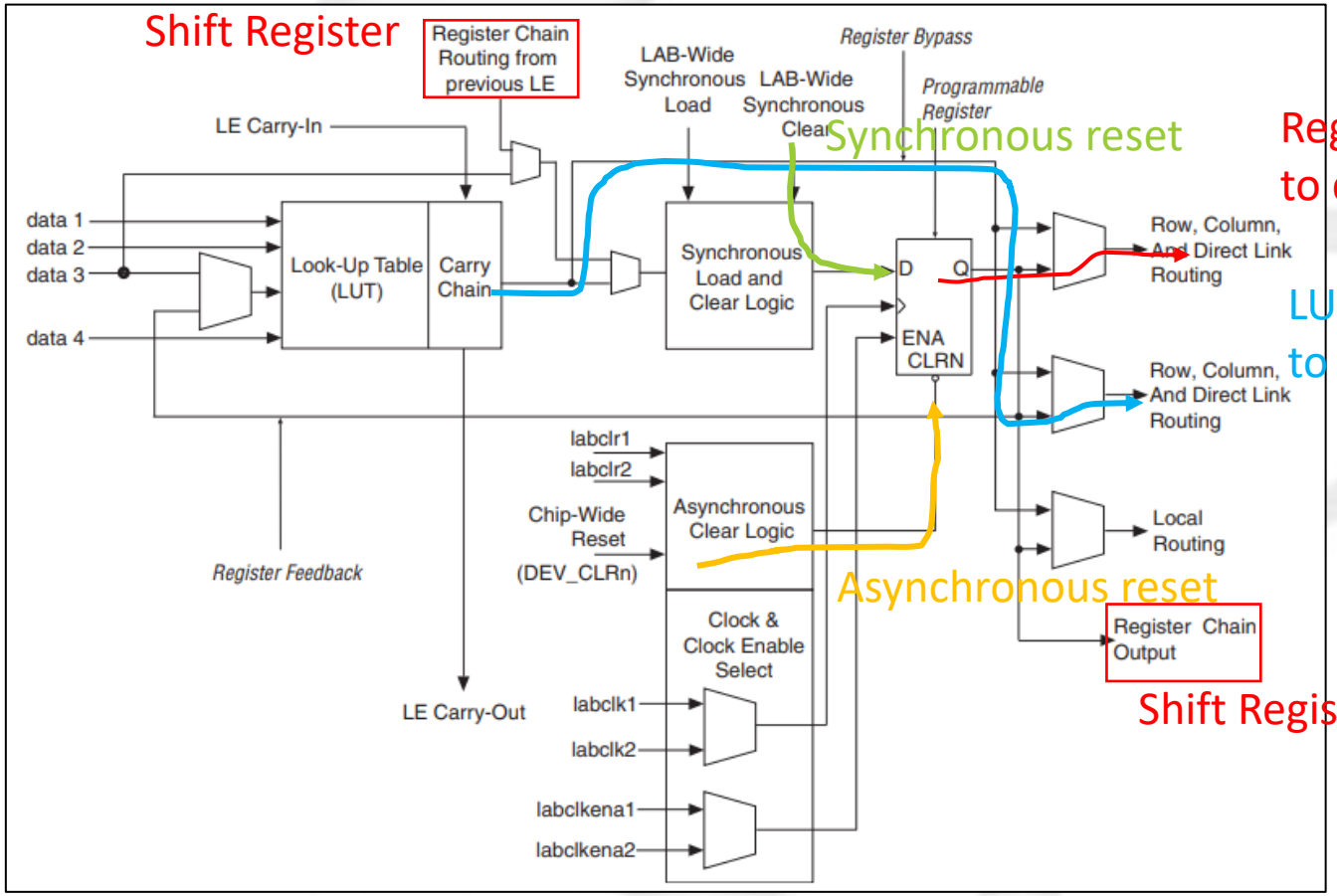
Logic Elements in the Cyclone IV

- LEs are compact and provide advanced features with efficient logic usage.



https://cdrdv2-public.intel.com/653677/cyiv-51002.pdf

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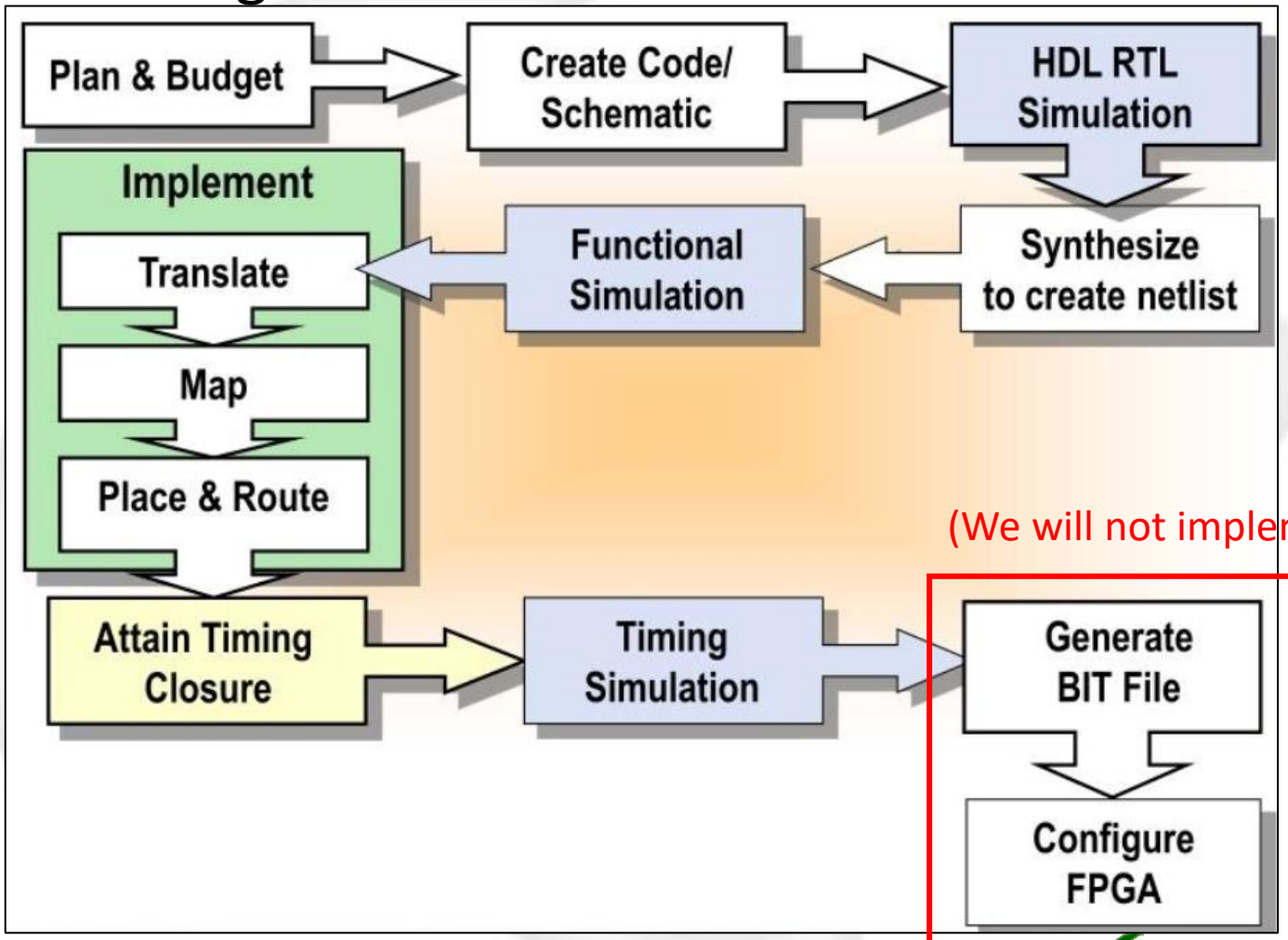
Basic Flow Diagram

- FPGA design flow overview



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Basic Design Flow (1/2)

- Design Constraint
  - Constraints are used to influence the FPGA synthesis and implementation.
  - To specify the design performance requirements that must be made and guide the tools toward meeting those requirements.
  - The primary constraint types are:
    - Synthesis
      - Influence the details of how the synthesis of HDL code to RTL occurs
    - I/O (Pin Assignment)
      - To assign a signal to a specific I/O (pin) or I/O bank
    - Timing
      - To specify the timing characteristics of the design.
      - May affect all internal timing interconnections or delays.
    - Area
      - To map specific circuit to a range of resources within the FPGA.

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Basic Design Flow (2/2)

- Synthesis
  - After coding up your HDL code, you will need a tool to check the syntax and generate a netlist.
- Implementation
  - Translate
    - Merges multiple design files and design constraint information to produce a compatible design file (netlist).
  - Map
    - Fits the design within the available resources on the target.
      - Maps the schematic to physical logic units.
      - Compiles functions into basic LUT-based groups.
  - Placement & Routing
    - Place components onto the chip, connect the components, and extract timing data into reports

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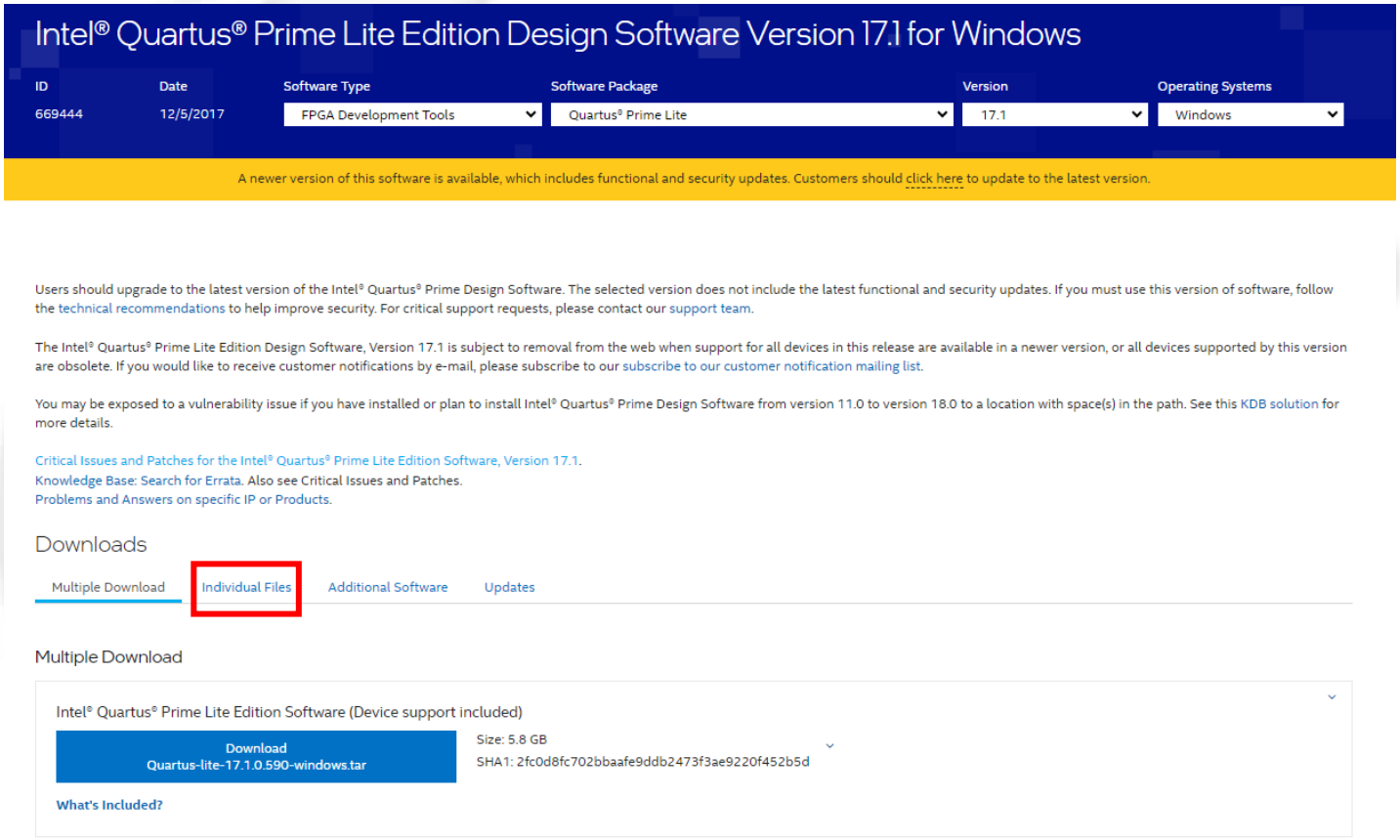
Tool Installation (1/9)

- Quartus Prime 17.1 Lite: Download Link
- Click Individual Files



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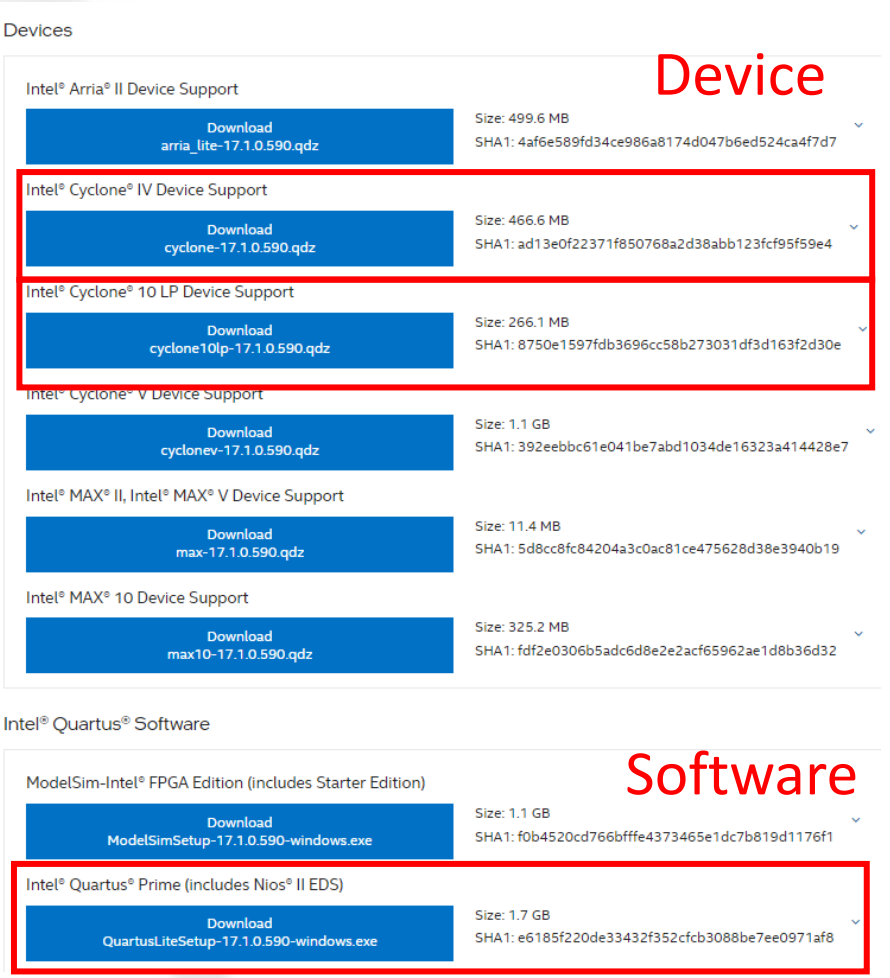
Tool Installation (2/9)

- Download the executable files for two specific devices and one software program.



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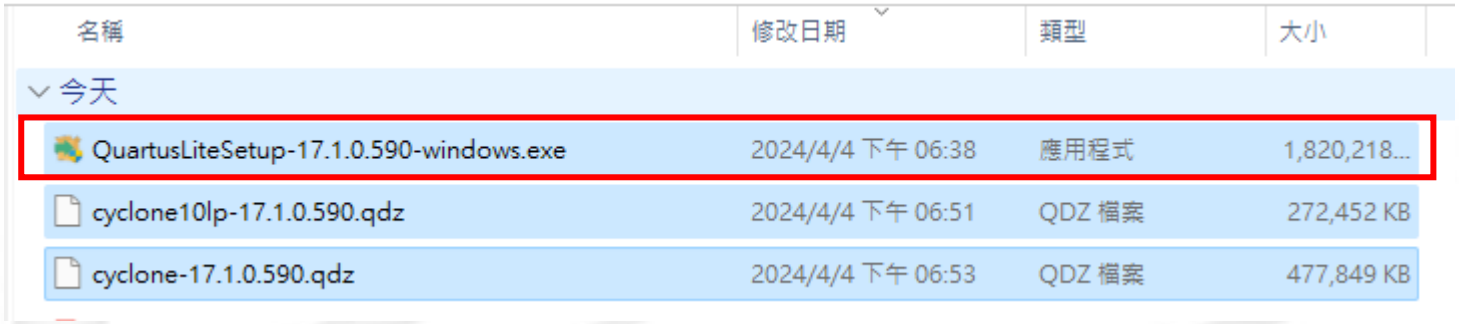
Tool Installation (3/9)

- Three file been downloaded, click executable file to installation.



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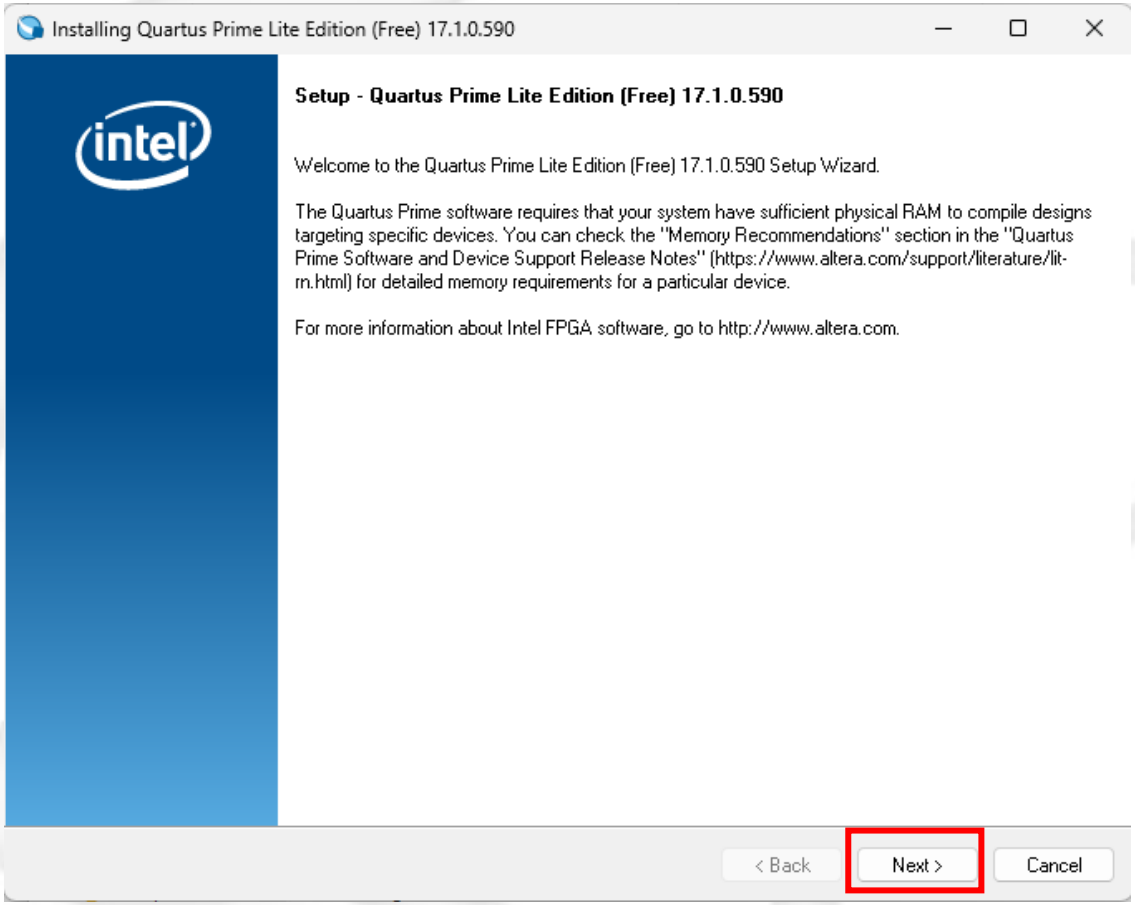
Tool Installation (4/9)

- Click Next



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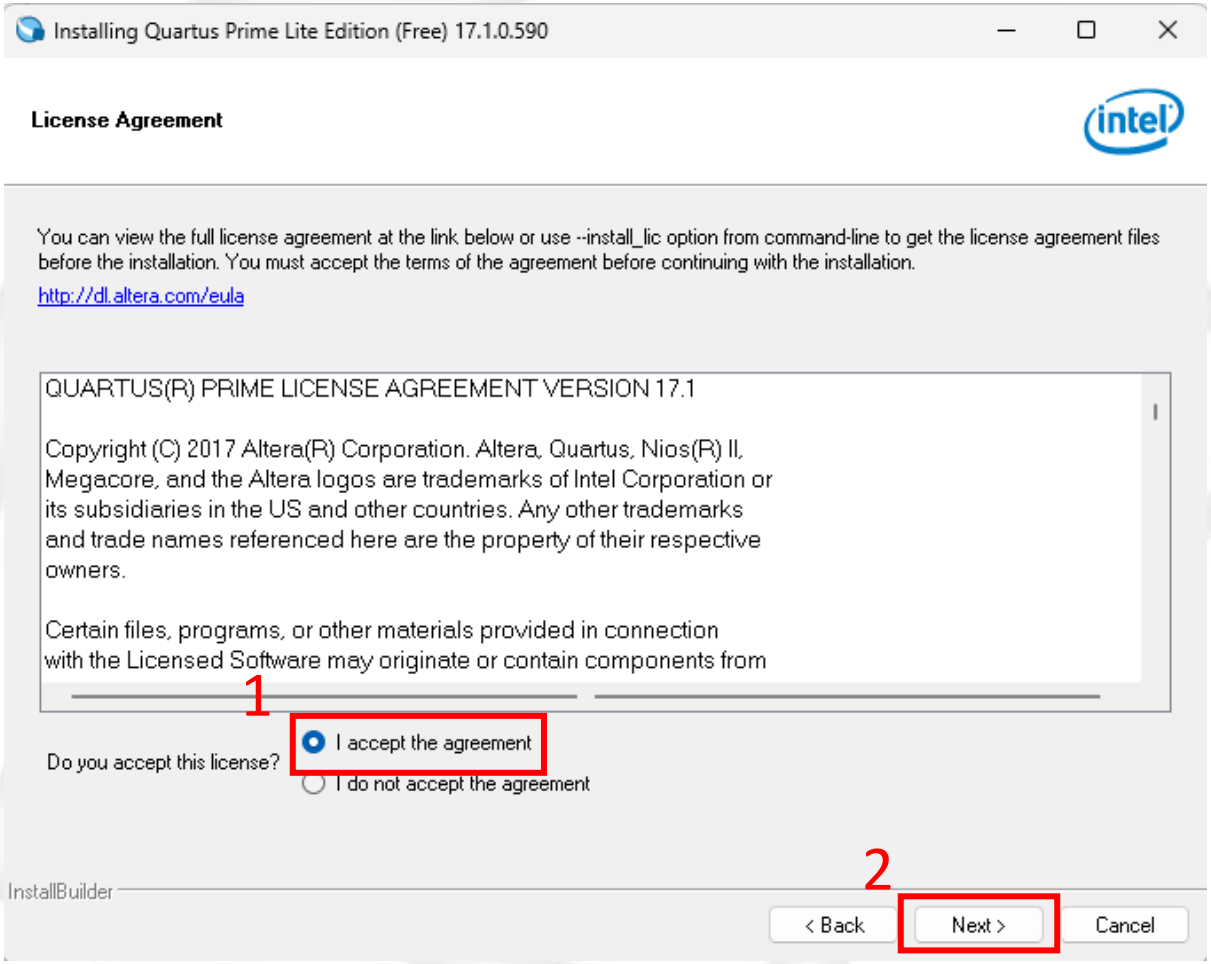
Tool Installation (5/9)



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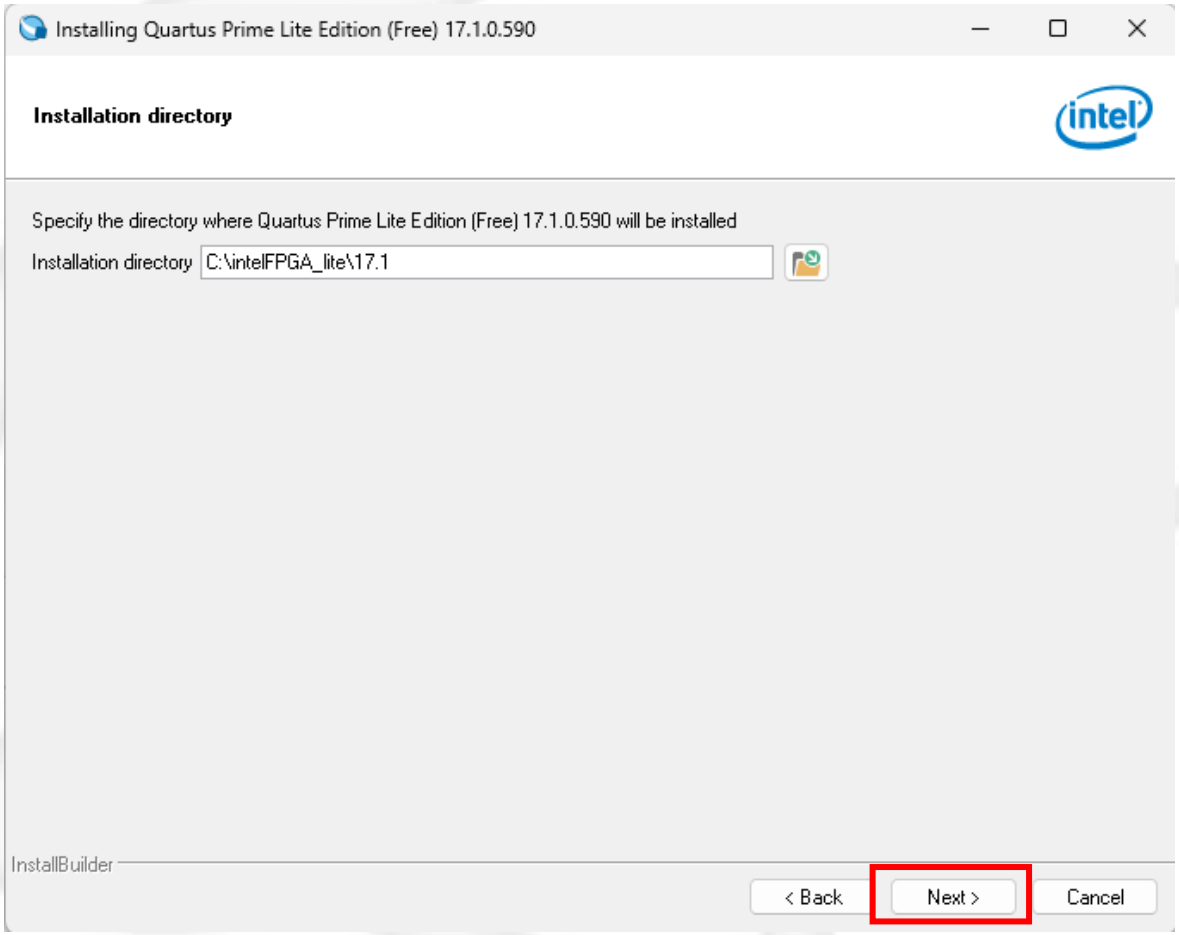
Tool Installation (6/9)

- Click Next



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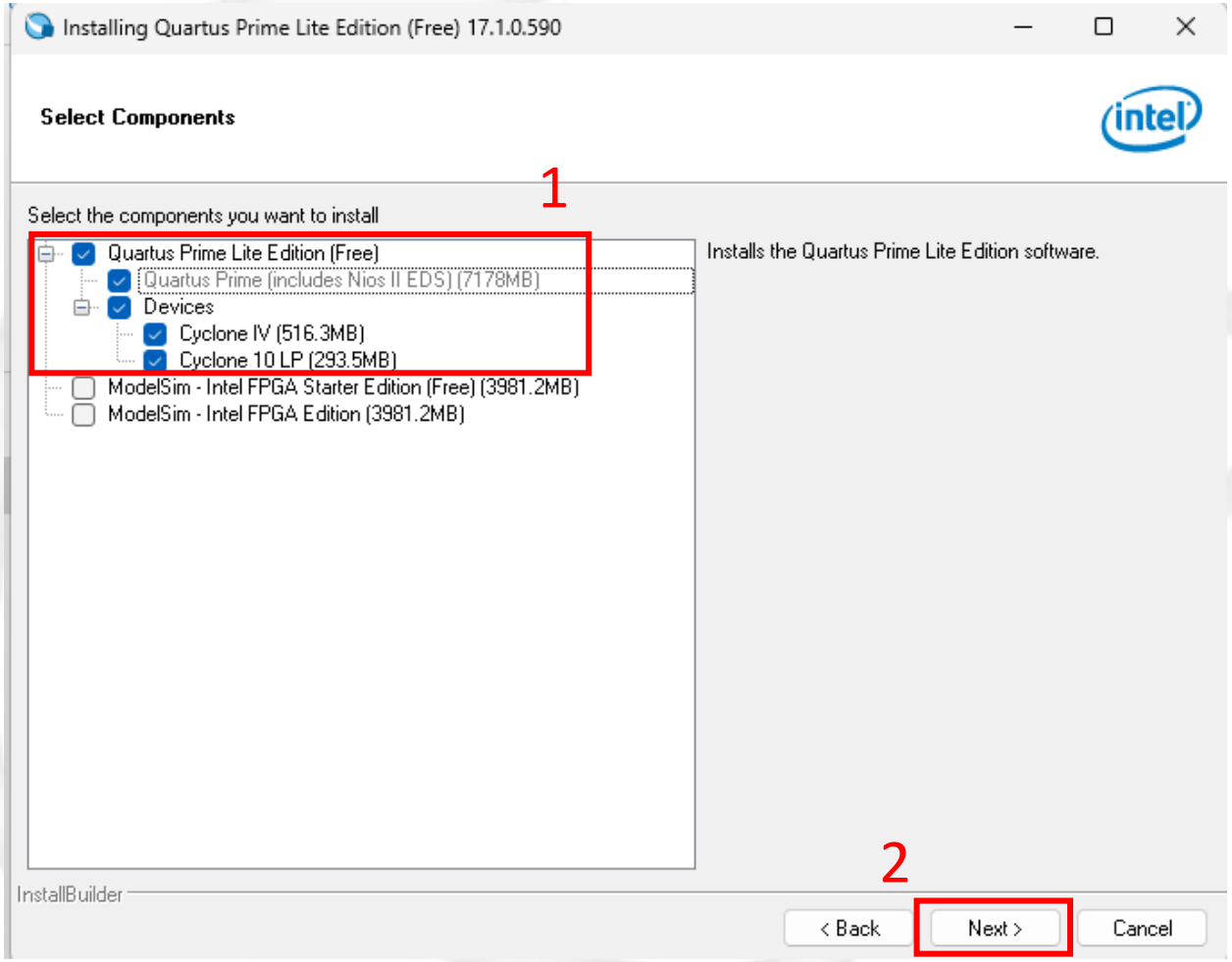
Tool Installation (7/9)

- Select the Devices we had download before.



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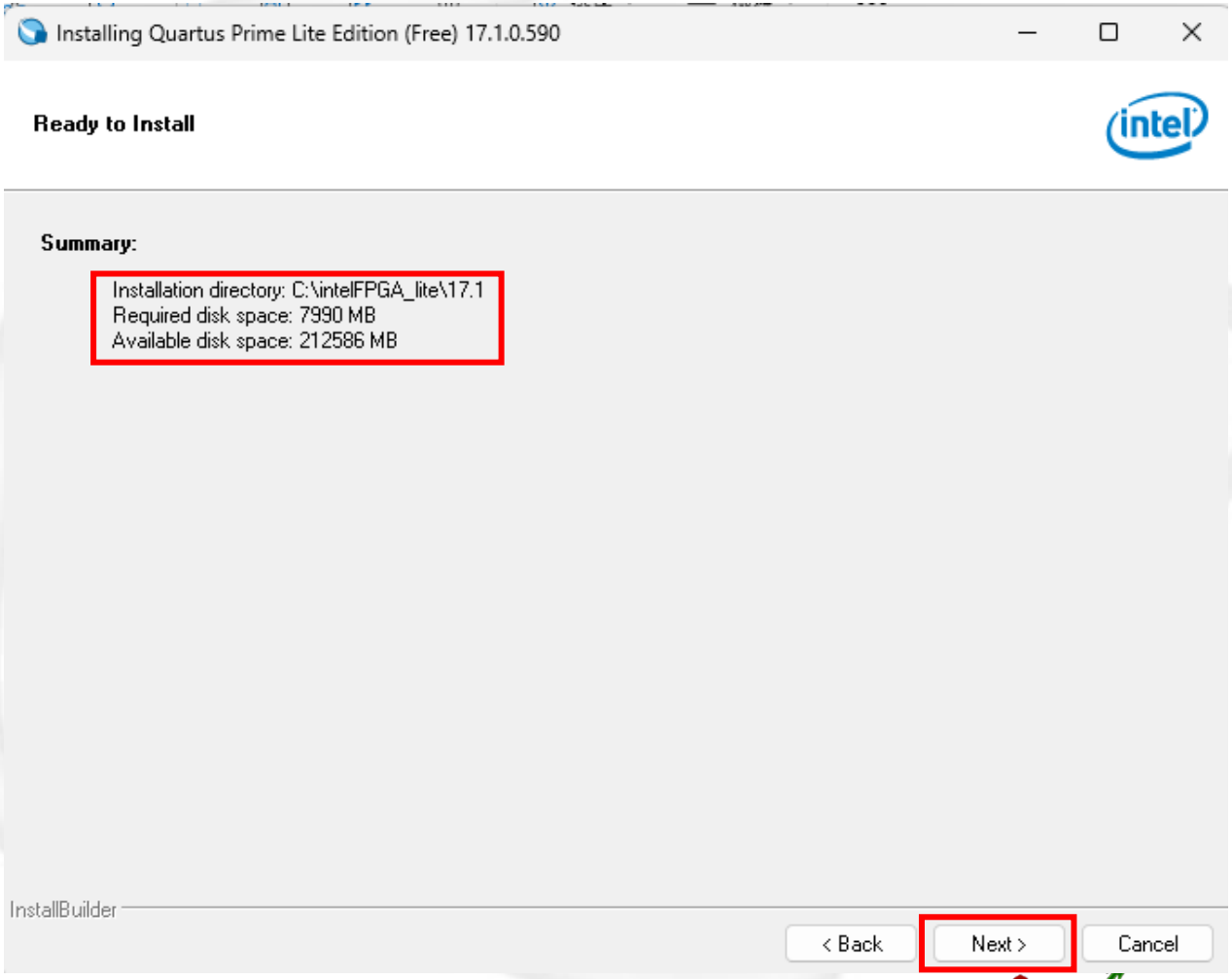
Tool Installation (8/9)

- Ensure your pc has enough space for installation.



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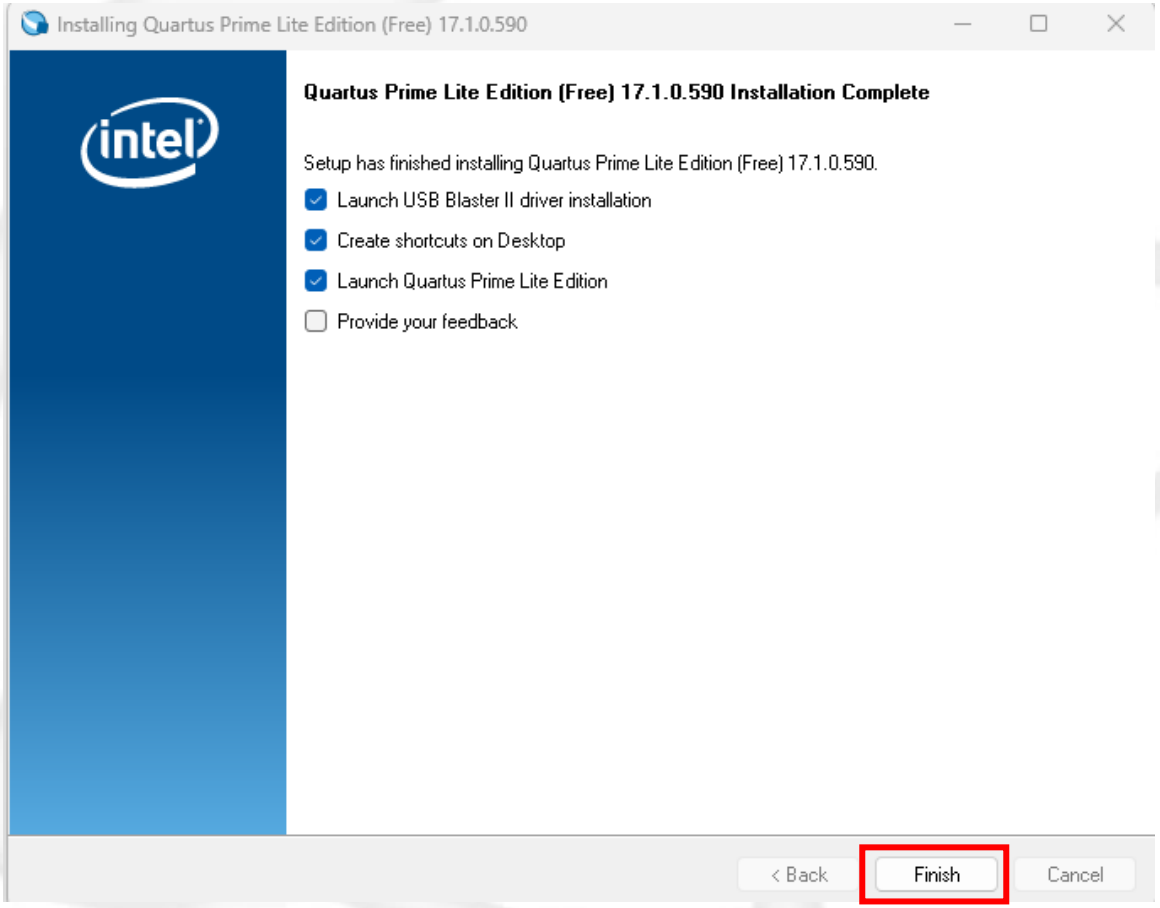
Tool Installation (9/9)

- Wait for installation and click finish at the end.



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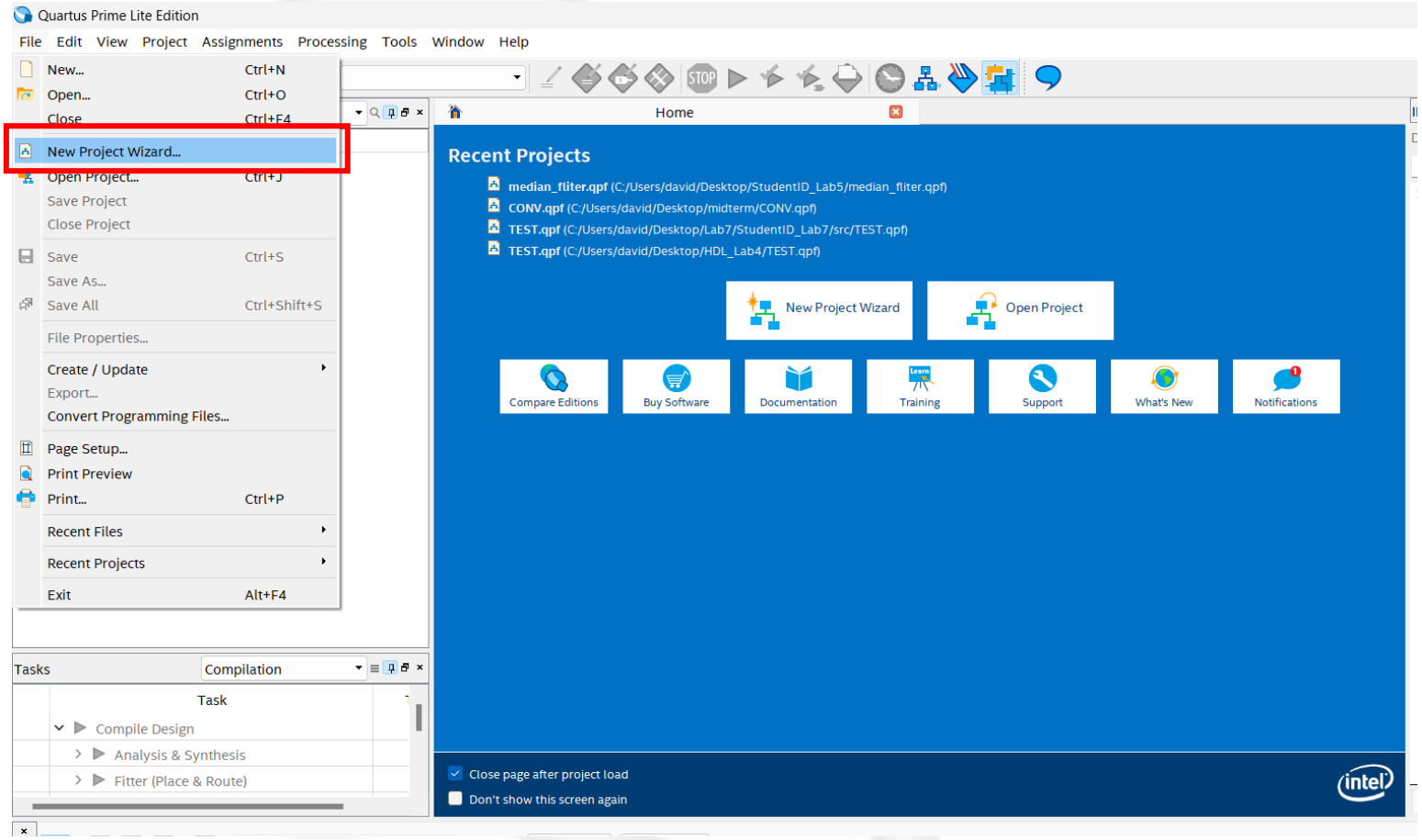
Create new Project (1/7)

- File > New Project Wizard…



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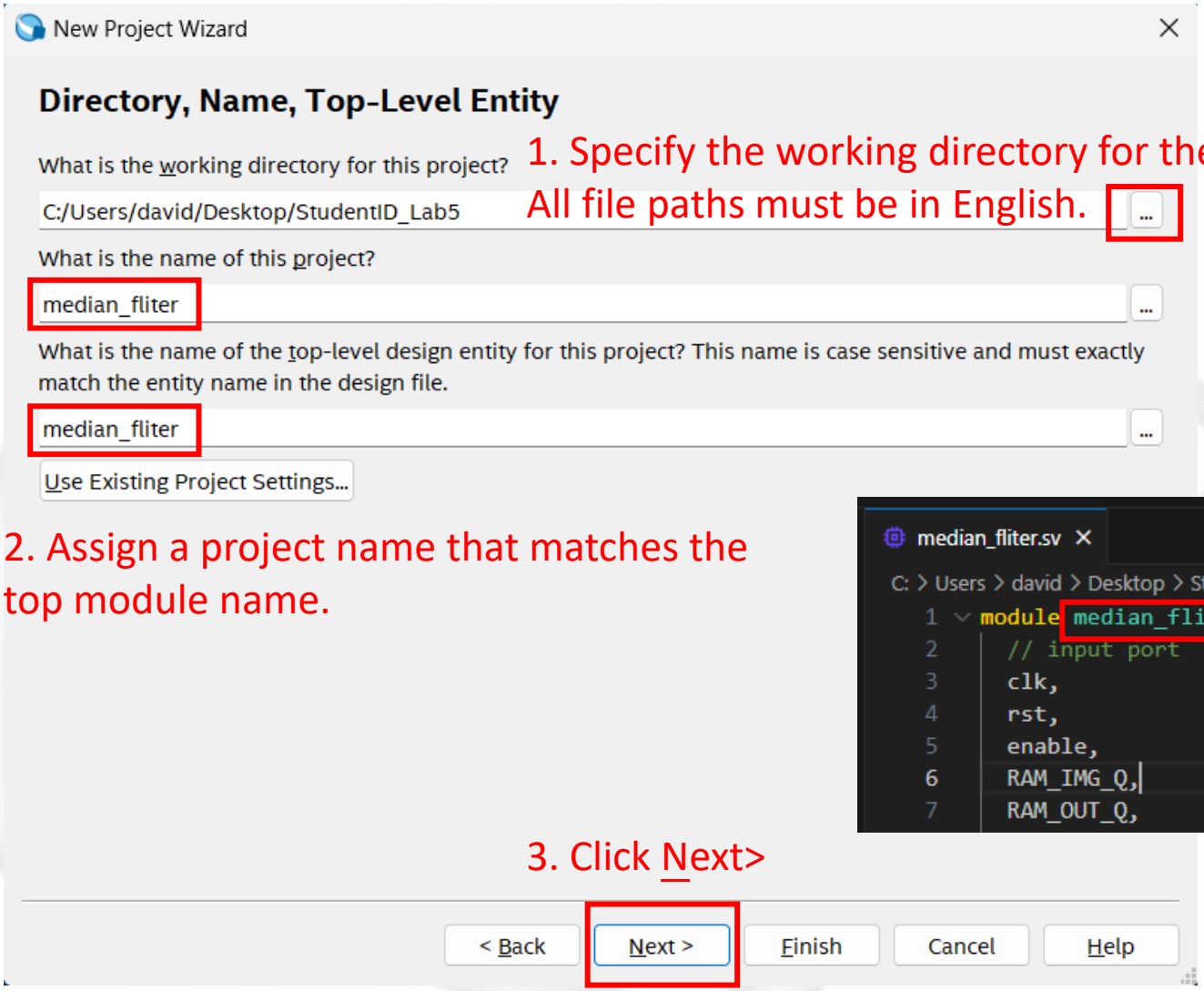
Create new Project (2/7)



1. Specify the working directory for the project.
All file paths must be in English.

2. Assign a project name that matches the top module name.

3. Click Next>

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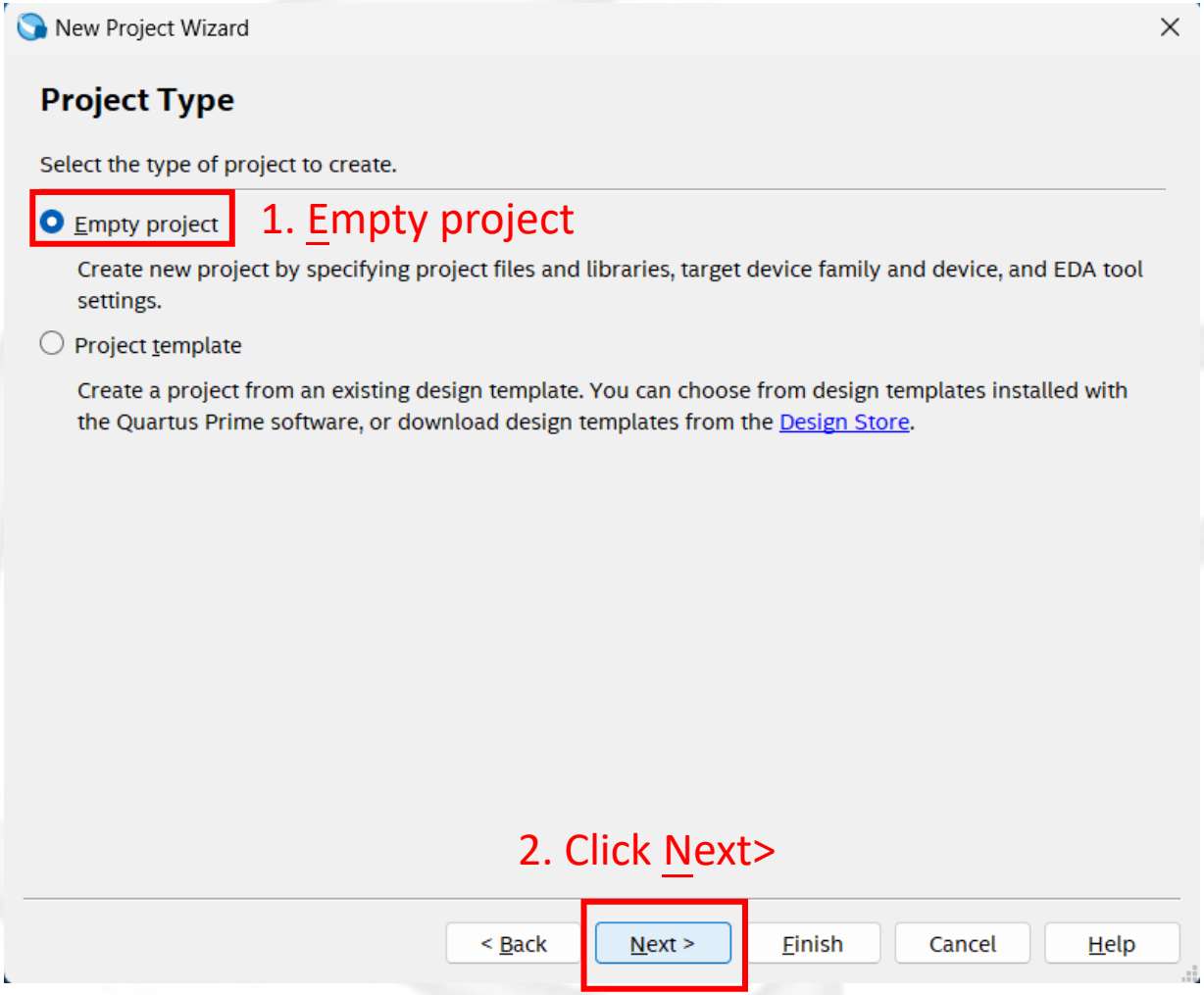
Create new Project (3/7)



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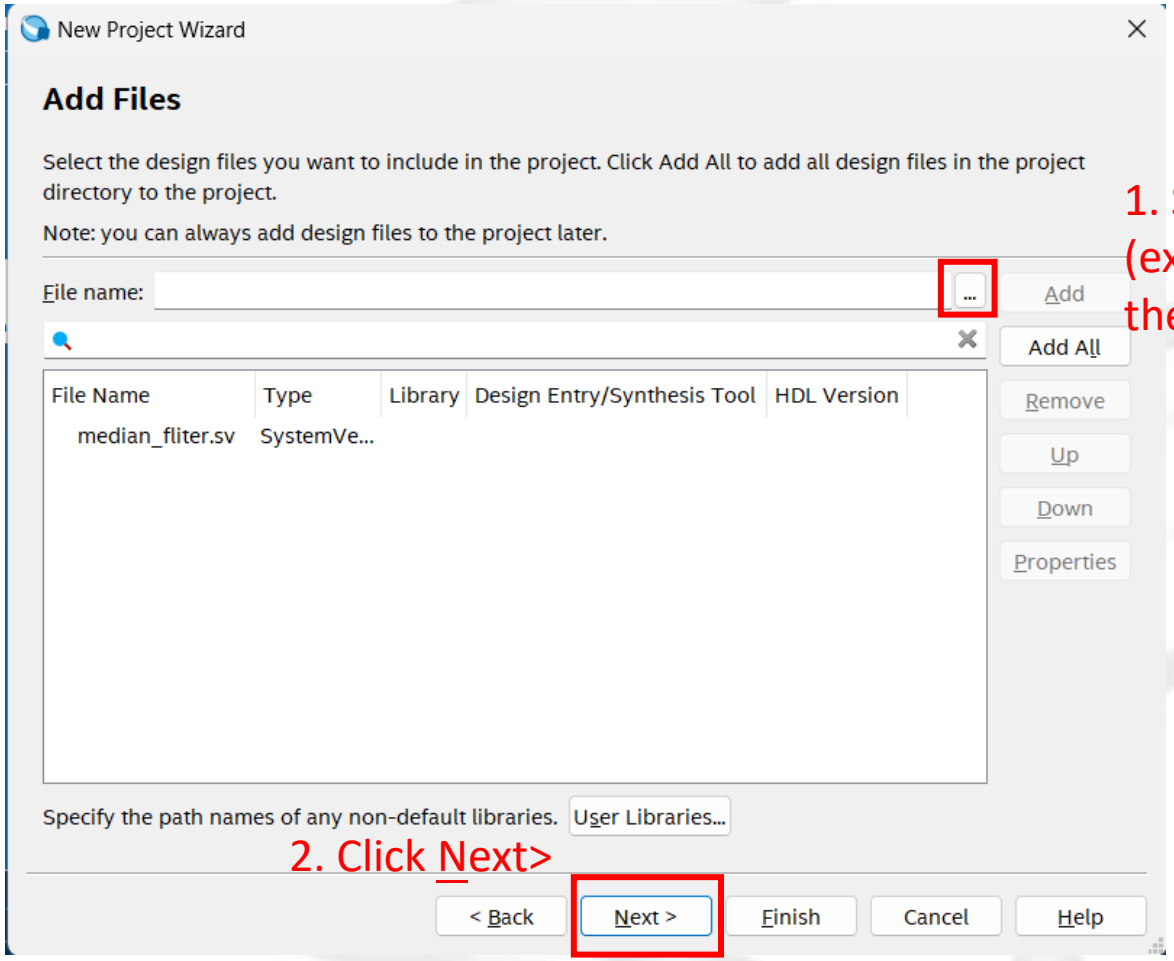
Create new Project (4/7)



1. Select existing design files (excluding testbenches) from the browse dialog.

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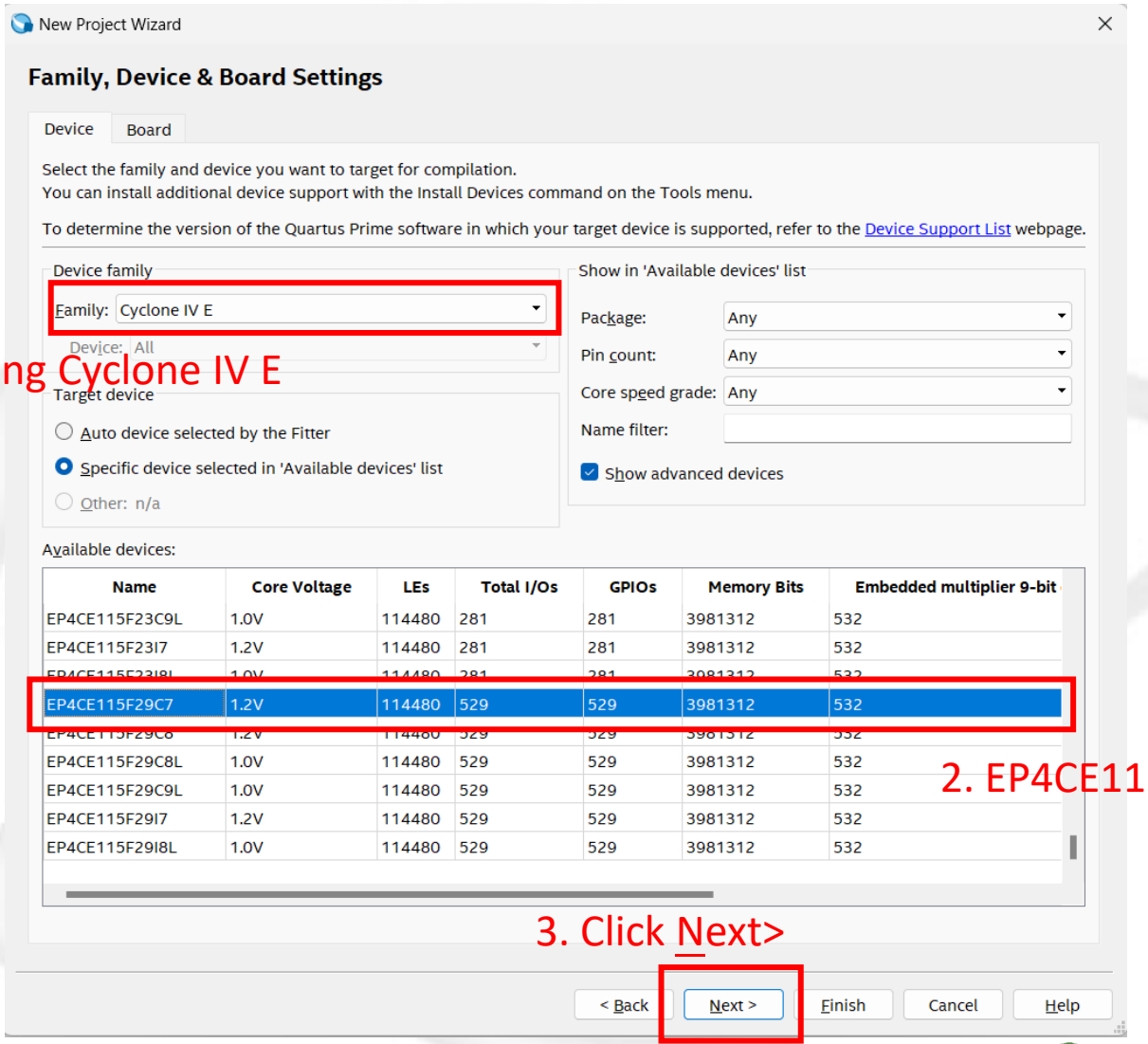
Create new Project (5/7)



1. Choosing Cyclone IV E

2. EP4CE115F29C7

3. Click Next>

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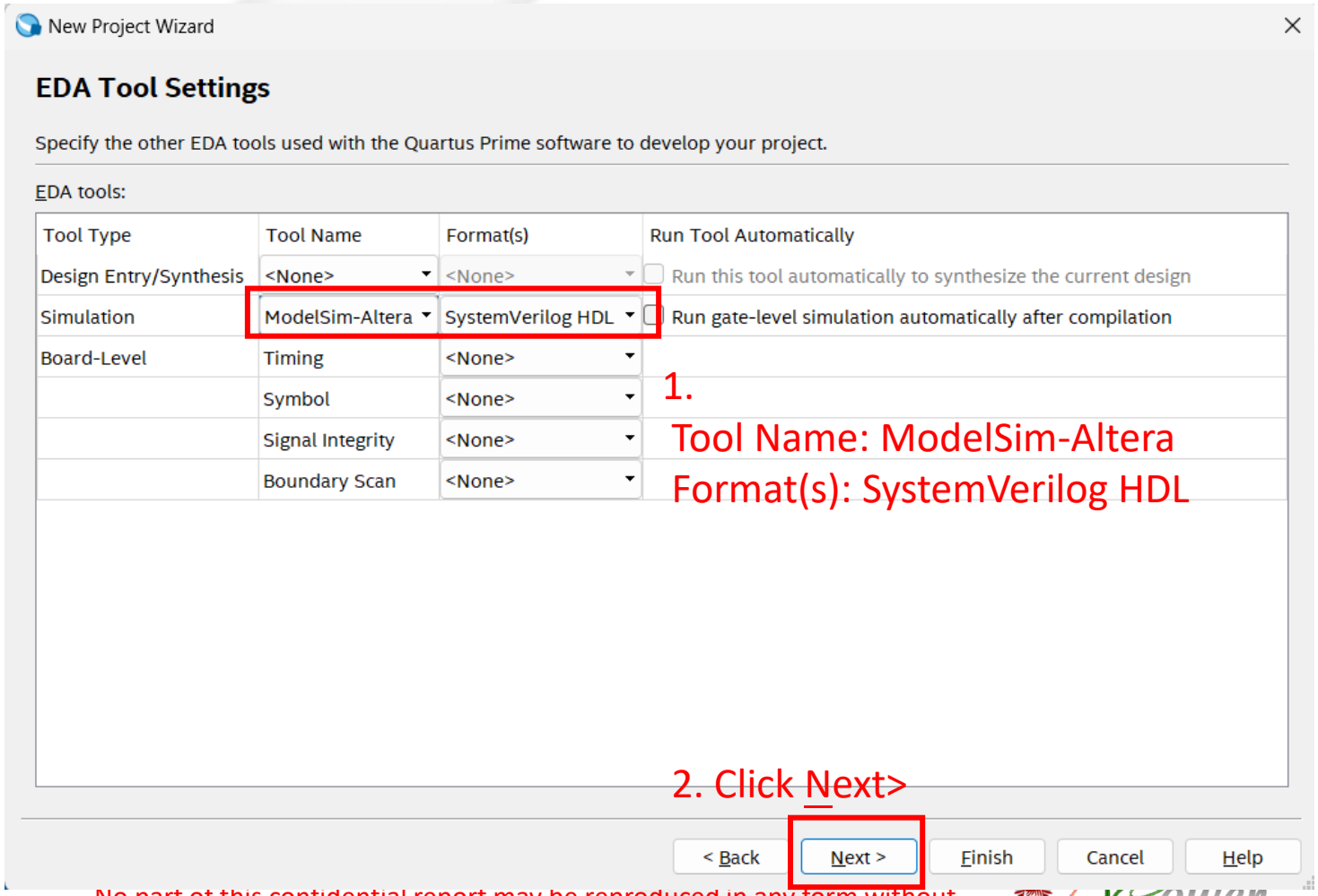
Create new Project (6/7)

- Specify the Simulation EDA tools.



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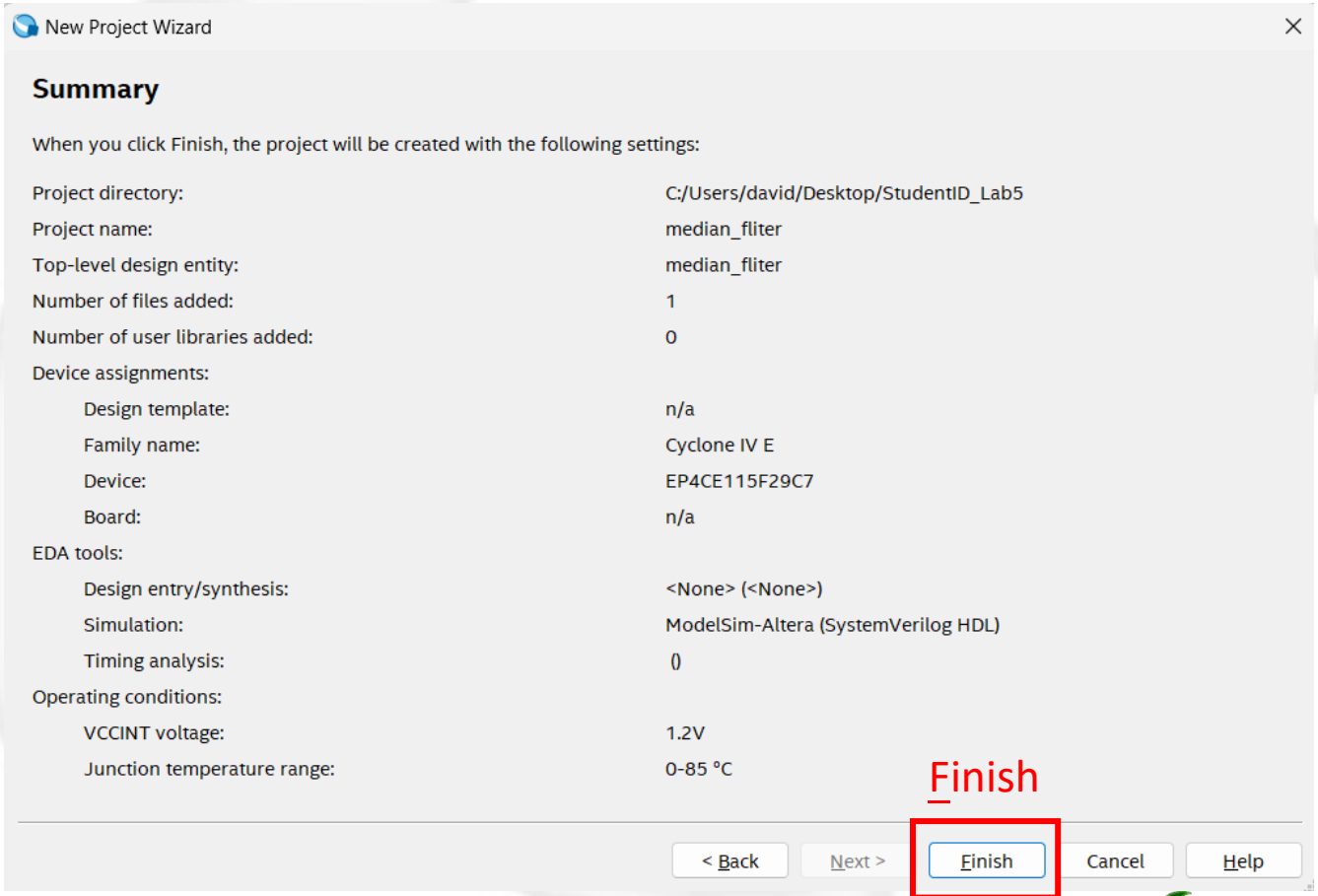
Create new Project (7/7)

- Ensure the project summary remains consistent with the previous setting.



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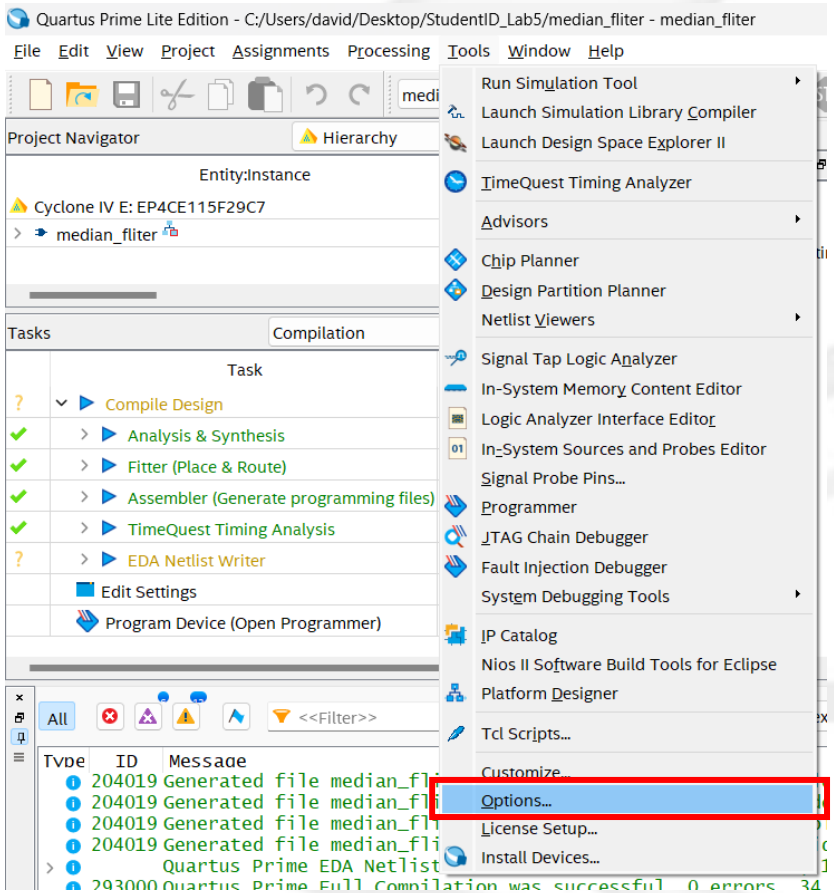
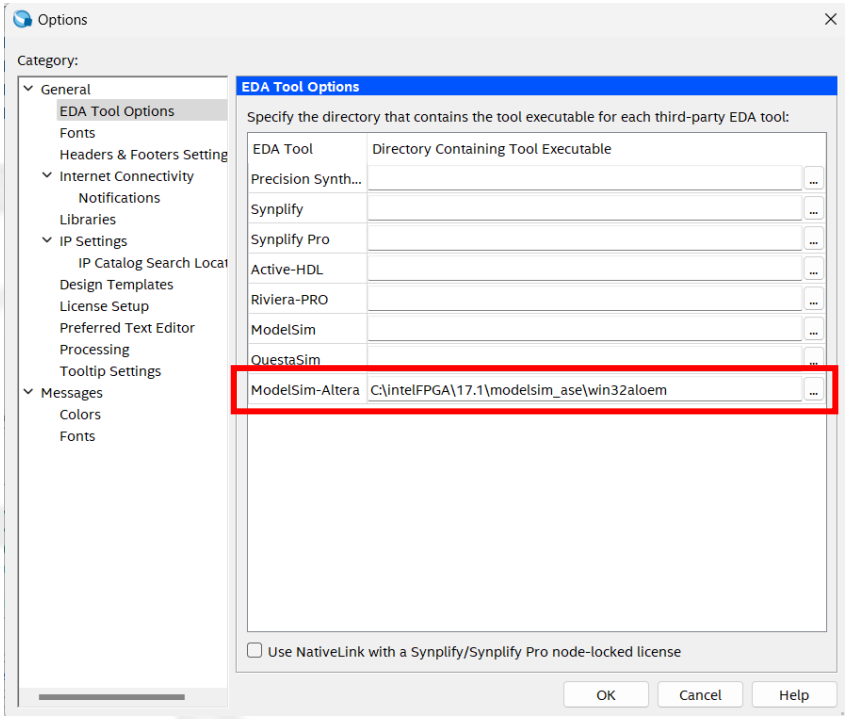
Setting Options for EDA Tools (1/4)

- Tool > Options…

Following our ModelSim installation tutorial typically installs the executable in this default location. However, there may be variations depending on your specific setup.





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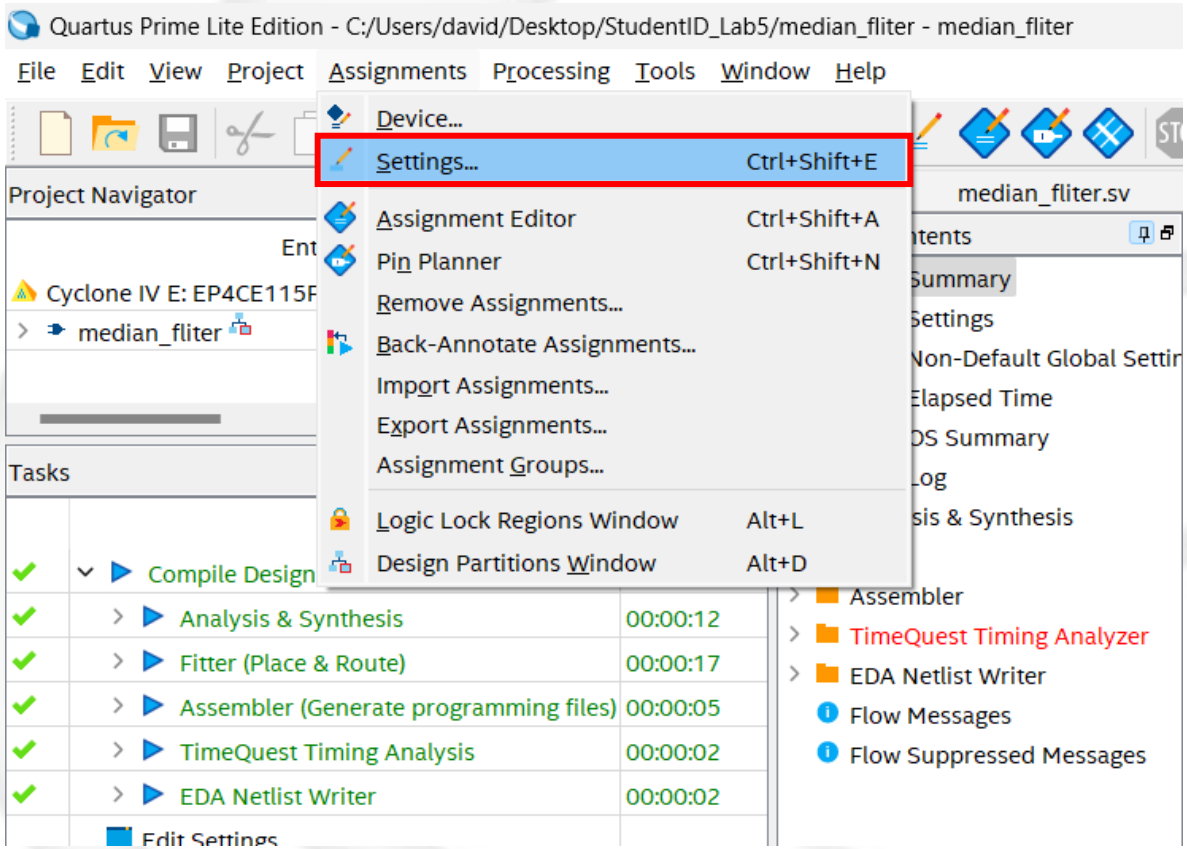
Setting Options for EDA Tools (2/4)

- Assignments > Settings



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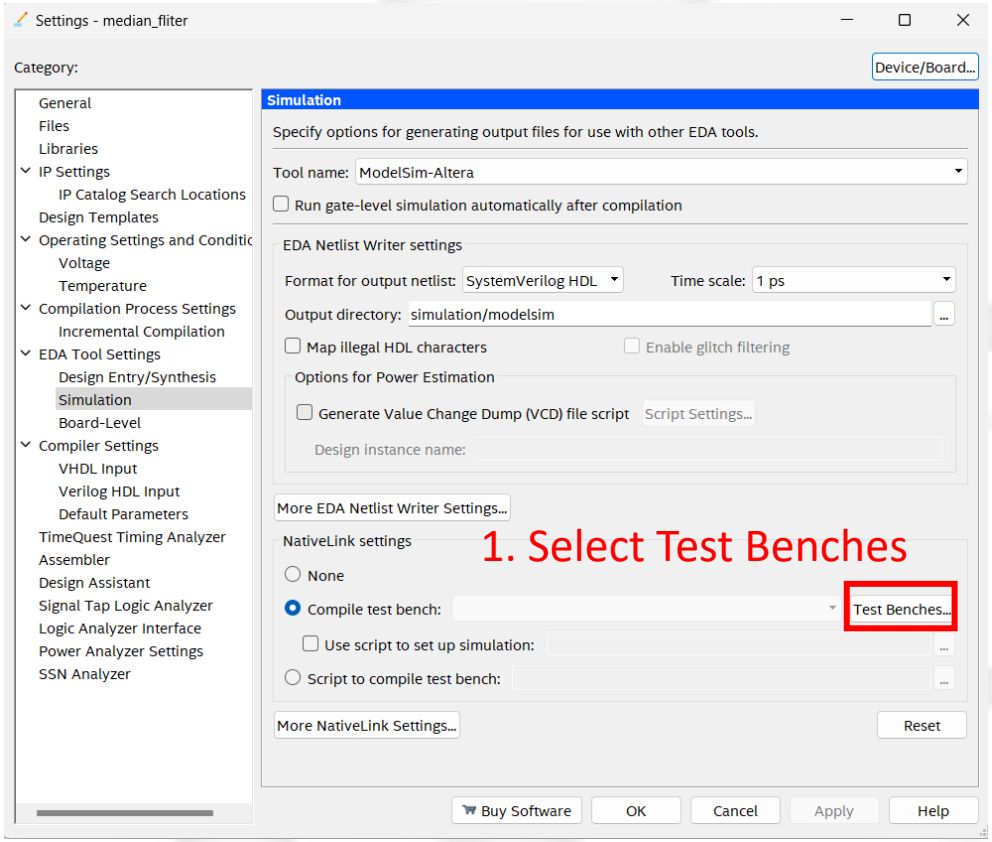
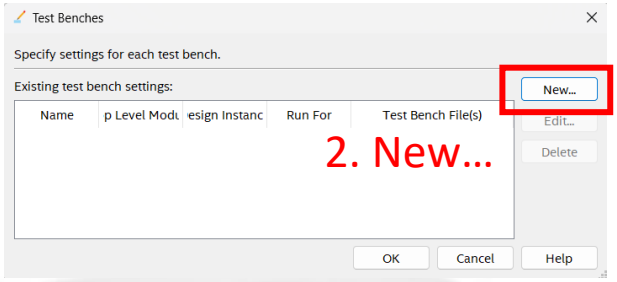
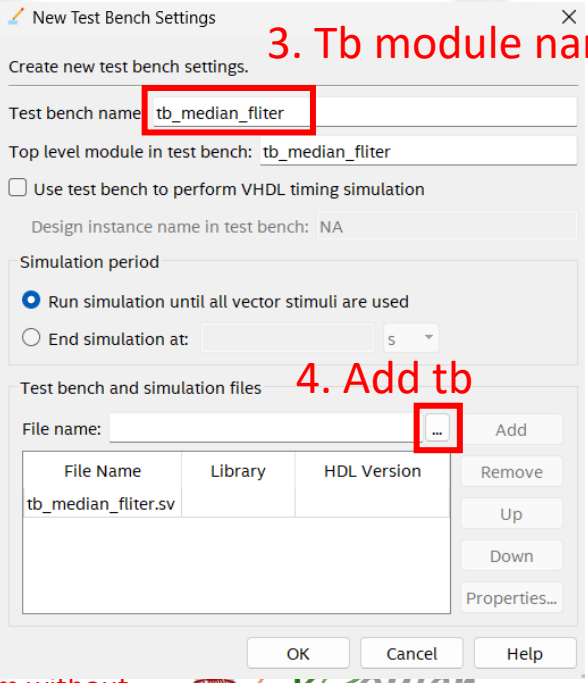
Setting Options for EDA Tools (3/4)

- Add test bench to project at ModelSim.







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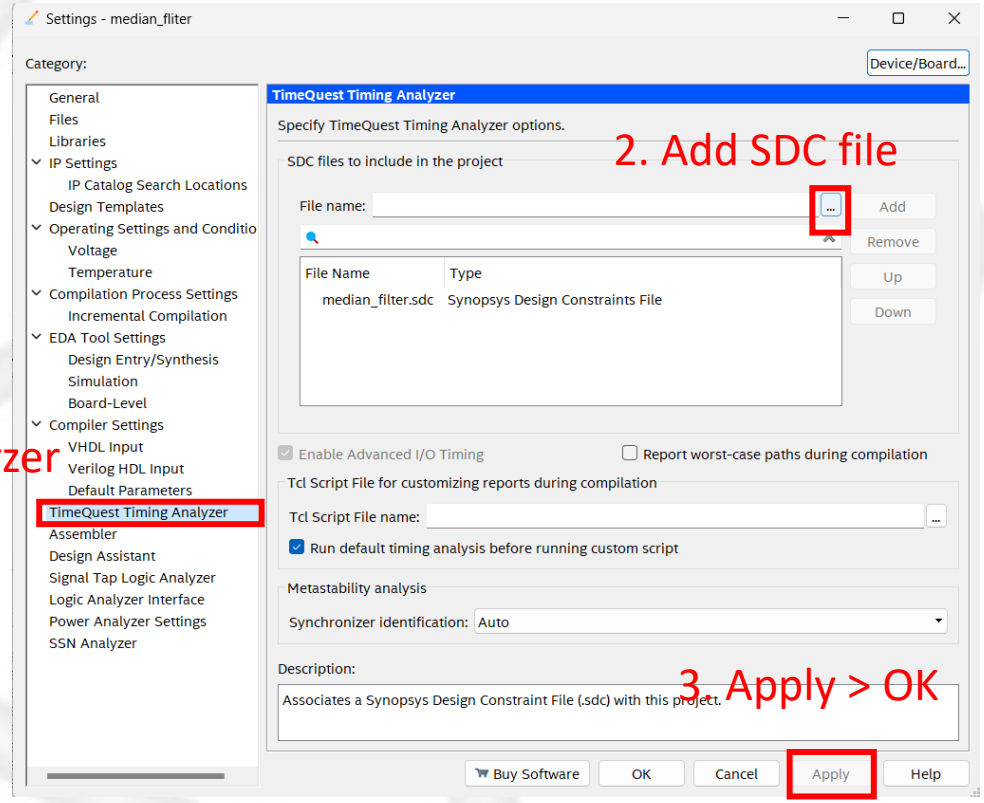
Setting Options for EDA Tools (4/4)

- Synopsys Design Constraints (SDC) files can be used to define the clock period during the synthesis stage.

1. TimeQuest Timing Analyzer



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Synopsys Design Constraints files

- By default, clock cycles in SDC files are specified in nanoseconds (ns). Ensure the clock period in the SDC file matches the value defined in your testbench.
- The clock port name in the SDC file should match the corresponding clock port name in your top-level module.

median_filter.sdc

C: > Users > david > Desktop > StudentID_Lab5 > median_filter.sdc

```
1  # operating conditions and boundary conditions #
2
3  set cycle 50.0
4  create_clock -name clk  -period $cycle   [get_ports  clk]
5  set_input_delay  1   -clock clk [remove_from_collection [all_inputs] [get_ports clk]]
6  set_output_delay 1    -clock clk [all_outputs]
```

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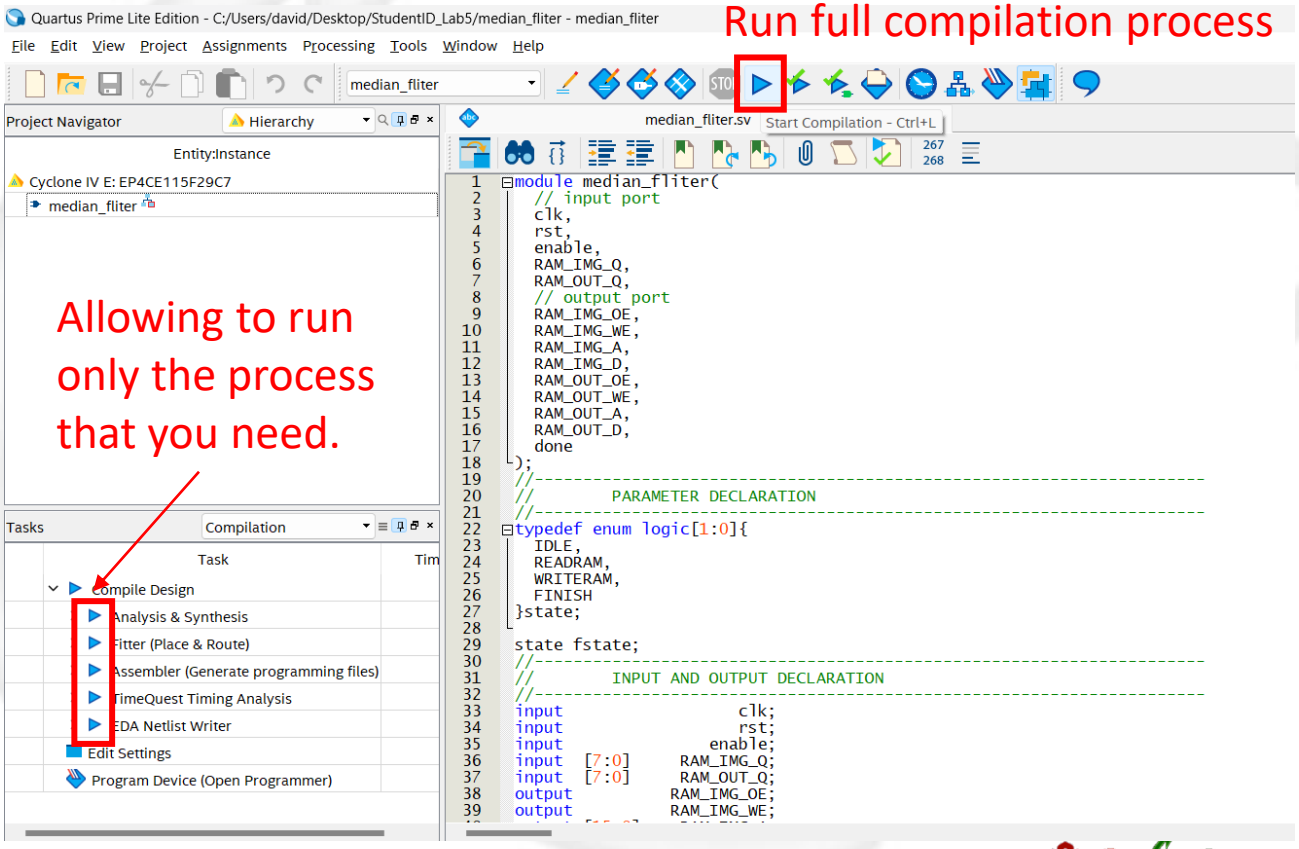
Design Compilation

- When you run any module, the Compiler runs automatically and generates detailed reports at each stage.



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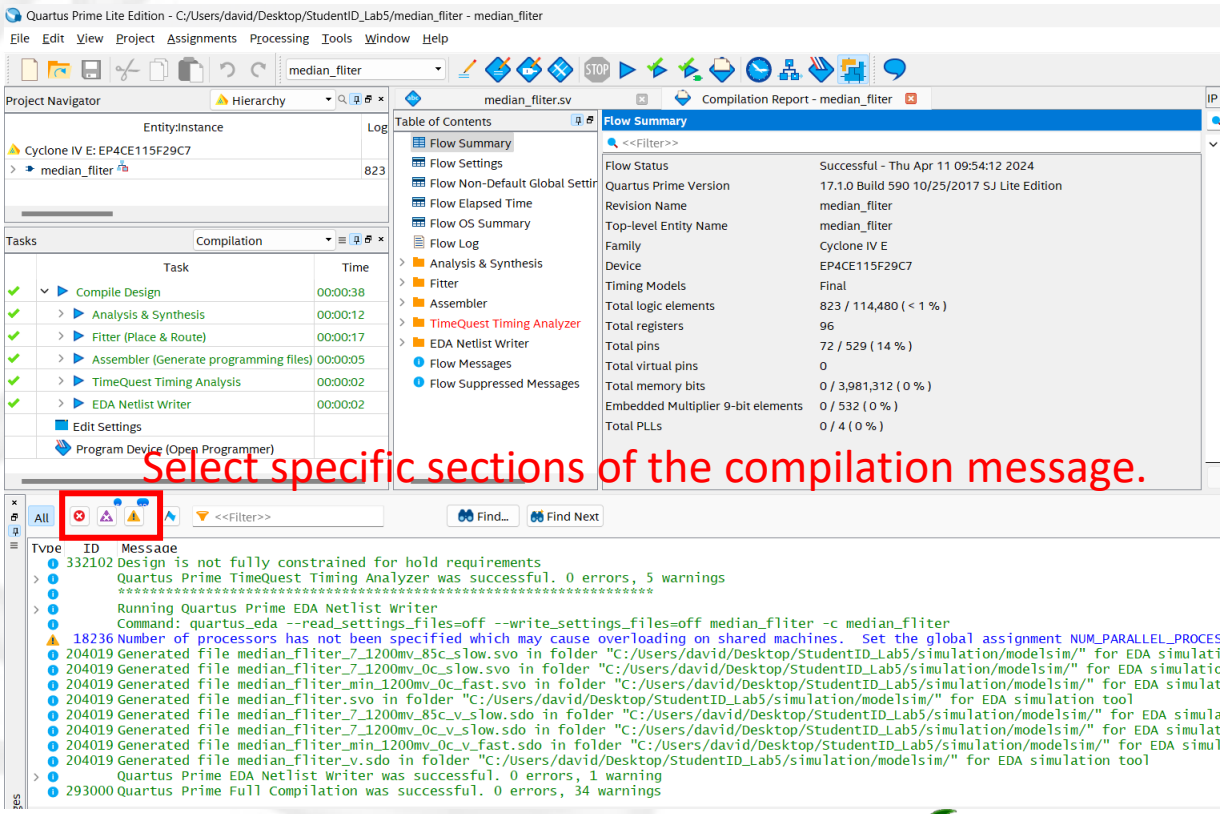
Error and Warning Messages

- Upon compilation, errors will be displayed in the terminal, Double-clicking the error message should navigate you to the line of code where the error occurred.



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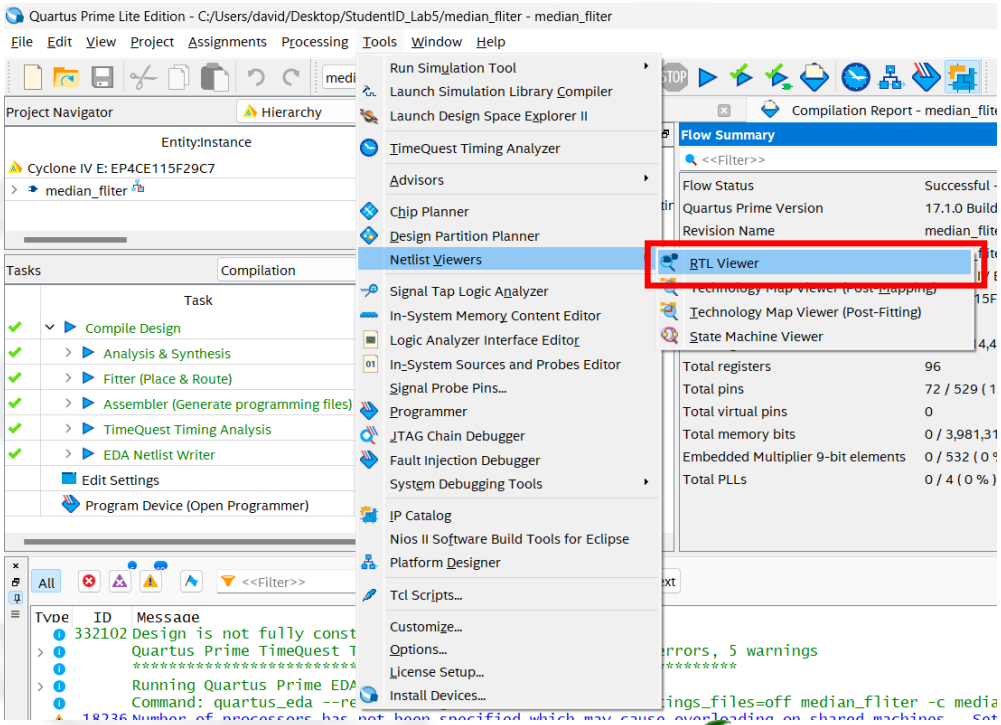
RTL Viewer Overview (1/3)

- Allowing you to view a register transfer level (RTL) graphical representation of Intel® Quartus® Prime integrated synthesis results.
- Tool > Netlist Viewers > RTL Viewer



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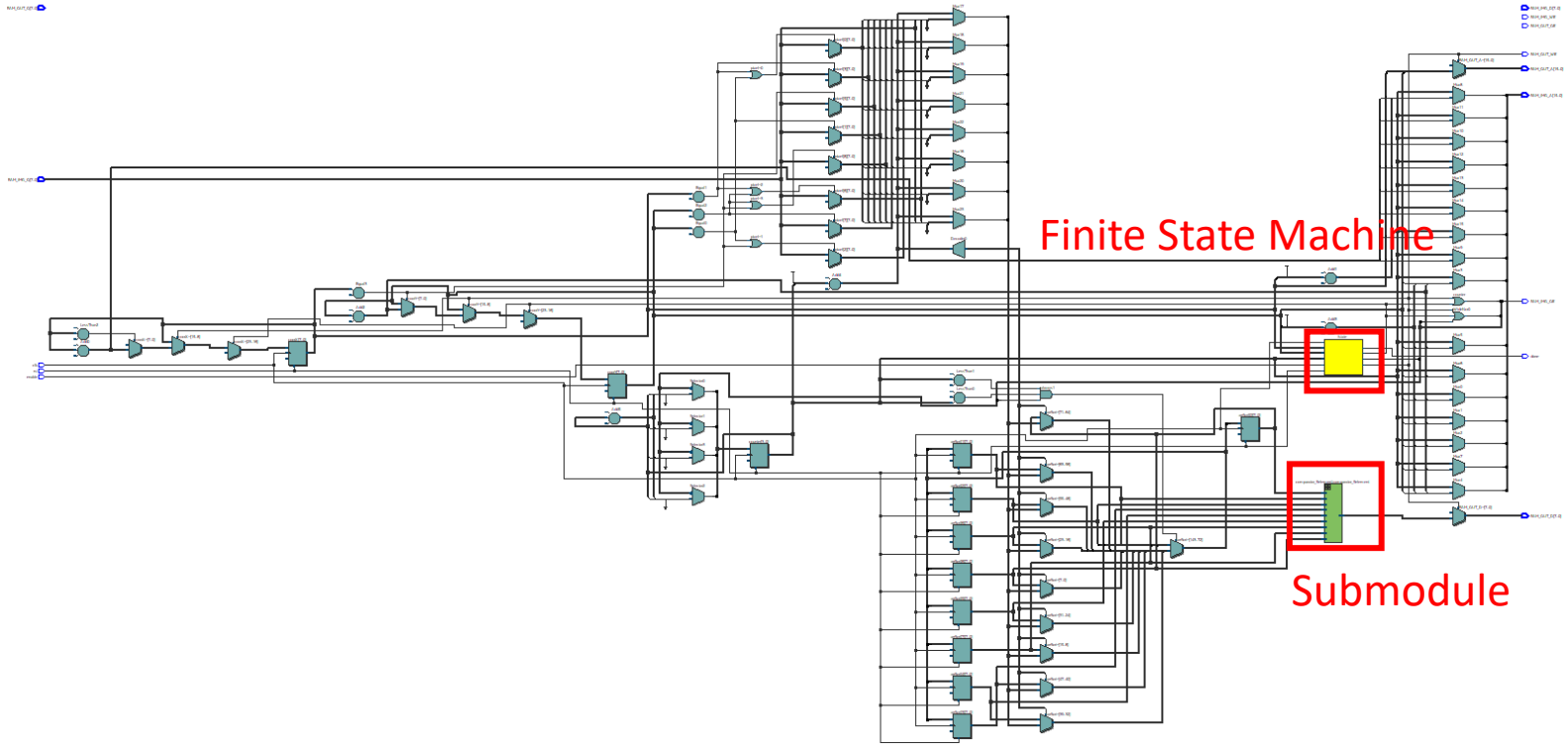
RTL Viewer Overview (2/3)

- Schematic view of the design netlist after software performs netlist extraction, but before technology mapping and synthesis or fitter optimizations.



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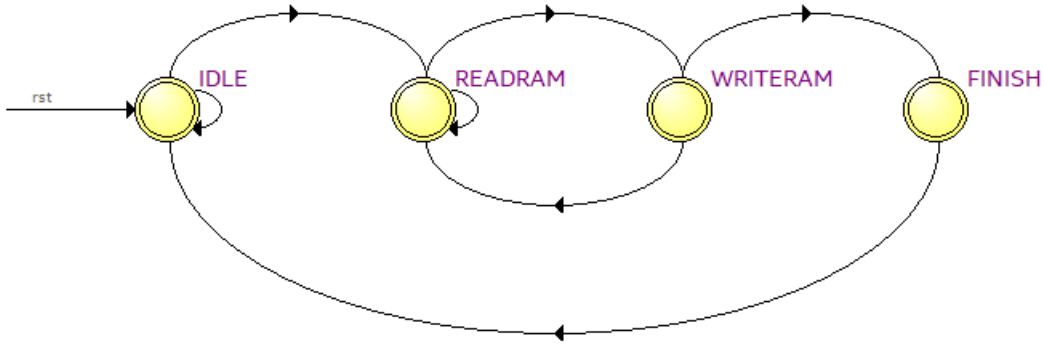
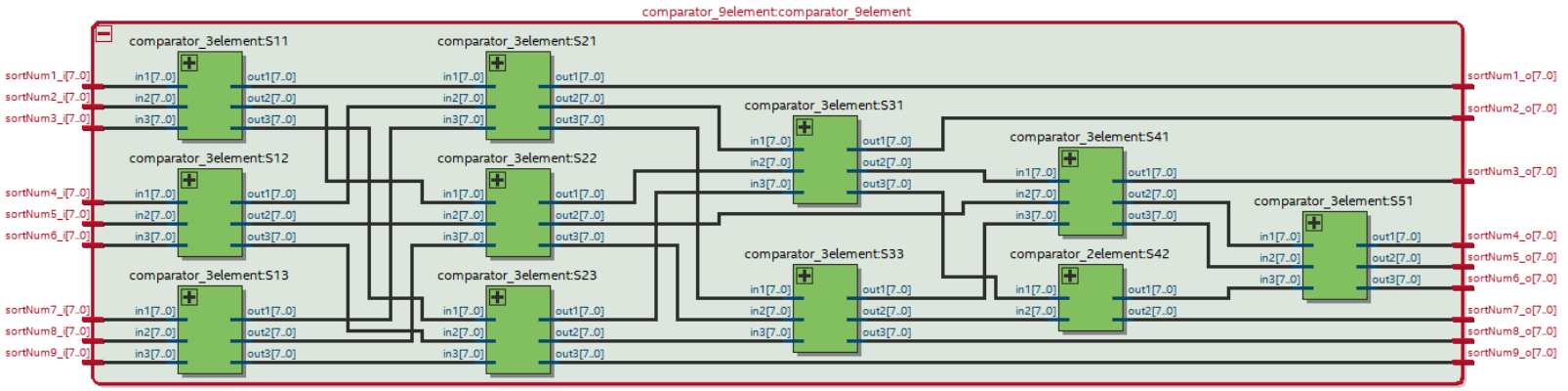
RTL Viewer Overview (3/3)

- Double click to view FSM.



- Double click to view submodule (Sorting Combinational circuit)



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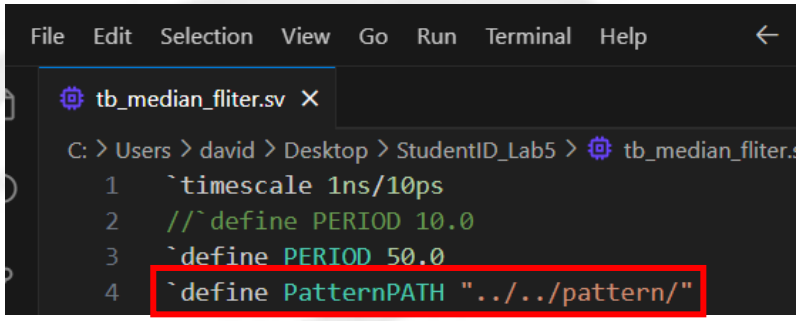
Before ModelSim Simulation

- Within Quartus projects, simulation files are typically located at $(your_path)/simulation/modelsim. Be mindful of using relative file paths in your testbench to ensure proper access.



- Ensure you close ModelSim before returning to Quartus after completing each waveform simulation. Important

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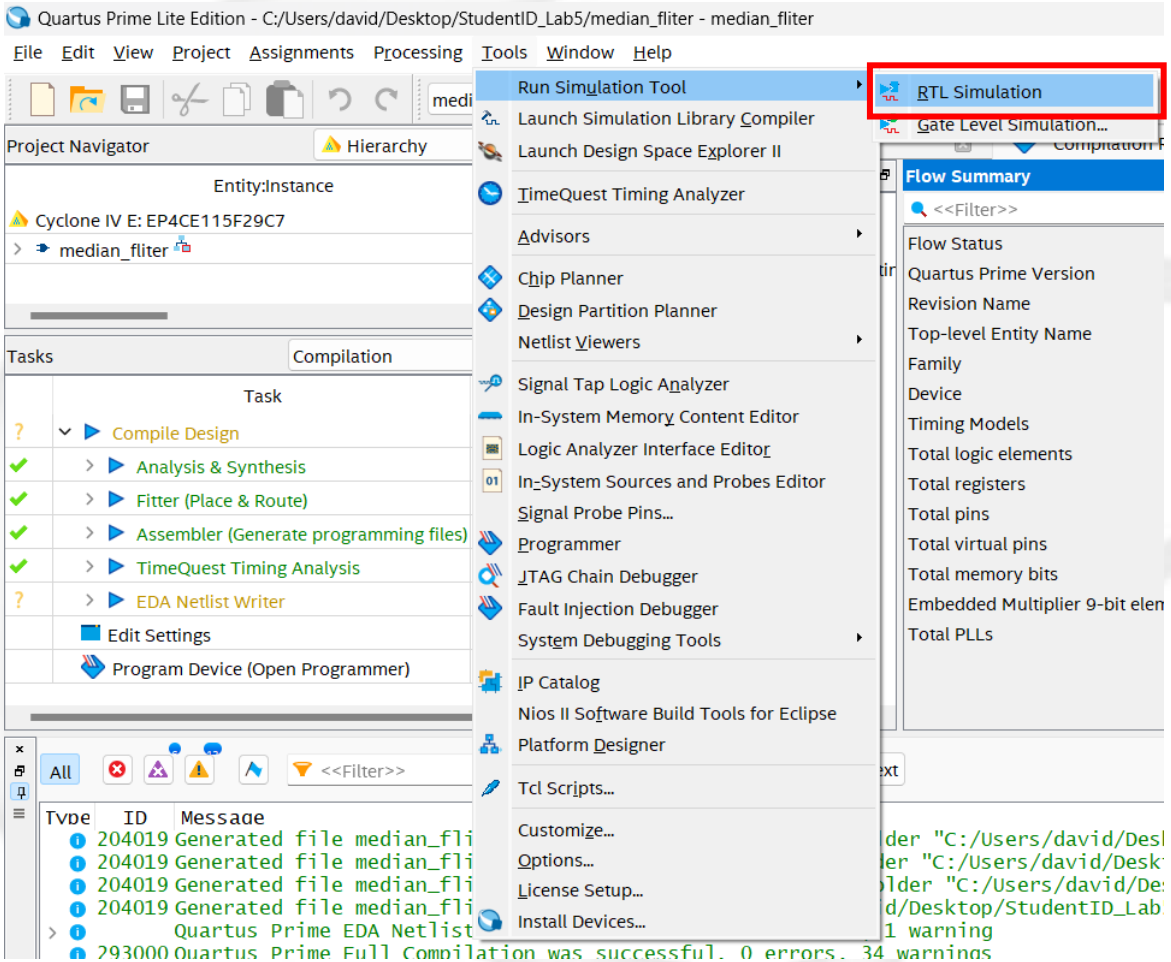
Run RTL simulation

- Tool > Run Simulation Tool > RTL Simulation



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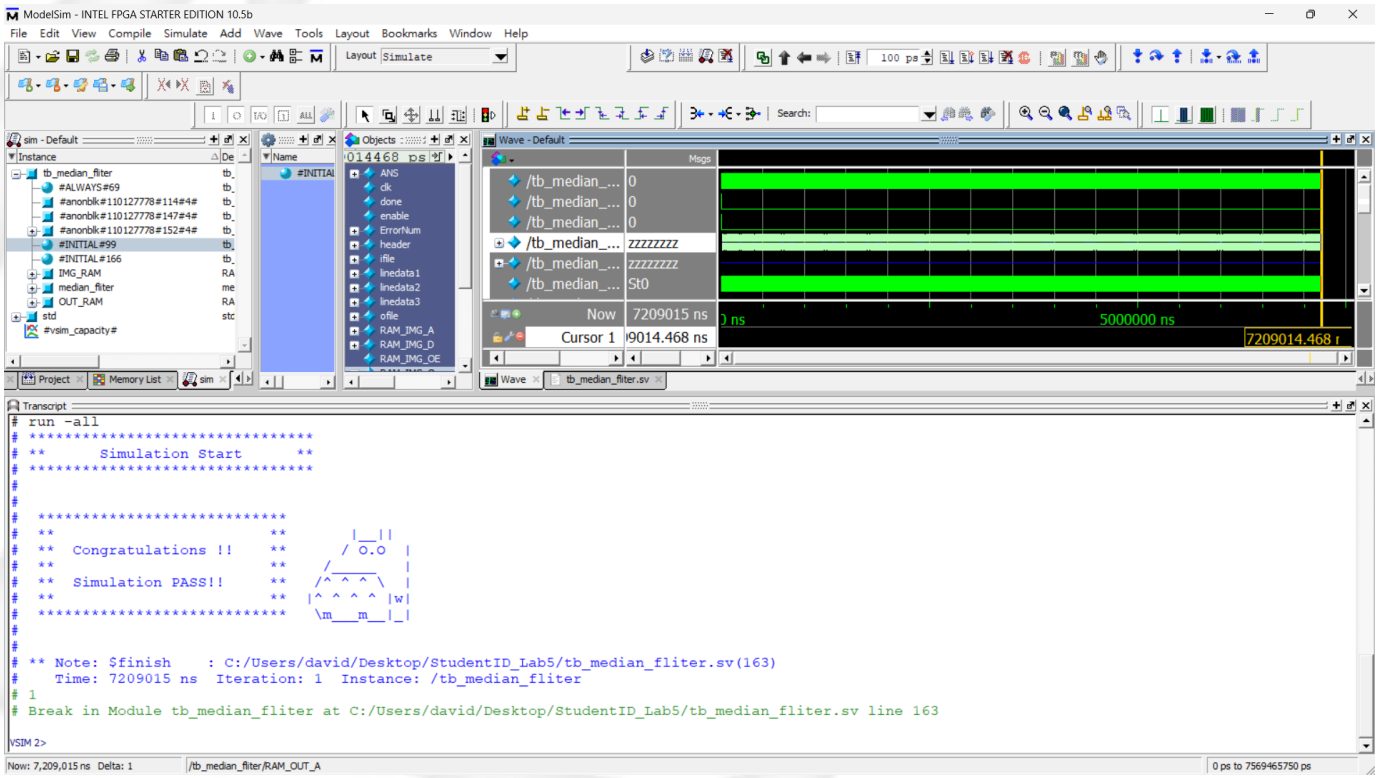
Run RTL simulation and Launch ModelSim

- Running the simulation through Quartus should produce results identical to those obtained by directly running it on ModelSim with pre-synthesis RTL.



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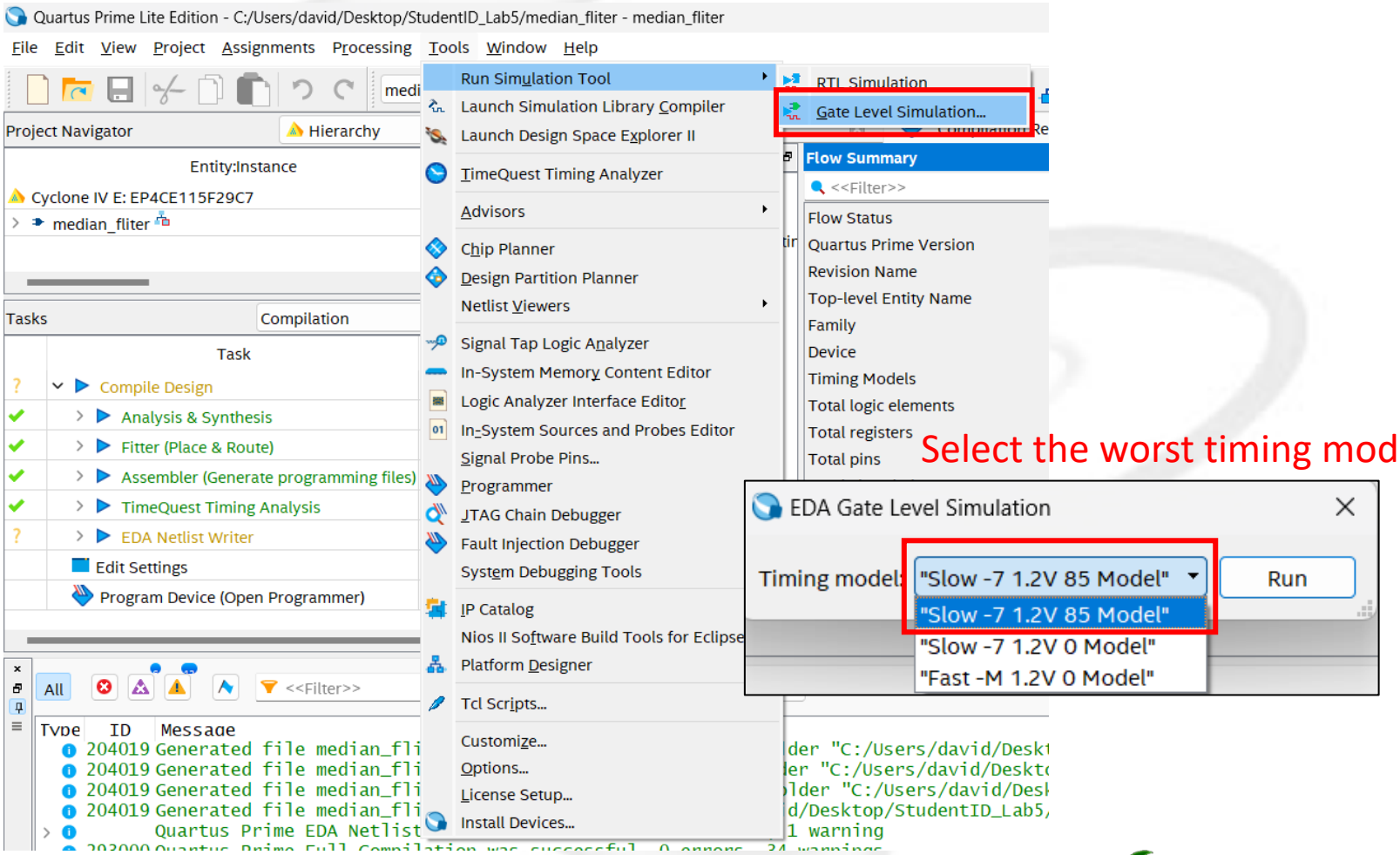
Run Gate-Level Simulation

- Tool > Run Simulation Tool > RTL Simulation



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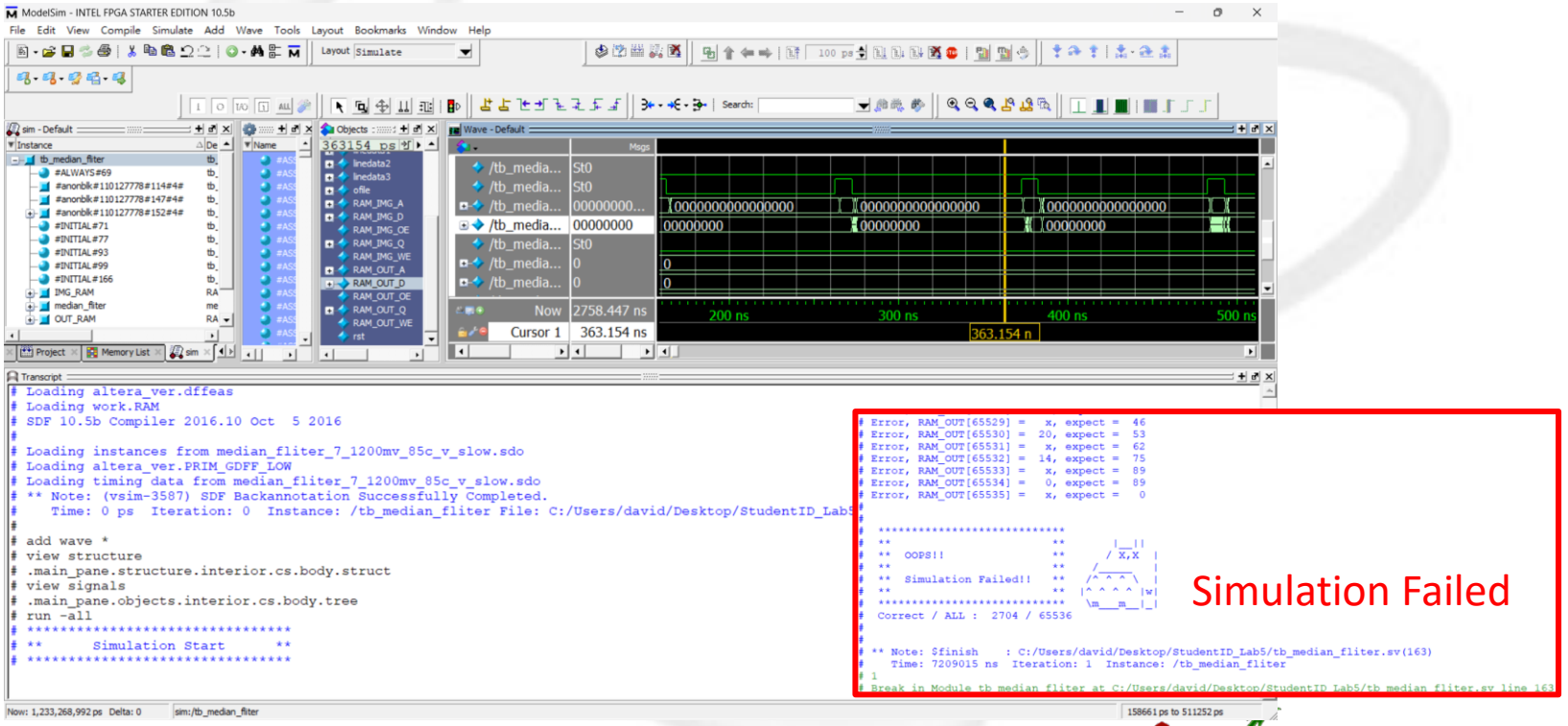
Run Gate-Level Simulation and Launch ModelSim

- After synthesis, the waveform may exhibit transition uncertainty. Additionally, simulation results might indicate timing violations due to insufficient clock frequency, leading to final failure.



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Outline

- Introduction to FPGA
- Tool Installation
- Quartus Basic GUI
  - Create Project
  - EDA tools Setting
  - Compilation & Synthesis
  - Waveform Simulation
  - Power, Performance and Area

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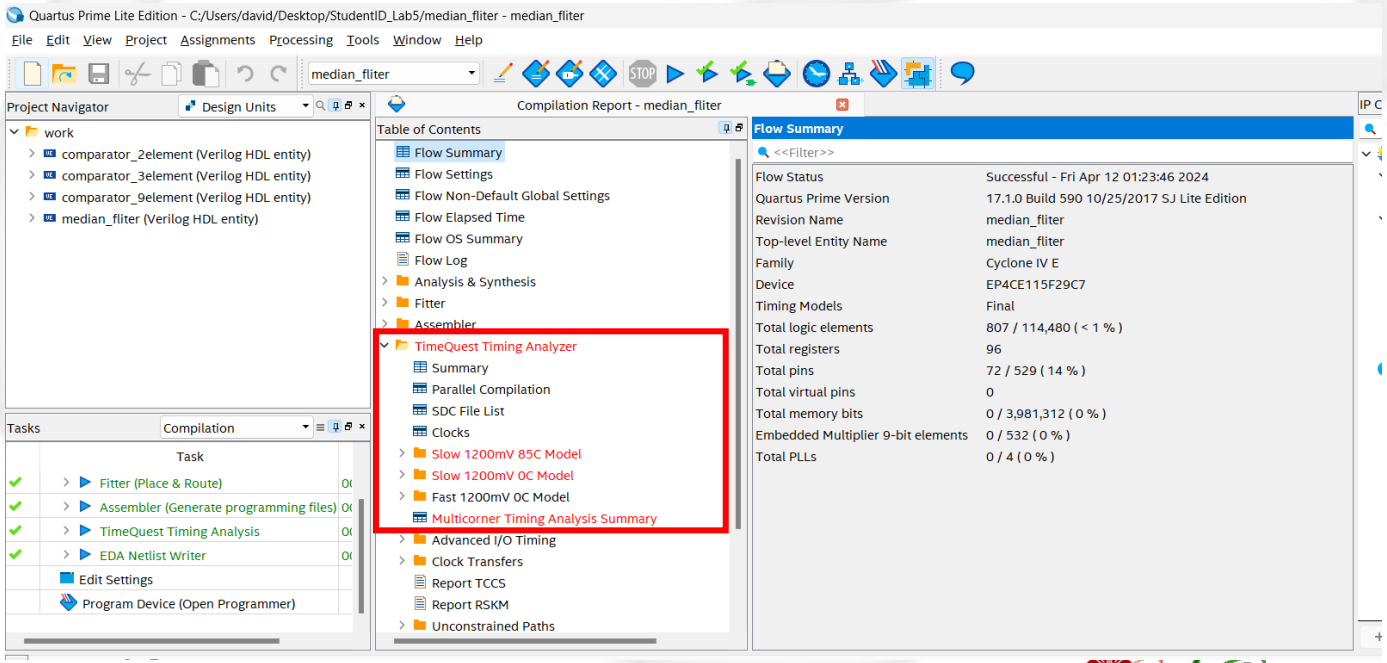
TimeQuest Timing Analyzer (1/3)

- In TimeQuest Timing Analyzer, red text after synthesis indicates potential timing violations in your design. To address this, you'll need to increase the clock period defined in both the SDC file and testbench, followed by another synthesis run.



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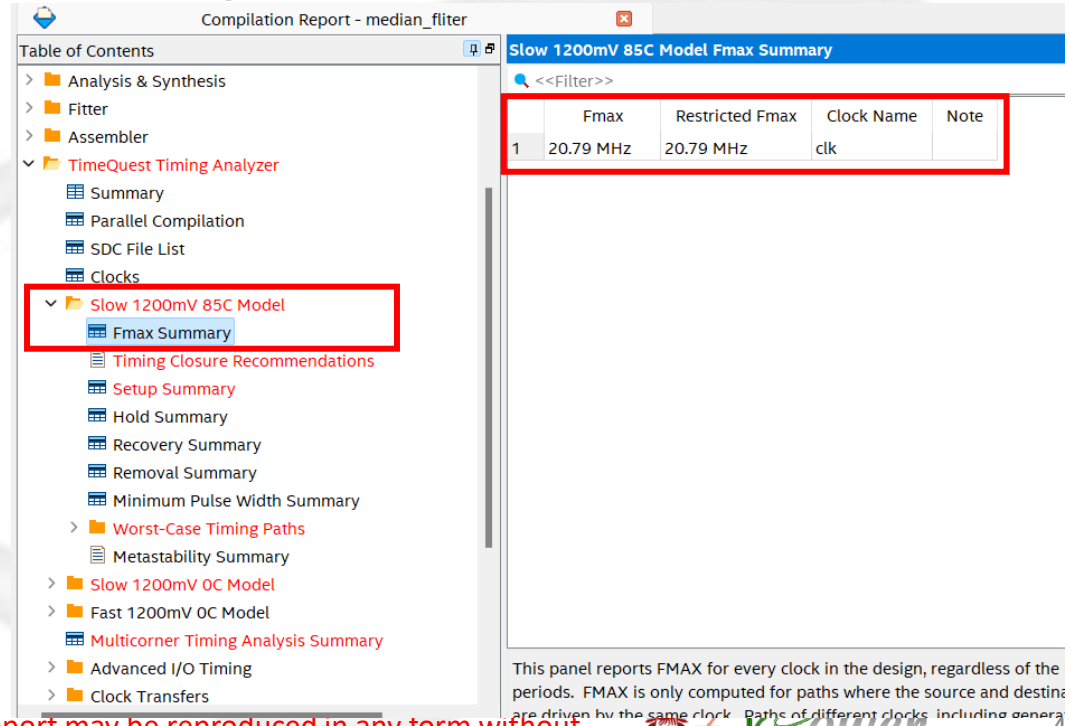
TimeQuest Timing Analyzer (2/3)

- In this scenario, timing violations occur in two timing models (Slow 1200mV 85C Model & Slow 1200mV 0C Model). Clicking on the specific timing model and reviewing the Fmax Summary will reveal the expected clock frequency for your design.



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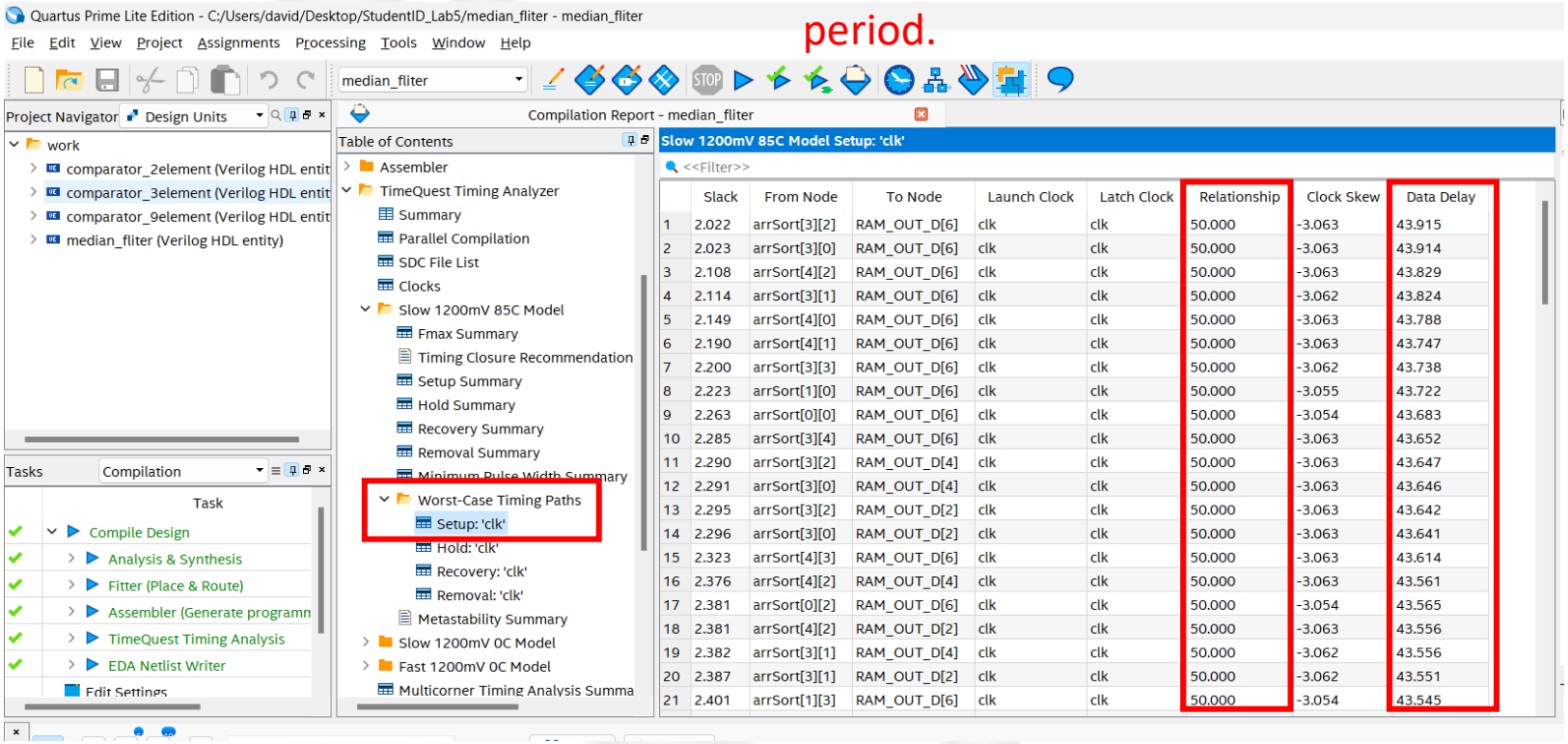
TimeQuest Timing Analyzer (3/3)

- The worst-case timing paths highlight the critical path in your design.

The setup timing slack is calculated by subtracting the data delay from the clock period.



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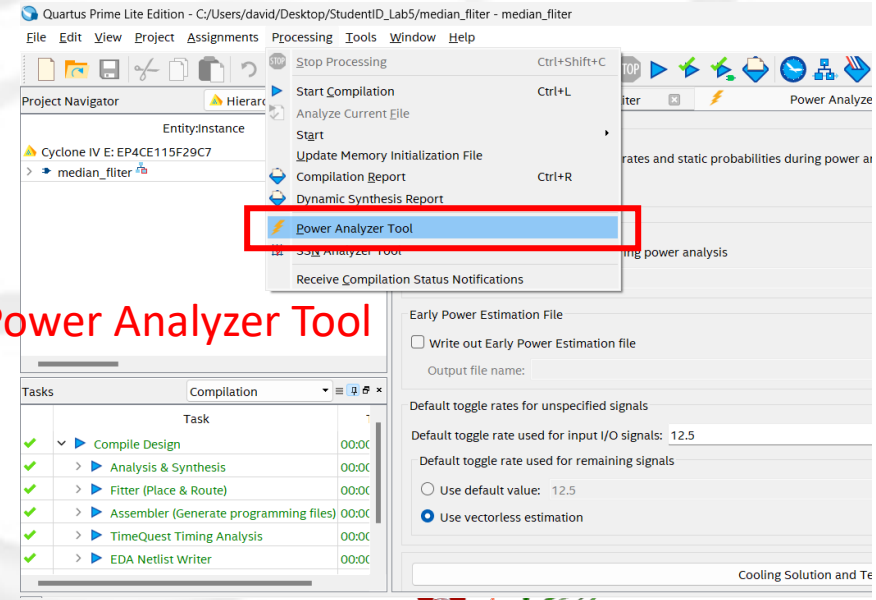
Power Analyzer Tool (1/5)

- For accurate power estimation during simulation, utilize the VCD file format for waveform data capture.

```
tb_median_fliter.sv
C: > Users > david > Desktop > StudentID_Lab5 > tb_median
10   module tb_median_fliter;
177  initial begin
178    $dumpfile("tb_median_fliter.vcd");
179    $dumpvars(0, tb_median_fliter);
180  end
```

The $dumpvars task shall be used to list which variables to dump into the file specified by $dumpfile.
Freely adjust the scope to view any desired waveform region.

- Once you have generated the VCD file, proceed with power analysis.



Processing > Power Analyzer Tool

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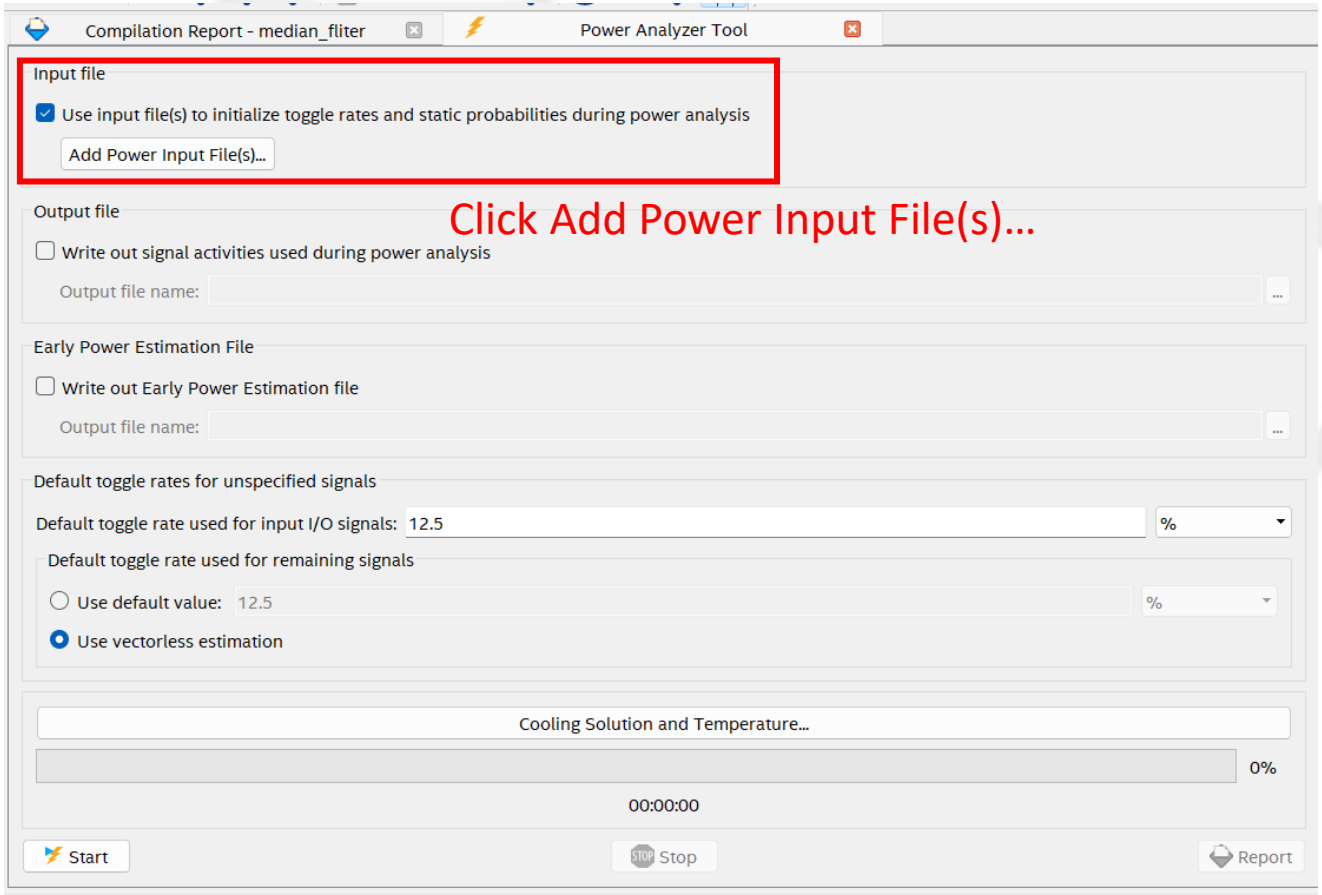
Power Analyzer Tool (2/5)

- Import the VCD file for dynamic power analysis.



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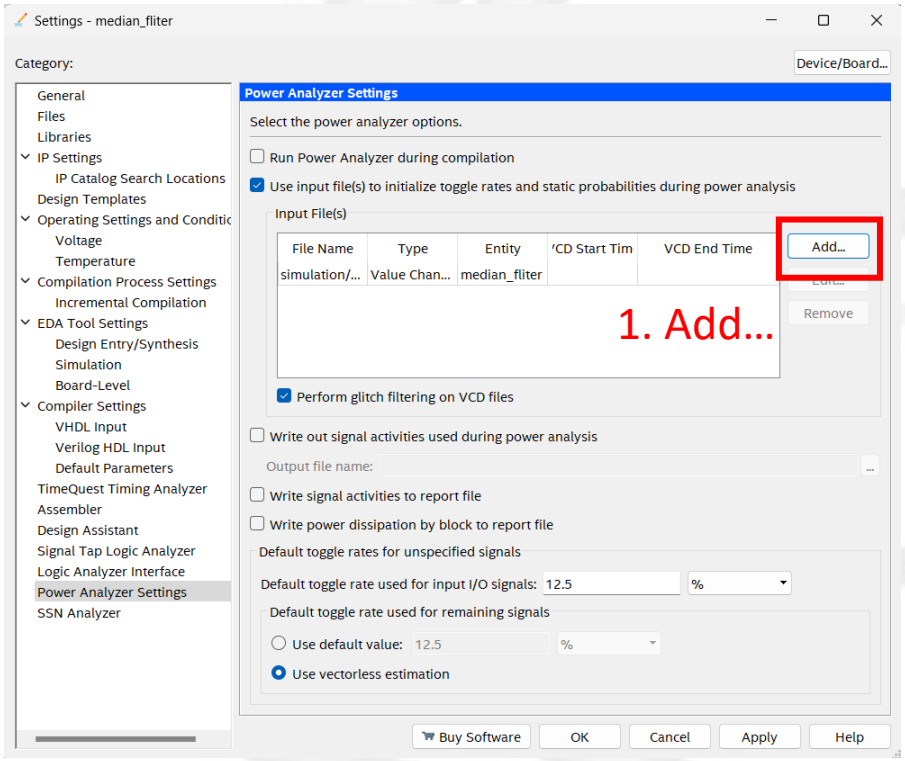
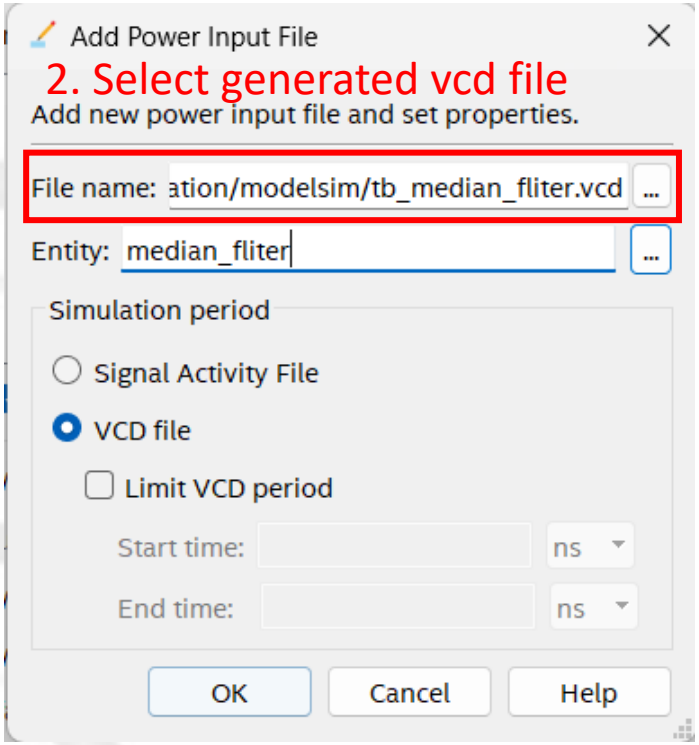
Power Analyzer Tool (3/5)

- Quartus generates the simulation folder, which contains the VCD file.





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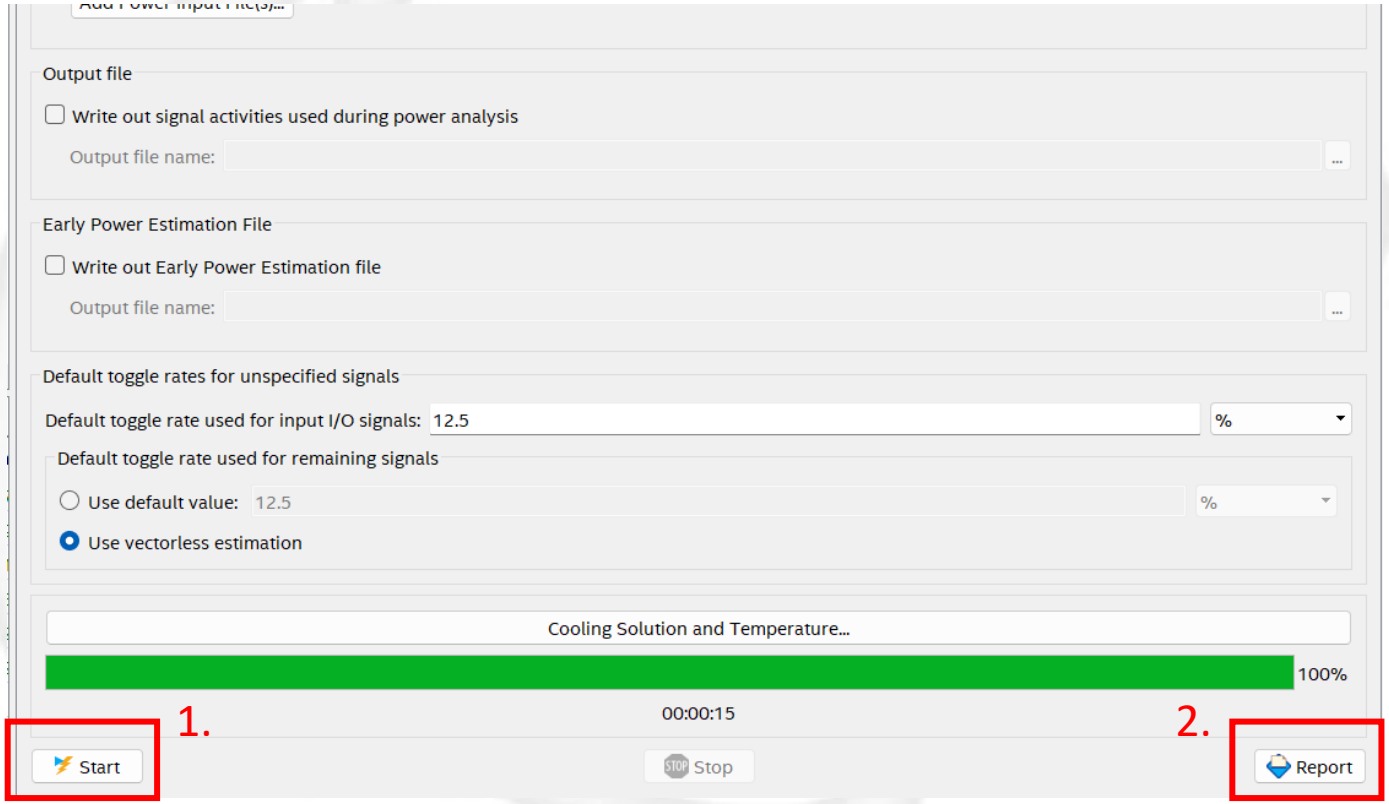
Power Analyzer Tool (4/5)

- Click "Start" to initiate the power analysis. Once complete, access the power estimation report by clicking "Report."



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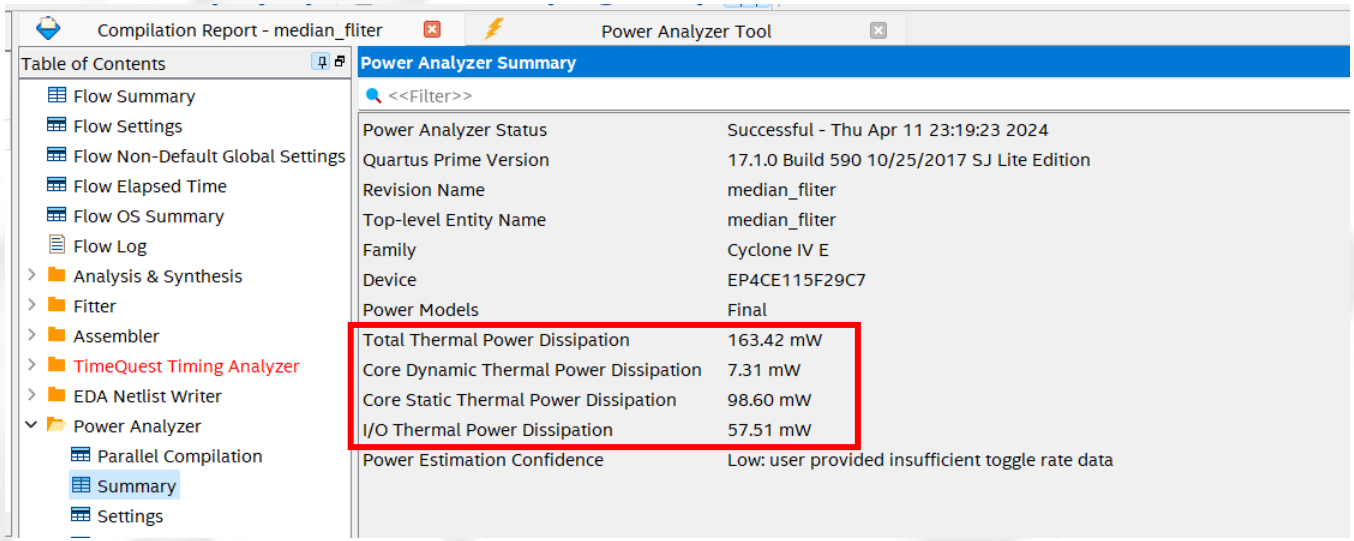
Power Analyzer Tool (5/5)

- Summary of Power Analysis



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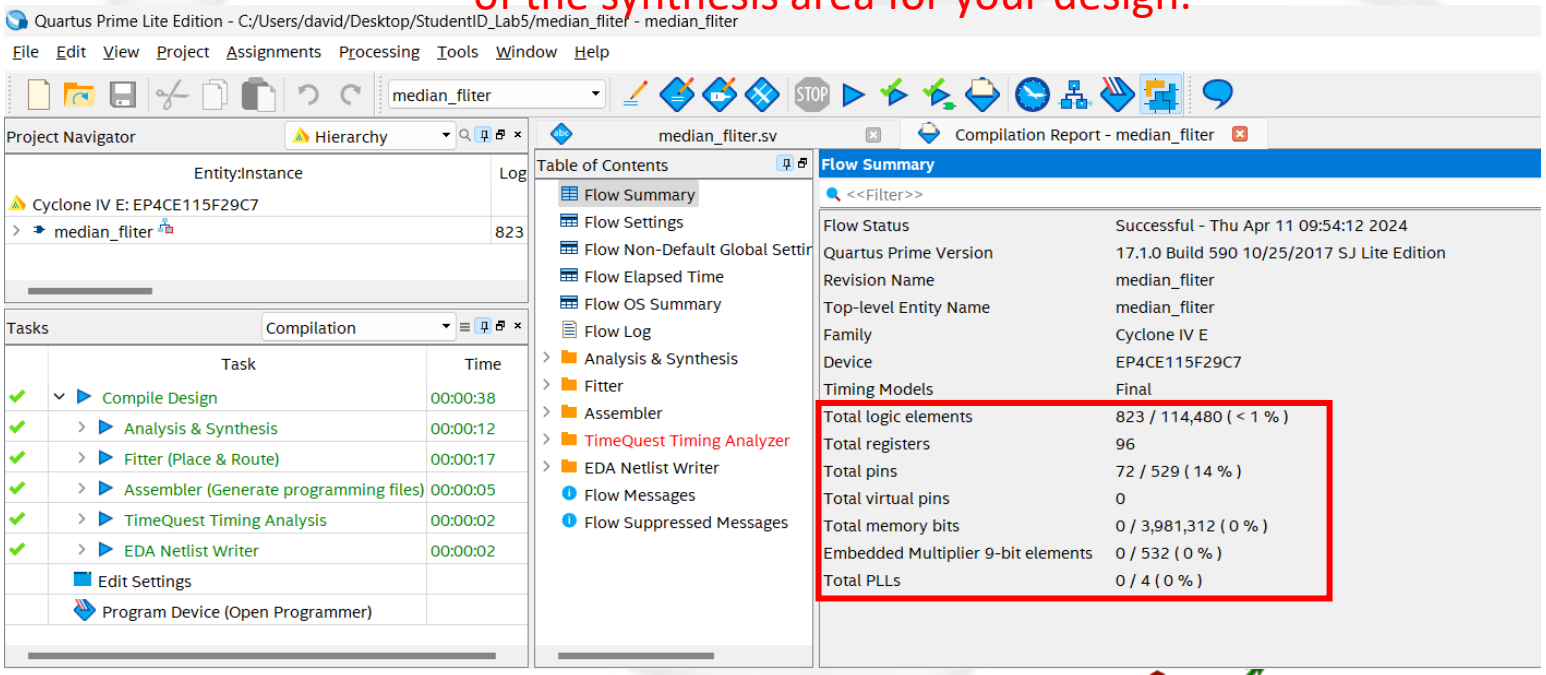
Flow Summary

- The Flow Summary section of the compilation report indicates whether the design exceeds the available device resources, and reports resource utilization, including pins, memory bits, DSP blocks, and PLLs.

The logic elements provide a preliminary estimate of the synthesis area for your design.



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Thank you for your attention

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