Siemens HDL Simulator : ModelSim

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Outline

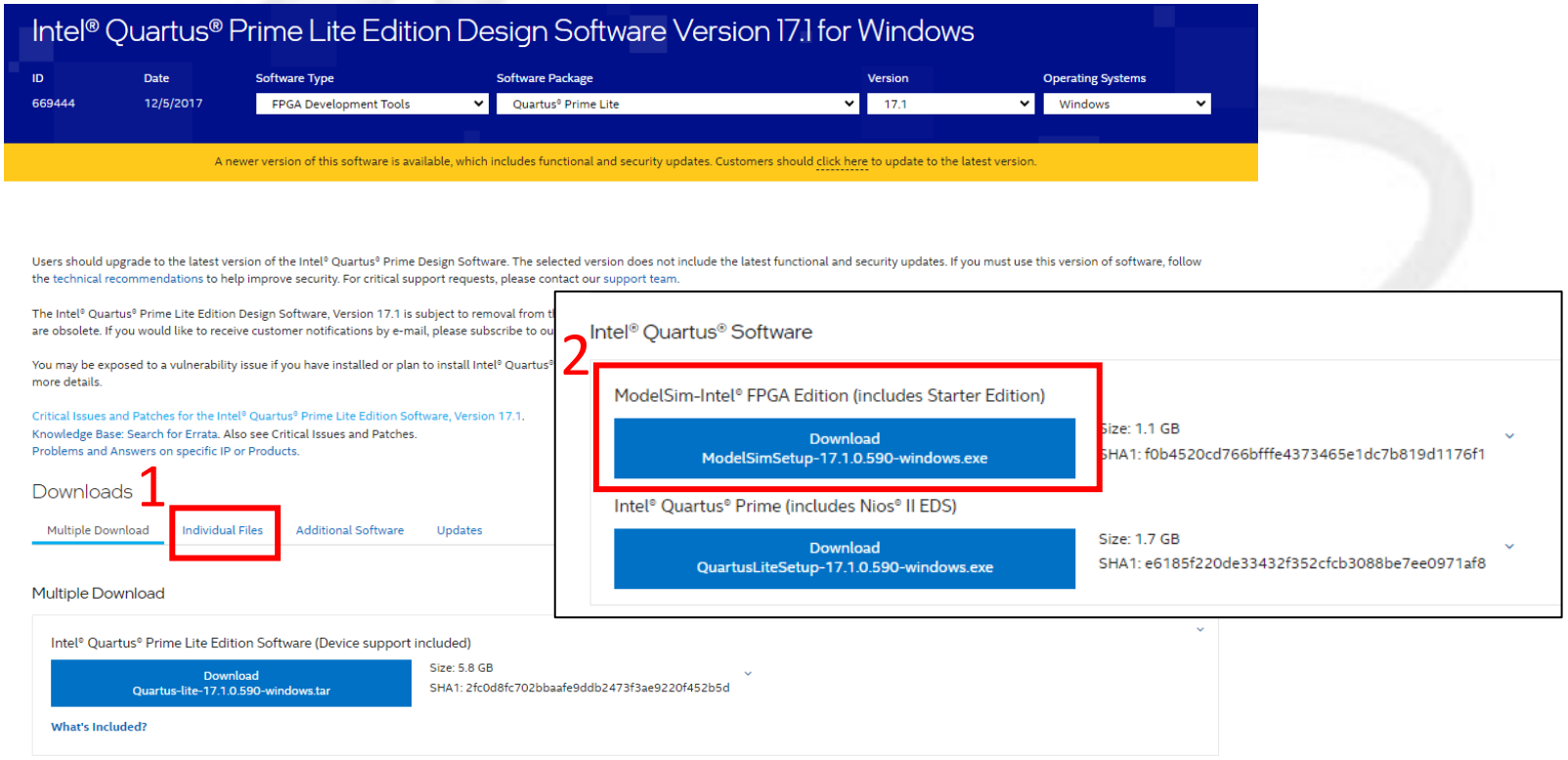
- Tool Introduction
- Tool Installation
- Basic Simulation Flow
- Debugging using Modelsim

Tool Introduction

- ModelSim is a verification and simulation tool for VHDL, Verilog, SystemVerilog, and mixed-language designs.
- Feature:
  - Check HDL code for syntax error
  - Simulate and dump waveform

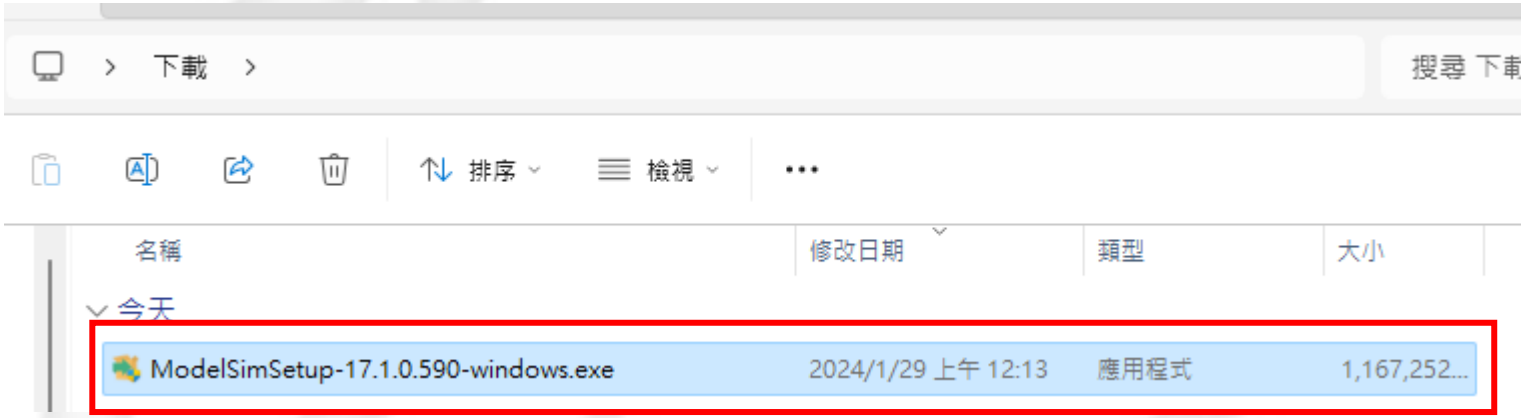
Tool Installation (1/7)

- ModelSim Edition 10.5b: Download Link
- Individual Files > Download ModelSimSetup…



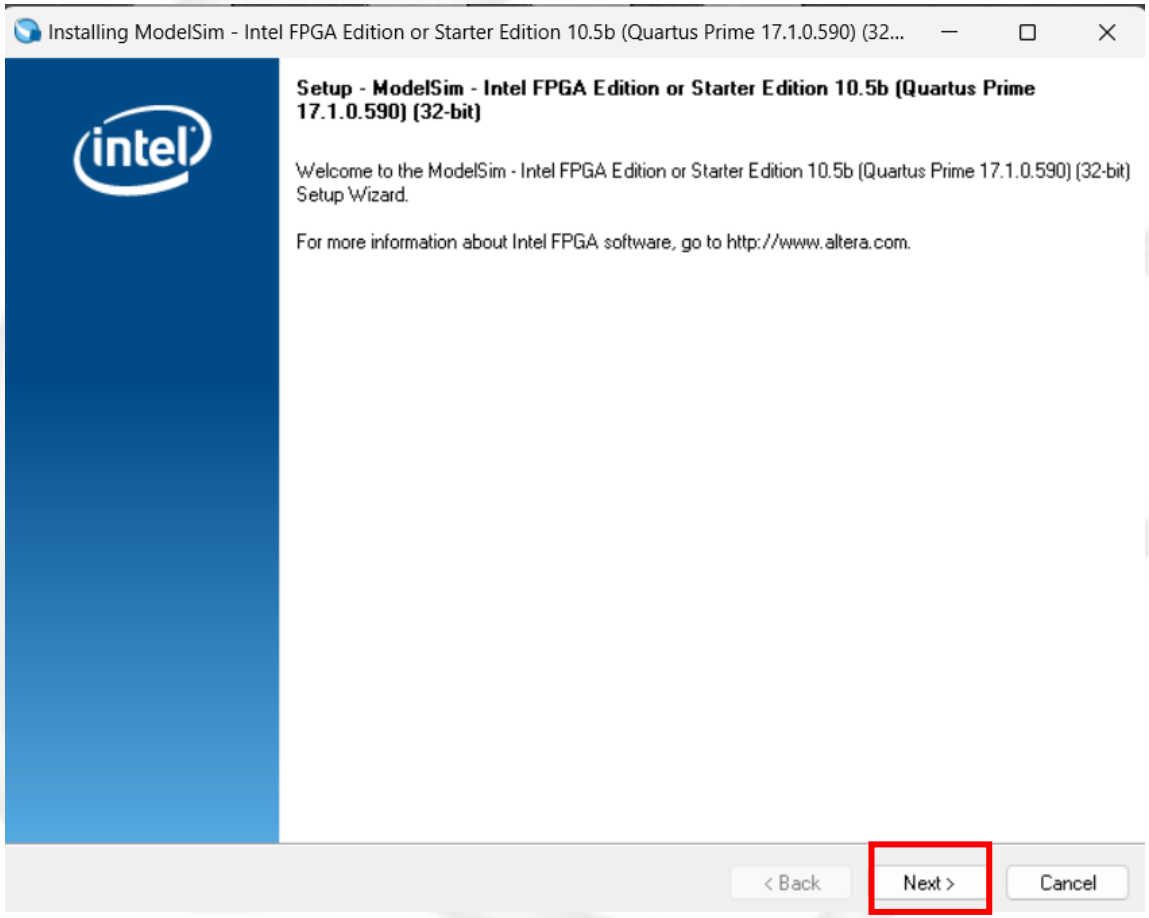
Tool Installation (2/7)

- Click .exe file to installation



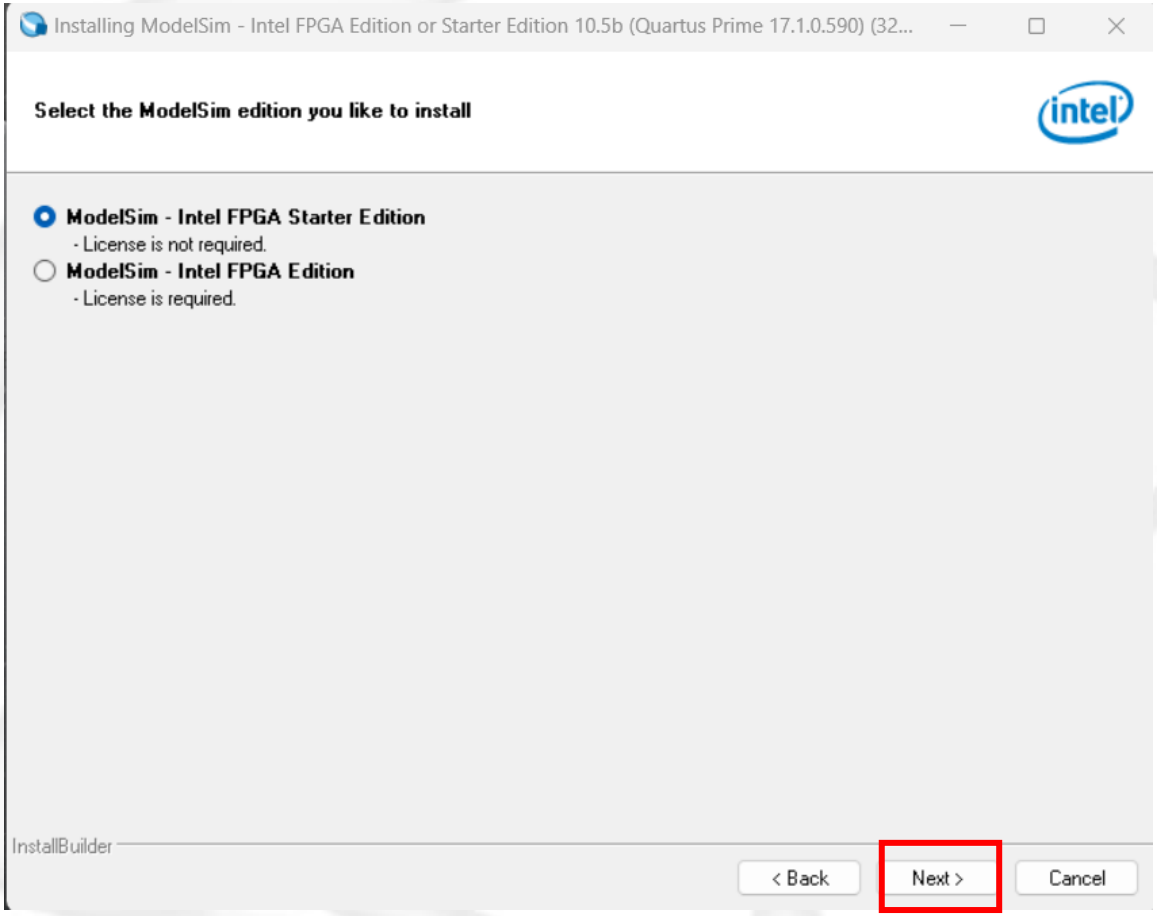
Tool Installation (3/7)

- Next



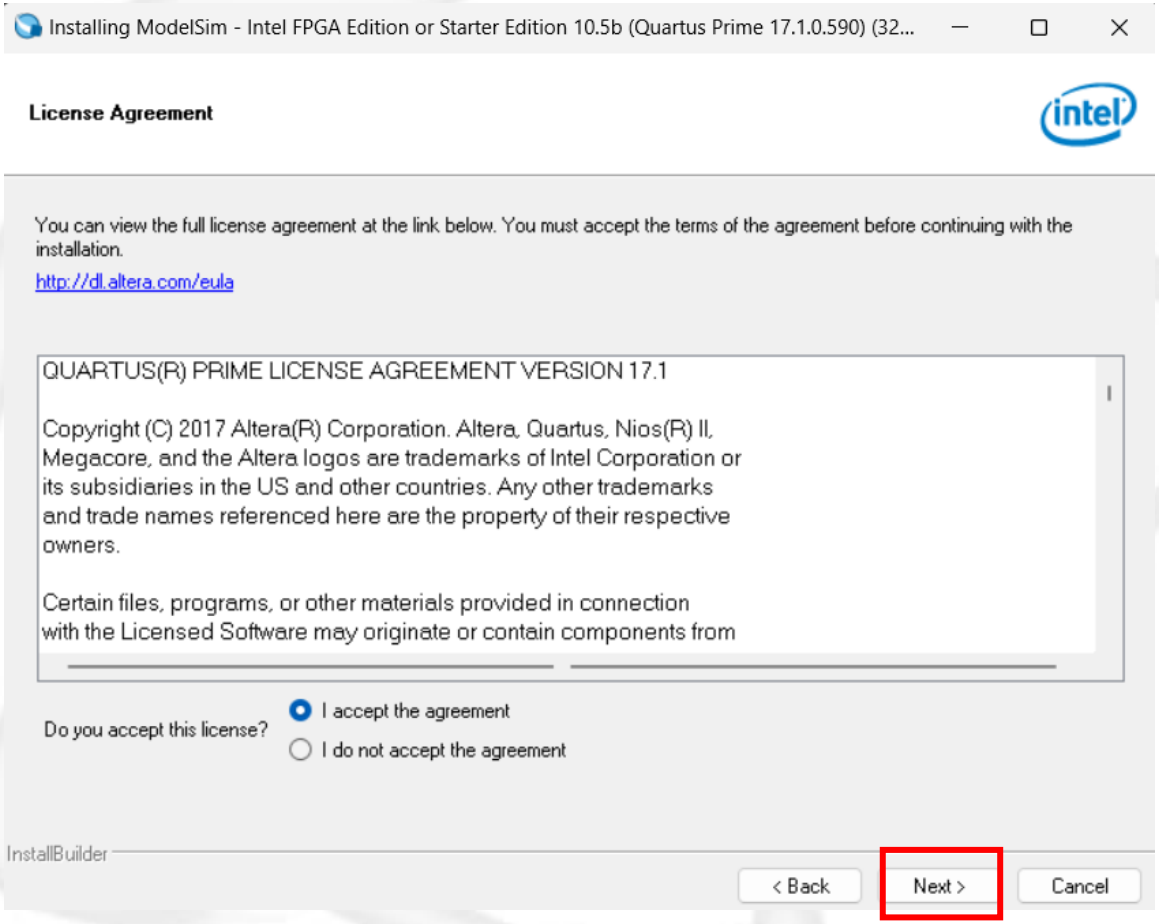
Tool Installation (4/7)

- Select ModelSim - Intel FPGA Starter Edition



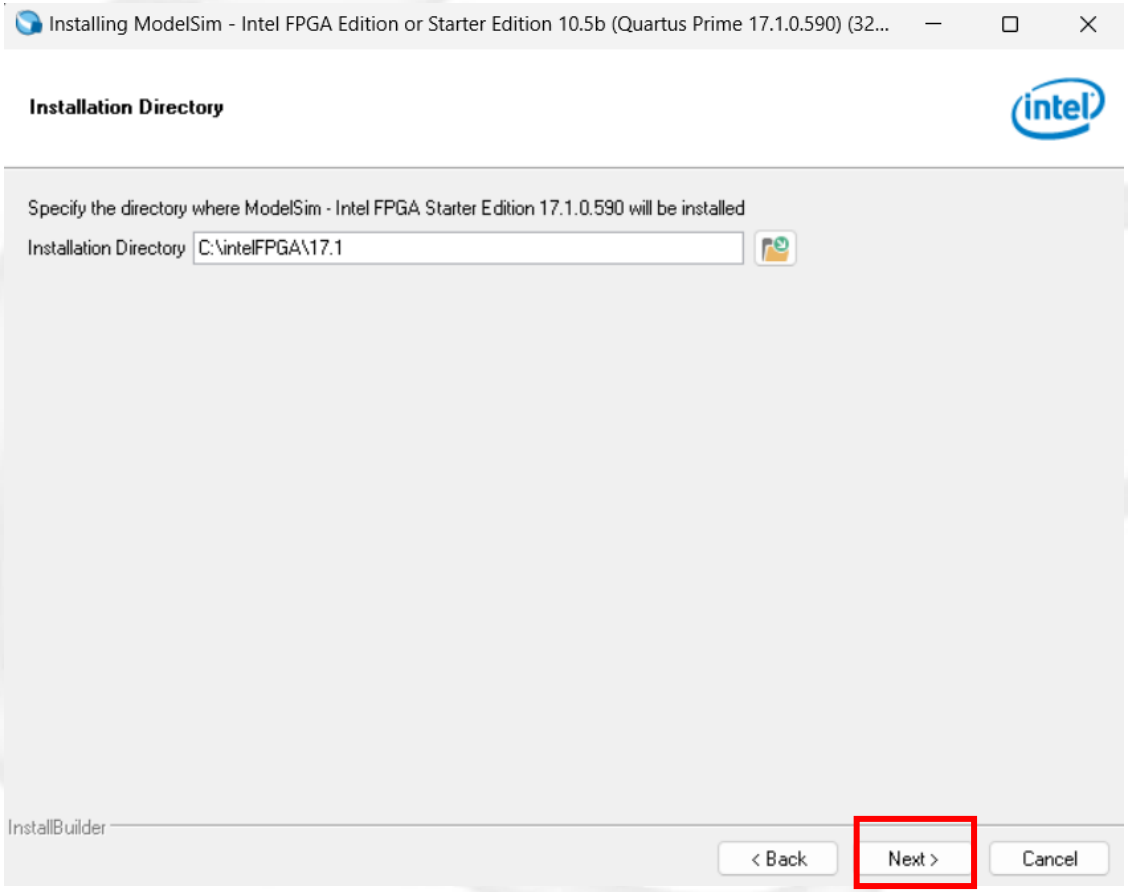
Tool Installation (5/7)

- I accept the agreement > Next



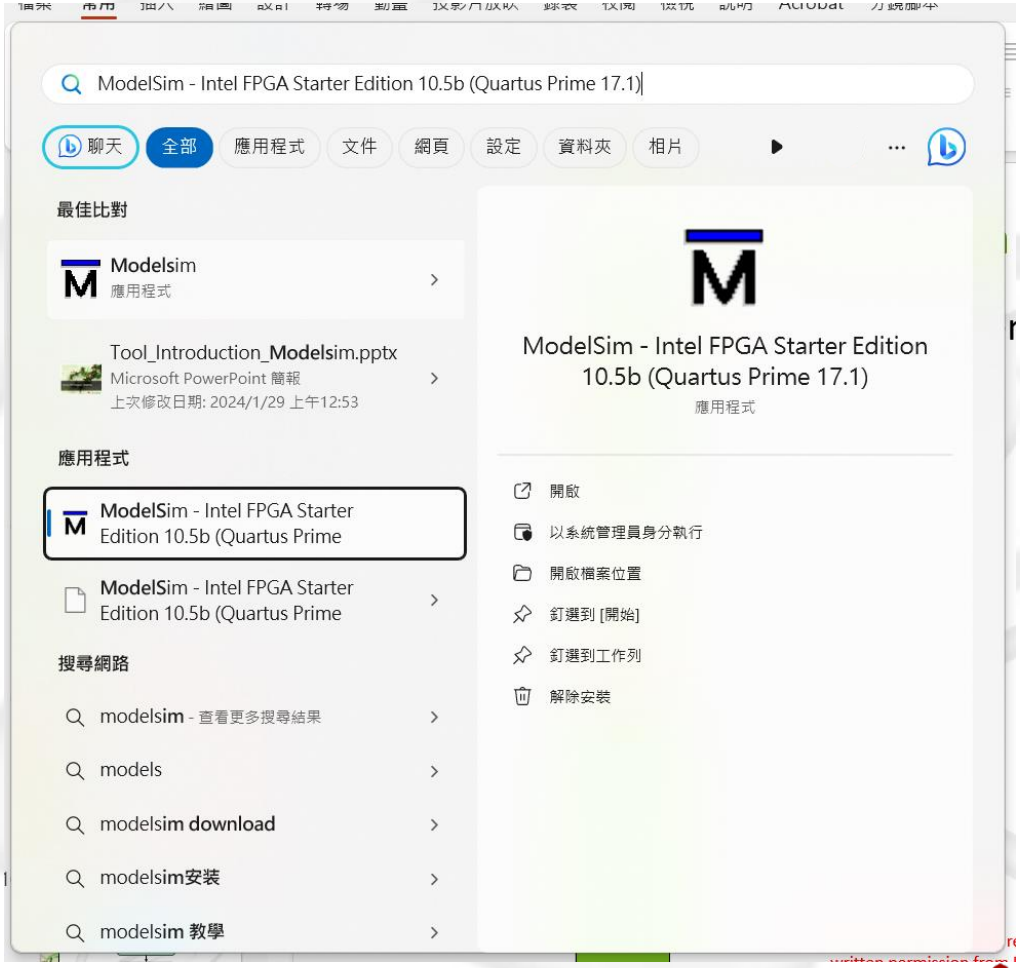
Tool Installation (6/7)

- Continue clicking “Next” until reach the end of installation.



Tool Installation (7/7)

- Search and open ModelSim.



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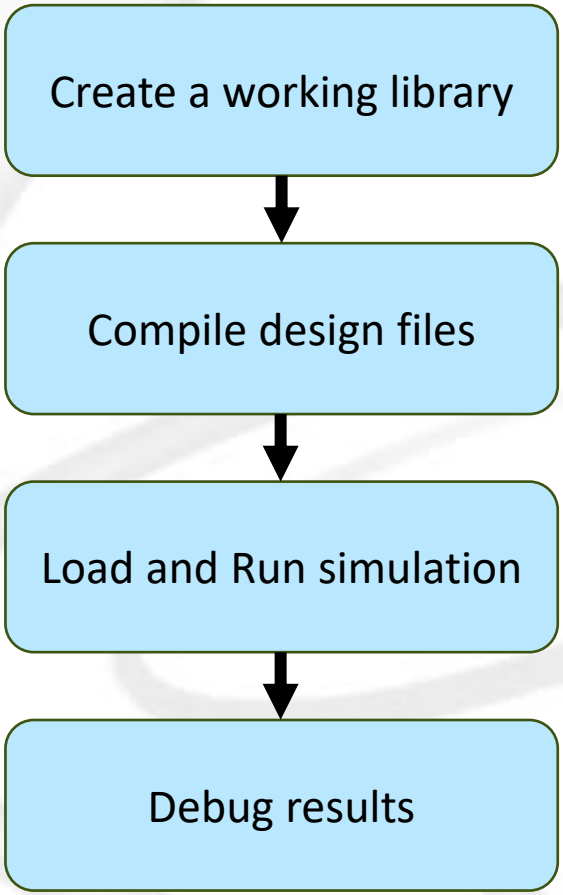
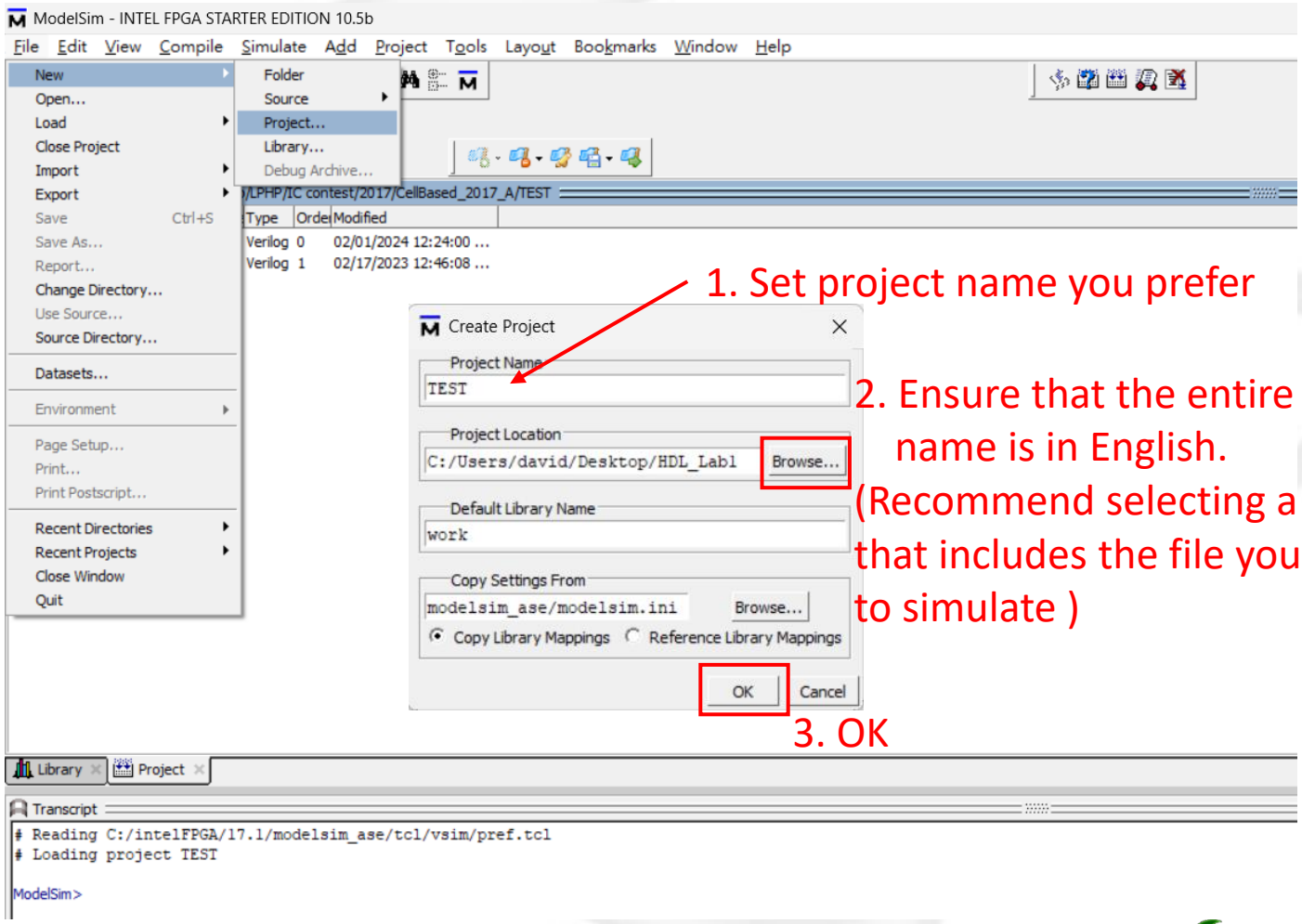
Basic Simulation Flow (1/8)

- Step for simulating a design in ModelSim.



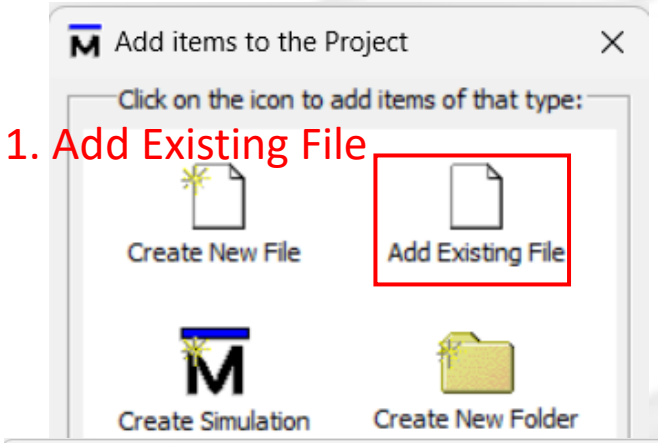
Basic Simulation Flow (2/8)

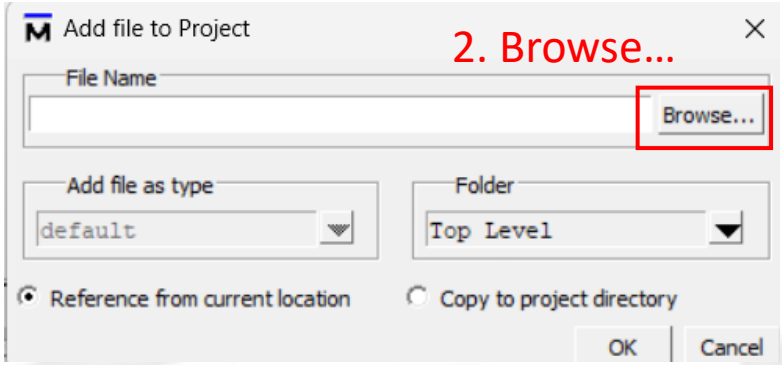
- Create New project: File > New > Project…

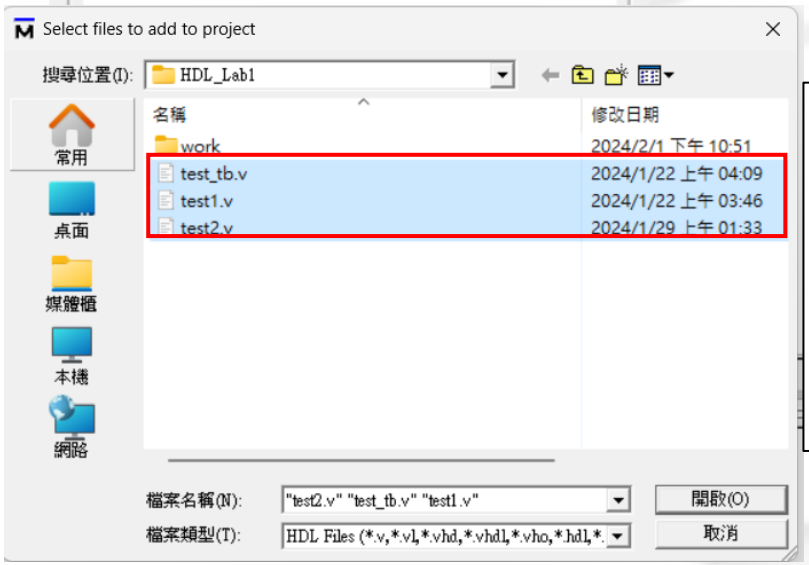


Basic Simulation Flow (3/8)

- Add items to the project.





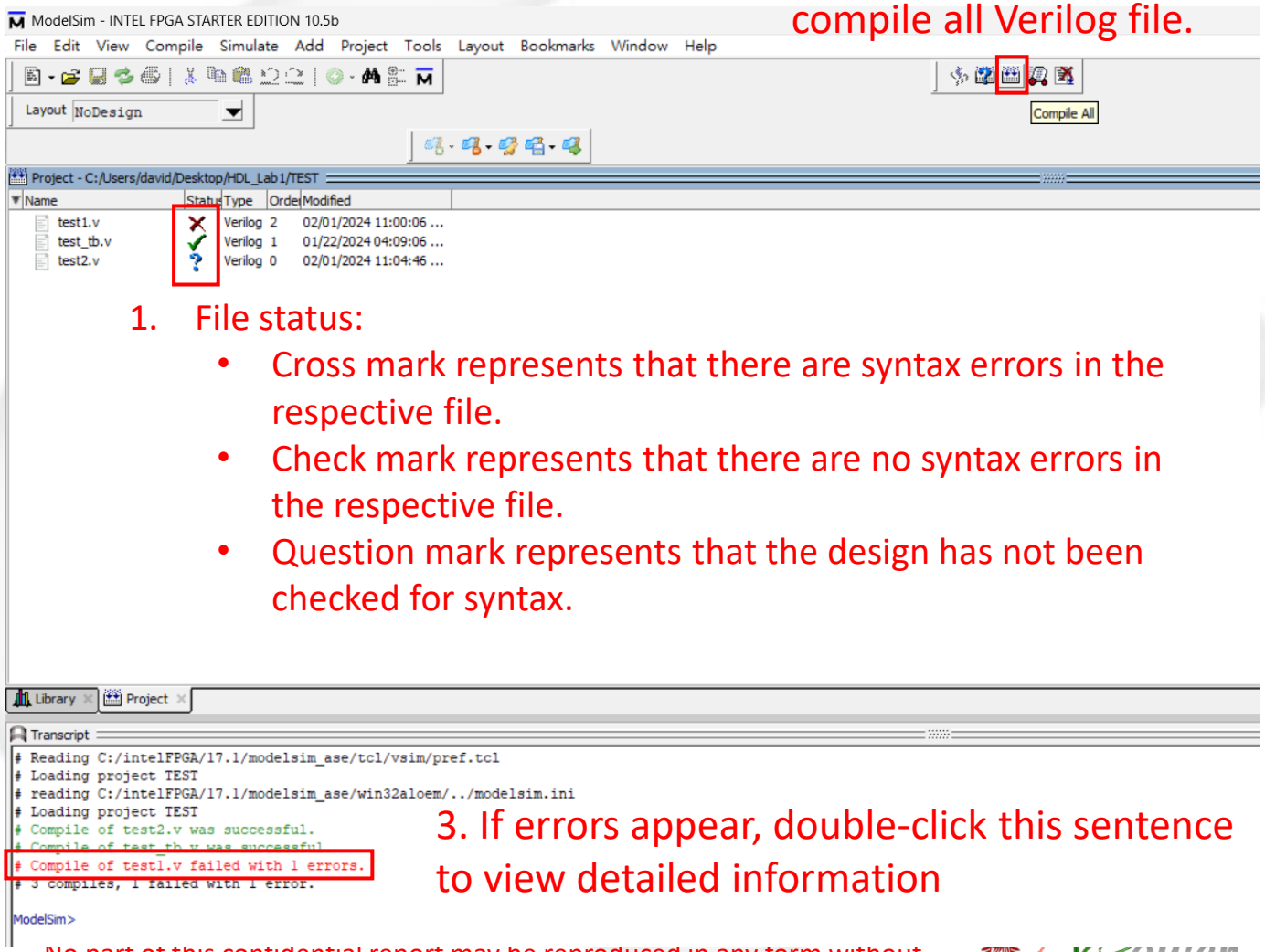


3. Choose the file you want to include in project.
(if your Design Under Verification (DUV) is already included in the testbench, there is no need to add it to the project again)

Basic Simulation Flow (4/8)

- Compile the Design

2. Click “Compile All” to compile all Verilog file.

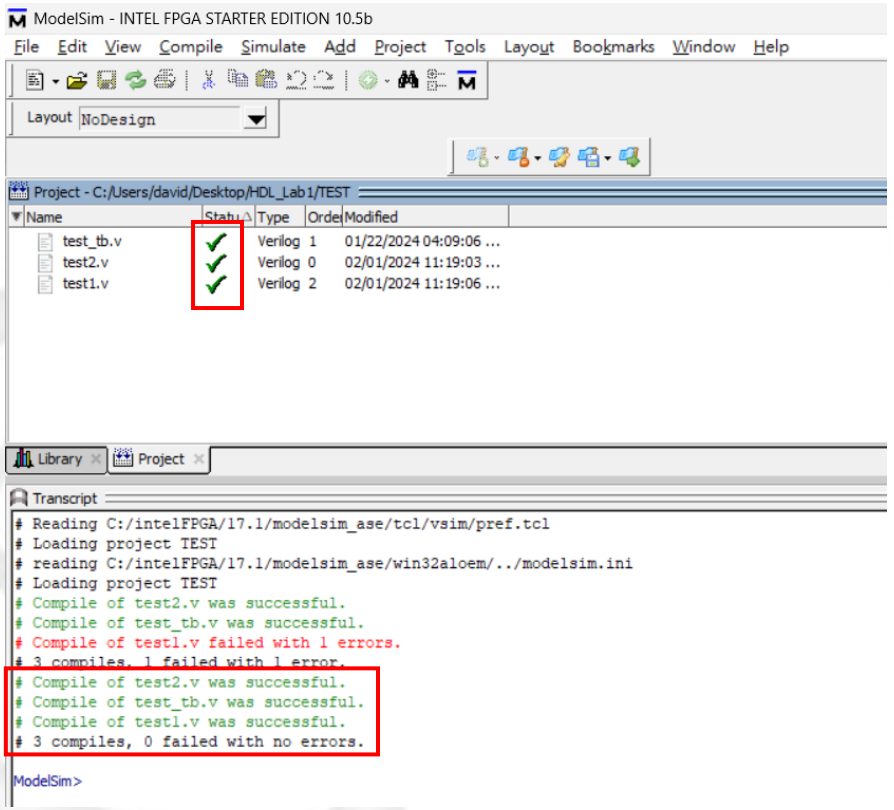


1. File status:
   - Cross mark represents that there are syntax errors in the respective file.
   - Check mark represents that there are no syntax errors in the respective file.
   - Question mark represents that the design has not been checked for syntax.

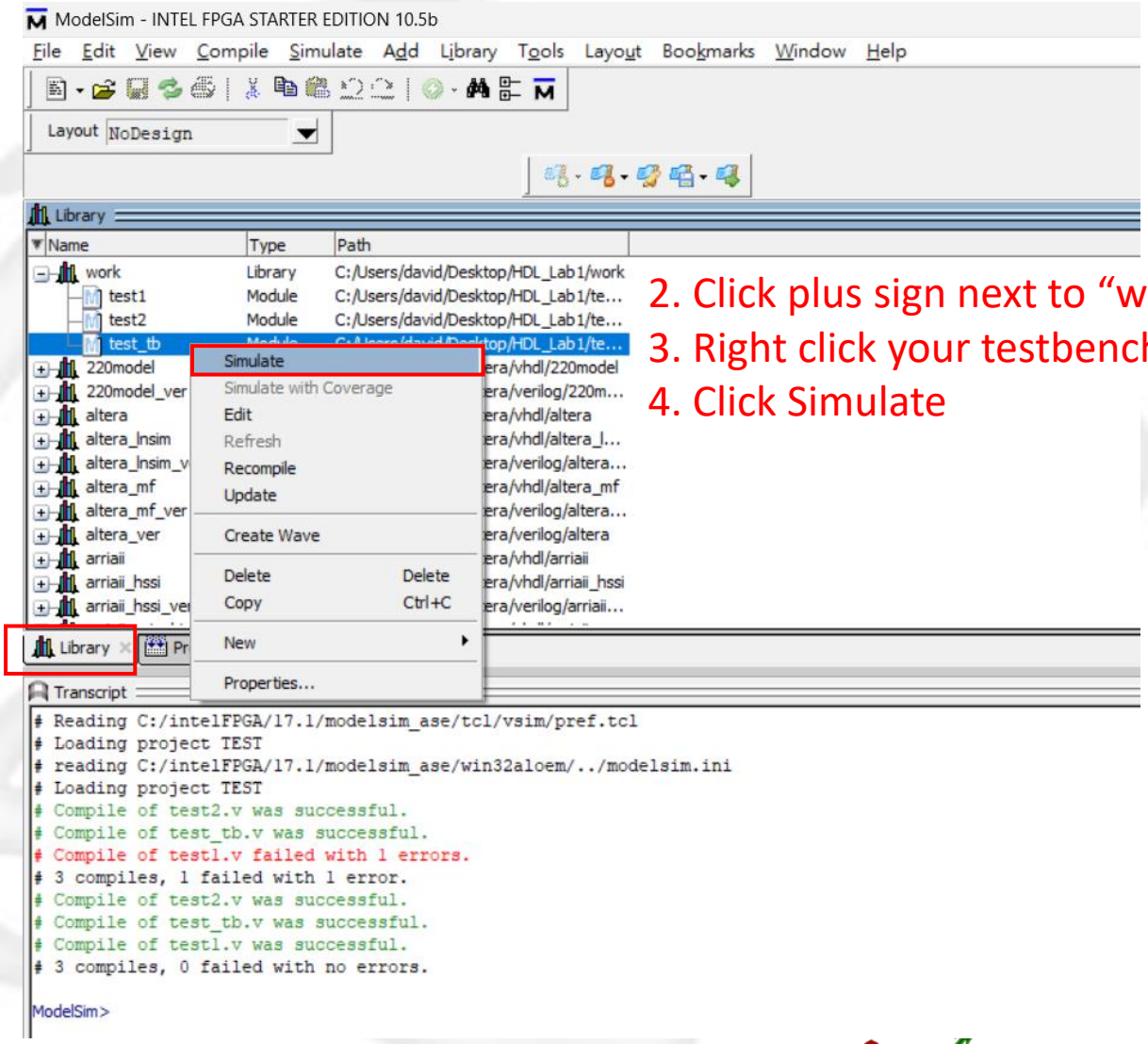
3. If errors appear, double-click this sentence to view detailed information

Basic Simulation Flow (5/8)

- You can directly revise the file using your preferred editor and recompile all files until all designs have no syntax errors.



Basic Simulation Flow (6/8)



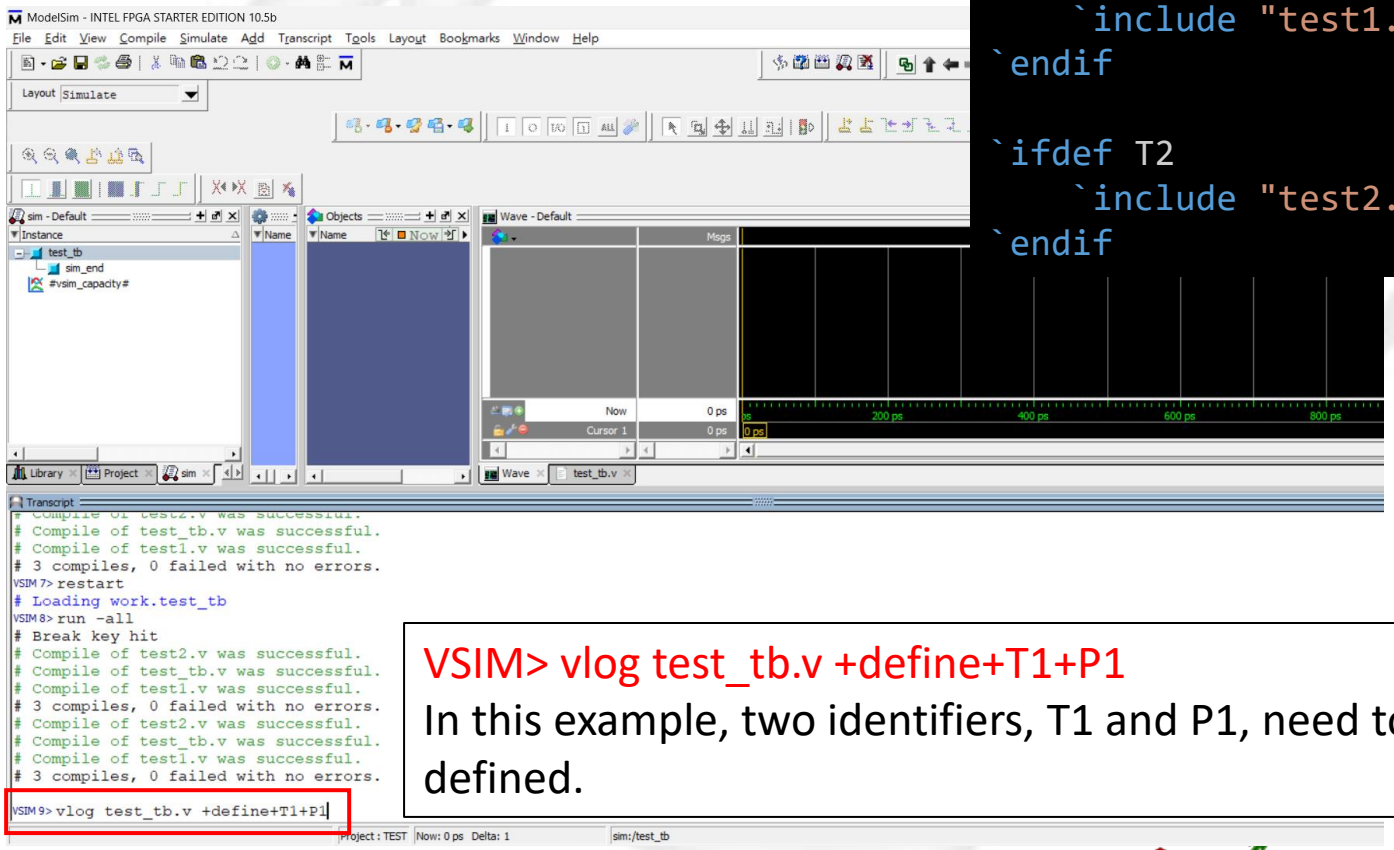
1. Click Library
2. Click plus sign next to “work”
3. Right click your testbench file
4. Click Simulate

Basic Simulation Flow (7/8) – option

- If there are some "`ifdef" identifier in your testbench, you need to define that before run the simulation.

```
`ifdef T1
    `include "test1.v"
`endif

`ifdef T2
    `include "test2.v"
`endif
```

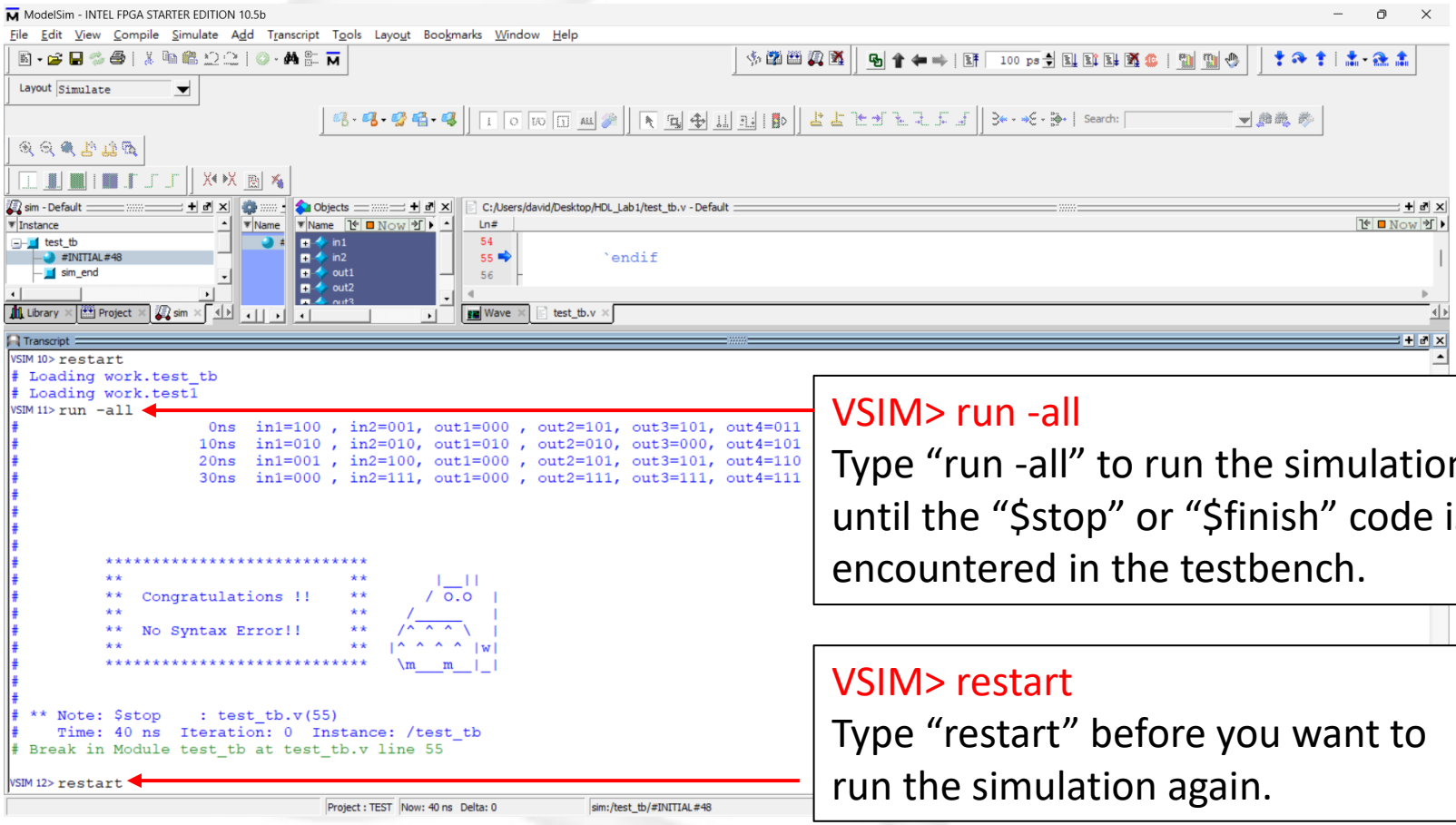


VSIM> vlog test_tb.v +define+T1+P1

In this example, two identifiers, T1 and P1, need to be defined.

Basic Simulation Flow (8/8)

- Run simulation



VSIM> run -all

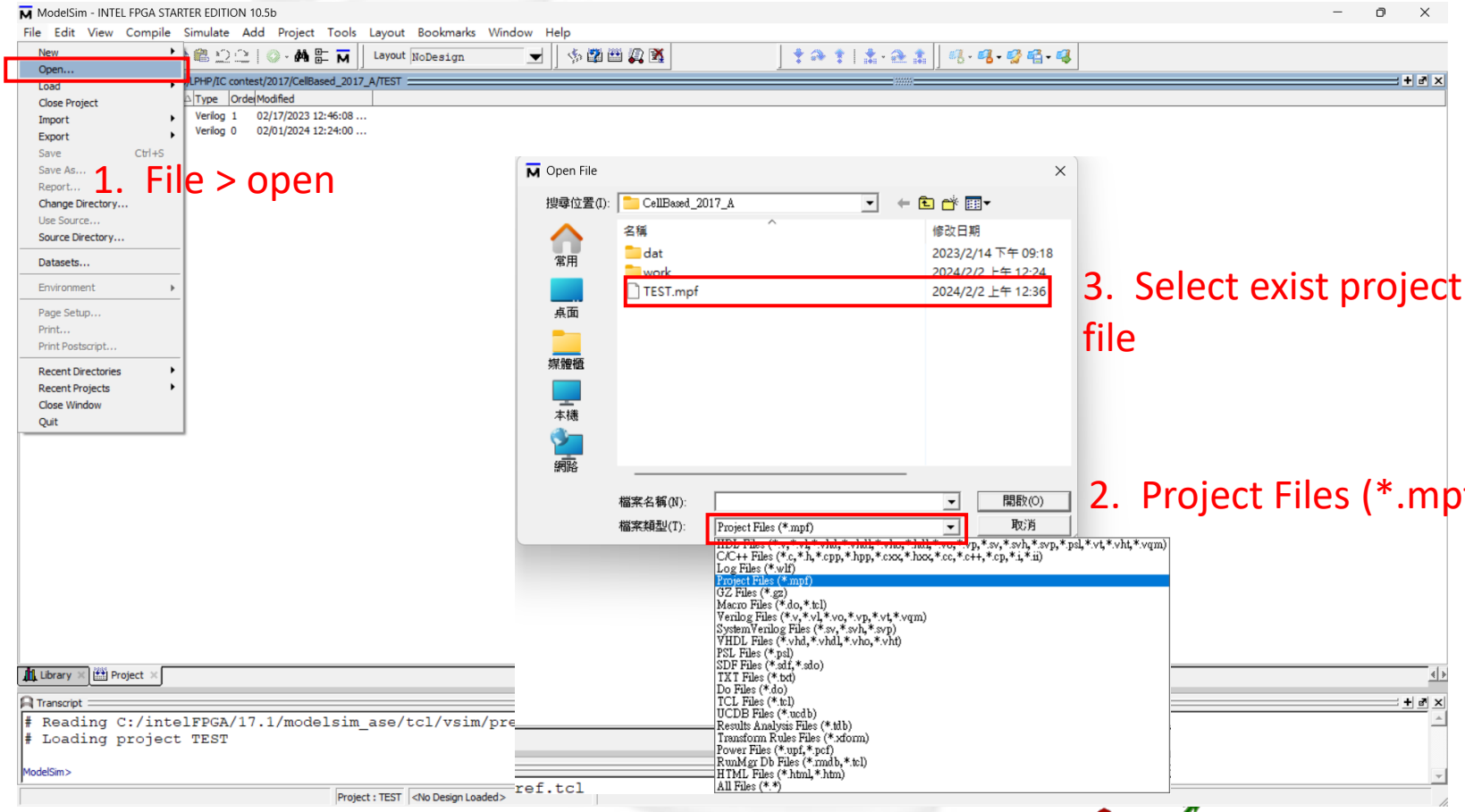
Type “run -all” to run the simulation until the “$stop” or “$finish” code is encountered in the testbench.

VSIM> restart

Type “restart” before you want to run the simulation again.

Appendix: Open Exist Project

- If accidentally close the ModelSim project, there's no need to recreate a new project.



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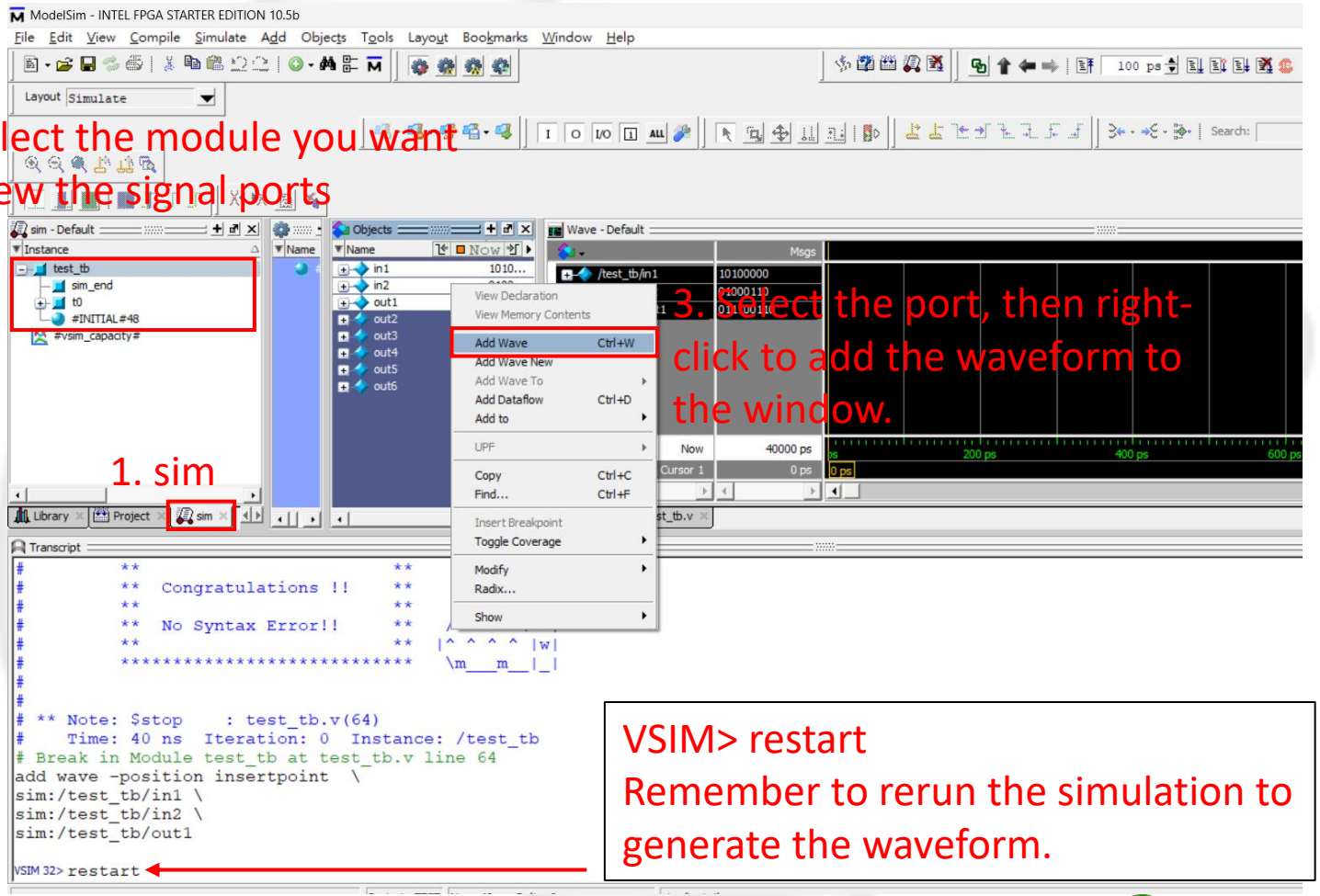
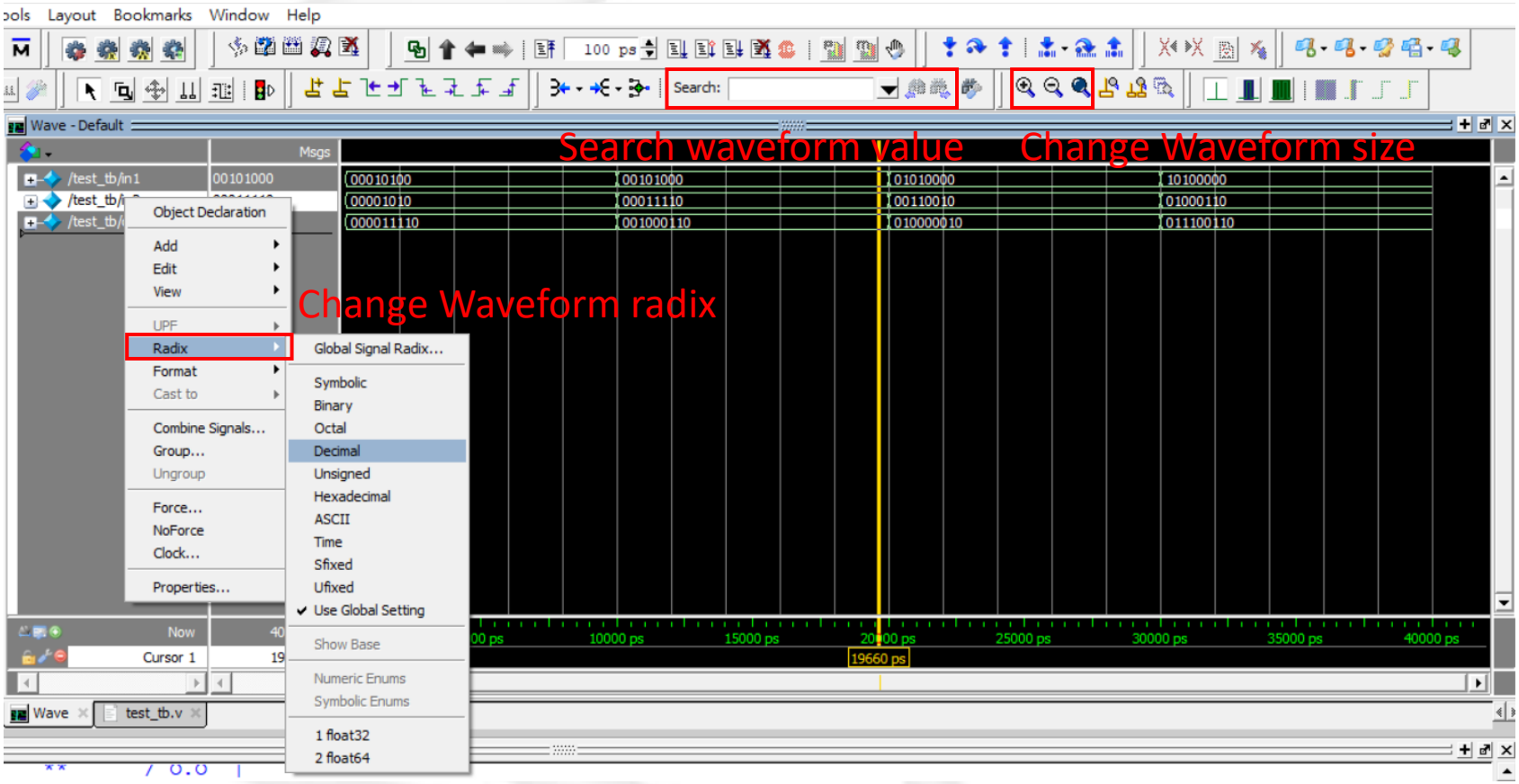
Debugging (1/3)

- Add waveforms for debugging.



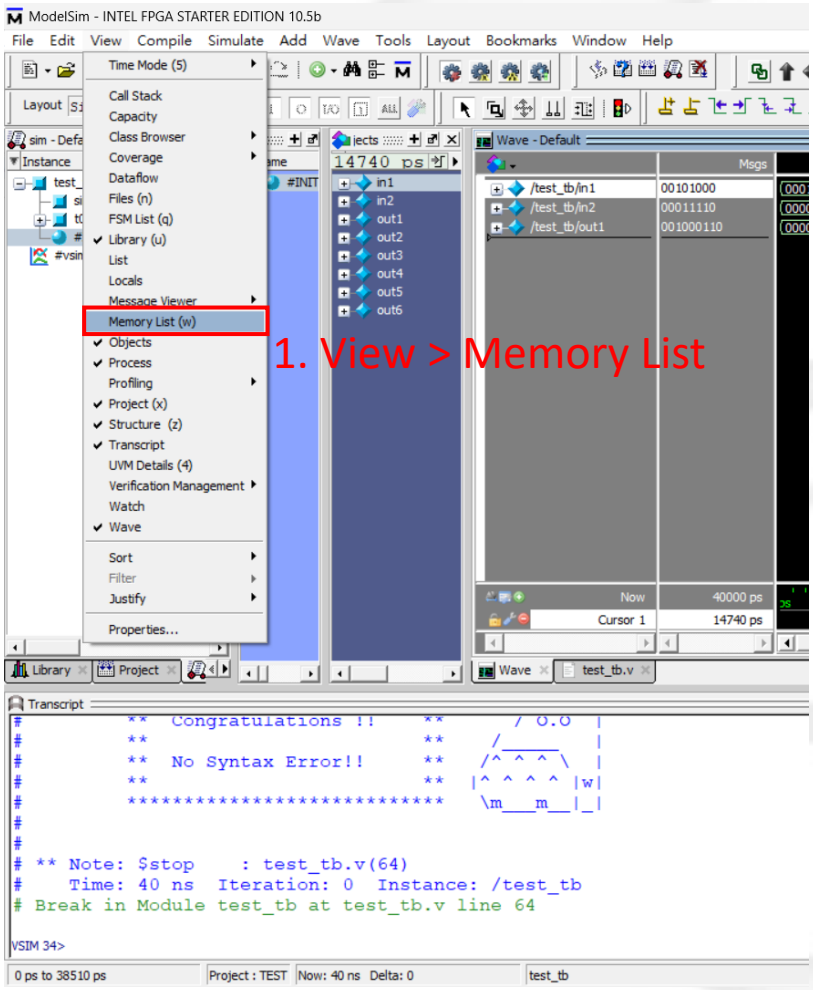
Debugging (2/3)

- Adjust the waveform as needed

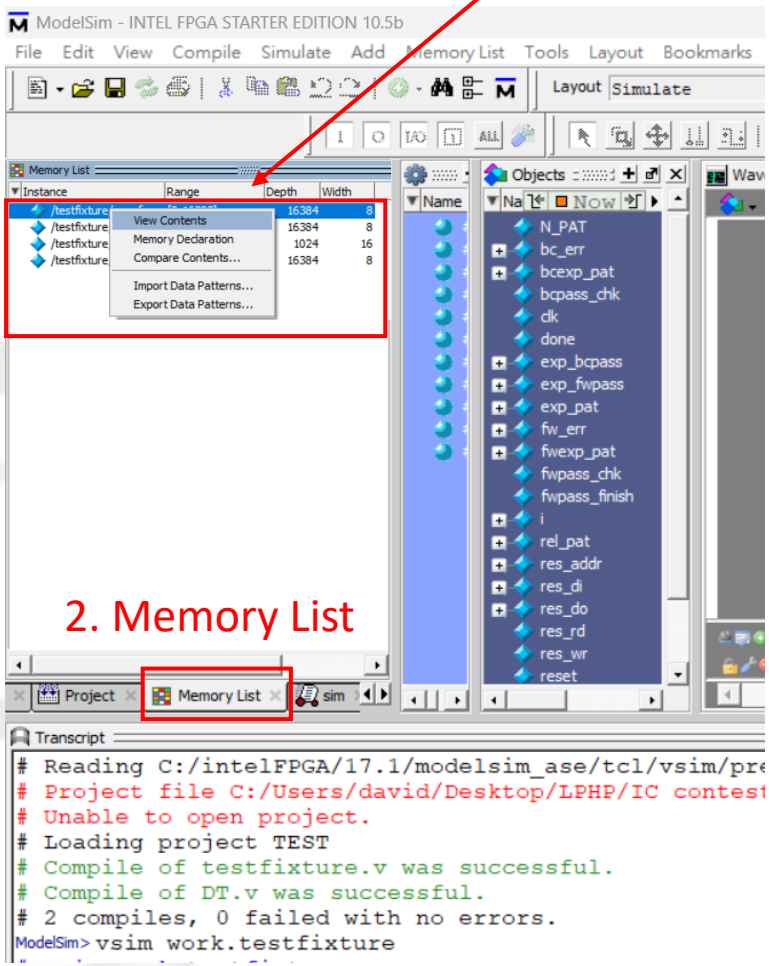


Debugging (3/3)

- Memory list



3. Choose the memory you want to visualize



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Thanks for your attention !!