

# Intel FPGA Software: Quartus Prime

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Date : 2024/04/18



# Outline

- Introduction to FPGA
- Tool Installation
- Quartus Basic GUI
  - ➔ Create Project
  - ➔ EDA tools Setting
  - ➔ Compilation & Synthesis
  - ➔ Waveform Simulation
  - ➔ Power, Performance and Area

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# Introduction to FPGA (1/2)

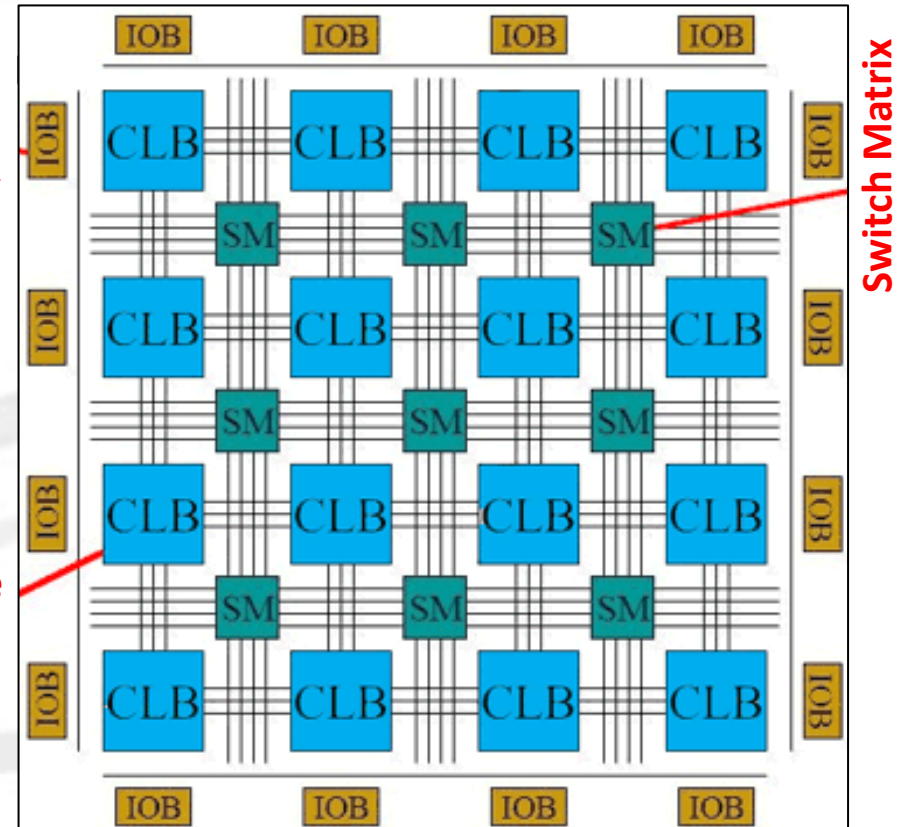
- ❑ The two most popular choices for FPGAs are Xilinx (AMD) and Altera (Intel).
- ❑ FPGA Device Family Comparison

Application	AMD-Xilinx Devices	Intel-Altera Devices
Highest performance	Versal* Prime Versal* Premium	Intel® Agilex™ F-Series Intel® Agilex™ I-Series
High performance	Virtex* UltraScale+* Kintex* UltraScale+* Xynq* UltraScale+*	Intel® Agilex™ F-Series Intel® Agilex™ I-Series  Intel® Stratix® 10 GX/SX/TX/MX/DX
Mid-range	Virtex* UltraScale* Kintex* UltraScale* Zynq* -7000	Intel® Stratix® 10 GX/SX/TX/MX/DX  Intel® Arria® 10 GX/SX
Low cost	Artix* -7	Intel® Cyclone® 10GX

# Introduction to FPGA (2/2)

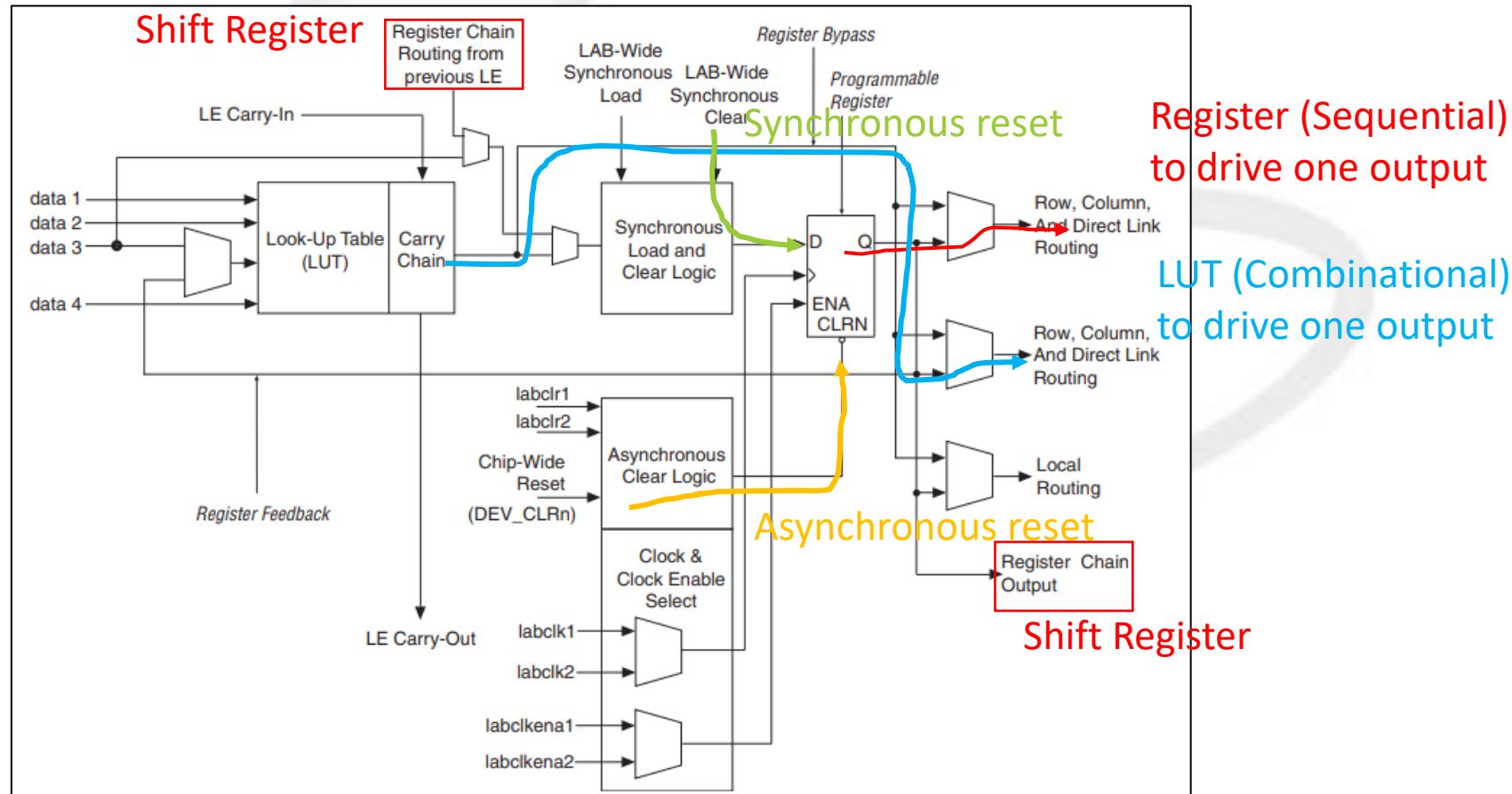
- Logic Blocks
  - ➔ General logic blocks
  - ➔ Programmable to perform different
- Reconfigurable Interconnect
  - ➔ Programmable routing channels
  - ➔ Connecting blocks and I/O
- I/O Blocks
  - ➔ Connecting the chip to the outside
- Dedicated Hardware
  - ➔ Memory (SRAM, BRAM, URAM)
  - ➔ DSP (Multiplier)
  - ➔ Special function unit

Most of the delay in the FPGA comes from the interconnect



# Logic Elements in the Cyclone IV

- LEs are compact and provide advanced features with efficient logic usage.

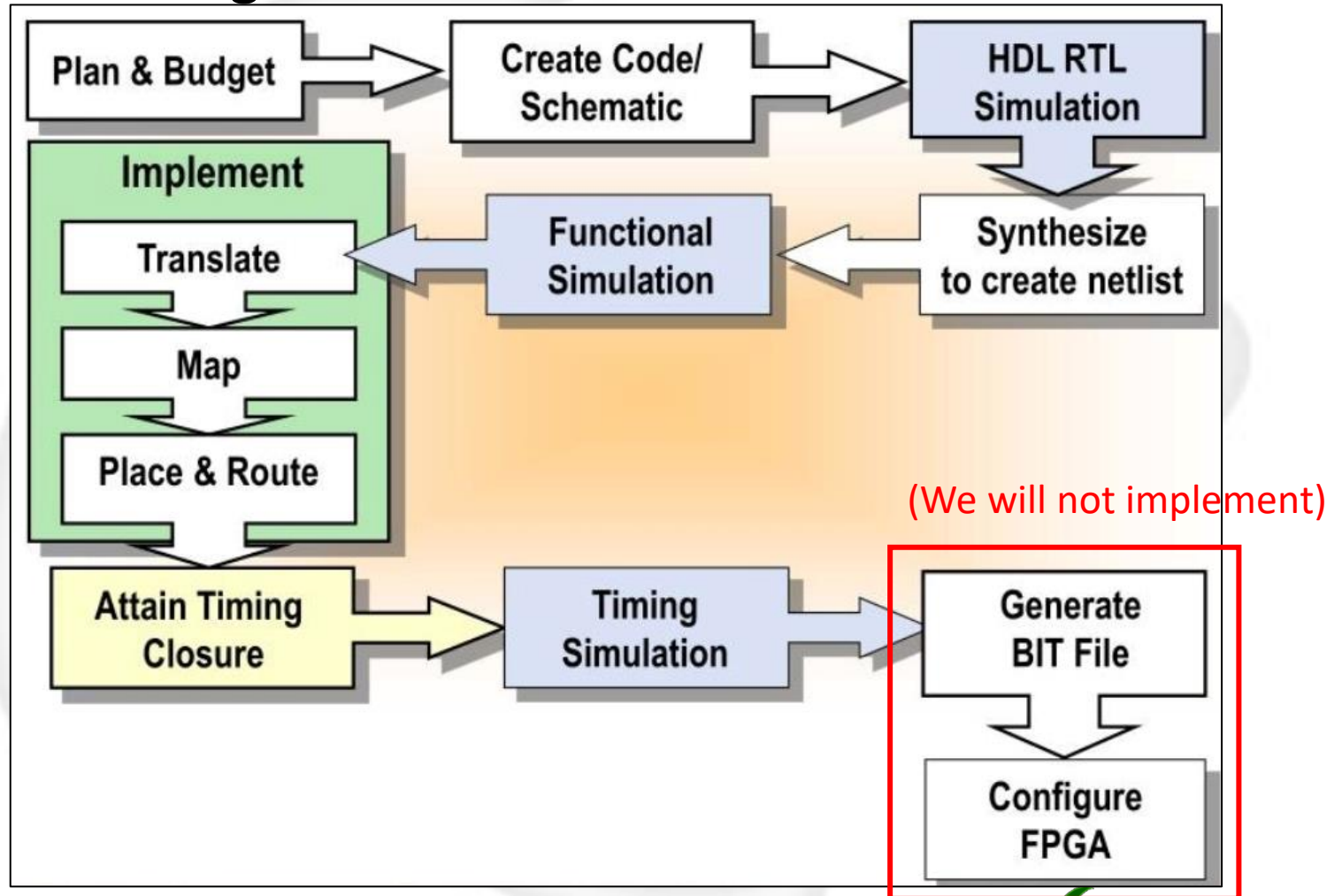


<https://cdrdv2-public.intel.com/653677/cyiv-51002.pdf>

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# Basic Flow Diagram

## □ FPGA design flow overview





# Basic Design Flow (1/2)

## □ Design Constraint

- ➔ Constraints are used to influence the FPGA synthesis and implementation.
- ➔ To specify the design performance requirements that must be made and guide the tools toward meeting those requirements.
- ➔ The primary constraint types are:
  - ◆ Synthesis
    - Influence the details of how the synthesis of HDL code to RTL occurs
  - ◆ I/O (Pin Assignment)
    - To assign a signal to a specific I/O (pin) or I/O bank
  - ◆ Timing
    - To specify the timing characteristics of the design.
    - May affect all internal timing interconnections or delays.
  - ◆ Area
    - To map specific circuit to a range of resources within the FPGA.



# Basic Design Flow (2/2)

## □ Synthesis

- ➔ After coding up your HDL code, you will need a tool to **check the syntax and generate a netlist.**

## □ Implementation

### ➔ Translate

- ◆ Merges multiple design files and design constraint information to produce a compatible design file (netlist).

### ➔ Map

- ◆ Fits the design within the available resources on the target.
  - Maps the schematic to physical logic units.
  - Compiles functions into basic LUT-based groups.

### ➔ Placement & Routing

- ◆ Place components onto the chip, connect the components, and extract timing data into reports

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# Tool Installation (1/9)

- ❑ Quartus Prime 17.1 Lite: [Download Link](#)
- ❑ Click Individual Files

Intel® Quartus® Prime Lite Edition Design Software Version 17.1 for Windows

ID	Date	Software Type	Software Package	Version	Operating Systems
669444	12/5/2017	FPGA Development Tools	Quartus® Prime Lite	17.1	Windows

A newer version of this software is available, which includes functional and security updates. Customers should [click here](#) to update to the latest version.

Users should upgrade to the latest version of the Intel® Quartus® Prime Design Software. The selected version does not include the latest functional and security updates. If you must use this version of software, follow the [technical recommendations](#) to help improve security. For critical support requests, please contact our [support team](#).

The Intel® Quartus® Prime Lite Edition Design Software, Version 17.1 is subject to removal from the web when support for all devices in this release are available in a newer version, or all devices supported by this version are obsolete. If you would like to receive customer notifications by e-mail, please subscribe to our [subscribe to our customer notification mailing list](#).

You may be exposed to a vulnerability issue if you have installed or plan to install Intel® Quartus® Prime Design Software from version 11.0 to version 18.0 to a location with space(s) in the path. See this [KDB solution](#) for more details.

[Critical Issues and Patches for the Intel® Quartus® Prime Lite Edition Software, Version 17.1.](#)

Knowledge Base: Search for Errata. Also see Critical Issues and Patches.

[Problems and Answers on specific IP or Products.](#)

## Downloads

Multiple Download **Individual Files** Additional Software Updates

### Multiple Download

Intel® Quartus® Prime Lite Edition Software (Device support included)

Download  
Quartus-lite-17.1.0.590-windows.tar

Size: 5.8 GB

SHA1: 2fc0d8fc702bbafe9ddb2473f3ae9220f452b5d

[What's Included?](#)

# Tool Installation (2/9)

- Download the executable files for two specific devices and one software program.

## Devices

### Intel® Arria® II Device Support

Download  
arria\_lite-17.1.0.590.qdz

Size: 499.6 MB  
SHA1: 4af6e589fd34ce986a8174d047b6ed524ca4f7d7

### Intel® Cyclone® IV Device Support

Download  
cyclone-17.1.0.590.qdz

Size: 466.6 MB  
SHA1: ad13e0f22371f850768a2d38abb123cf95f59e4

### Intel® Cyclone® 10 LP Device Support

Download  
cyclone10lp-17.1.0.590.qdz

Size: 266.1 MB  
SHA1: 8750e1597fdb3696cc58b273031df3d163f2d30e

### Intel® Cyclone® V Device Support

Download  
cyclonev-17.1.0.590.qdz

Size: 1.1 GB  
SHA1: 392eebbcc61e041be7abd1034de16323a414428e7

### Intel® MAX® II, Intel® MAX® V Device Support

Download  
max-17.1.0.590.qdz

Size: 11.4 MB  
SHA1: 5d8cc8fc84204a3c0ac81ce475628d38e3940b19

### Intel® MAX® 10 Device Support

Download  
max10-17.1.0.590.qdz

Size: 325.2 MB  
SHA1: fdf2e0306b5adc6d8e2e2acf65962ae1d8b36d32

Device

## Intel® Quartus® Software

### ModelSim-Intel® FPGA Edition (includes Starter Edition)

Download  
ModelSimSetup-17.1.0.590-windows.exe

Size: 1.1 GB  
SHA1: f0b4520cd766bfff4373465e1dc7b819d1176f1

### Intel® Quartus® Prime (includes Nios® II EDS)

Download  
QuartusLiteSetup-17.1.0.590-windows.exe

Size: 1.7 GB  
SHA1: e6185f220de33432f352cfcb3088be7ee0971af8

Software



## Tool Installation (3/9)

- Three files have been downloaded, click executable file to installation.

名稱	修改日期	類型	大小
今天			
 QuartusLiteSetup-17.1.0.590-windows.exe	2024/4/4 下午 06:38	應用程式	1,820,218...
 cyclone10lp-17.1.0.590.qdz	2024/4/4 下午 06:51	QDZ 檔案	272,452 KB
 cyclone-17.1.0.590.qdz	2024/4/4 下午 06:53	QDZ 檔案	477,849 KB

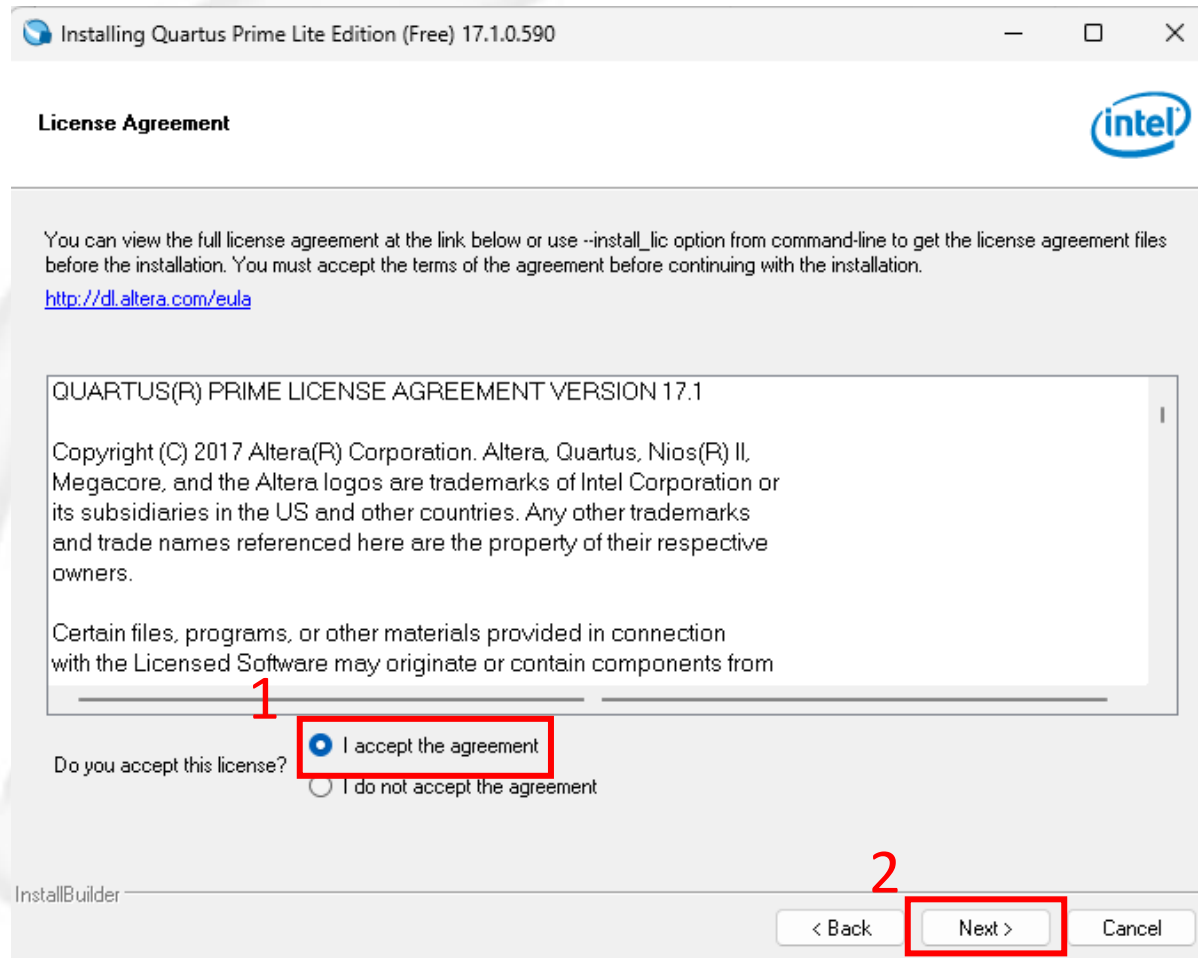
# Tool Installation (4/9)

□ Click Next



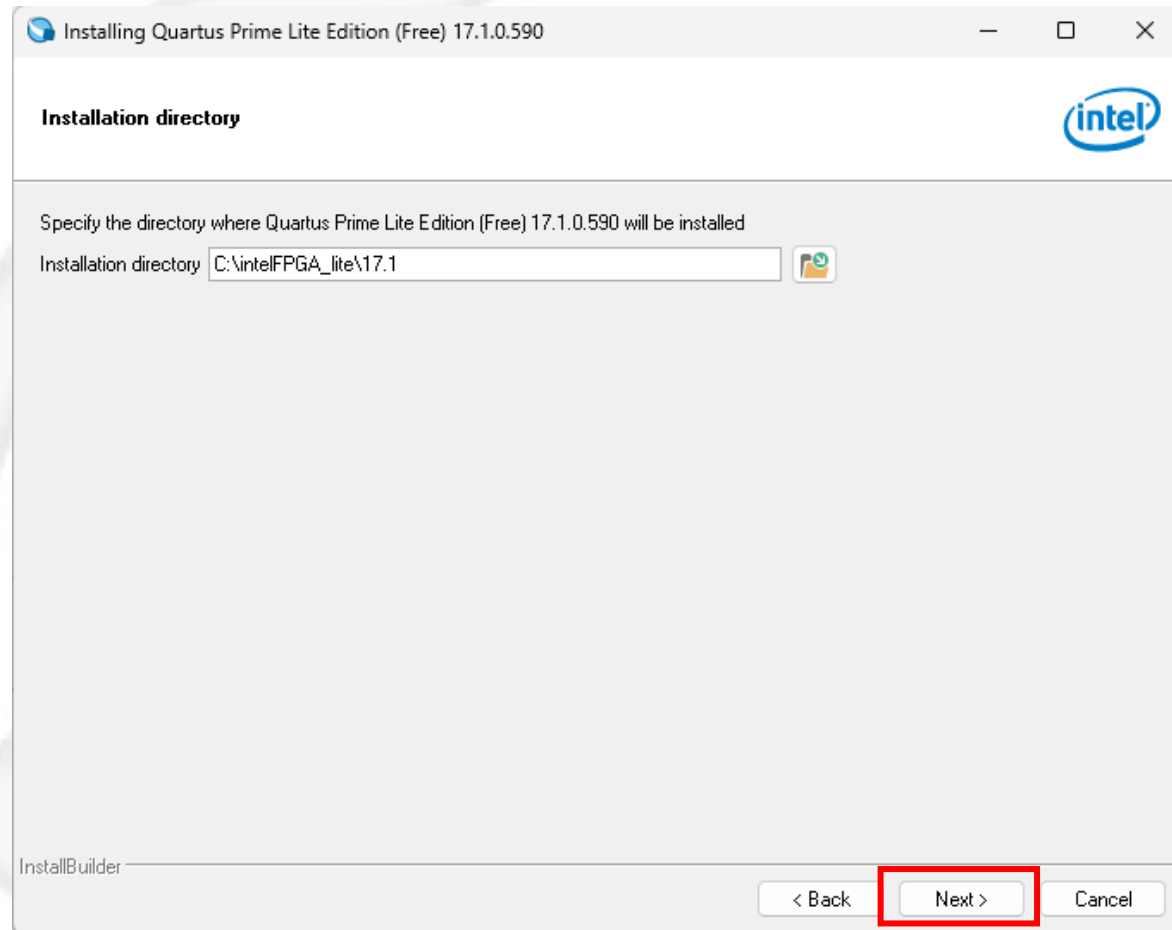
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# Tool Installation (5/9)



# Tool Installation (6/9)

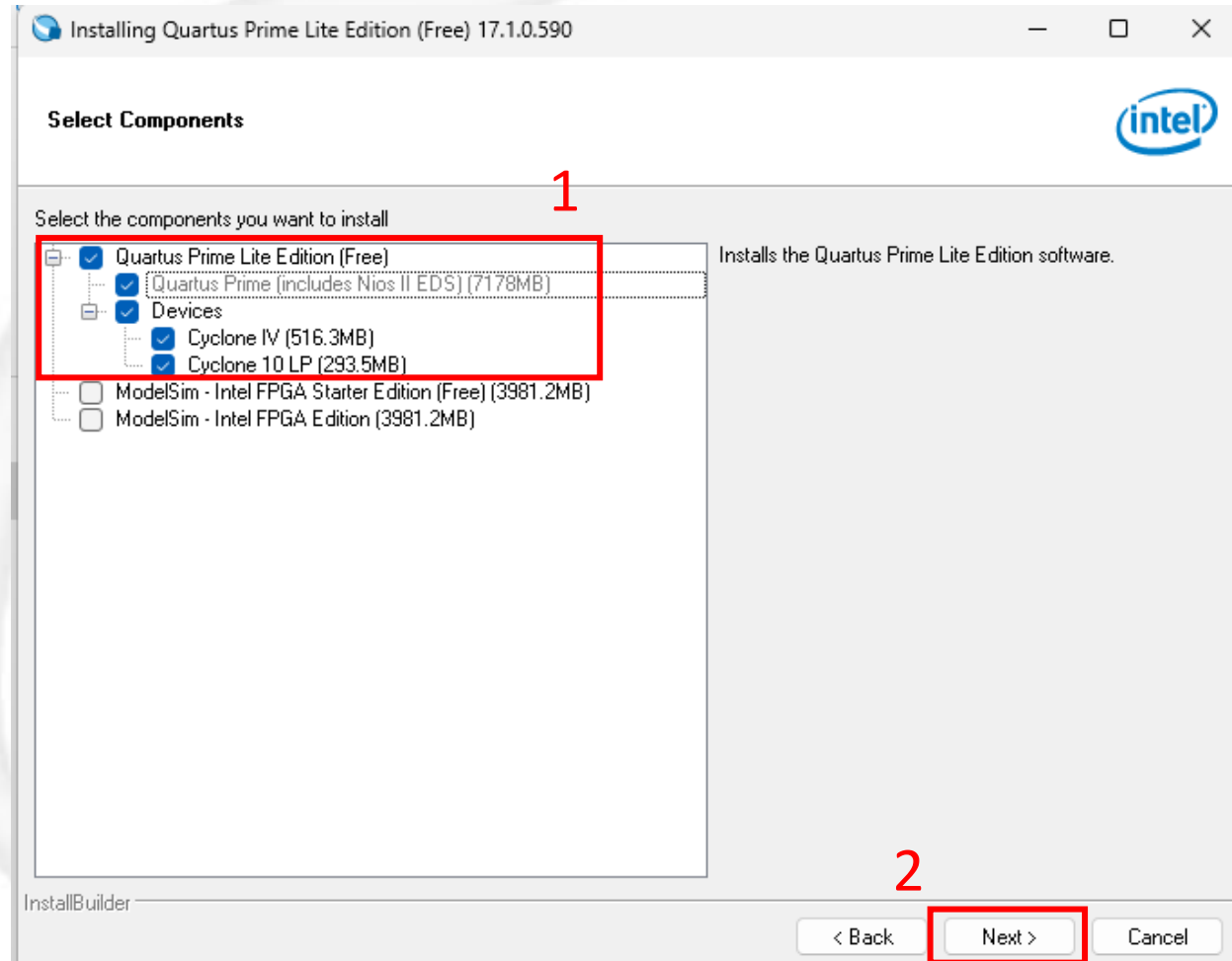
□ Click Next





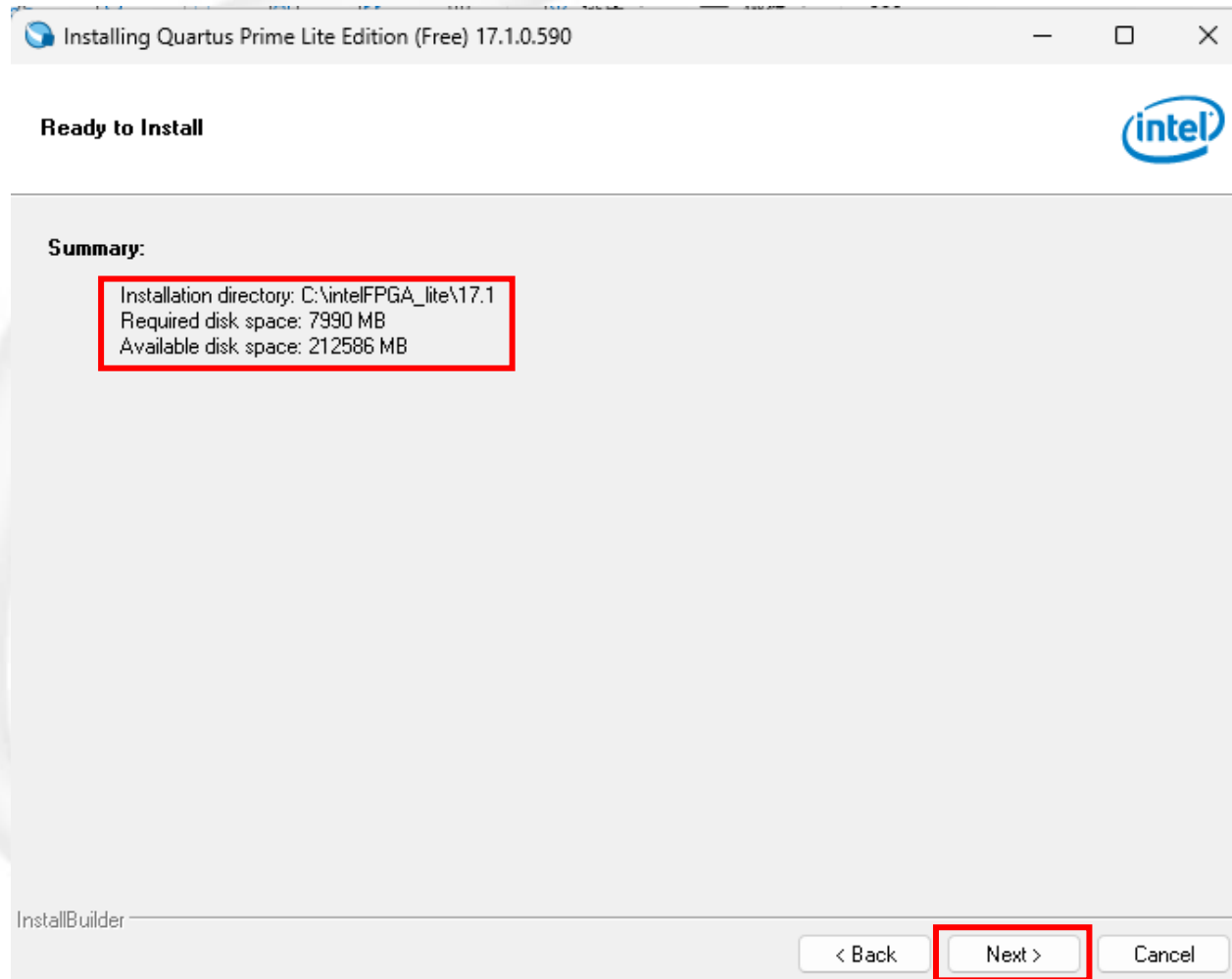
# Tool Installation (7/9)

- ❑ Select the Devices we had download before.



## Tool Installation (8/9)

- Ensure your pc has enough space for installation.



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## Tool Installation (9/9)

- Wait for installation and click finish at the end.



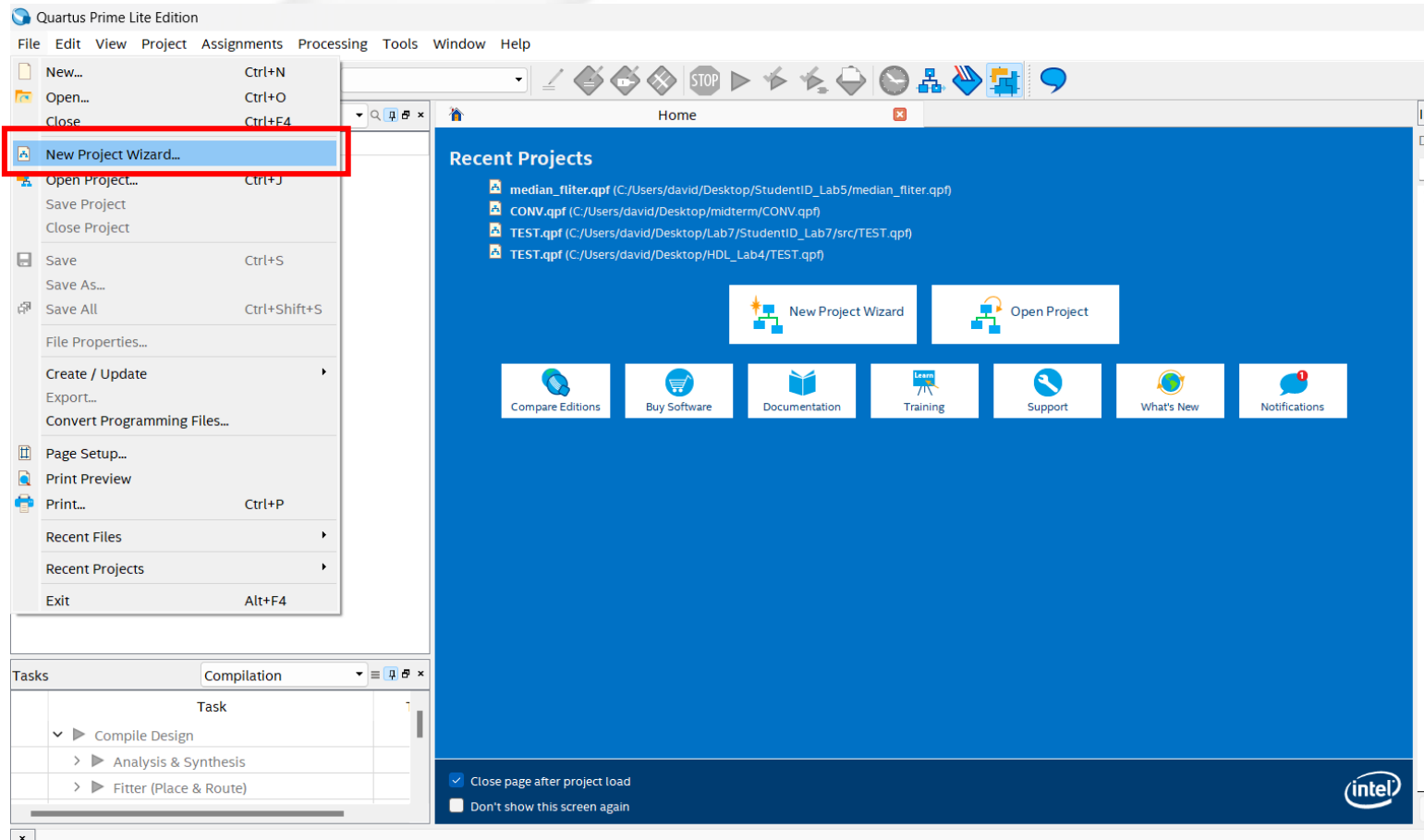
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# Create new Project (1/7)

□ File > New Project Wizard...



# Create new Project (2/7)

**New Project Wizard**

**Directory, Name, Top-Level Entity**

What is the working directory for this project? **1. Specify the working directory for the project. All file paths must be in English.**

C:/Users/david/Desktop/StudentID\_Lab5

What is the name of this project?

median\_fliter

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

median\_fliter

Use Existing Project Settings...

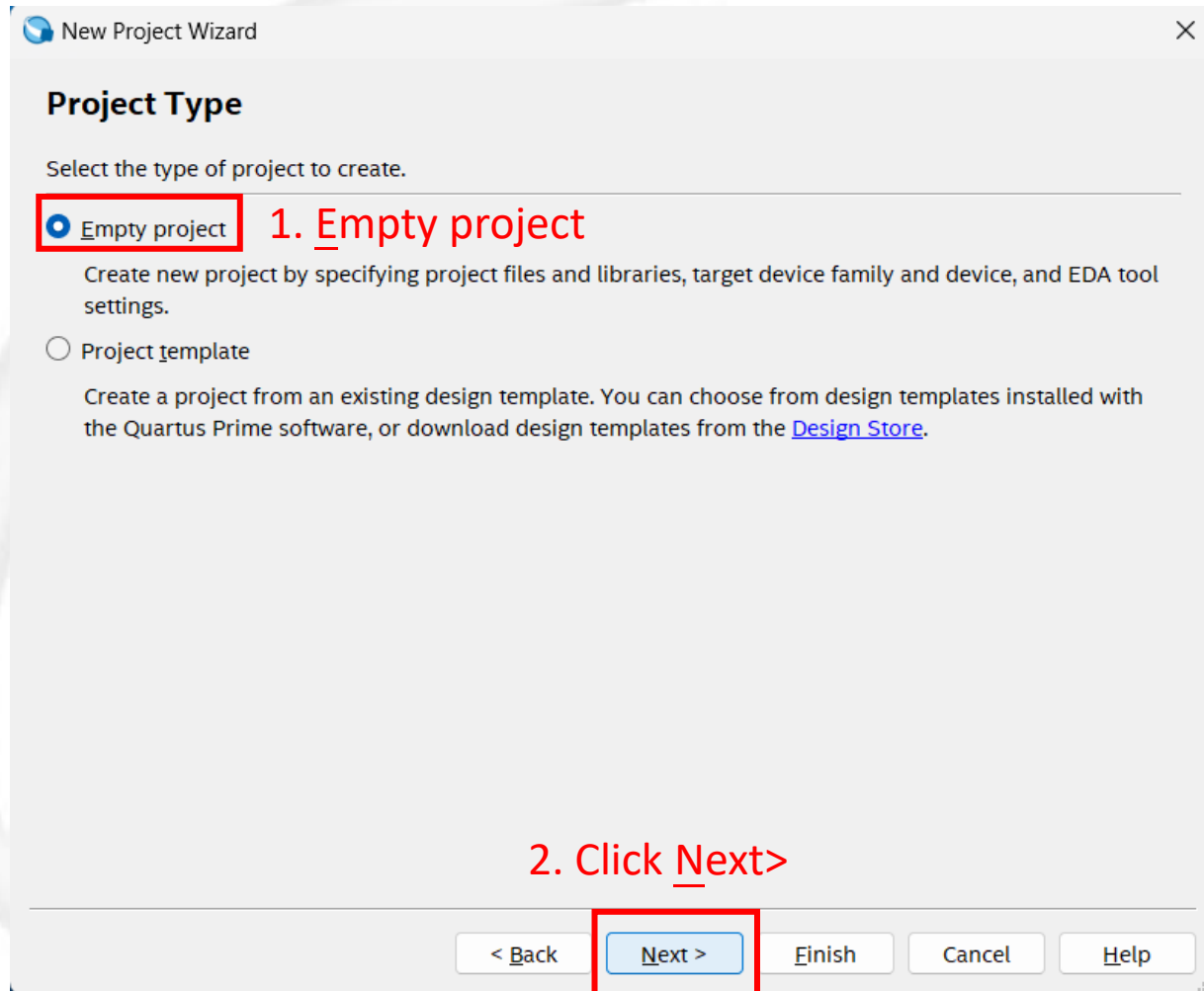
**2. Assign a project name that matches the top module name.**

**3. Click Next>**

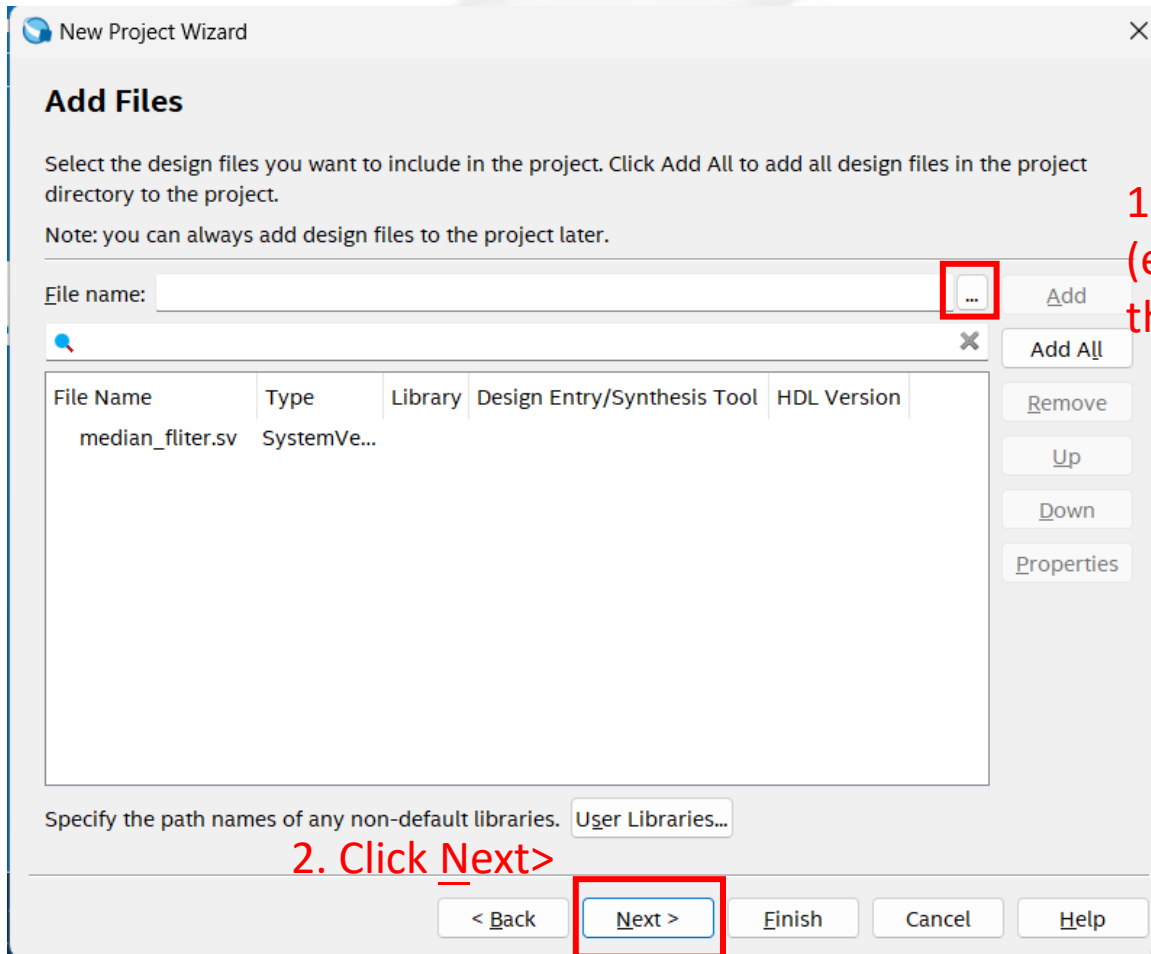
< Back Next > Finish Cancel Help

```
median_fliter.sv x
C: > Users > david > Desktop > StudentID_Lab5
1 module median_fliter
2 // input port
3 clk,
4 rst,
5 enable,
6 RAM_IMG_Q,
7 RAM_OUT_Q,
```

# Create new Project (3/7)



# Create new Project (4/7)



1. Select existing design files (excluding testbenches) from the browse dialog.

2. Click Next>



# Create new Project (5/7)

1. Choosing Cyclone IV E

New Project Wizard

### Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family  
Family: Cyclone IV E

Device: All

Target device  
☐ Auto device selected by the Fitter  
☒ Specific device selected in 'Available devices' list  
☐ Other: n/a

Show in 'Available devices' list  
 Package: Any  
 Pin count: Any  
 Core speed grade: Any  
 Name filter:  
☒ Show advanced devices

Available devices:

Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multiplier 9-bit
EP4CE115F23C9L	1.0V	114480	281	281	3981312	532
EP4CE115F23I7	1.2V	114480	281	281	3981312	532
EP4CE115F23I8L	1.0V	114480	281	281	3981312	532
EP4CE115F29C7	1.2V	114480	529	529	3981312	532
EP4CE115F29C8	1.2V	114480	529	529	3981312	532
EP4CE115F29C8L	1.0V	114480	529	529	3981312	532
EP4CE115F29C9L	1.0V	114480	529	529	3981312	532
EP4CE115F29I7	1.2V	114480	529	529	3981312	532
EP4CE115F29I8L	1.0V	114480	529	529	3981312	532

3. Click Next>

< Back Next > Finish Cancel Help

2. EP4CE115F29C7

# Create new Project (6/7)

- Specify the Simulation EDA tools.

New Project Wizard

## EDA Tool Settings

Specify the other EDA tools used with the Quartus Prime software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	SystemVerilog HDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

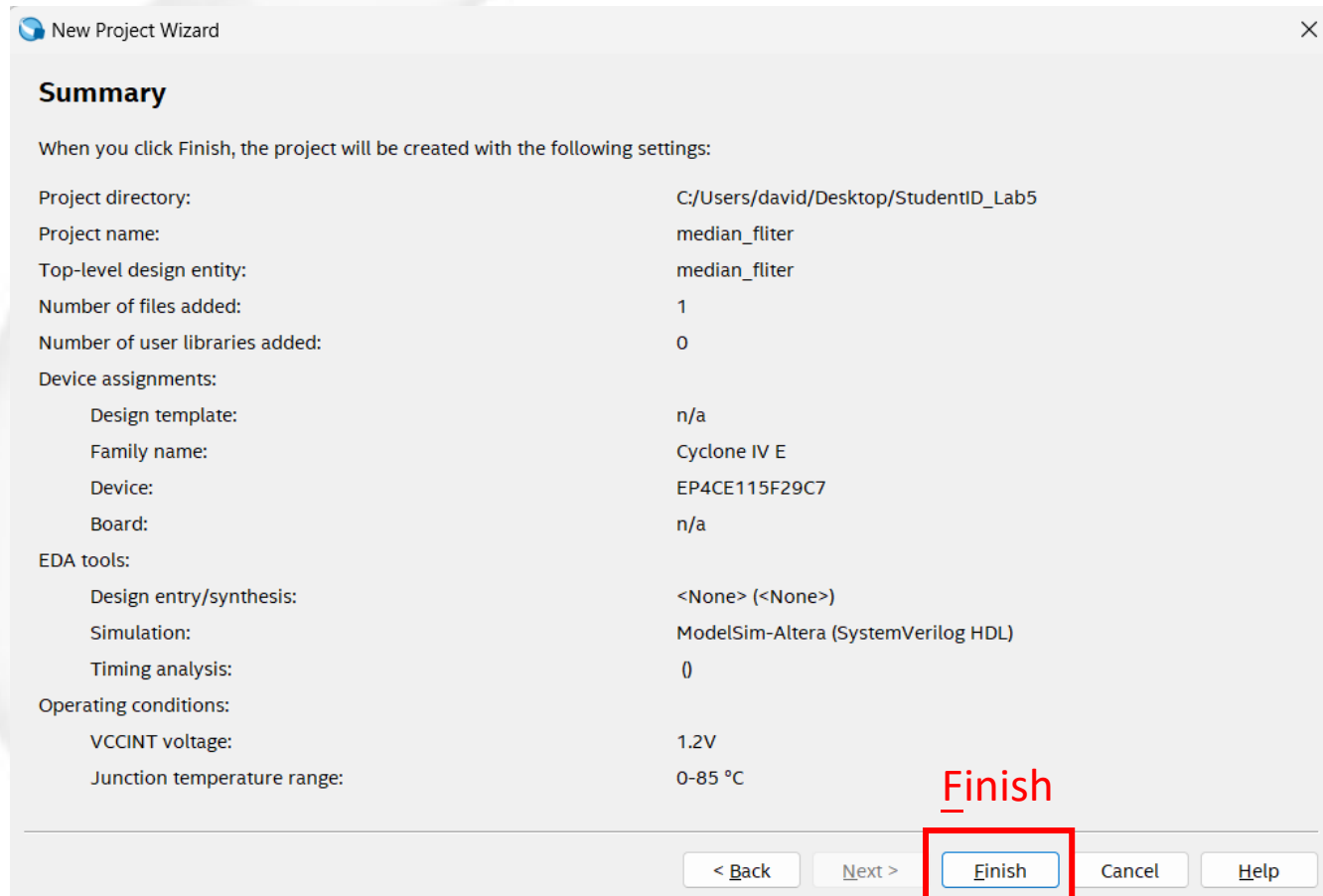
1. Tool Name: ModelSim-Altera  
Format(s): SystemVerilog HDL

2. Click Next>

< Back Next > Finish Cancel Help

# Create new Project (7/7)

- Ensure the project summary remains consistent with the previous setting.



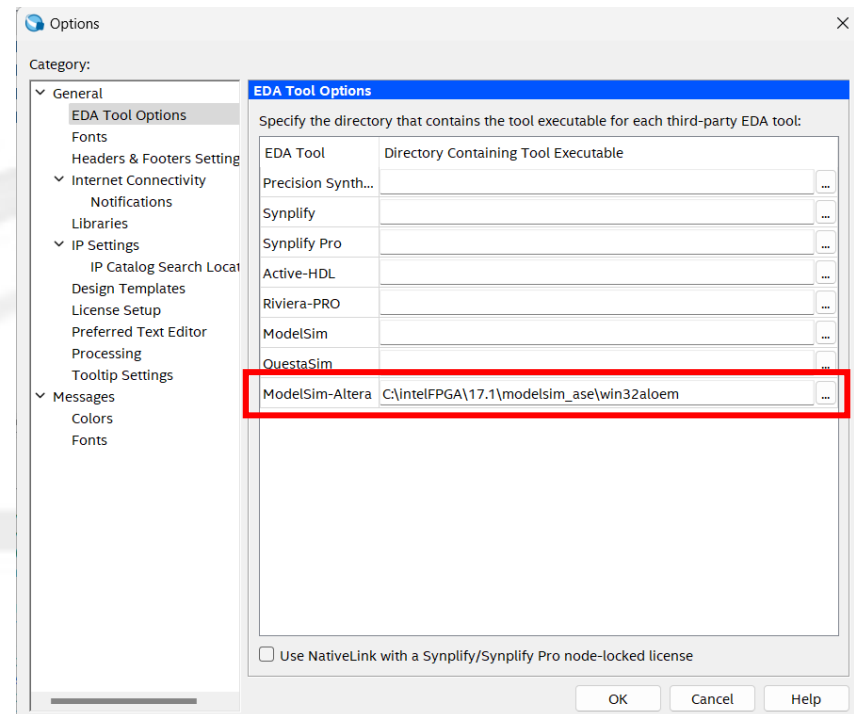
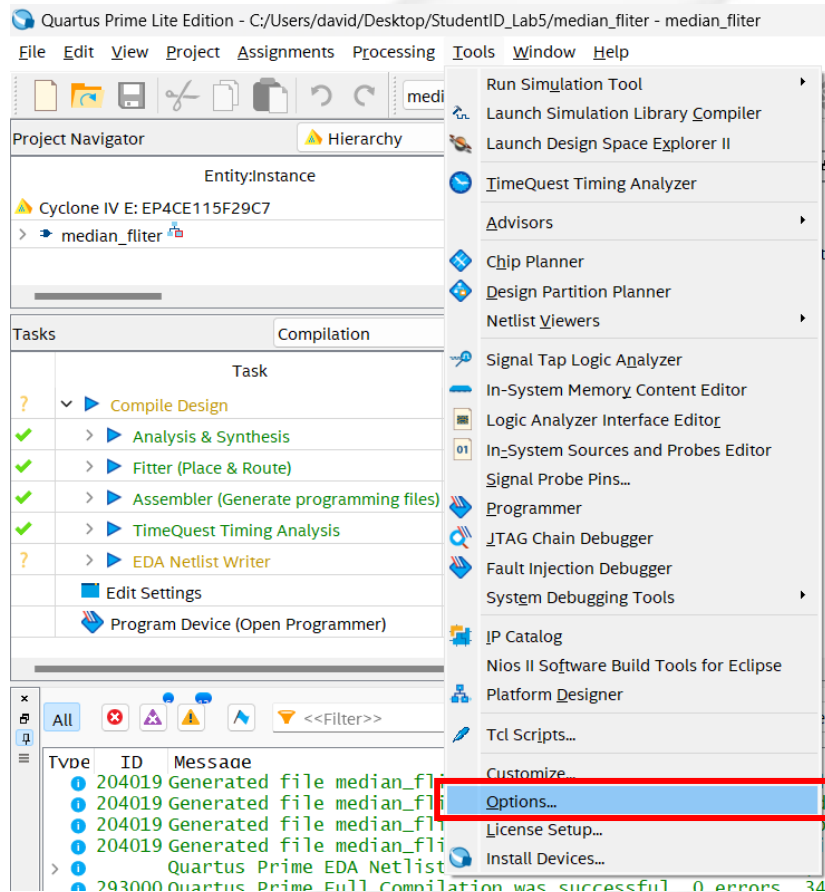
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# Setting Options for EDA Tools (1/4)

## Tool > Options...

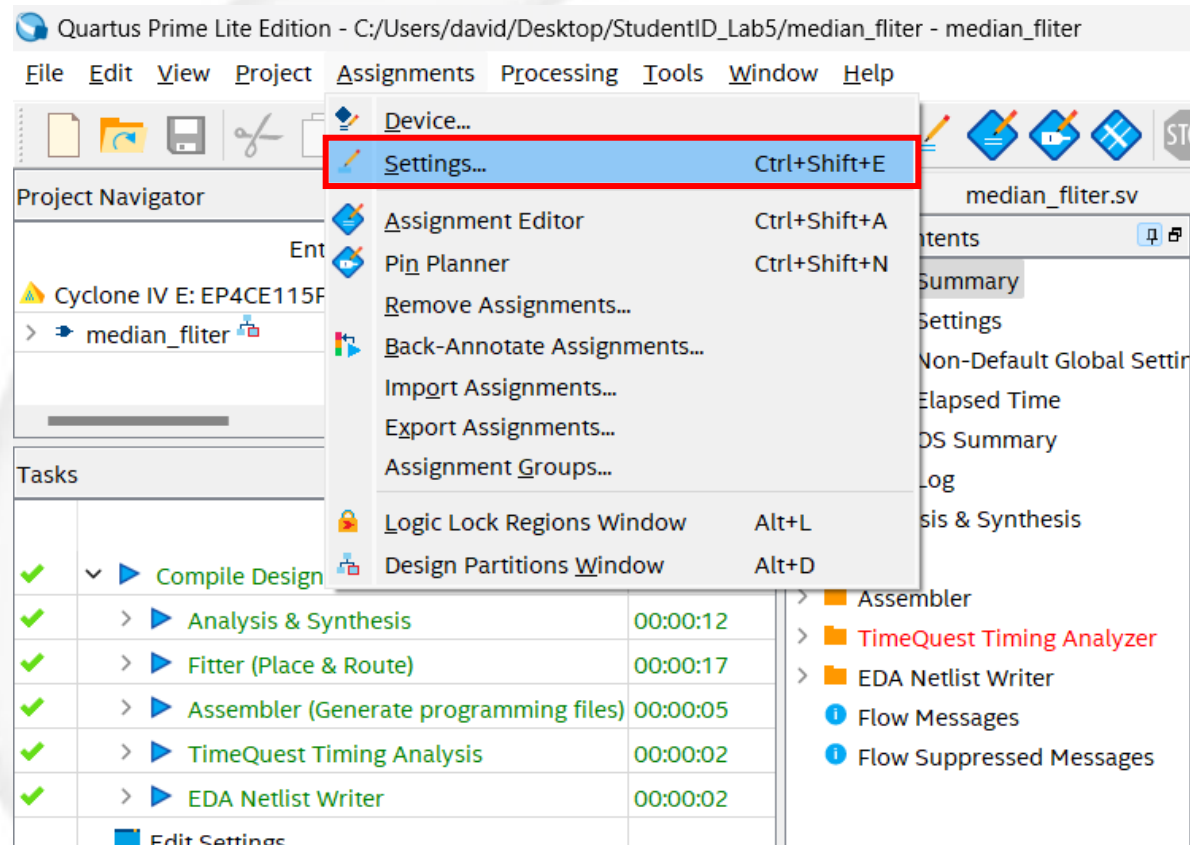
Following our ModelSim installation tutorial typically installs the executable in this default location. However, there may be variations depending on your specific setup.





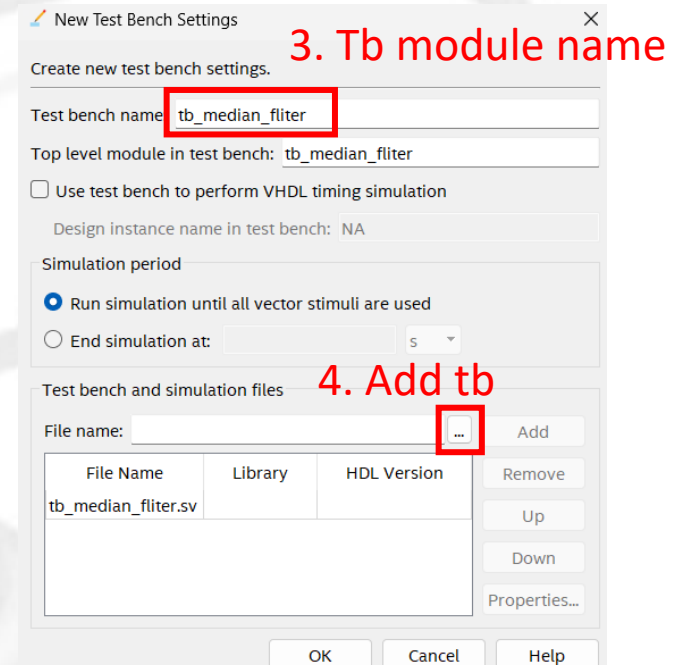
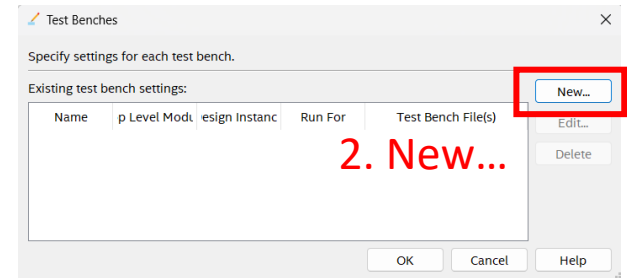
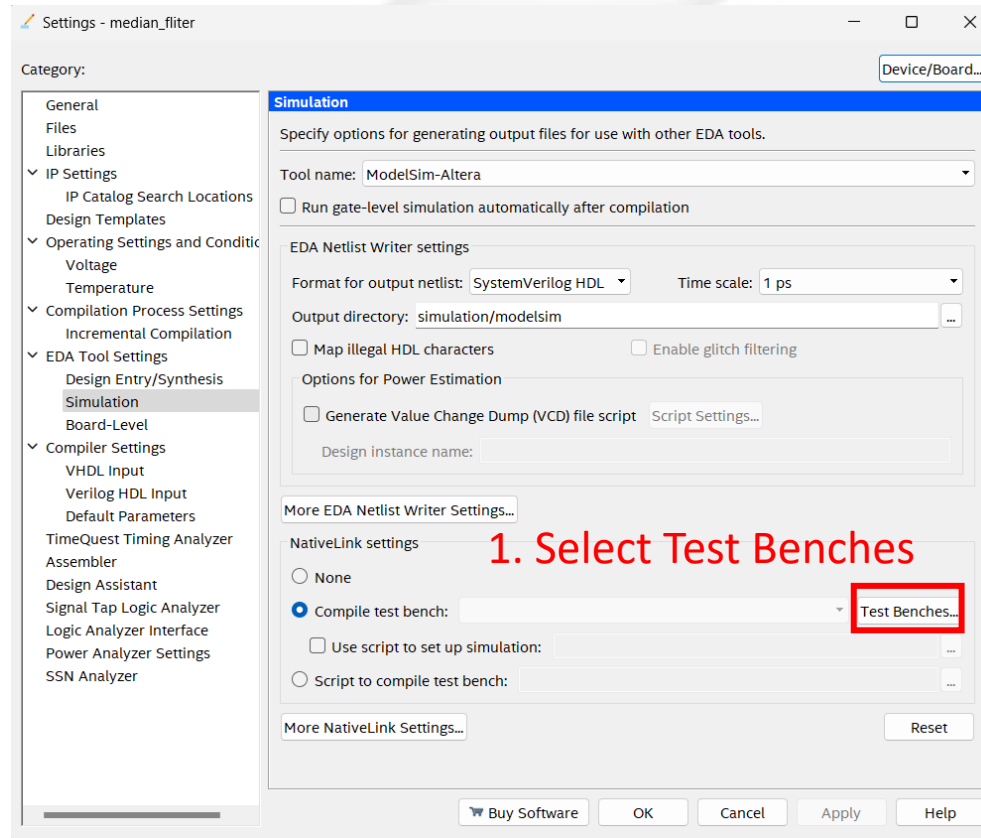
# Setting Options for EDA Tools (2/4)

## □ Assignments > Settings



# Setting Options for EDA Tools (3/4)

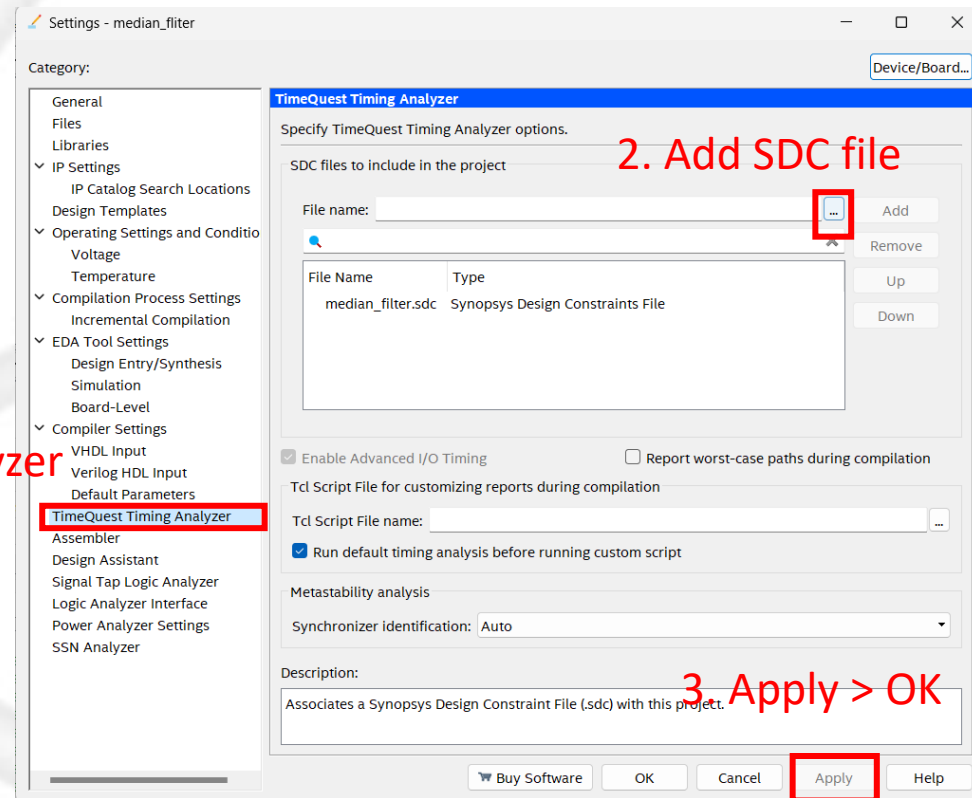
## □ Add test bench to project at ModelSim.



# Setting Options for EDA Tools (4/4)

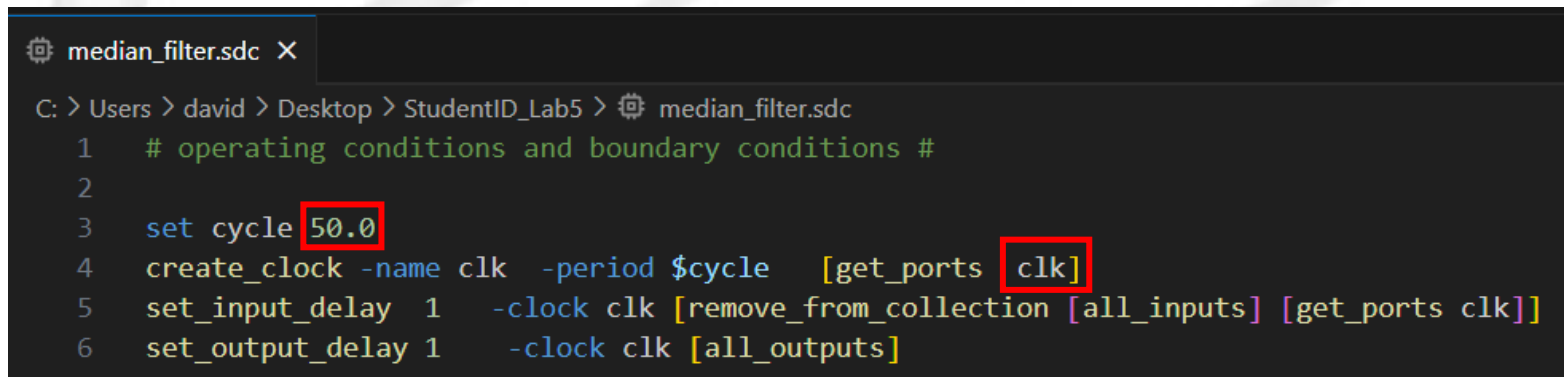
- Synopsys Design Constraints (SDC) files can be used to define the clock period during the synthesis stage.

1. TimeQuest Timing Analyzer



# Synopsys Design Constraints files

- ❑ By default, clock cycles in SDC files are specified in nanoseconds (ns). **Ensure the clock period in the SDC file matches the value defined in your testbench.**
- ❑ The clock port name in the SDC file should match the corresponding clock port name in your top-level module.



```
median_filter.sdc X
C: > Users > david > Desktop > StudentID_Lab5 > median_filter.sdc
1  # operating conditions and boundary conditions #
2
3  set cycle 50.0
4  create_clock -name clk -period $cycle [get_ports clk]
5  set_input_delay 1 -clock clk [remove_from_collection [all_inputs] [get_ports clk]]
6  set_output_delay 1 -clock clk [all_outputs]
```

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# Design Compilation

- When you run any module, the Compiler runs automatically and generates detailed reports at each stage.

Run full compilation process

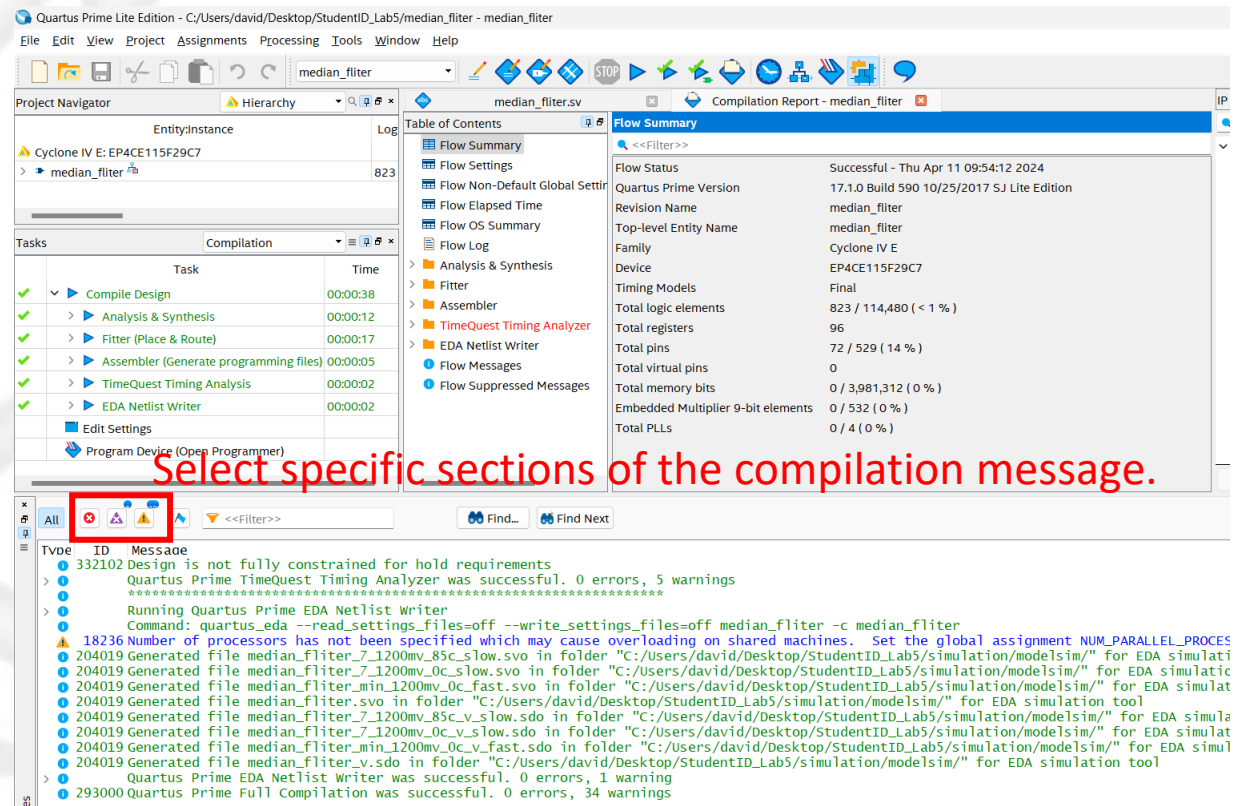
Allowing to run only the process that you need.

```

1 module median_filter(
2     // input port
3     clk,
4     rst,
5     enable,
6     RAM_IMG_Q,
7     RAM_OUT_Q,
8     // output port
9     RAM_IMG_OE,
10    RAM_IMG_WE,
11    RAM_IMG_A,
12    RAM_IMG_D,
13    RAM_OUT_OE,
14    RAM_OUT_WE,
15    RAM_OUT_A,
16    RAM_OUT_D,
17    done
18);
19
20 //-----
21 //      PARAMETER DECLARATION
22 //-----
23 typedef enum logic[1:0]{
24     IDLE,
25     READRAM,
26     WRITERAM,
27     FINISH
28 }state;
29
30 state fstate;
31 //-----
32 //      INPUT AND OUTPUT DECLARATION
33 //-----
34 input          clk;
35 input          rst;
36 input          enable;
37 input [7:0]    RAM_IMG_Q;
38 input [7:0]    RAM_OUT_Q;
39 output [7:0]   RAM_IMG_OE;
40 output [7:0]   RAM_IMG_WE;
  
```

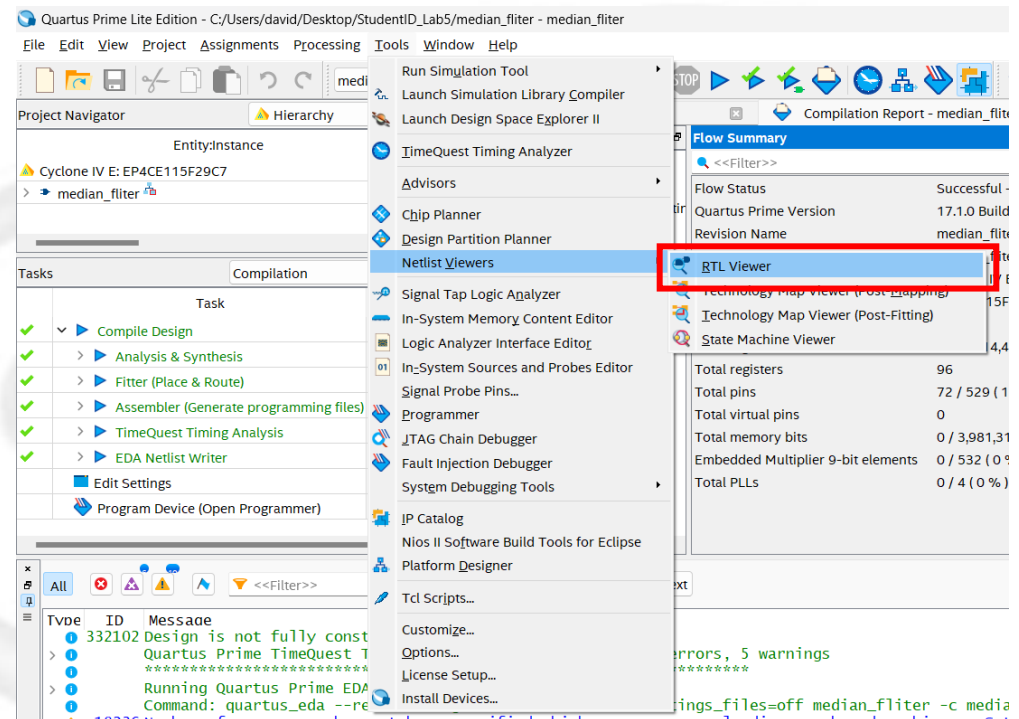
# Error and Warning Messages

- Upon compilation, errors will be displayed in the terminal, Double-clicking the error message should navigate you to the line of code where the error occurred.



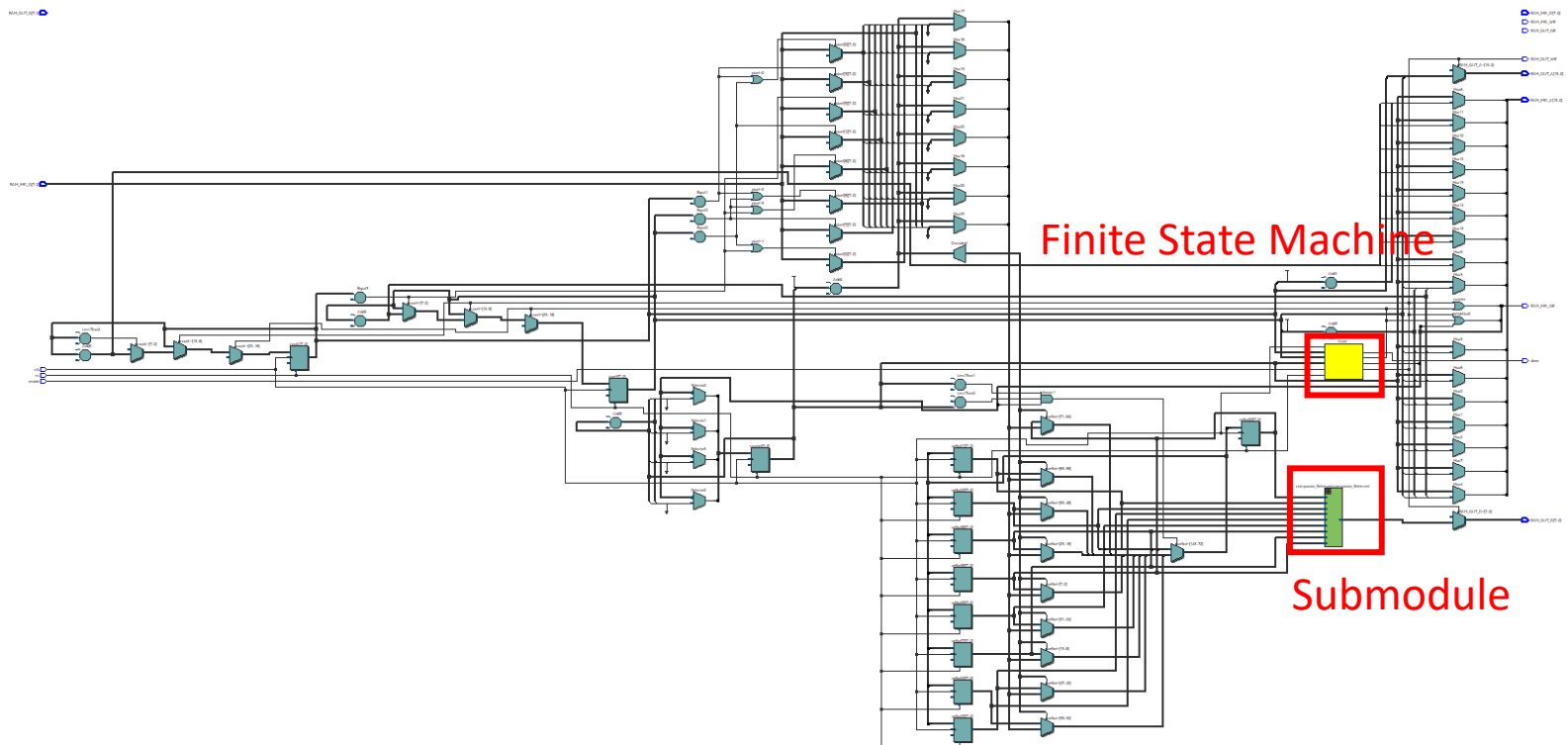
# RTL Viewer Overview (1/3)

- Allowing you to view a register transfer level (RTL) graphical representation of Intel® Quartus® Prime integrated **synthesis results**.
- Tool > Netlist Viewers > RTL Viewer



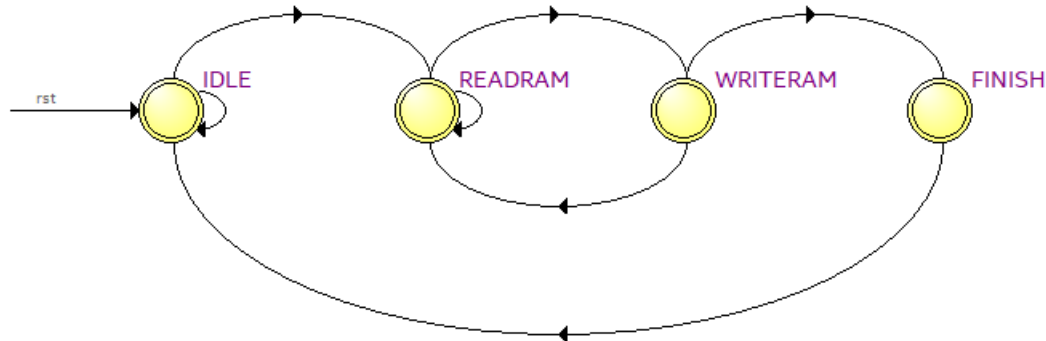
## RTL Viewer Overview (2/3)

- Schematic view of the design netlist after software performs netlist extraction, but before technology mapping and synthesis or fitter optimizations.

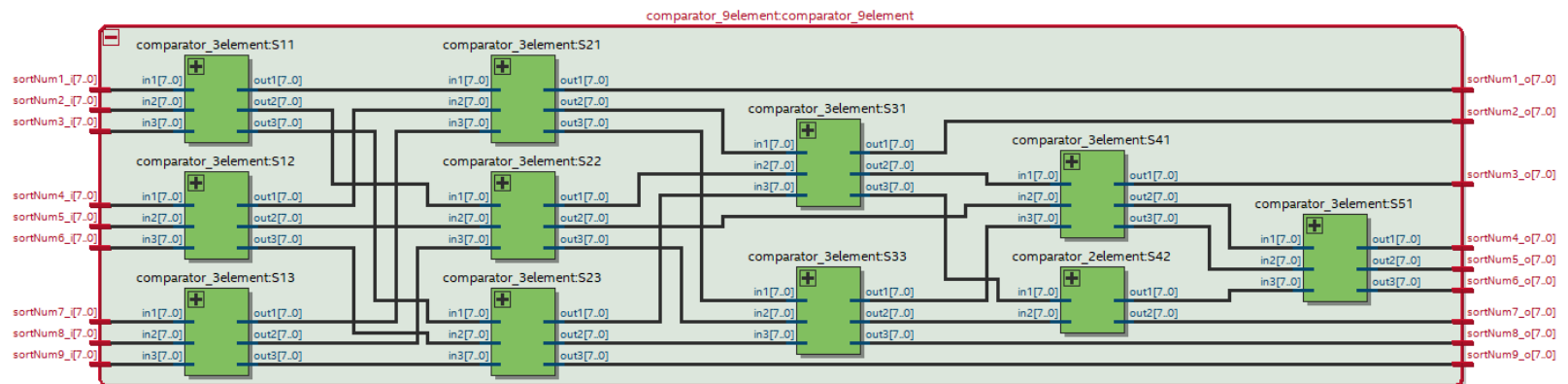


# RTL Viewer Overview (3/3)

□ Double click to view FSM.



□ Double click to view submodule (Sorting Combinational circuit)



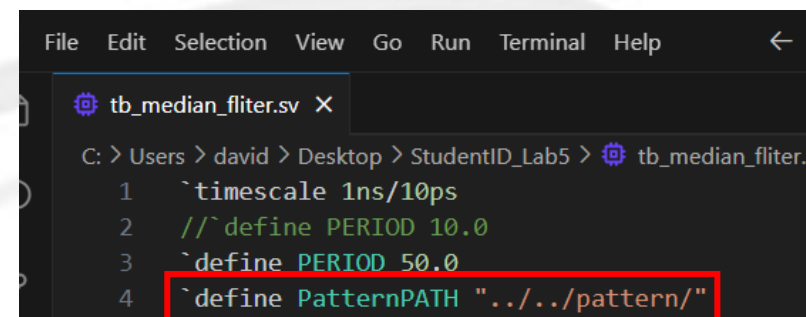


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# Before ModelSim Simulation

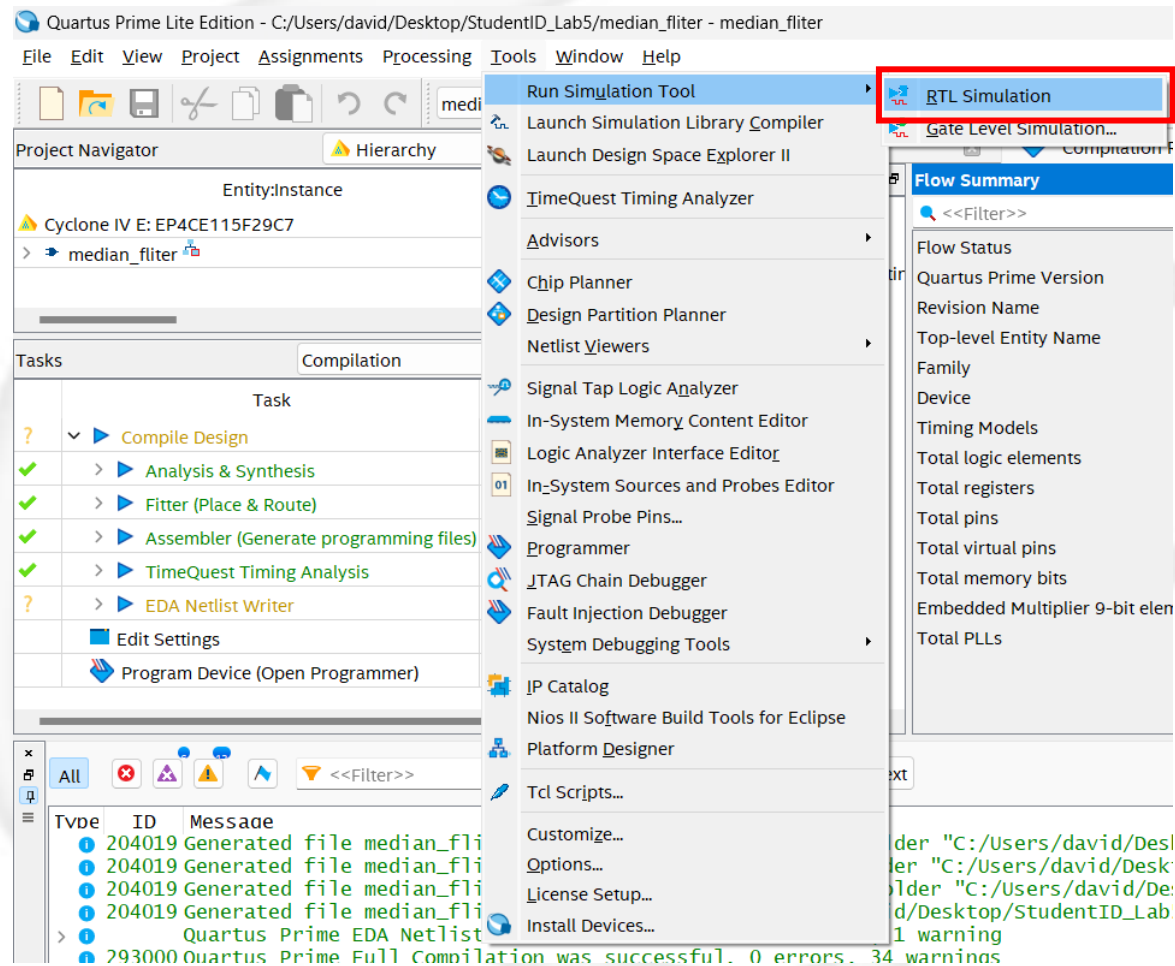
- Within Quartus projects, simulation files are typically located at  $\$(your\_path)/simulation/modelsim$ . Be mindful of using relative file paths in your testbench to ensure proper access.



- Ensure you close ModelSim before returning to Quartus after completing each waveform simulation. **Important**

# Run RTL simulation

□ Tool > Run Simulation Tool > RTL Simulation



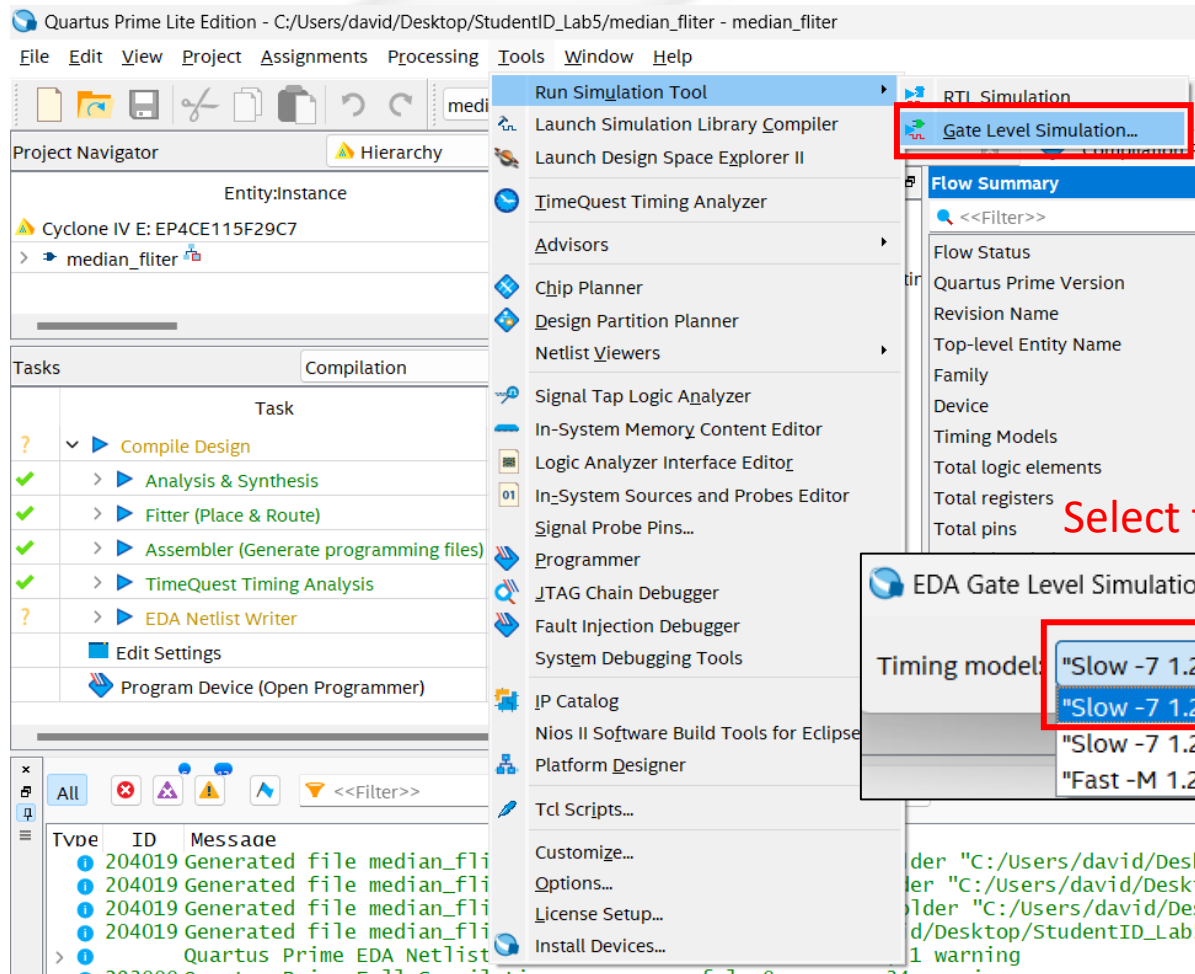
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**UPHCLAB**  
VLSI Design LAB

- 
- ModelSim - INTEL FPGA STARTER EDITION 10.5b
- File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
- Layout: Simulate
- 100 ps
- Search:
- sim - Default
- Instance
- tb\_medan\_filter
- #ALWAYS#69
- #anonblk#110127778#114#4#
- #anonblk#110127778#147#4#
- #anonblk#110127778#152#4#
- #INITIAL#99
- #INITIAL#166
- IMG\_RAM
- medan\_filter
- OUT\_RAM
- std
- #vsim\_capacity#
- Objects
- 014468 ps
- ANS
- dk
- done
- enable
- ErrorNum
- header
- ifile
- indata1
- indata2
- indata3
- ofile
- RAM\_IMG\_A
- RAM\_IMG\_D
- RAM\_IMG\_OE
- Wave - Default
- Maps
- /tb\_medan\_filter/ 0
- /tb\_medan\_filter/ 0
- /tb\_medan\_filter/ 0
- /tb\_medan\_filter/ zzzzzzz
- /tb\_medan\_filter/ zzzzzzz
- /tb\_medan\_filter/ St0
- Now 7209015 ns
- Cursor 1 9014.468 ns
- ns
- 5000000 ns
- 7209014.468 ns
- Transcript
- ```
# run -all
# *****
# ** Simulation Start **
# *****
#
# *****
# ** Congratulations !! **
# ** Simulation PASS!! **
# *****
#
# *****
# ** Note: $finish : C:/Users/david/Desktop/StudentID_Lab5/tb_medan_fltier.sv(163)
# Time: 7209015 ns Iteration: 1 Instance: /tb_medan_fltier
# 1
# Break in Module tb_medan_fltier at C:/Users/david/Desktop/StudentID_Lab5/tb_medan_fltier.sv line 163
VSM 2>
```
- Now: 7,209,015 ns, Delta: 1 /tb median flter/RAM OUT A 0 ps to 7569465750 ps

# Run Gate-Level Simulation

□ Tool > Run Simulation Tool > RTL Simulation

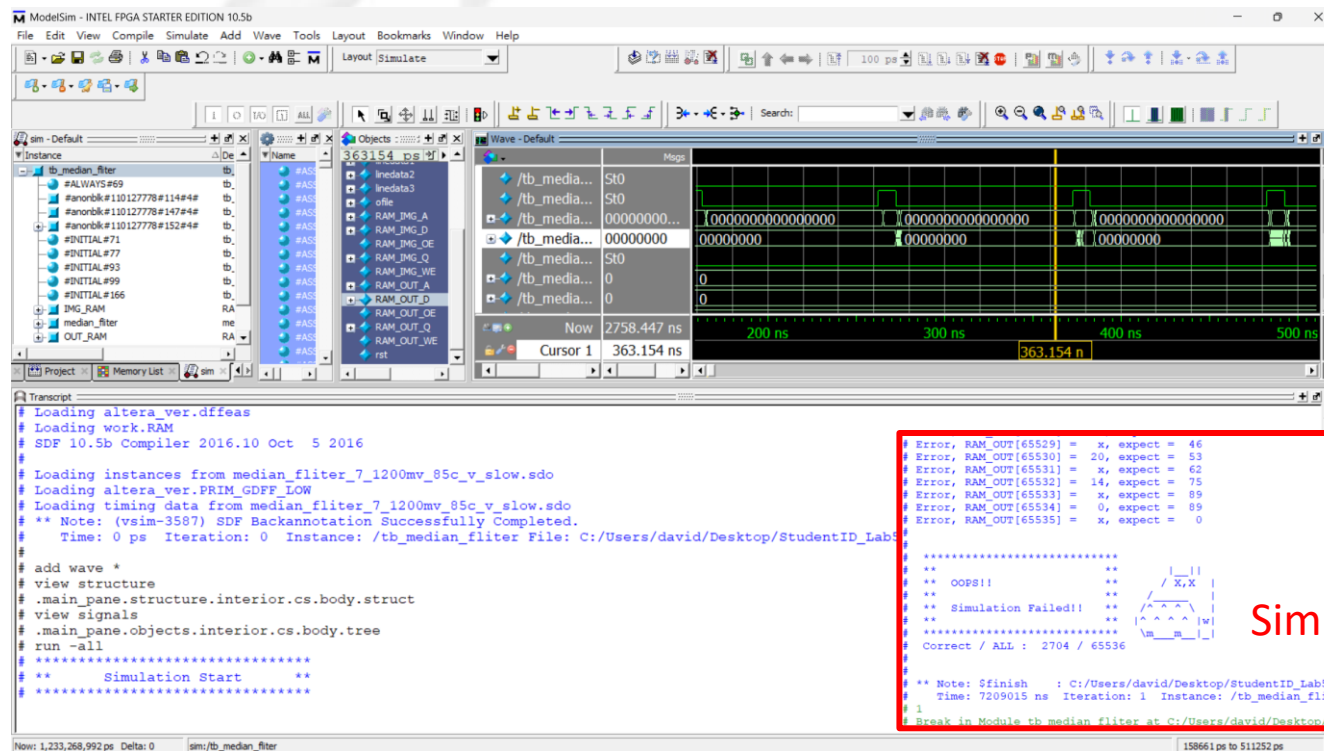


Select the worst timing model



# Run Gate-Level Simulation and Launch ModelSim

- After synthesis, the waveform may exhibit transition uncertainty. Additionally, simulation results might indicate timing violations due to **insufficient clock frequency, leading to final failure.**



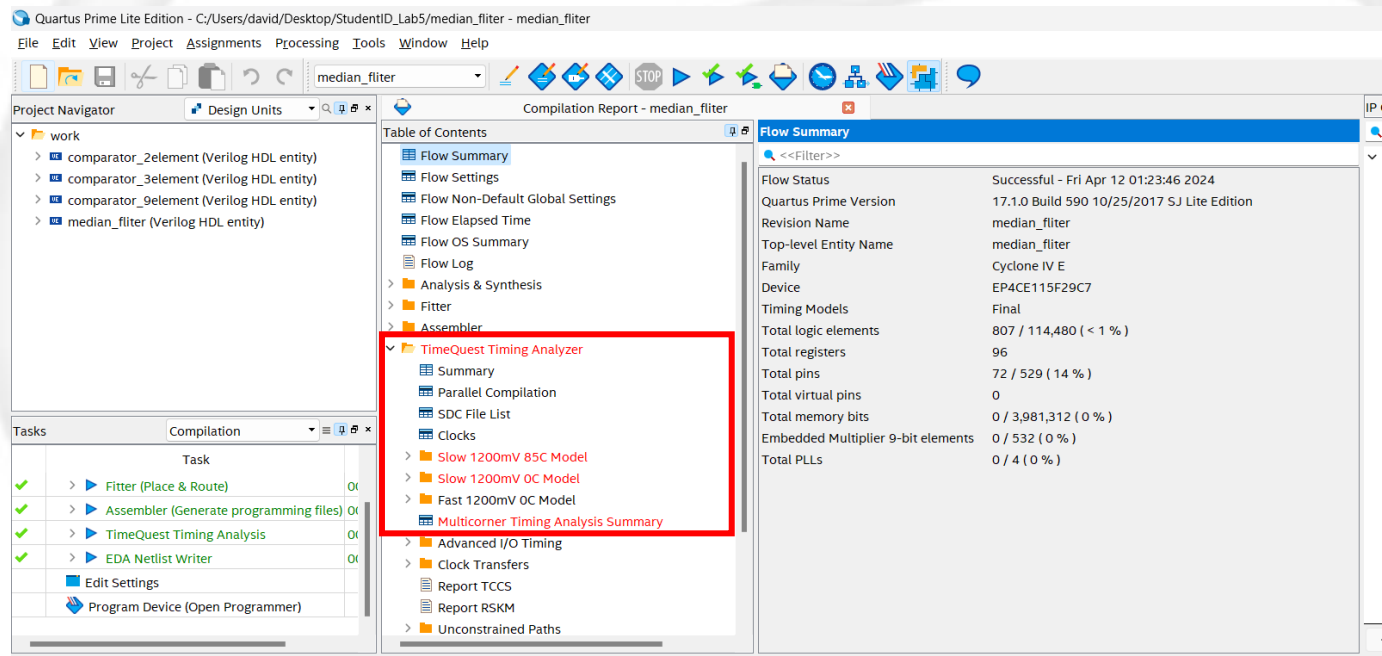
**Simulation Failed**

# Outline

- Introduction to FPGA
- Tool Installation
- Quartus Basic GUI
  - ➔ Create Project
  - ➔ EDA tools Setting
  - ➔ Compilation & Synthesis
  - ➔ Waveform Simulation
  - ➔ Power, Performance and Area

# TimeQuest Timing Analyzer (1/3)

- In TimeQuest Timing Analyzer, **red text** after synthesis indicates potential timing violations in your design. To address this, you'll need to **increase the clock period defined in both the SDC file and testbench**, followed by another synthesis run.



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# TimeQuest Timing Analyzer (2/3)

- In this scenario, timing violations occur in two timing models (Slow 1200mV 85C Model & Slow 1200mV 0C Model ). Clicking on the specific timing model and reviewing the **Fmax Summary** will reveal the expected clock frequency for your design.

The screenshot shows the TimeQuest Timing Analyzer interface. On the left, the 'Table of Contents' pane lists various analysis categories. The 'TimeQuest Timing Analyzer' folder is expanded, and the 'Slow 1200mV 85C Model' folder is selected, with its 'Fmax Summary' sub-item highlighted. On the right, the 'Slow 1200mV 85C Model Fmax Summary' report is displayed. It features a table with the following data:

|   | Fmax      | Restricted Fmax | Clock Name | Note |
|---|-----------|-----------------|------------|------|
| 1 | 20.79 MHz | 20.79 MHz       | clk        |      |

Below the table, a note states: 'This panel reports FMAX for every clock in the design, regardless of the periods. FMAX is only computed for paths where the source and destination are driven by the same clock. Paths of different clocks, including general...

# TimeQuest Timing Analyzer (3/3)

- The worst-case timing paths highlight the critical path in your design.

The setup timing slack is calculated by subtracting the data delay from the clock period.

Quartus Prime Lite Edition - C:/Users/david/Desktop/StudentID\_Lab5/median\_filter - median\_filter

File Edit View Project Assignments Processing Tools Window Help

median\_filter

Project Navigator Design Units

work

- comparator\_2element (Verilog HDL entity)
- comparator\_3element (Verilog HDL entity)
- comparator\_9element (Verilog HDL entity)
- median\_filter (Verilog HDL entity)

Table of Contents

- Assembler
- TimeQuest Timing Analyzer
  - Summary
  - Parallel Compilation
  - SDC File List
  - Clocks
  - Slow 1200mV 85C Model
    - Fmax Summary
    - Timing Closure Recommendation
    - Setup Summary
    - Hold Summary
    - Recovery Summary
    - Removal Summary
    - Minimum Pulse Width Summary
  - Worst-Case Timing Paths
    - Setup: 'clk'
    - Hold: 'clk'
    - Recovery: 'clk'
    - Removal: 'clk'
  - Metastability Summary
  - Slow 1200mV 0C Model
  - Fast 1200mV 0C Model
  - Multicorner Timing Analysis Summary

Compilation Report - median\_filter

Slow 1200mV 85C Model Setup: 'clk'

|    | Slack | From Node     | To Node      | Launch Clock | Latch Clock | Relationship | Clock Skew | Data Delay |
|----|-------|---------------|--------------|--------------|-------------|--------------|------------|------------|
| 1  | 2.022 | arrSort[3][2] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.063     | 43.915     |
| 2  | 2.023 | arrSort[3][0] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.063     | 43.914     |
| 3  | 2.108 | arrSort[4][2] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.063     | 43.829     |
| 4  | 2.114 | arrSort[3][1] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.062     | 43.824     |
| 5  | 2.149 | arrSort[4][0] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.063     | 43.788     |
| 6  | 2.190 | arrSort[4][1] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.063     | 43.747     |
| 7  | 2.200 | arrSort[3][3] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.062     | 43.738     |
| 8  | 2.223 | arrSort[1][0] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.055     | 43.722     |
| 9  | 2.263 | arrSort[0][0] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.054     | 43.683     |
| 10 | 2.285 | arrSort[3][4] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.063     | 43.652     |
| 11 | 2.290 | arrSort[3][2] | RAM_OUT_D[4] | clk          | clk         | 50.000       | -3.063     | 43.647     |
| 12 | 2.291 | arrSort[3][0] | RAM_OUT_D[4] | clk          | clk         | 50.000       | -3.063     | 43.646     |
| 13 | 2.295 | arrSort[3][2] | RAM_OUT_D[2] | clk          | clk         | 50.000       | -3.063     | 43.642     |
| 14 | 2.296 | arrSort[3][0] | RAM_OUT_D[2] | clk          | clk         | 50.000       | -3.063     | 43.641     |
| 15 | 2.323 | arrSort[4][3] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.063     | 43.614     |
| 16 | 2.376 | arrSort[4][2] | RAM_OUT_D[4] | clk          | clk         | 50.000       | -3.063     | 43.561     |
| 17 | 2.381 | arrSort[0][2] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.054     | 43.565     |
| 18 | 2.381 | arrSort[4][2] | RAM_OUT_D[2] | clk          | clk         | 50.000       | -3.063     | 43.556     |
| 19 | 2.382 | arrSort[3][1] | RAM_OUT_D[4] | clk          | clk         | 50.000       | -3.062     | 43.556     |
| 20 | 2.387 | arrSort[3][1] | RAM_OUT_D[2] | clk          | clk         | 50.000       | -3.062     | 43.551     |
| 21 | 2.401 | arrSort[1][3] | RAM_OUT_D[6] | clk          | clk         | 50.000       | -3.054     | 43.545     |

Tasks

Compilation

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- TimeQuest Timing Analysis
- EDA Netlist Writer
- Fdlt Settings



# Power Analyzer Tool (1/5)

- For accurate power estimation during simulation, utilize the VCD file format for waveform data capture.

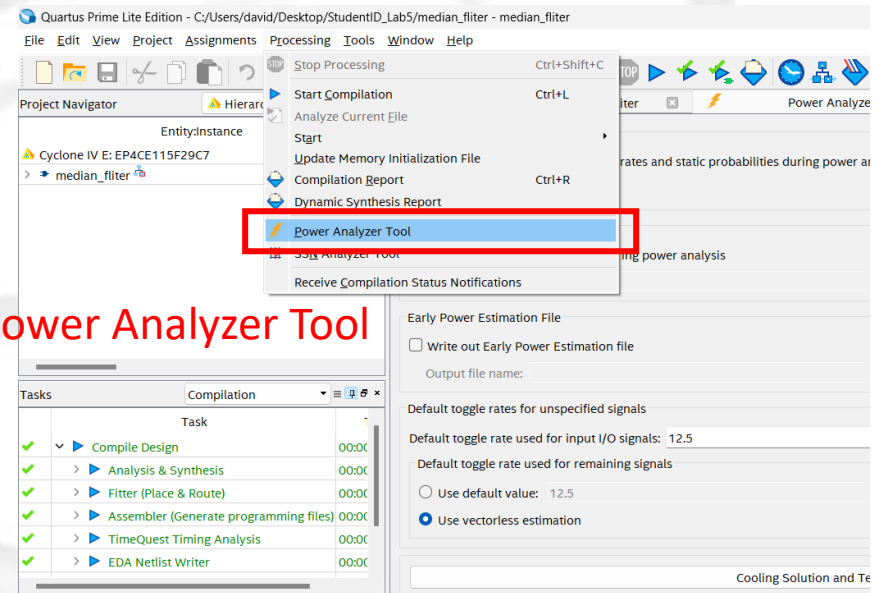
```
tb_median_fliter.v
C: > Users > david > Desktop > StudentID_Lab5 > tb_media
10  module tb_median_fliter;
177  initial begin
178      $dumpfile("tb_median_fliter.vcd");
179      $dumpvars(0, tb_median_fliter);
180  end
```

The \$dumpvars task shall be used to list which variables to dump into the file specified by \$dumpfile.

Freely adjust the scope to view any desired waveform region.

- Once you have generated the VCD file, proceed with power analysis.

Processing > Power Analyzer Tool



# Power Analyzer Tool (2/5)

- Import the VCD file for dynamic power analysis.

Compilation Report - median\_filter    Power Analyzer Tool

**Input file**

☒ Use input file(s) to initialize toggle rates and static probabilities during power analysis

Add Power Input File(s)...

**Output file**

☐ Write out signal activities used during power analysis

Output file name: ...

**Early Power Estimation File**

☐ Write out Early Power Estimation file

Output file name: ...

**Default toggle rates for unspecified signals**

Default toggle rate used for input I/O signals: 12.5 %

Default toggle rate used for remaining signals

☐ Use default value: 12.5 %

☒ Use vectorless estimation

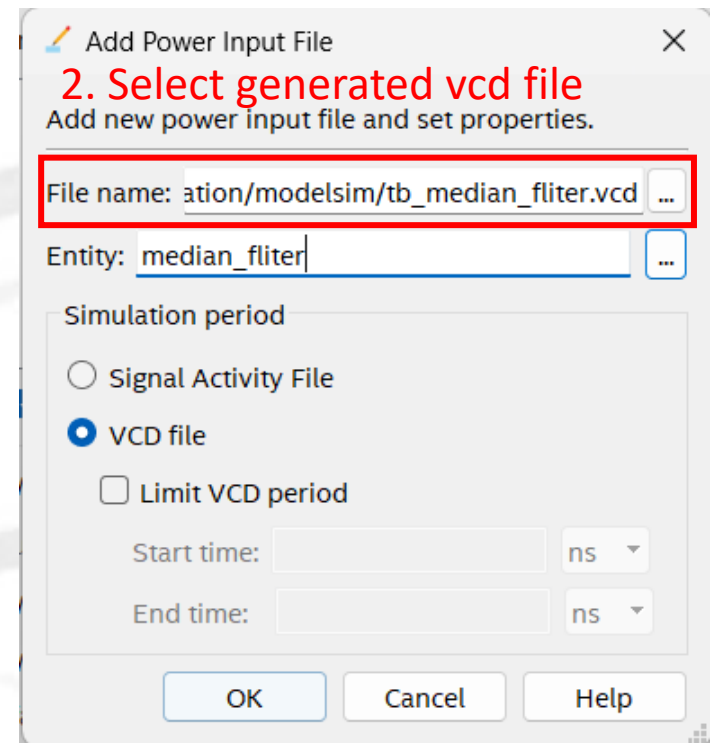
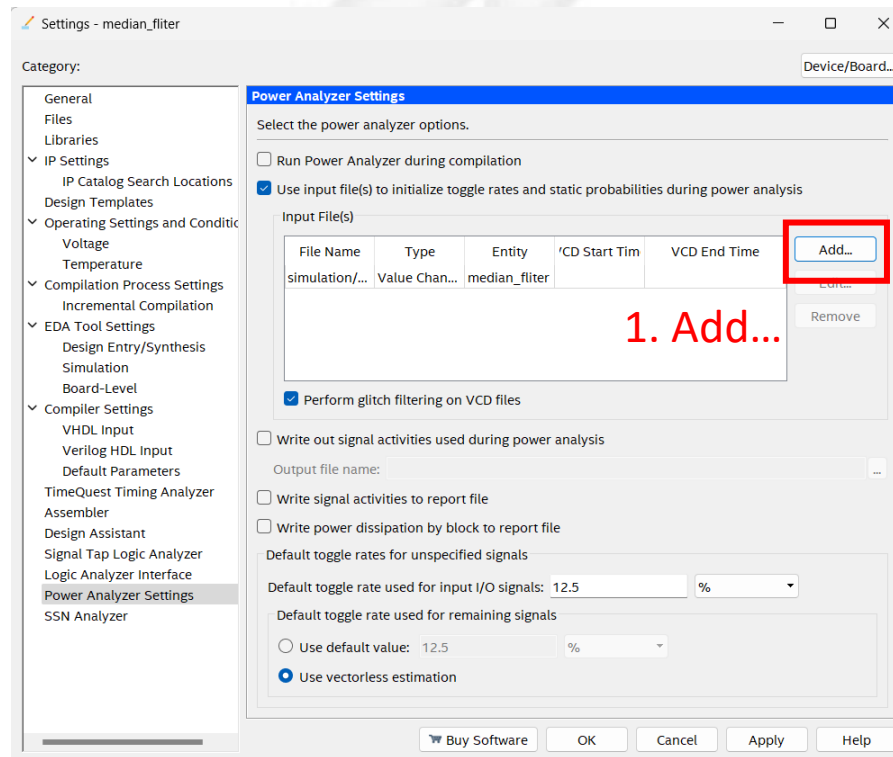
Cooling Solution and Temperature...

00:00:00

Start    Stop    Report

# Power Analyzer Tool (3/5)

- Quartus generates the **simulation folder**, which contains the VCD file.



## Power Analyzer Tool (4/5)

- Click "Start" to initiate the power analysis. Once complete, access the power estimation report by clicking "Report."

Output file

☐ Write out signal activities used during power analysis

Output file name:

Early Power Estimation File

☐ Write out Early Power Estimation file

Output file name:

Default toggle rates for unspecified signals

Default toggle rate used for input I/O signals: 12.5 %

Default toggle rate used for remaining signals

☐ Use default value: 12.5 %

☒ Use vectorless estimation

Cooling Solution and Temperature...

100%

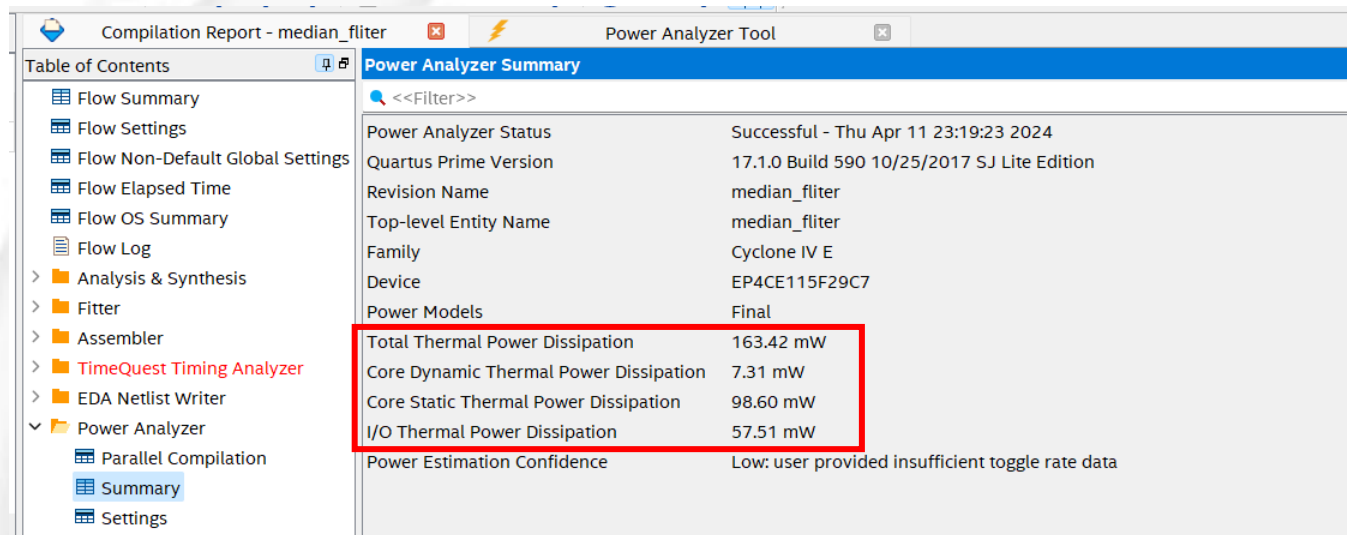
00:00:15

1. Start

2. Report

# Power Analyzer Tool (5/5)

## □ Summary of Power Analysis



| Power Analyzer Summary                 |                                                  |
|----------------------------------------|--------------------------------------------------|
| <<Filter>>                             |                                                  |
| Power Analyzer Status                  | Successful - Thu Apr 11 23:19:23 2024            |
| Quartus Prime Version                  | 17.1.0 Build 590 10/25/2017 SJ Lite Edition      |
| Revision Name                          | median_filter                                    |
| Top-level Entity Name                  | median_filter                                    |
| Family                                 | Cyclone IV E                                     |
| Device                                 | EP4CE115F29C7                                    |
| Power Models                           | Final                                            |
| Total Thermal Power Dissipation        | 163.42 mW                                        |
| Core Dynamic Thermal Power Dissipation | 7.31 mW                                          |
| Core Static Thermal Power Dissipation  | 98.60 mW                                         |
| I/O Thermal Power Dissipation          | 57.51 mW                                         |
| Power Estimation Confidence            | Low: user provided insufficient toggle rate data |



# Flow Summary

- The Flow Summary section of the compilation report indicates whether the design exceeds the available device resources, and reports resource utilization, including pins, memory bits, DSP blocks, and PLLs.

The logic elements provide a preliminary estimate of the synthesis area for your design.

Quartus Prime Lite Edition - C:/Users/david/Desktop/StudentID\_Lab5/median\_filter - median\_filter

File Edit View Project Assignments Processing Tools Window Help

median\_filter

Project Navigator

Entity:Instance Log

Cyclone IV E: EP4CE115F29C7

median\_filter 823

Tasks

Compilation

| Task                                   | Time     |
|----------------------------------------|----------|
| Compile Design                         | 00:00:38 |
| Analysis & Synthesis                   | 00:00:12 |
| Fitter (Place & Route)                 | 00:00:17 |
| Assembler (Generate programming files) | 00:00:05 |
| TimeQuest Timing Analysis              | 00:00:02 |
| EDA Netlist Writer                     | 00:00:02 |
| Edit Settings                          |          |
| Program Device (Open Programmer)       |          |

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- TimeQuest Timing Analyzer
- EDA Netlist Writer
- Flow Messages
- Flow Suppressed Messages

Flow Summary

<<Filter>>

|                                    |                                             |
|------------------------------------|---------------------------------------------|
| Flow Status                        | Successful - Thu Apr 11 09:54:12 2024       |
| Quartus Prime Version              | 17.1.0 Build 590 10/25/2017 SJ Lite Edition |
| Revision Name                      | median_filter                               |
| Top-level Entity Name              | median_filter                               |
| Family                             | Cyclone IV E                                |
| Device                             | EP4CE115F29C7                               |
| Timing Models                      | Final                                       |
| Total logic elements               | 823 / 114,480 (< 1 %)                       |
| Total registers                    | 96                                          |
| Total pins                         | 72 / 529 (14 %)                             |
| Total virtual pins                 | 0                                           |
| Total memory bits                  | 0 / 3,981,312 (0 %)                         |
| Embedded Multiplier 9-bit elements | 0 / 532 (0 %)                               |
| Total PLLs                         | 0 / 4 (0 %)                                 |

*Thank you for your attention*