

Siemens HDL Simulator : ModelSim

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Outline

- Tool Introduction
- Tool Installation
- Basic Simulation Flow
- Debugging using Modelsim

Tool Introduction

- ❑ **ModelSim** is a verification and simulation tool for VHDL, Verilog, SystemVerilog, and mixed-language designs.
- ❑ Feature:
 - ➔ Check HDL code for syntax error
 - ➔ Simulate and dump waveform

Tool Installation (1/7)

- ❑ ModelSim Edition 10.5b: [Download Link](#)
- ❑ Individual Files > Download ModelSimSetup...

Intel® Quartus® Prime Lite Edition Design Software Version 17.1 for Windows

ID	Date	Software Type	Software Package	Version	Operating Systems
669444	12/5/2017	FPGA Development Tools	Quartus® Prime Lite	17.1	Windows

A newer version of this software is available, which includes functional and security updates. Customers should [click here](#) to update to the latest version.

Users should upgrade to the latest version of the Intel® Quartus® Prime Design Software. The selected version does not include the latest functional and security updates. If you must use this version of software, follow the [technical recommendations](#) to help improve security. For critical support requests, please contact our [support team](#).

The Intel® Quartus® Prime Lite Edition Design Software, Version 17.1 is subject to removal from the website if it is obsolete. If you would like to receive customer notifications by e-mail, please subscribe to our [newsletter](#).

You may be exposed to a vulnerability issue if you have installed or plan to install Intel® Quartus® Prime Design Software. For more details, see [Critical Issues and Patches for the Intel® Quartus® Prime Lite Edition Software, Version 17.1](#).

[Knowledge Base: Search for Errata](#). Also see [Critical Issues and Patches](#).
[Problems and Answers on specific IP or Products](#).

Downloads **1**

Multiple Download Individual Files Additional Software Updates

Multiple Download

Intel® Quartus® Prime Lite Edition Software (Device support included)

Download Quartus-lite-17.1.0.590-windows.tar Size: 5.8 GB SHA1: 2fc0d8fc702bbaafe9ddb2473f3ae9220f452b5d

What's Included?

Intel® Quartus® Software

ModelSim-Intel® FPGA Edition (includes Starter Edition)

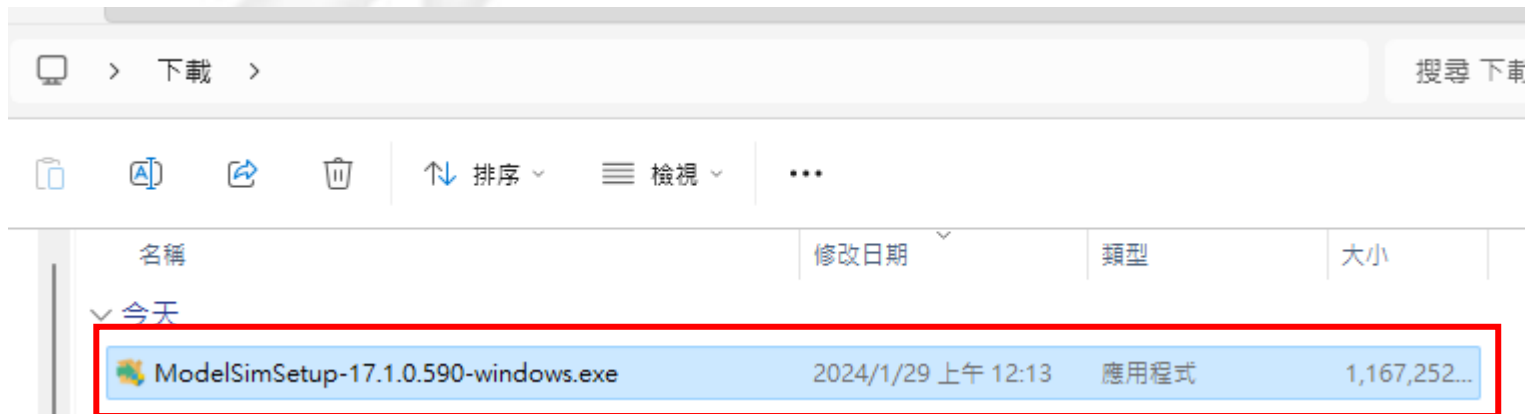
Download ModelSimSetup-17.1.0.590-windows.exe Size: 1.1 GB SHA1: f0b4520cd766bffe4373465e1dc7b819d1176f1

Intel® Quartus® Prime (includes Nios® II EDS)

Download QuartusLiteSetup-17.1.0.590-windows.exe Size: 1.7 GB SHA1: e6b185f220de33432f352cfc3088be7ee0971af8

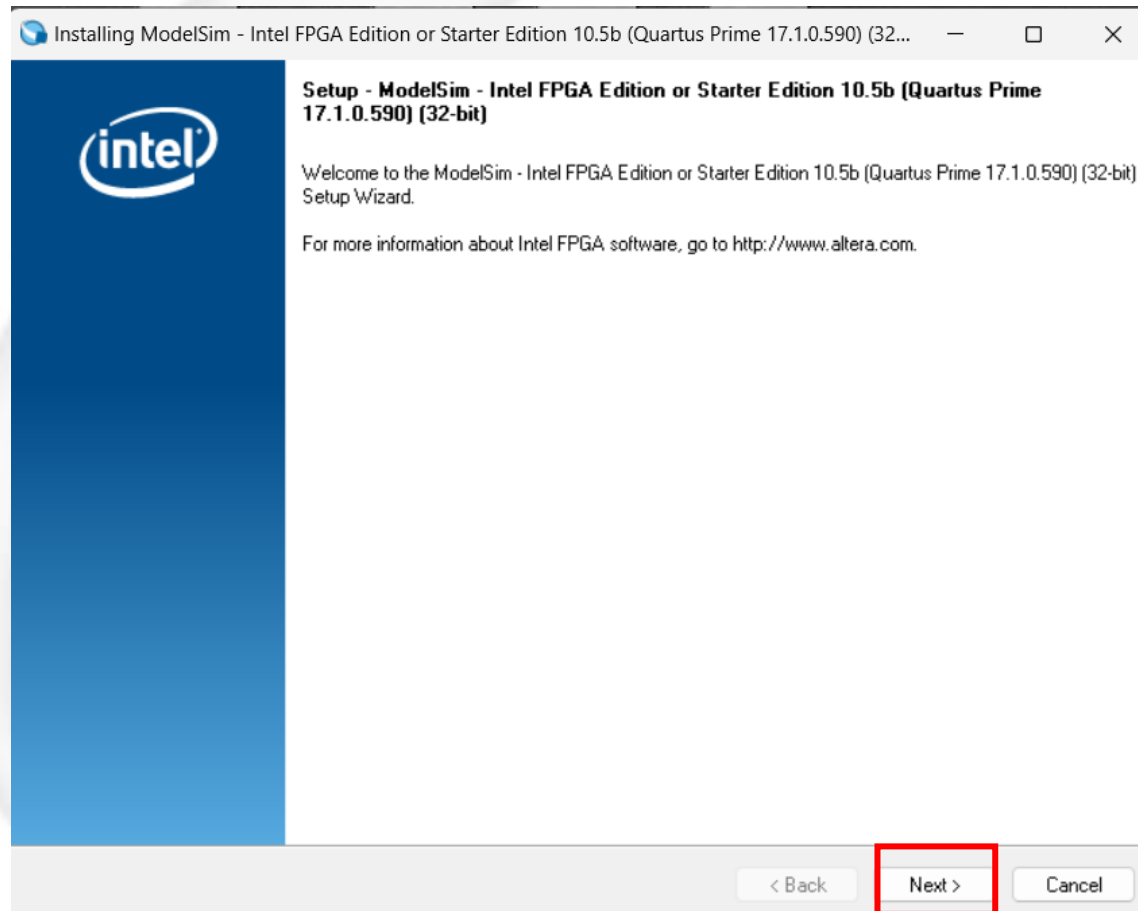
Tool Installation (2/7)

- Click .exe file to installation



Tool Installation (3/7)

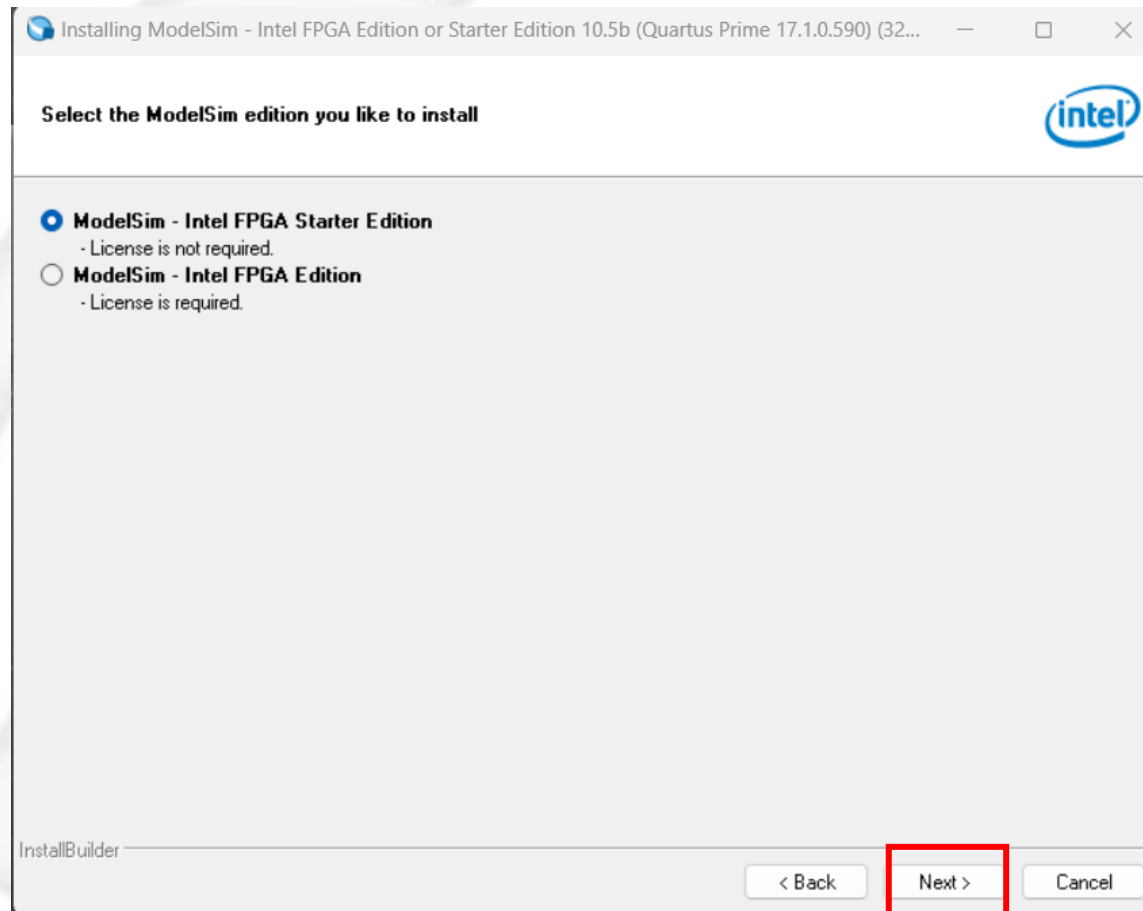
□ Next



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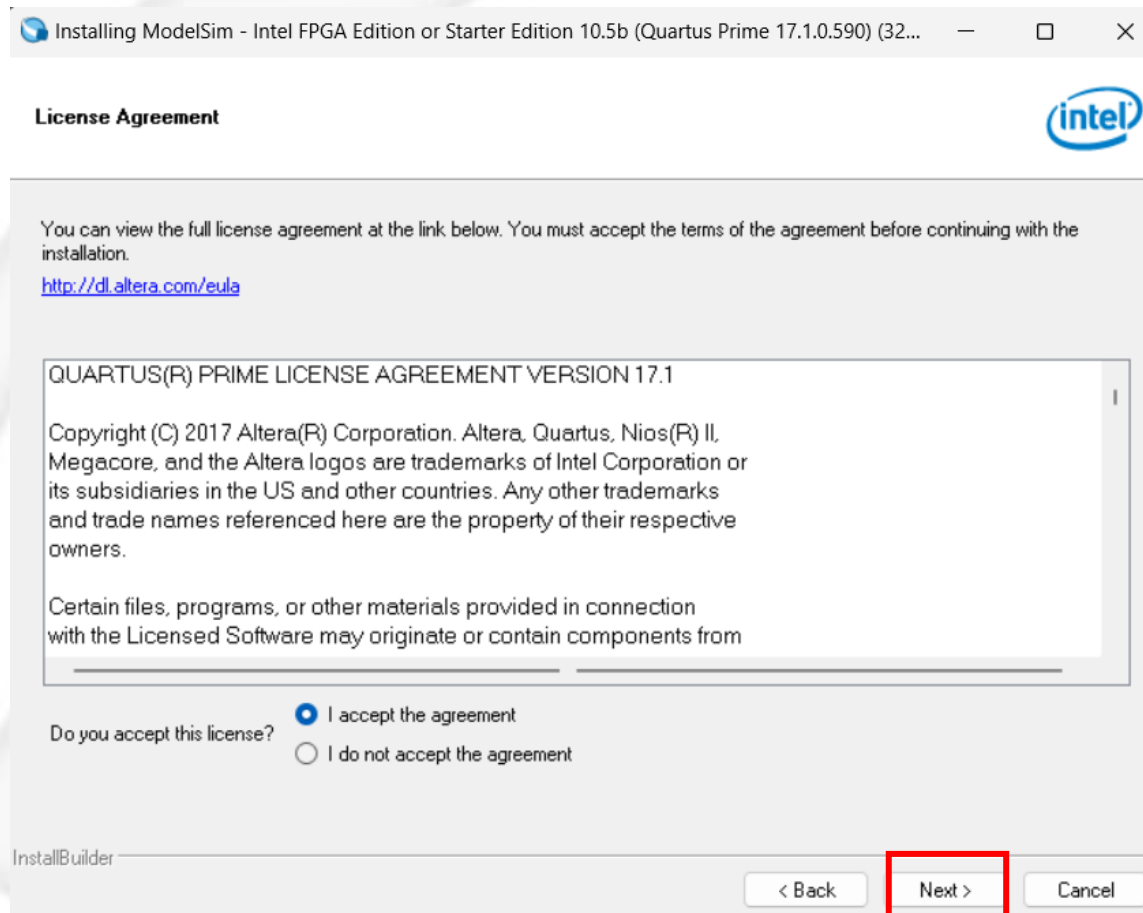
Tool Installation (4/7)

- ❑ Select ModelSim - Intel FPGA Starter Edition



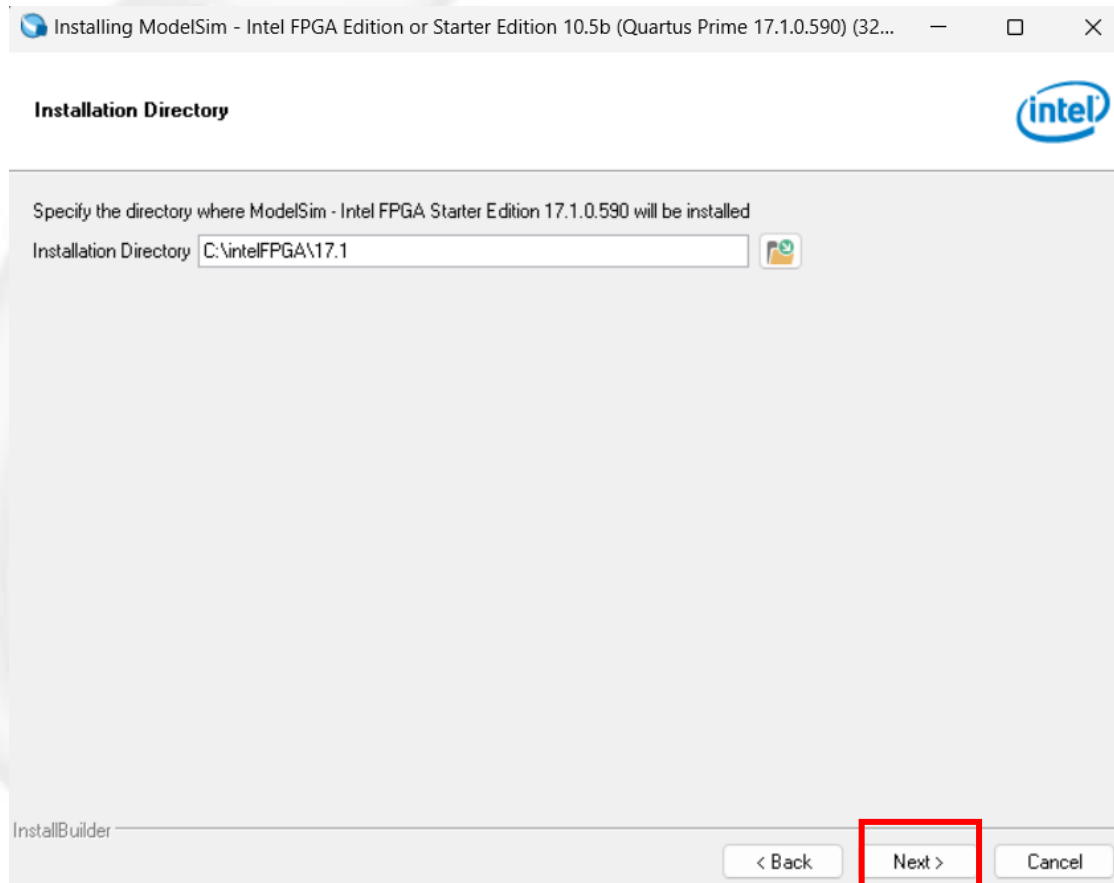
Tool Installation (5/7)

- I accept the agreement > Next



Tool Installation (6/7)

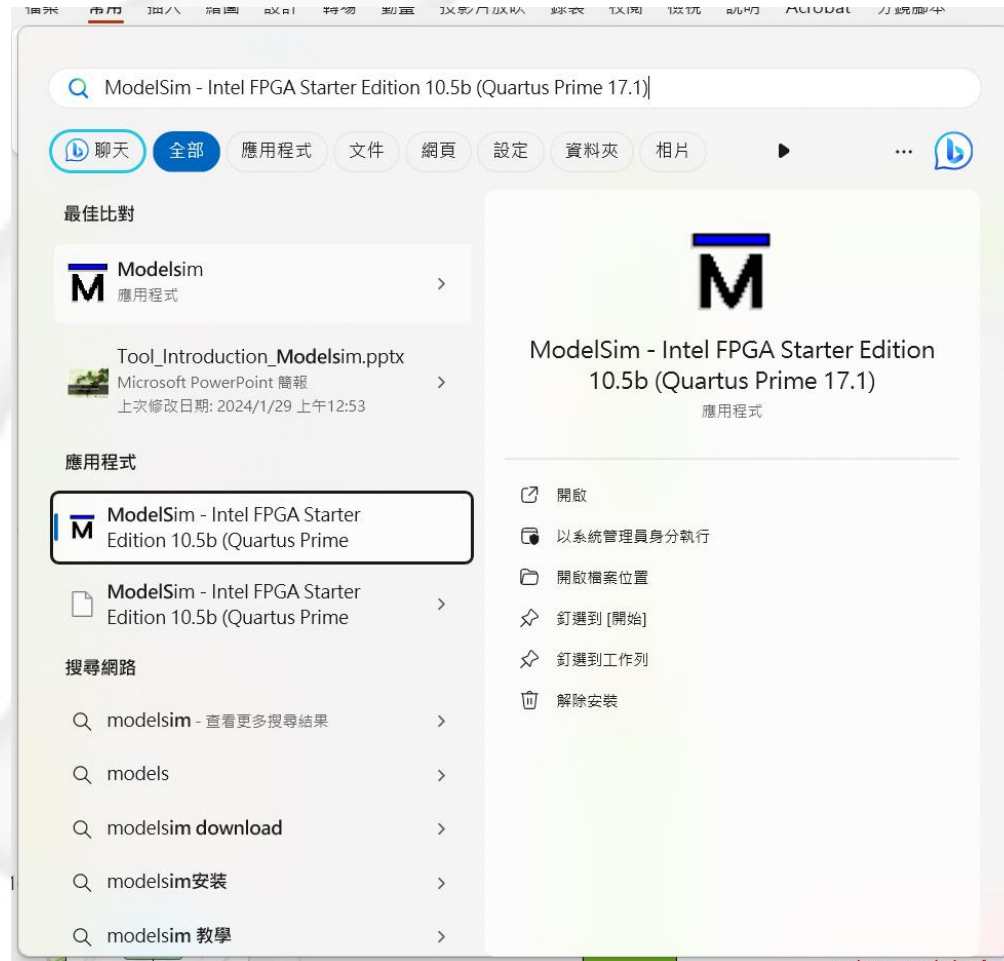
- ❑ Continue clicking “Next” until reach the end of installation.



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Tool Installation (7/7)

□ Search and open ModelSim.



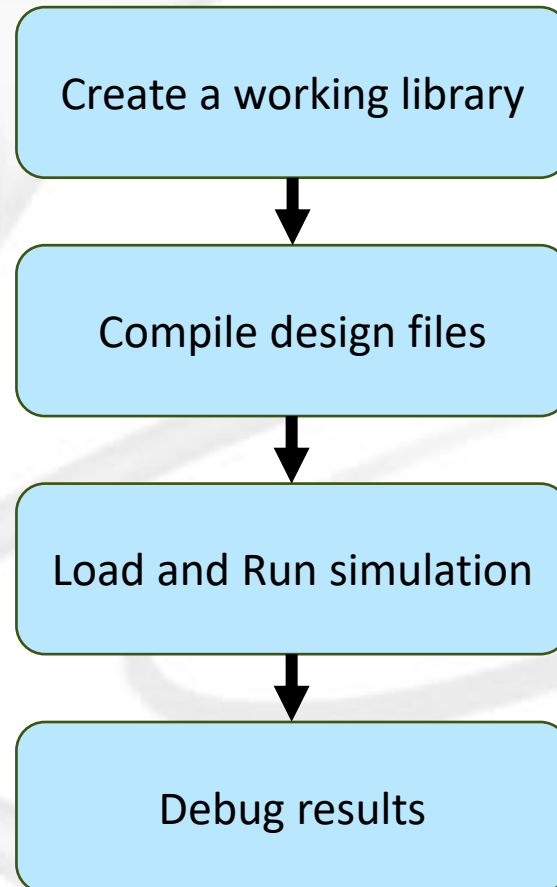
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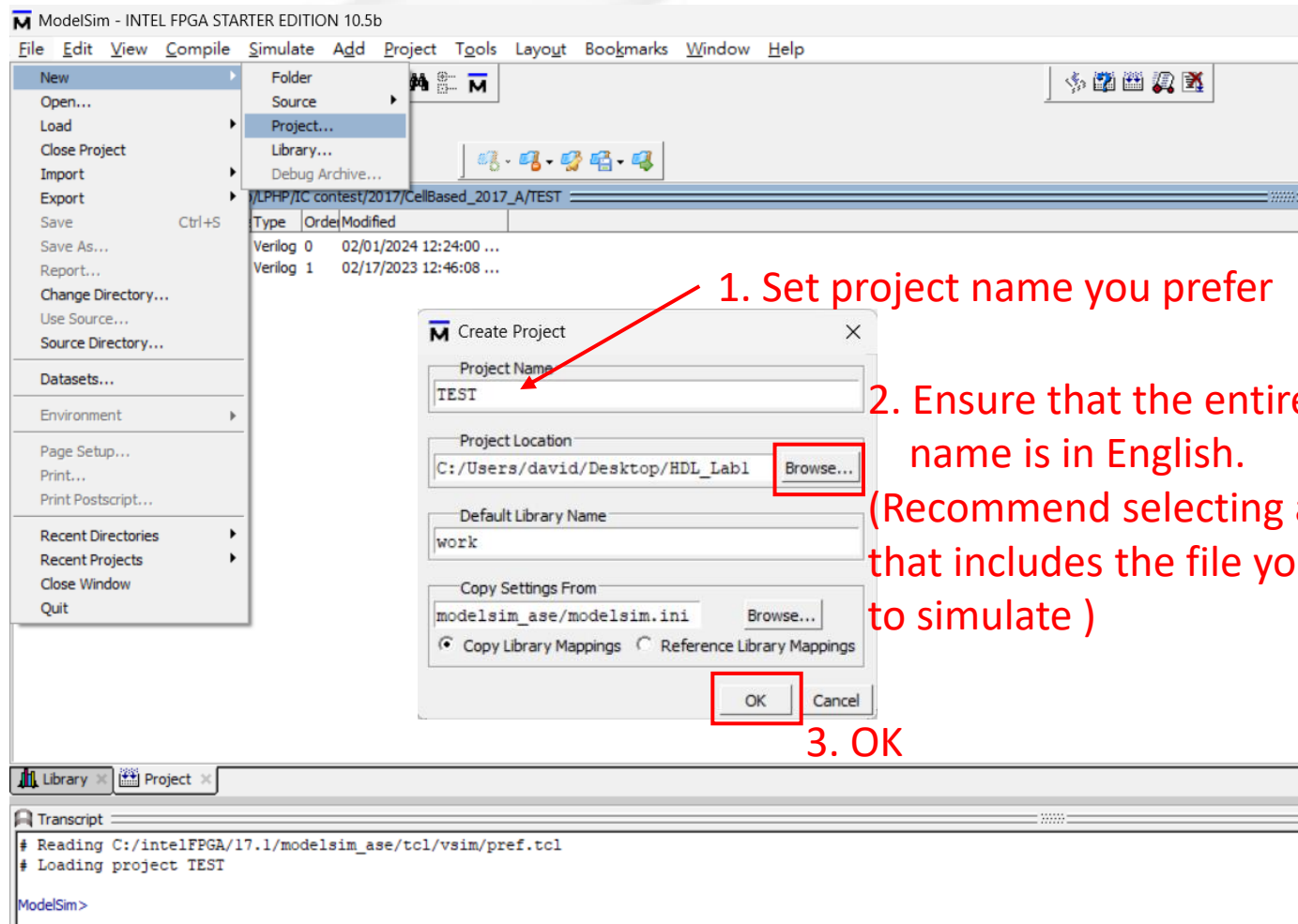
Basic Simulation Flow (1/8)

- Step for simulating a design in ModelSim.



Basic Simulation Flow (2/8)

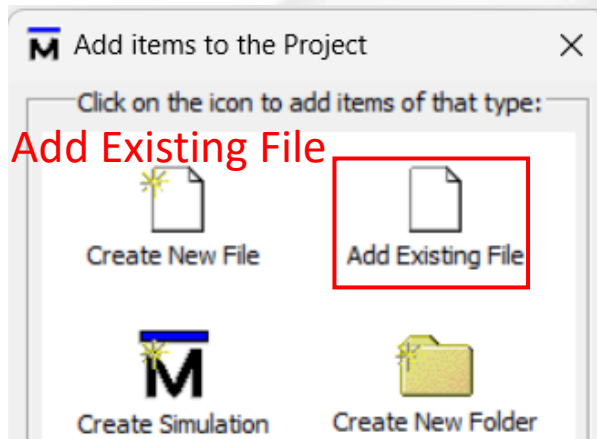
□ Create New project: File > New > Project...



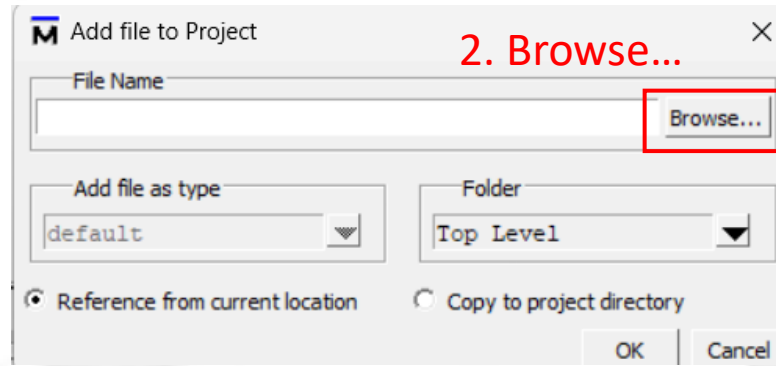
Basic Simulation Flow (3/8)

- Add items to the project.

1. Add Existing File

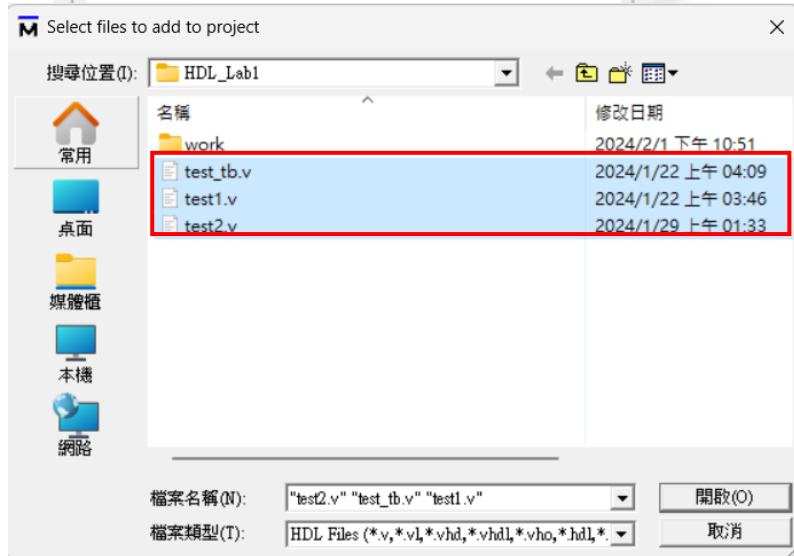


2. Browse...



3. Choose the file you want to include in project.

(if your Design Under Verification (DUV) is already included in the testbench, there is no need to add it to the project again)



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Basic Simulation Flow (4/8)

□ Compile the Design

2. Click “Compile All” to compile all Verilog file.

The screenshot shows the ModelSim - INTEL FPGA STARTER EDITION 10.5b interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Project, Tools, Layout, Bookmarks, Window, and Help. The toolbar contains various icons, with the 'Compile All' icon (a document with a lightning bolt) highlighted by a red box. Below the toolbar, the 'Project' window shows a list of files: test1.v, test_tb.v, and test2.v. The 'Status' column for these files shows a red 'X' for test1.v, a green checkmark for test_tb.v, and a question mark for test2.v. A red box highlights the status icons. Below the project window, the 'Transcript' window shows the following text:

```
# Reading C:/intelFPGA/17.1/modelsim_ase/tcl/vsim/pref.tcl
# Loading project TEST
# reading C:/intelFPGA/17.1/modelsim_ase/win32aloem/./modelsim.ini
# Loading project TEST
# Compile of test2.v was successful.
# Compile of test_tb.v was successful.
# Compile of test1.v failed with 1 errors.
# 3 compiles, 1 failed with 1 error.
```

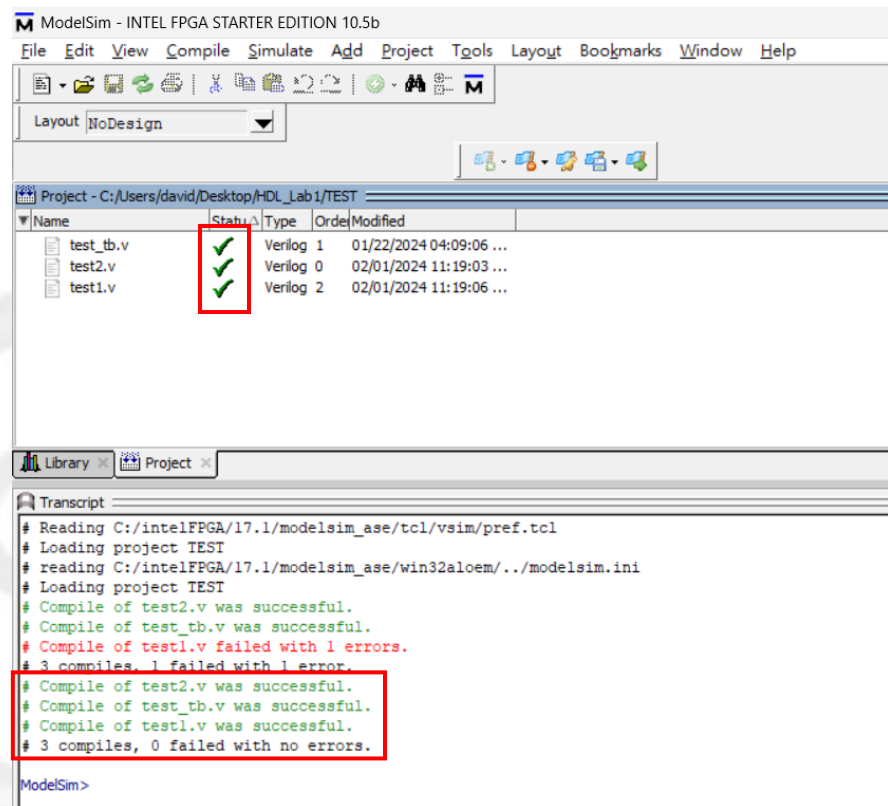
A red box highlights the line '# Compile of test1.v failed with 1 errors.' in the transcript. To the right of the transcript, the text '3. If errors appear, double-click this sentence to view detailed information' is displayed.

1. File status:

- Cross mark represents that there are syntax errors in the respective file.
- Check mark represents that there are no syntax errors in the respective file.
- Question mark represents that the design has not been checked for syntax.

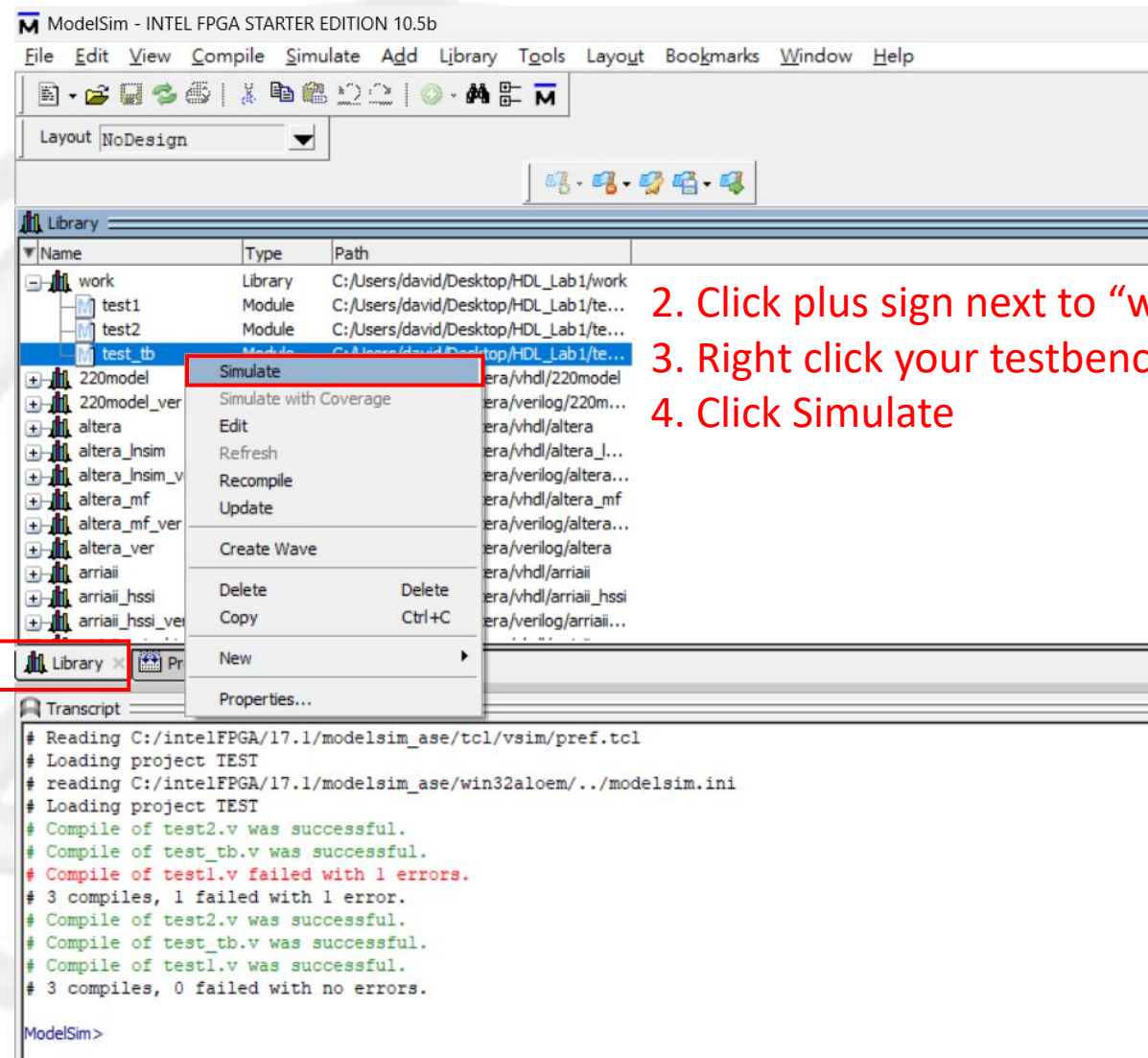
Basic Simulation Flow (5/8)

- You can directly revise the file using your preferred editor and recompile all files until all designs have no syntax errors.



Basic Simulation Flow (6/8)

1. Click Library



2. Click plus sign next to "work"
3. Right click your testbench file
4. Click Simulate

Basic Simulation Flow (7/8) – option

- If there are some “`ifdef” identifier in your testbench, you need to define that before run the simulation.

```
`ifdef T1
    `include "test1.v"
`endif

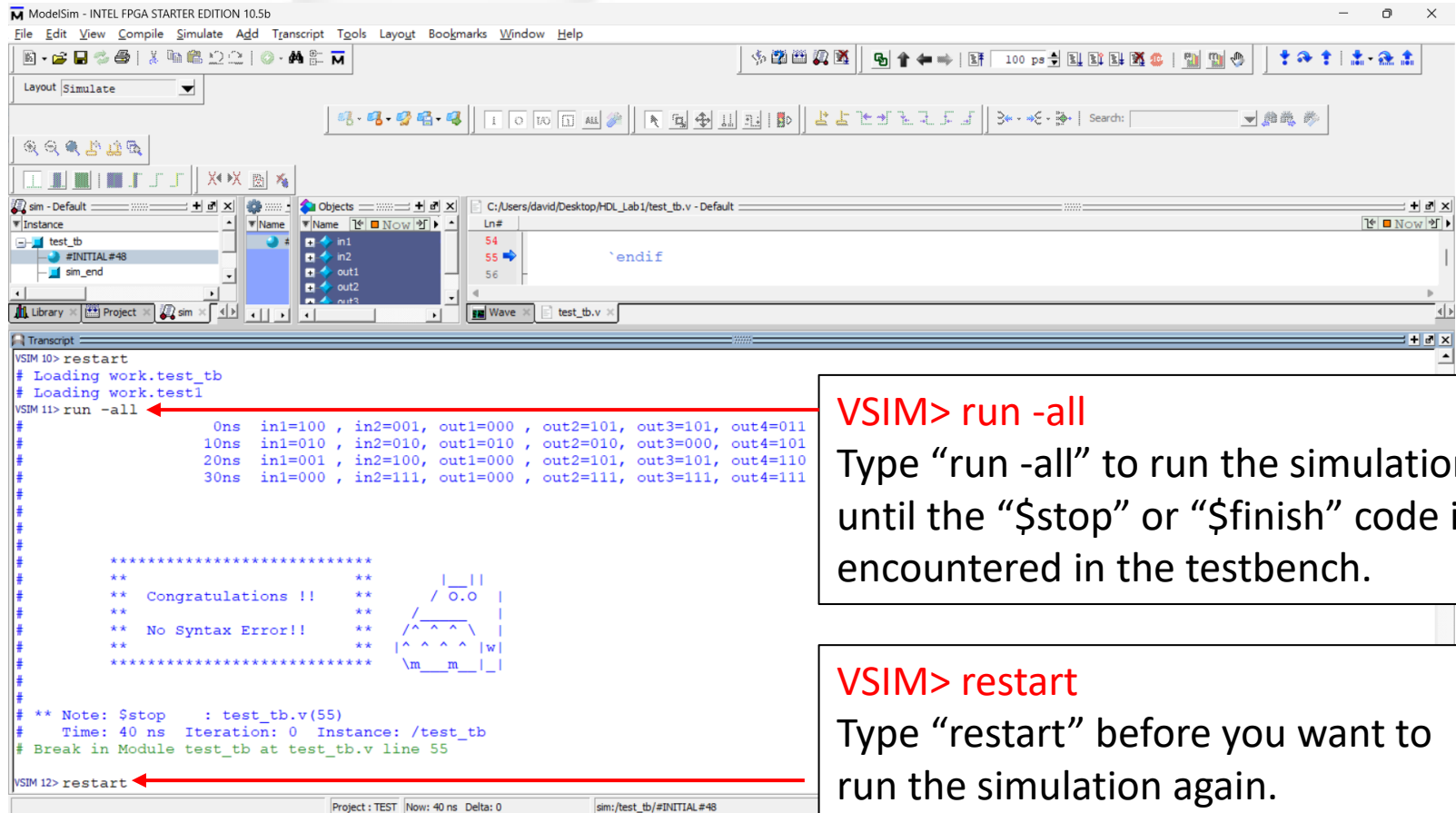
`ifdef T2
    `include "test2.v"
`endif
```

VSIM> vlog test_tb.v +define+T1+P1

In this example, two identifiers, T1 and P1, need to be defined.

Basic Simulation Flow (8/8)

□ Run simulation



```
ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Transcript Tools Layout Bookmarks Window Help

Layout: Simulate

sim - Default
Instance: test_tb
  #INITIAL#48
  sim_end

Objects:
  in1
  in2
  out1
  out2
  out3

C:/Users/david/Desktop/HDL_Lab1/test_tb.v - Default
Ln#
54
55
56
`endif

Transcript:
VSI10> restart
# Loading work.test_tb
# Loading work.test1
VSI11> run -all
0ns in1=100, in2=001, out1=000, out2=101, out3=101, out4=011
10ns in1=010, in2=010, out1=010, out2=010, out3=000, out4=101
20ns in1=001, in2=100, out1=000, out2=101, out3=101, out4=110
30ns in1=000, in2=111, out1=000, out2=111, out3=111, out4=111

*****
** Congratulations !! **
** No Syntax Error!! **
*****

** Note: $stop : test_tb.v(55)
Time: 40 ns Iteration: 0 Instance: /test_tb
# Break in Module test_tb at test_tb.v line 55

VSI12> restart
```

VSI11> run -all

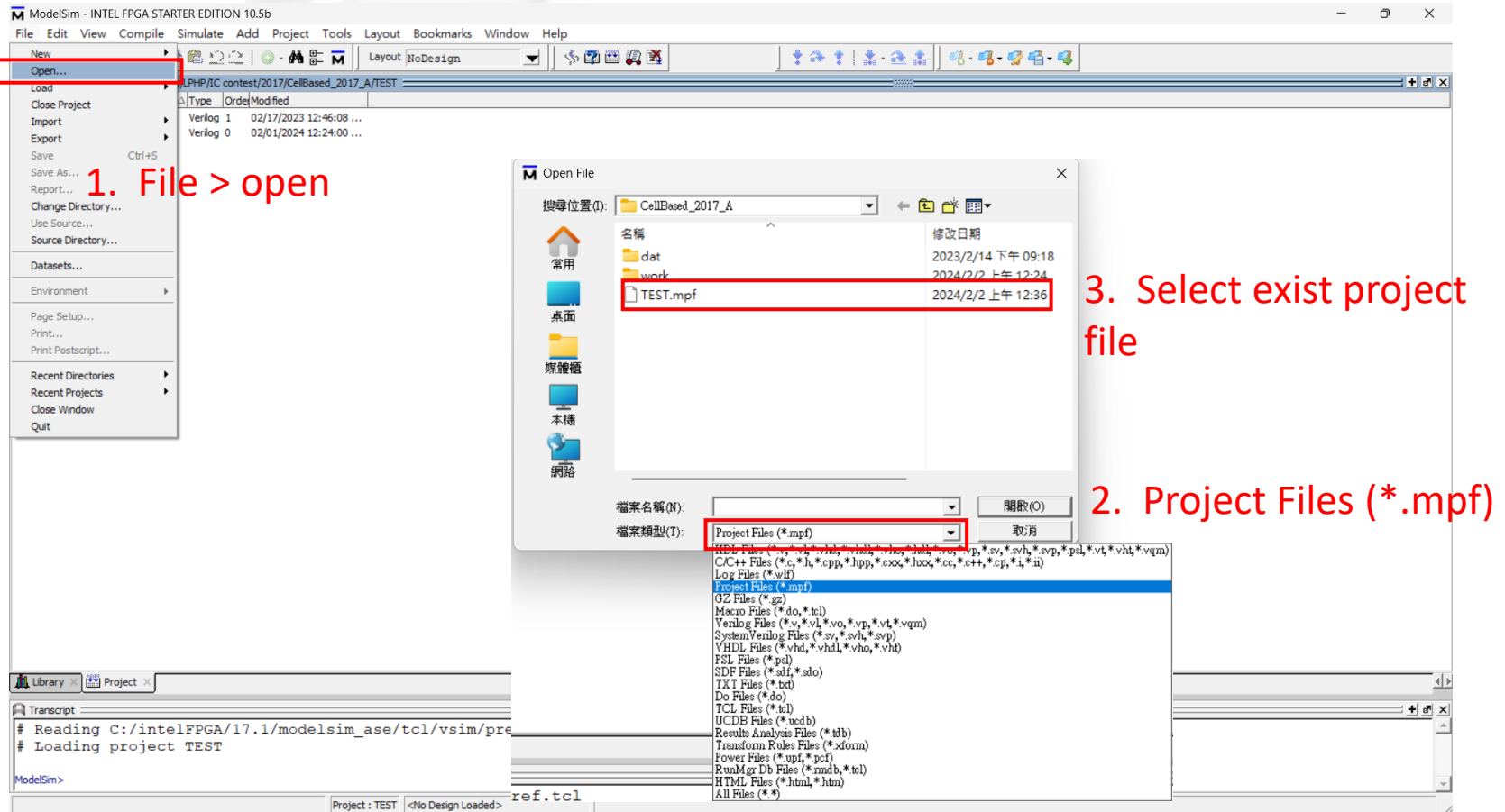
Type “run -all” to run the simulation until the “\$stop” or “\$finish” code is encountered in the testbench.

VSI12> restart

Type “restart” before you want to run the simulation again.

Appendix: Open Exist Project

- If accidentally close the ModelSim project, there's no need to recreate a new project.



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Debugging (1/3)

□ Add waveforms for debugging.

2. Select the module you want to view the signal ports

The screenshot shows the ModelSim interface with the following components:

- Instance Tree:** A red box highlights the 'test_tb' module under the 'sim - Default' instance.
- Objects Window:** A red box highlights the 'Add Wave' option in the context menu for the 'test_tb' module.
- Wave Window:** A red box highlights the 'test_tb/in1' signal in the list of signals to be added to the waveform.
- Transcript Window:** A red box highlights the 'restart' command in the transcript.

1. sim

3. Select the port, then right-click to add the waveform to the window.

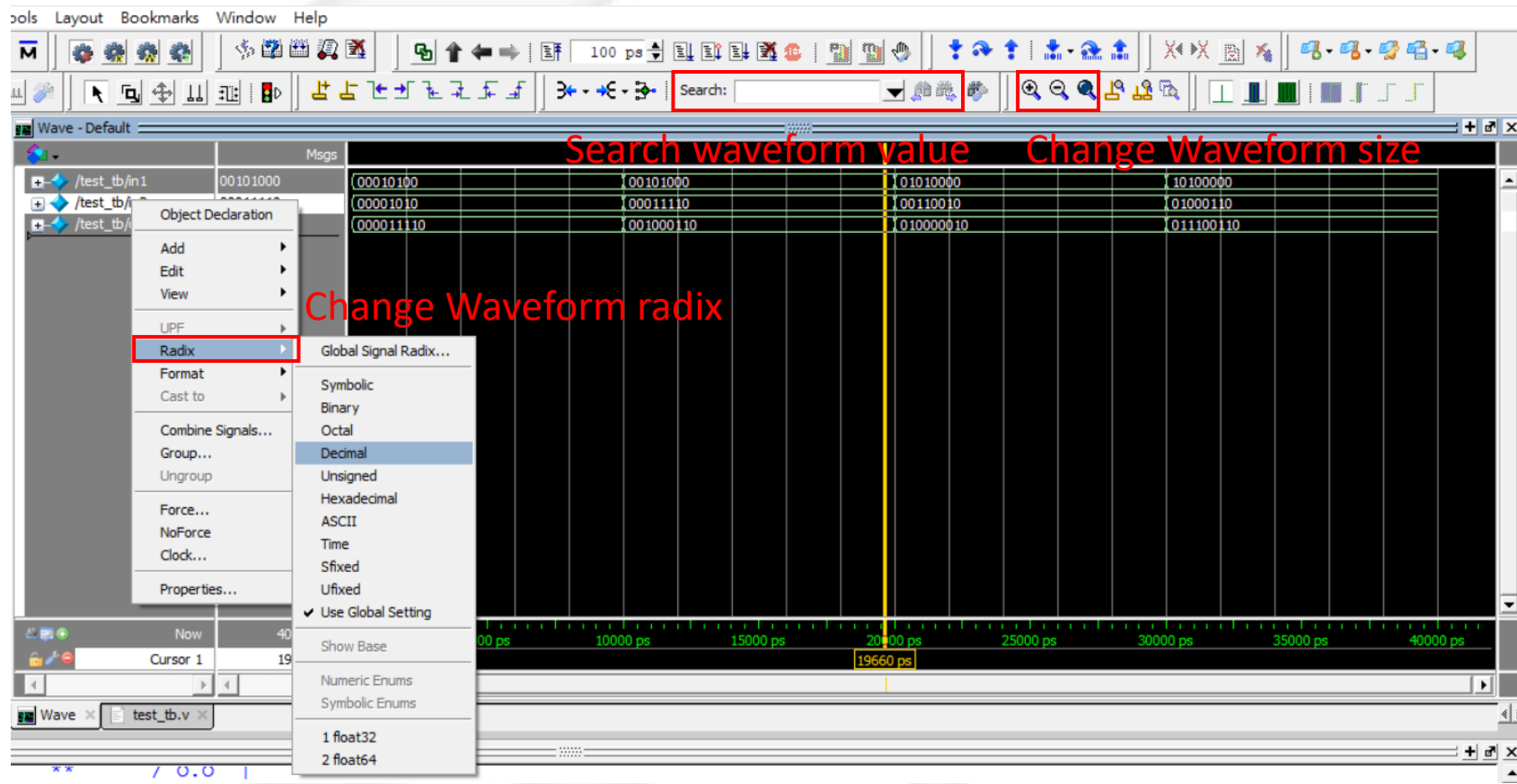
```
VSIM 32> restart
```

VSIM> restart

Remember to rerun the simulation to generate the waveform.

Debugging (2/3)

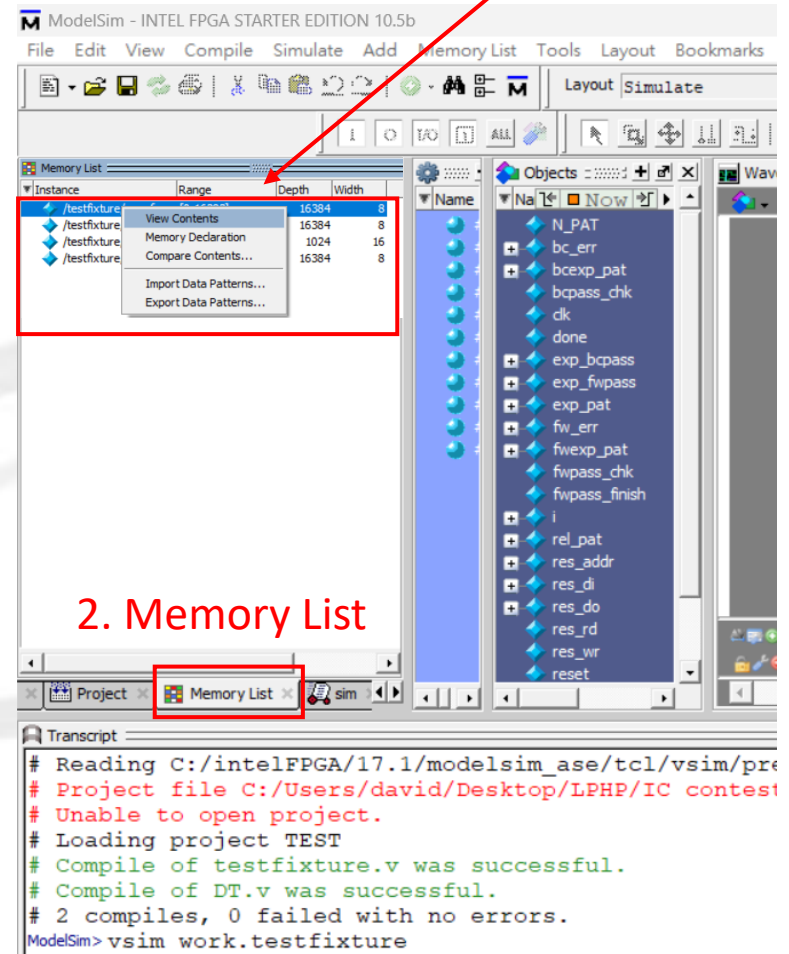
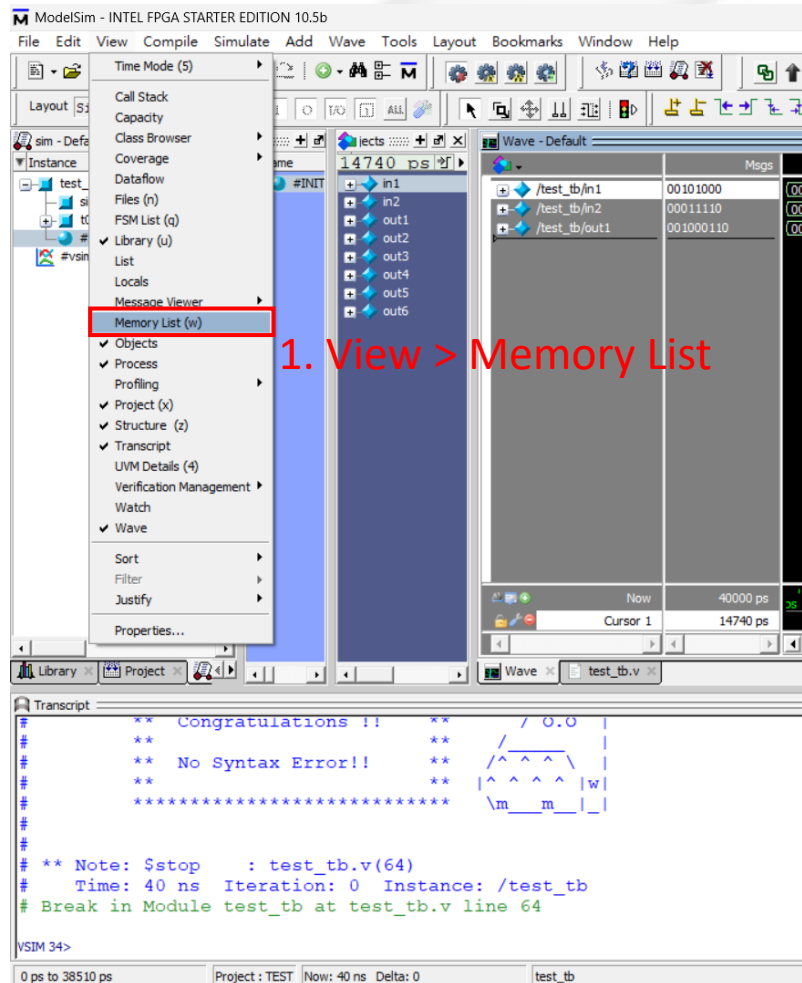
- Adjust the waveform as needed



Debugging (3/3)

Memory list

3. Choose the memory you want to visualize





Thanks for your attention !!