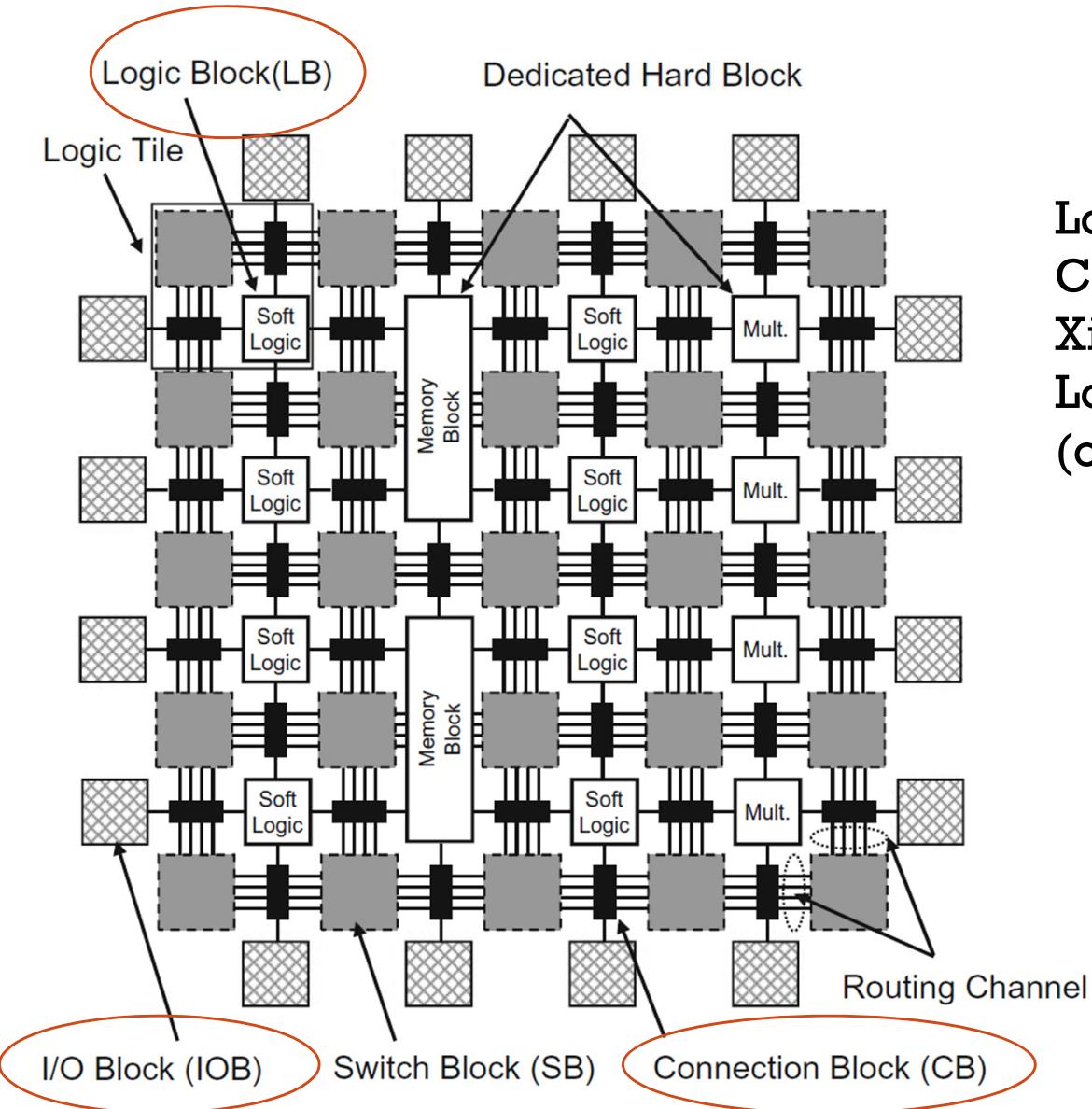


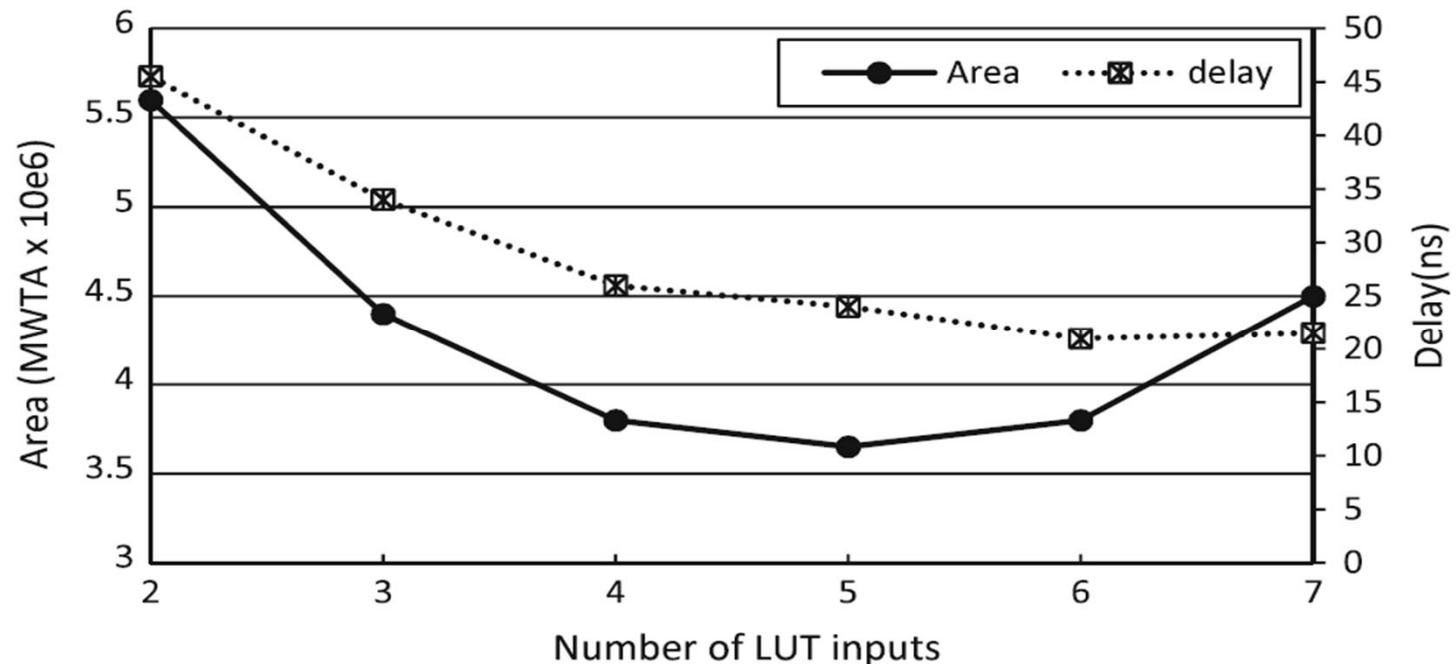
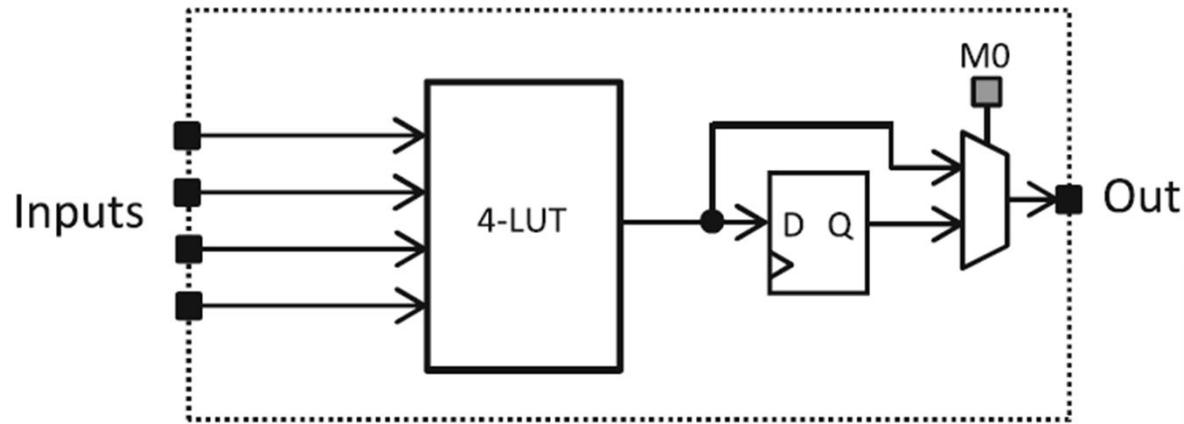
FPGA STRUCTURE: LOGIC BLOCK

ISLAND-STYLE FPGA

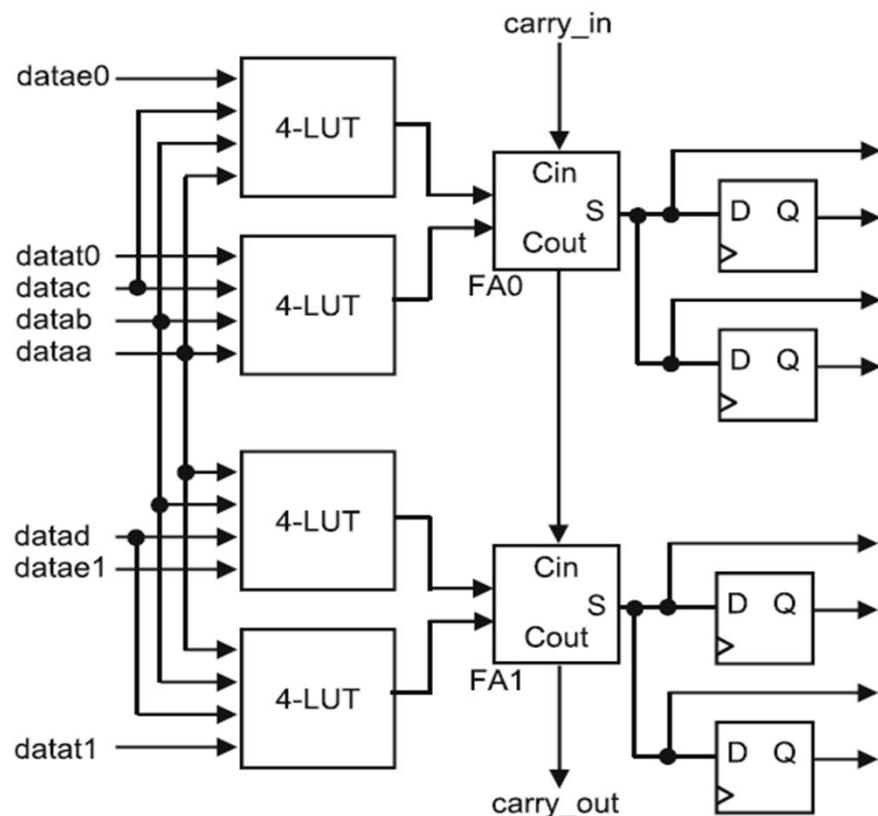


Logic Block =
Configurable Logic Block (CLB) in
Xilinx FPGA =
Logic Array Block (LAB) in Altera
(or Intel)

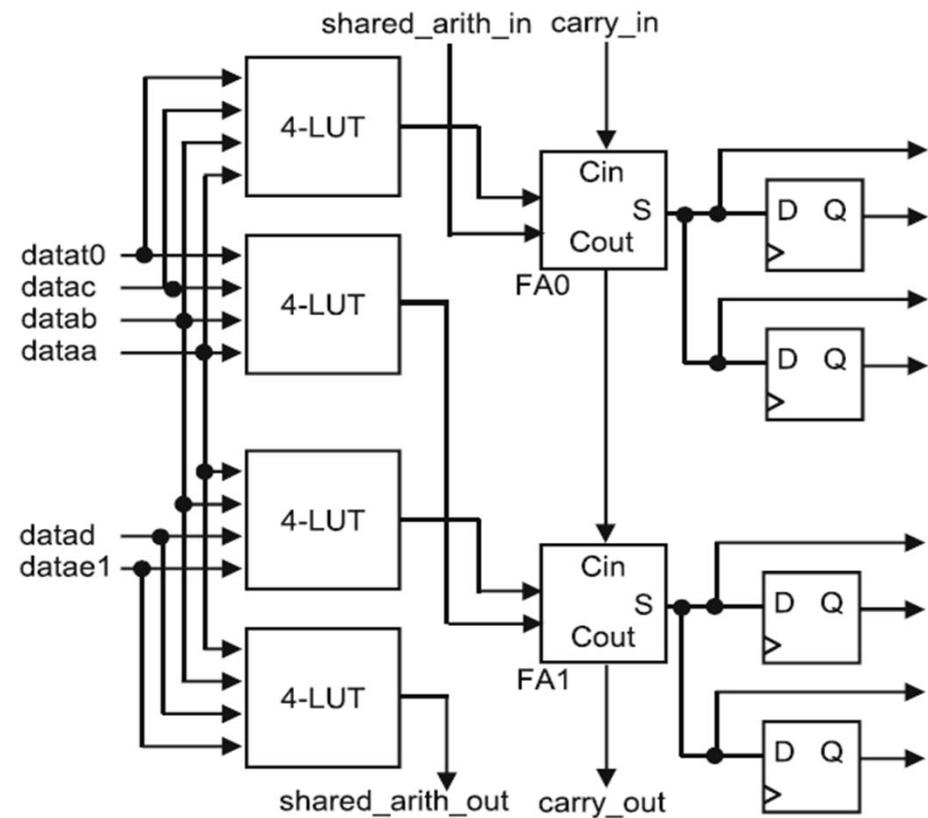
BASIC LOGIC ELEMENTS (BLES)



DEDICATED CARRY LOGIC



(a) Arithmetic Mode

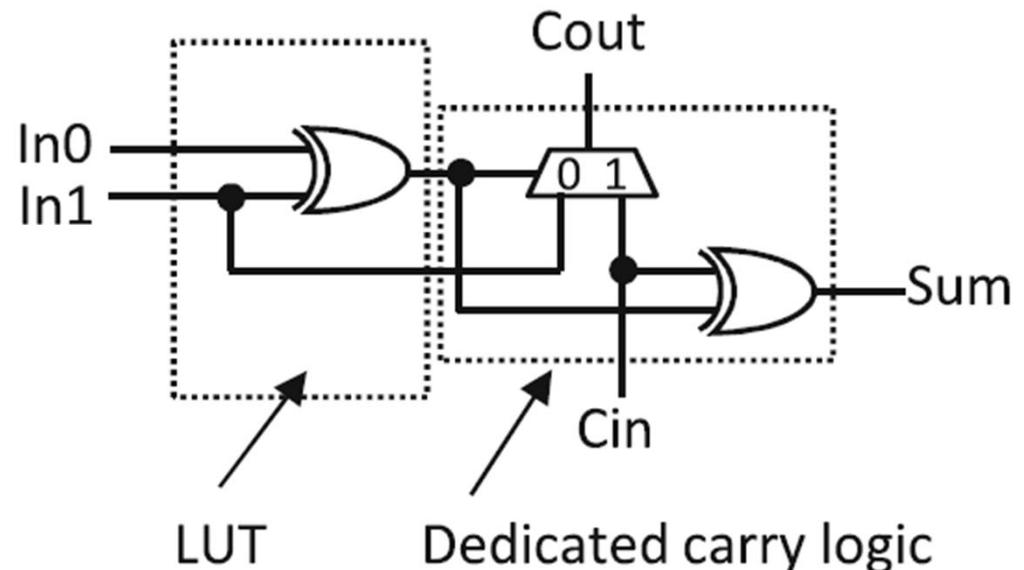


(b) Share Mode

CARRY LOGIC IN XILINX FPGA

Truth table of full adder

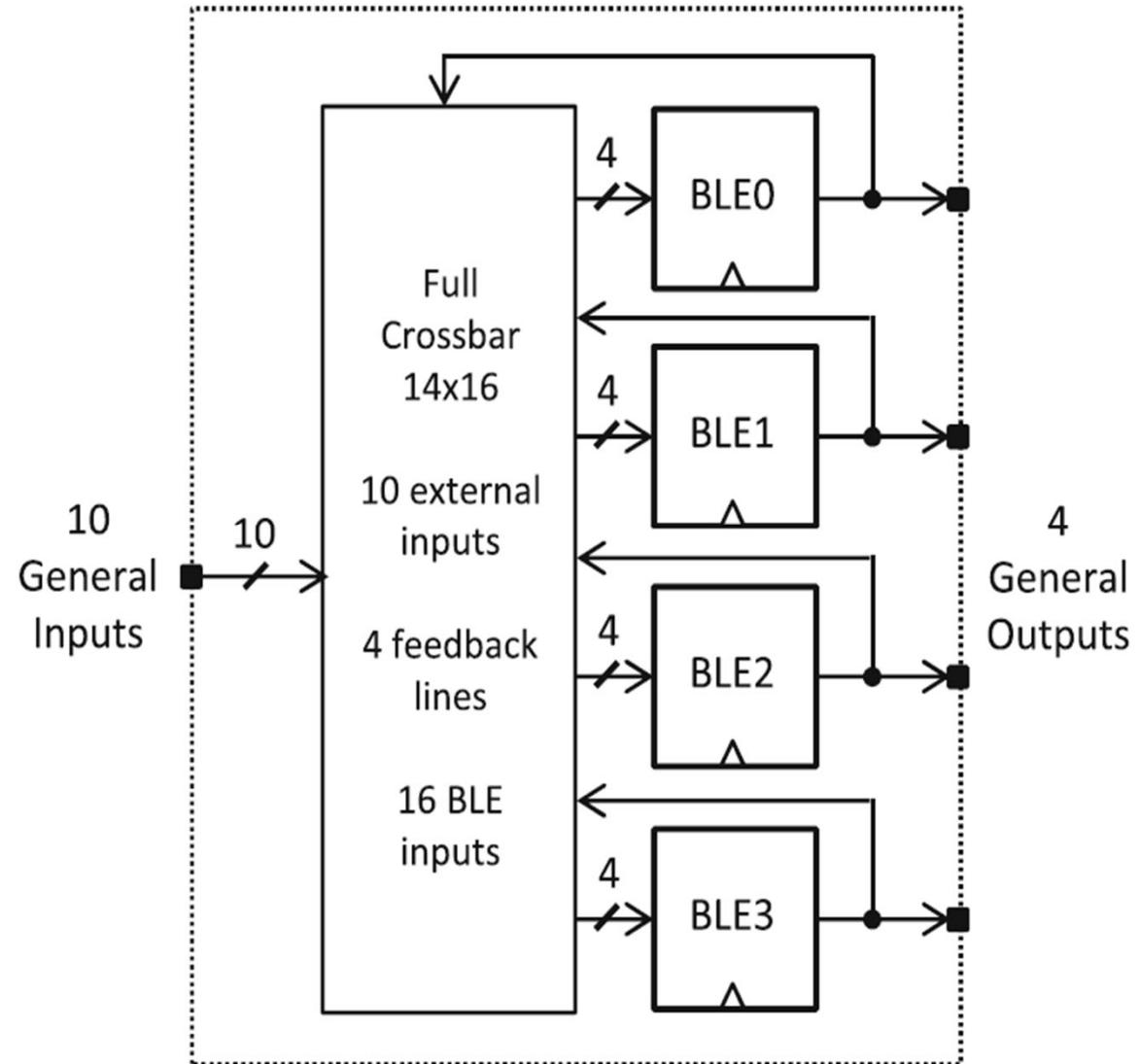
In0	In1	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



LOGIC CLUSTER

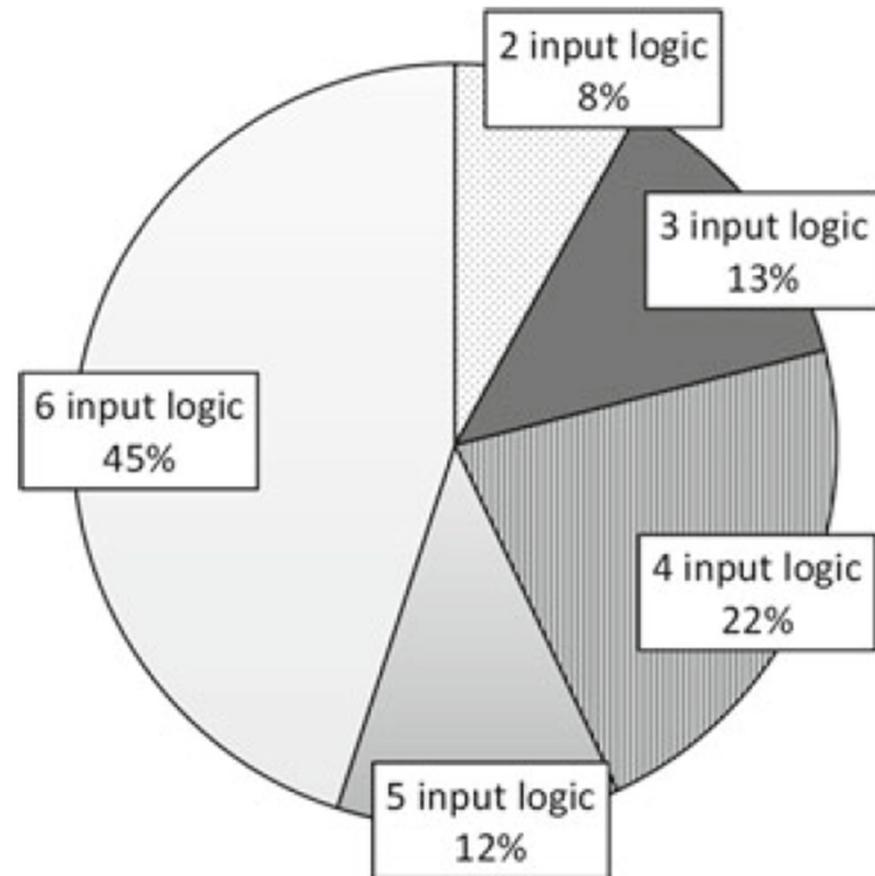
- Increase the number of functions in a logic block without increasing the number of LUT inputs

- Features
 - Faster due to local wiring (hard wires) in the logic cluster
 - Low power consumption due to low parasitic capacitance of local wiring



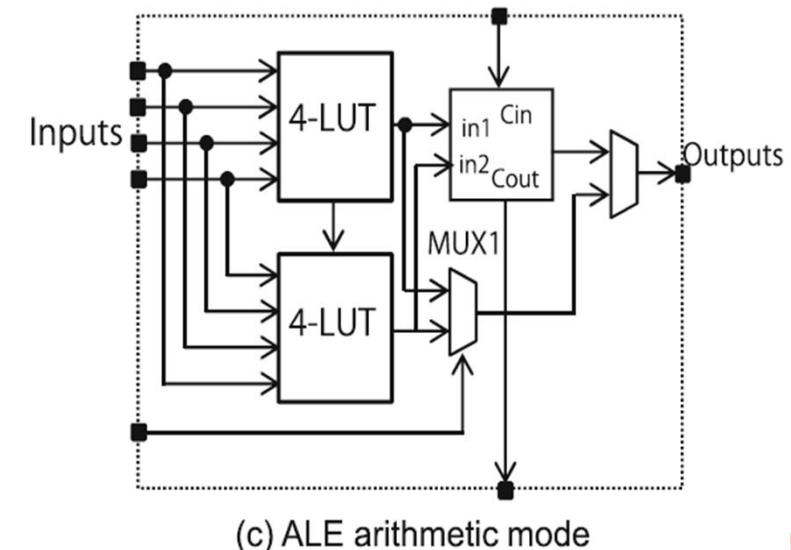
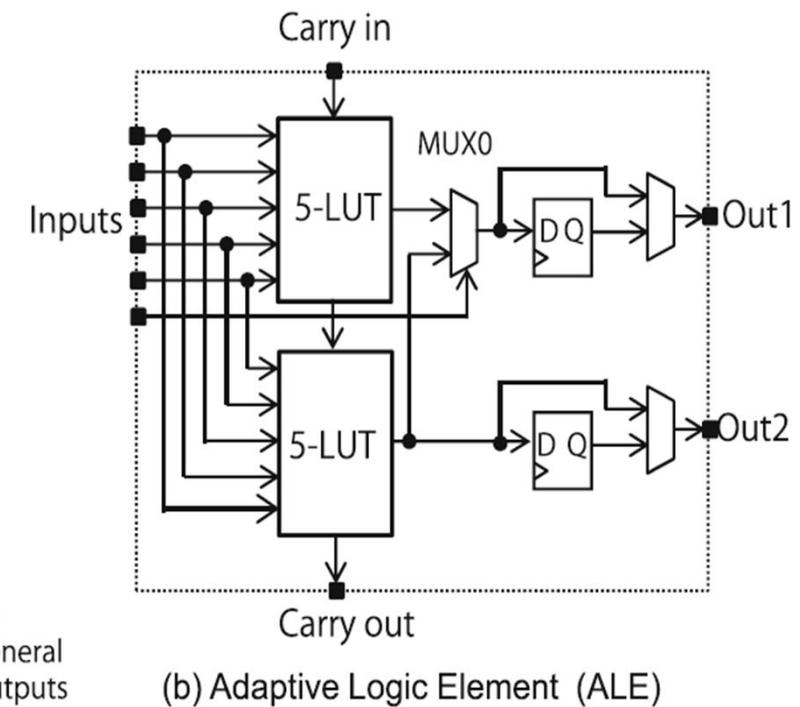
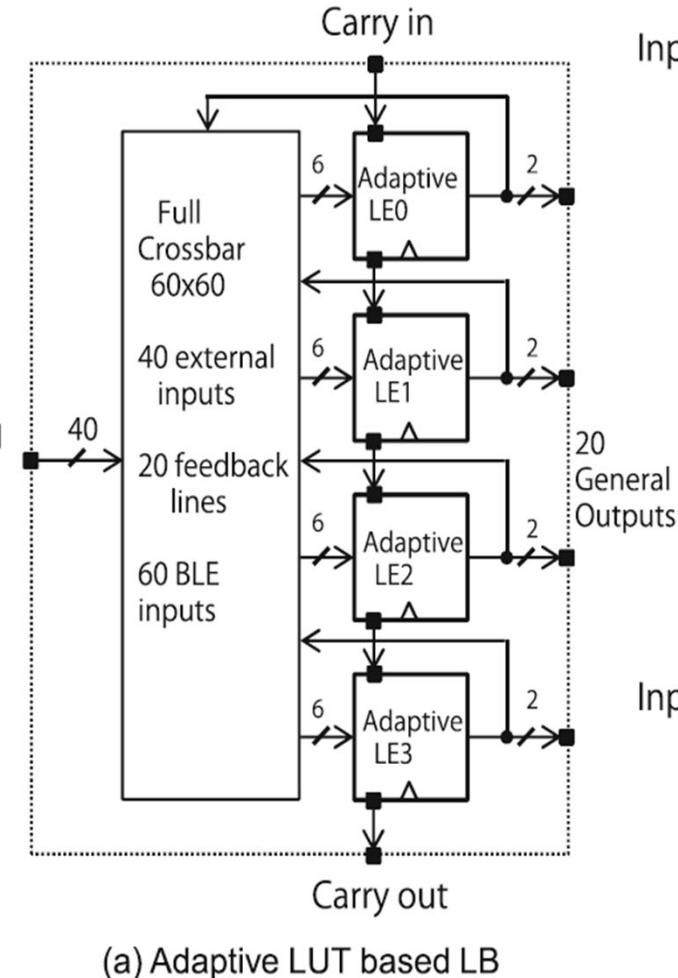
IMPLEMENTATION RATIO OF LOGIC FUNCTION AFTER TECHNOLOGY MAPPING

- 45% of the total logic function mapped as 6-input logic. Half the configuration memory bits of the 6-input LUT are not used. So did others.



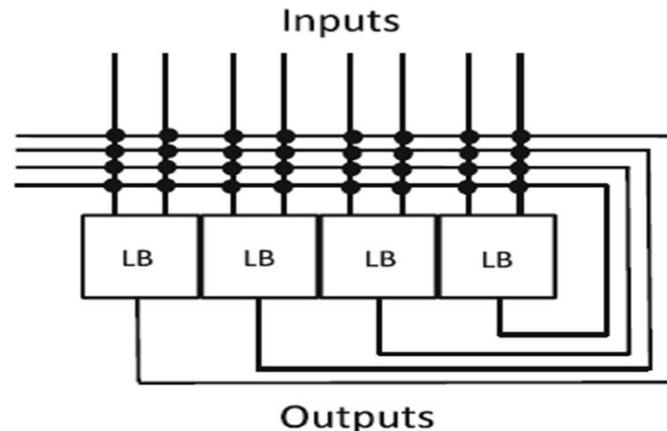
ADAPTIVE LUT BASED LB

- Adaptive Logic Element (ALE)
- Local connection block: a full crossbar of 60x60
- 2-output adaptive LUTs and FFs
- Two 5-LUTs sharing all inputs
- Operating as one 6-LUT or two 5-LUTs

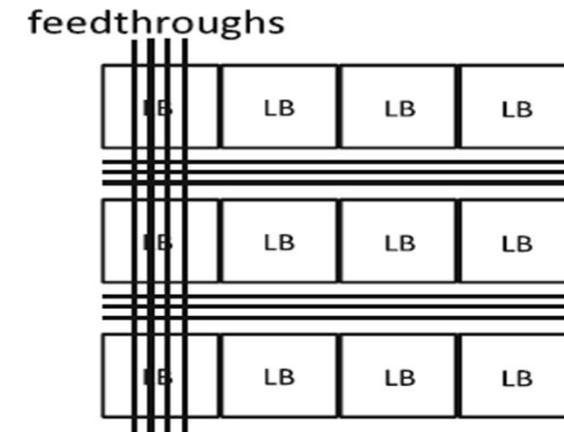


FPGA STRUCTURE: ROUTING BLOCK

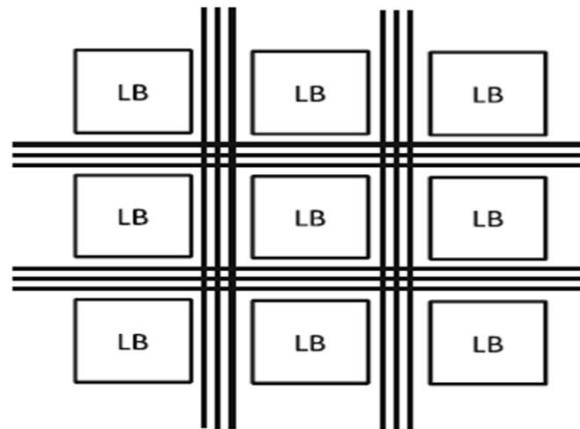
CLASSIFICATION OF FPGA GLOBAL ROUTING STRUCTURE



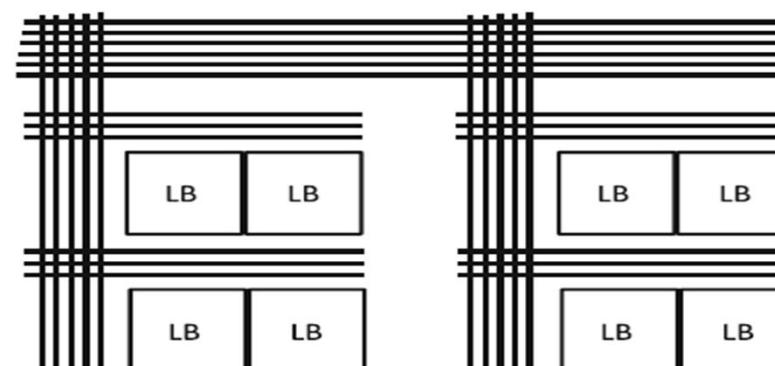
(a) Full cross bar type



(b) 1 dimensional type



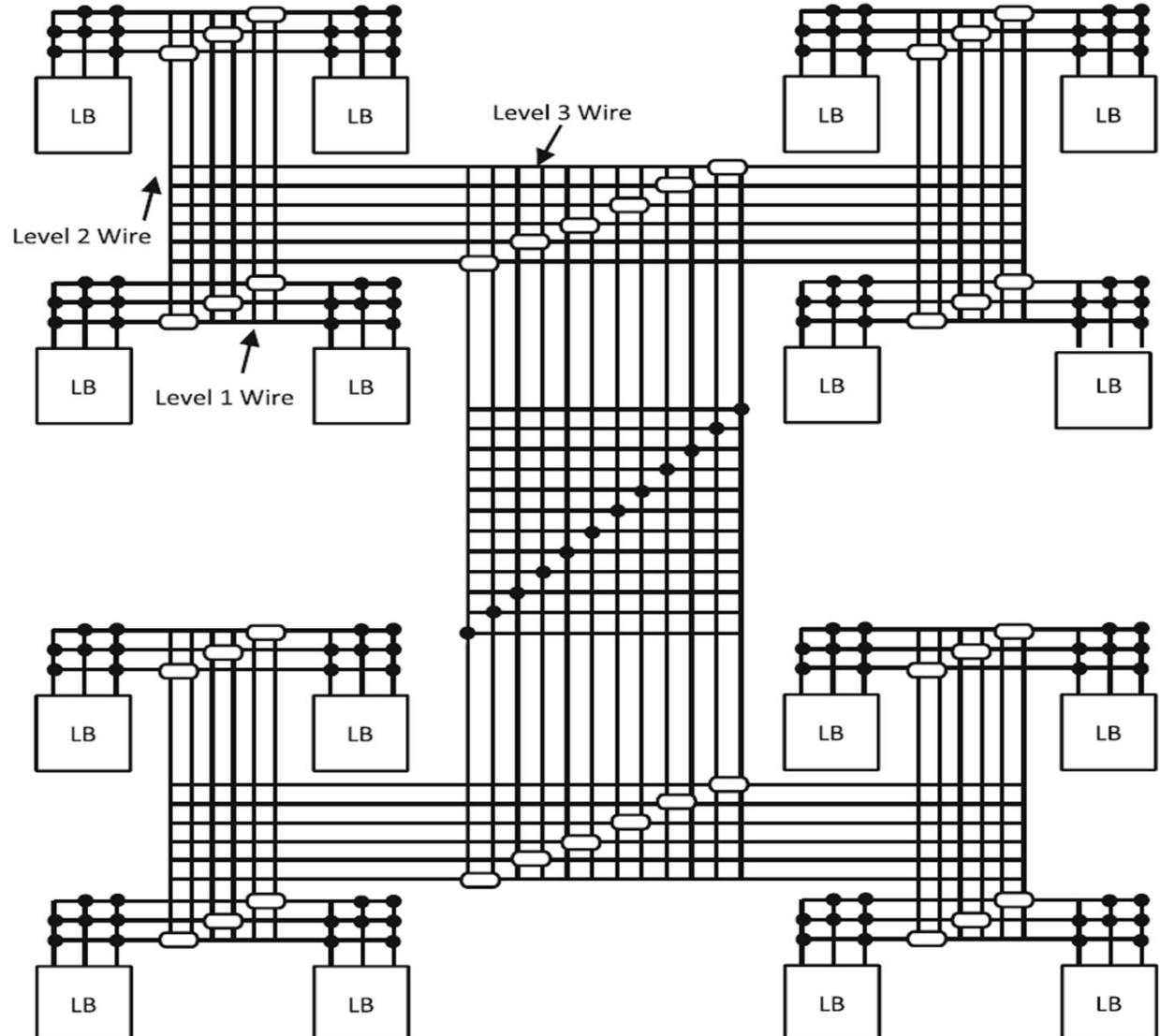
(c) 2 dimensional type
(Island style)



(d) Hierarchical type

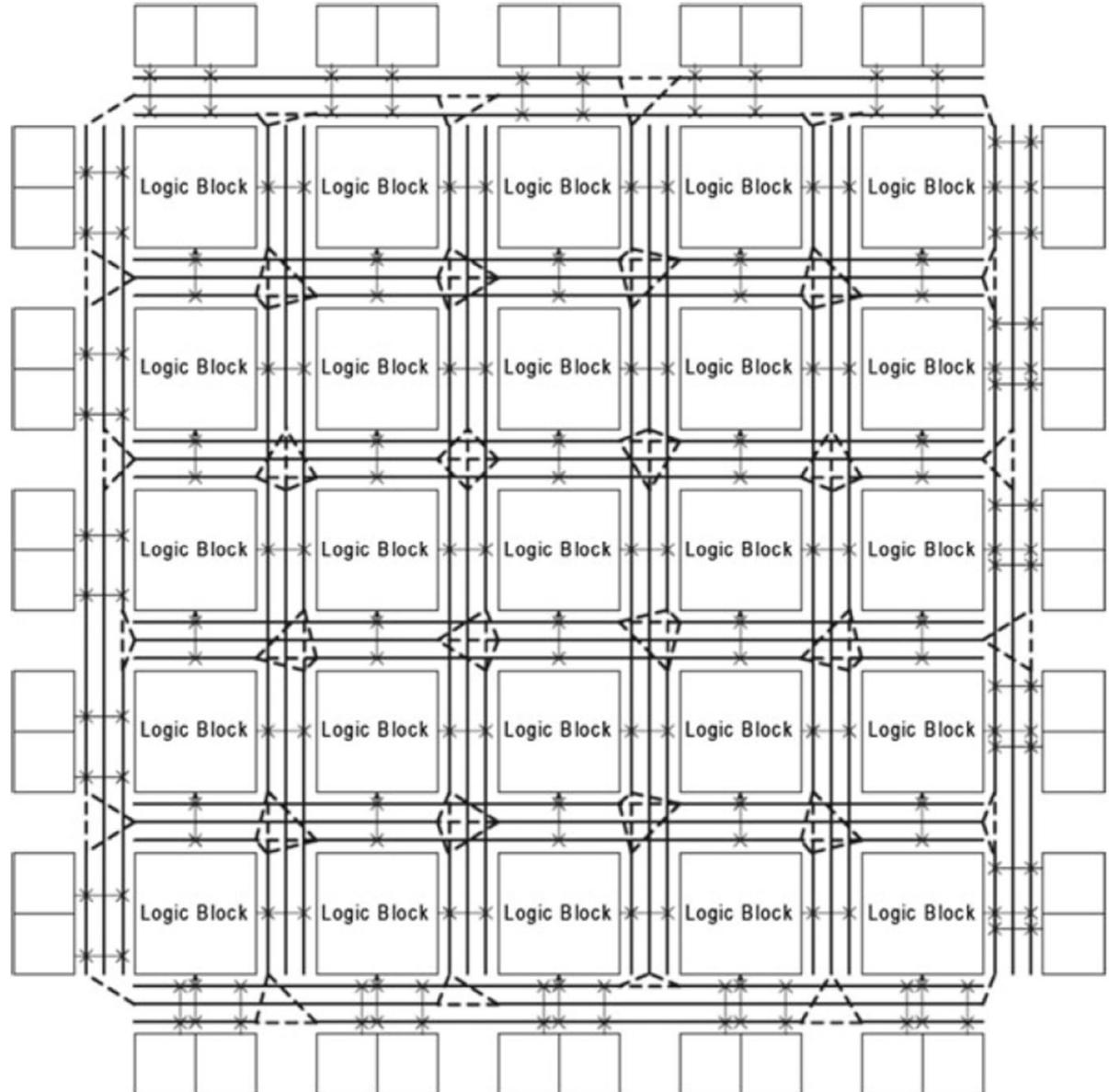
HIERARCHICAL-TYPE FPGA

- Altera Flex 10K, Apex, Apex II
- High-speed, hierarchical syn. Reconfigurable array
- Pros
 - High-speed operations when the application matches the structure
- Cons
 - Delay increases when LBs are close to each other but not connected at the same hierarchy

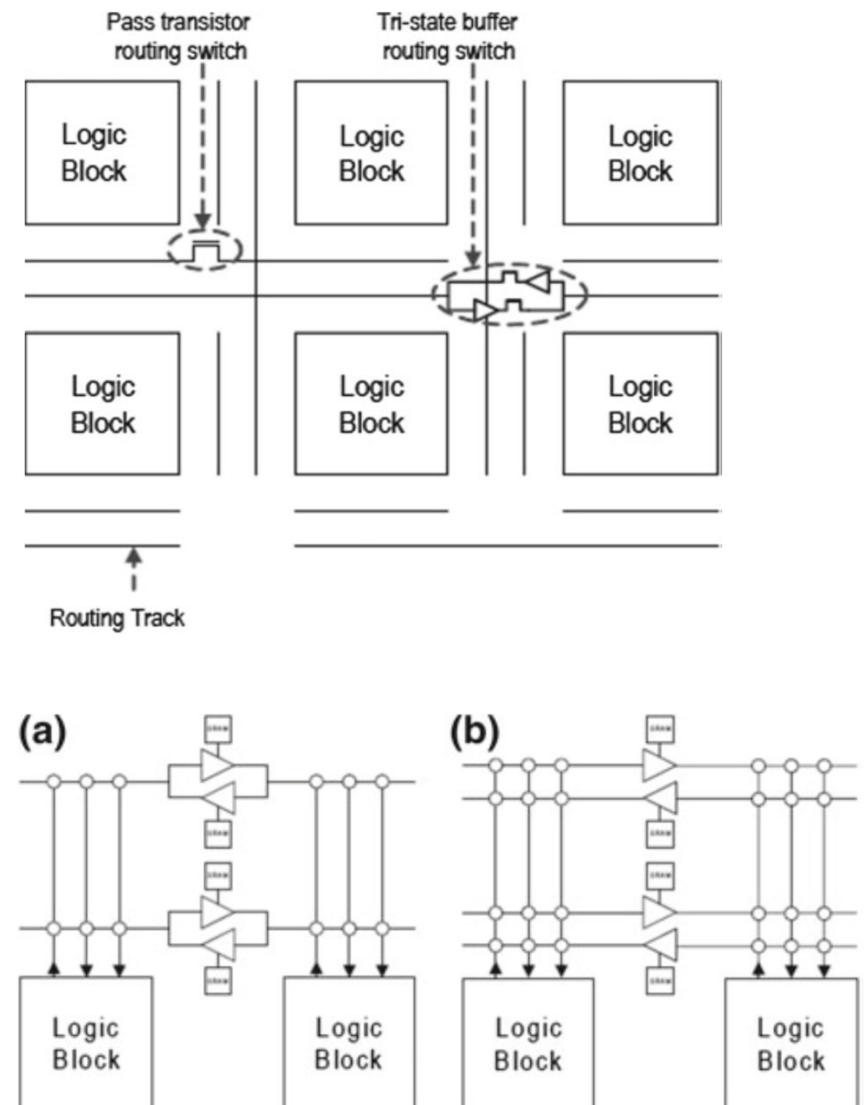
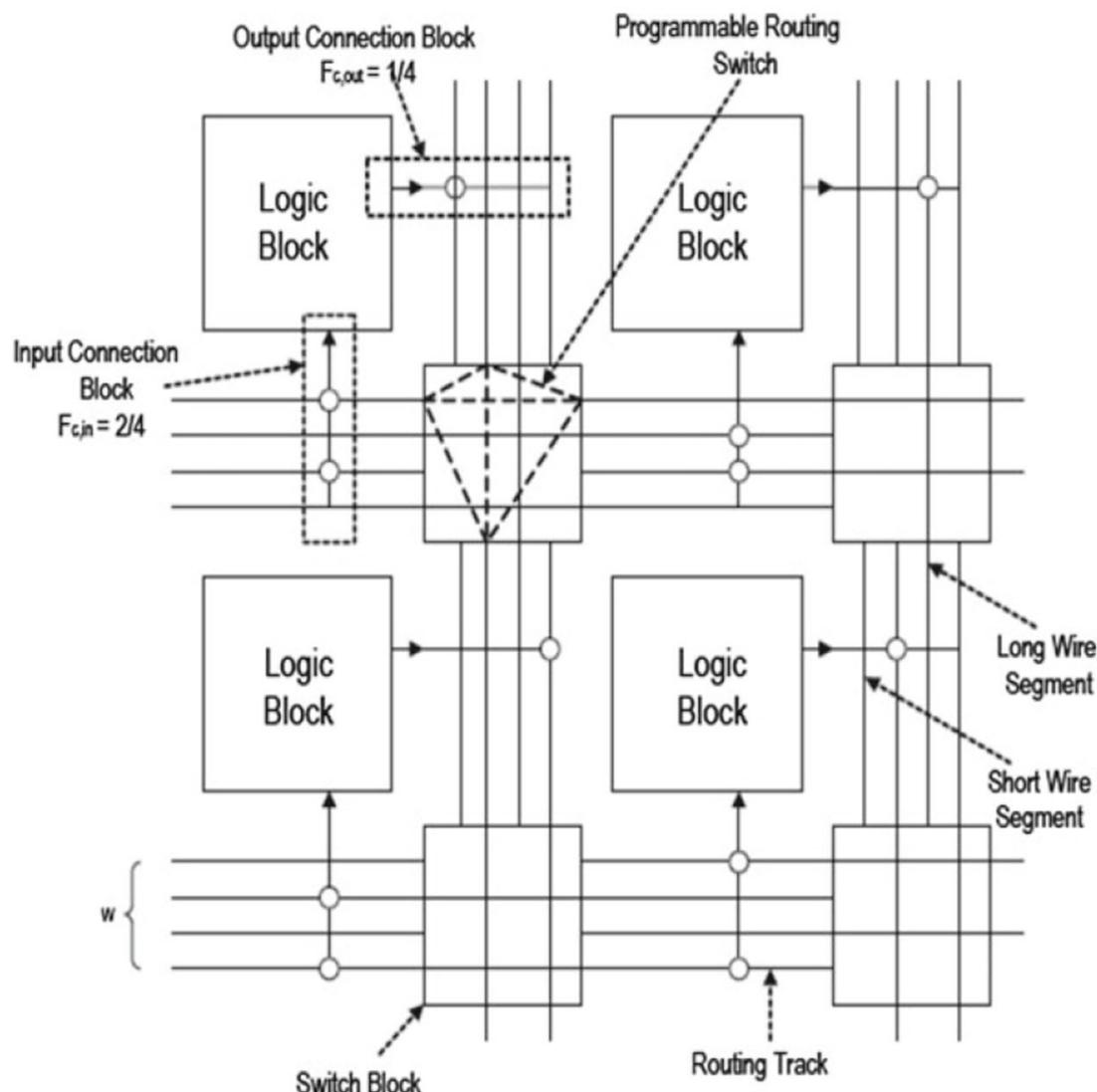


ISLAND-STYLE FPGA

- Adopted by most FPGAs in recent years
- Pros
 - Connections between LBs and RBs are generally two-pointed or four-pointed.
 - Uniformization of the logic tiles, the execution time of the routing process can be reduced.



DETAILED ROUTING ARCHITECTURE



SWITCH BLOCK

▪ Disjoint (Xilinx) Type

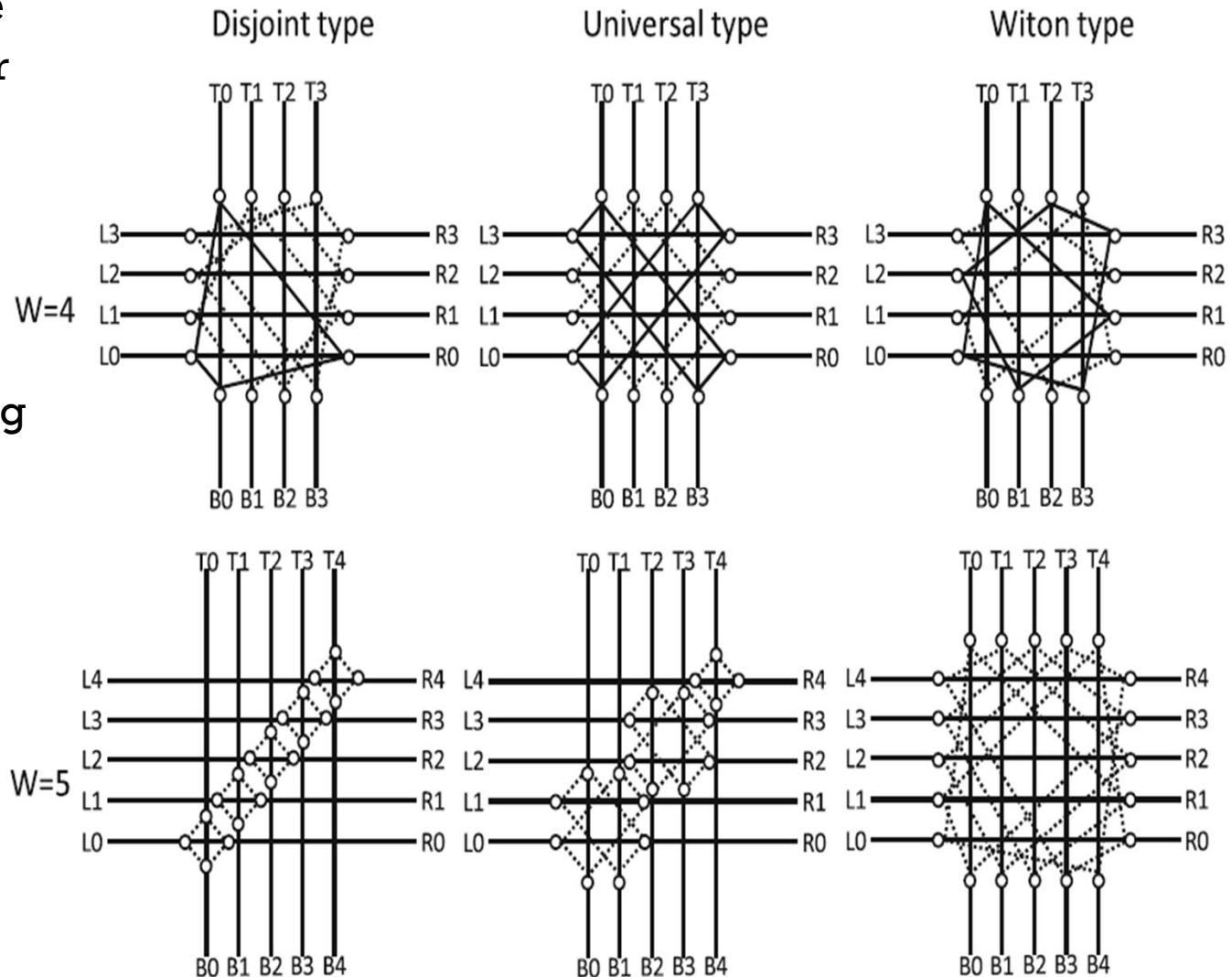
- Require a small number of switches
- Low flexibility

▪ Universal Type

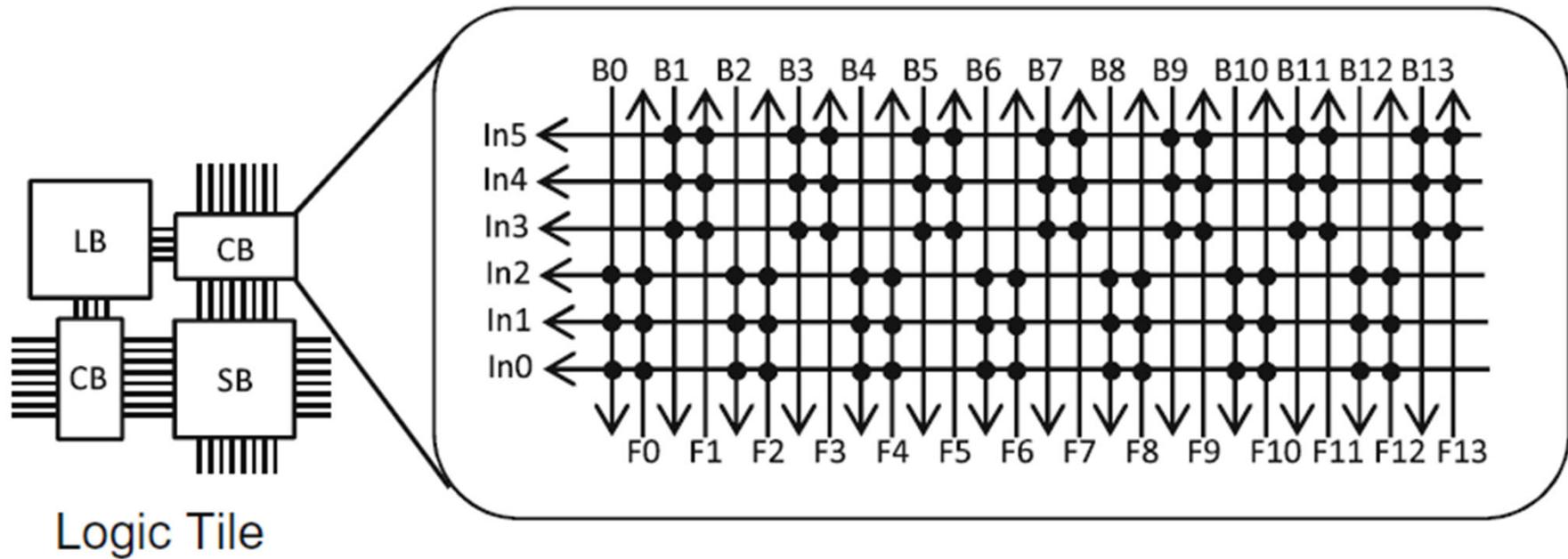
- Middle flexibility among three

▪ Wilton Type

- Higher flexibility than the other two
- More efficiency of manufacturing test of

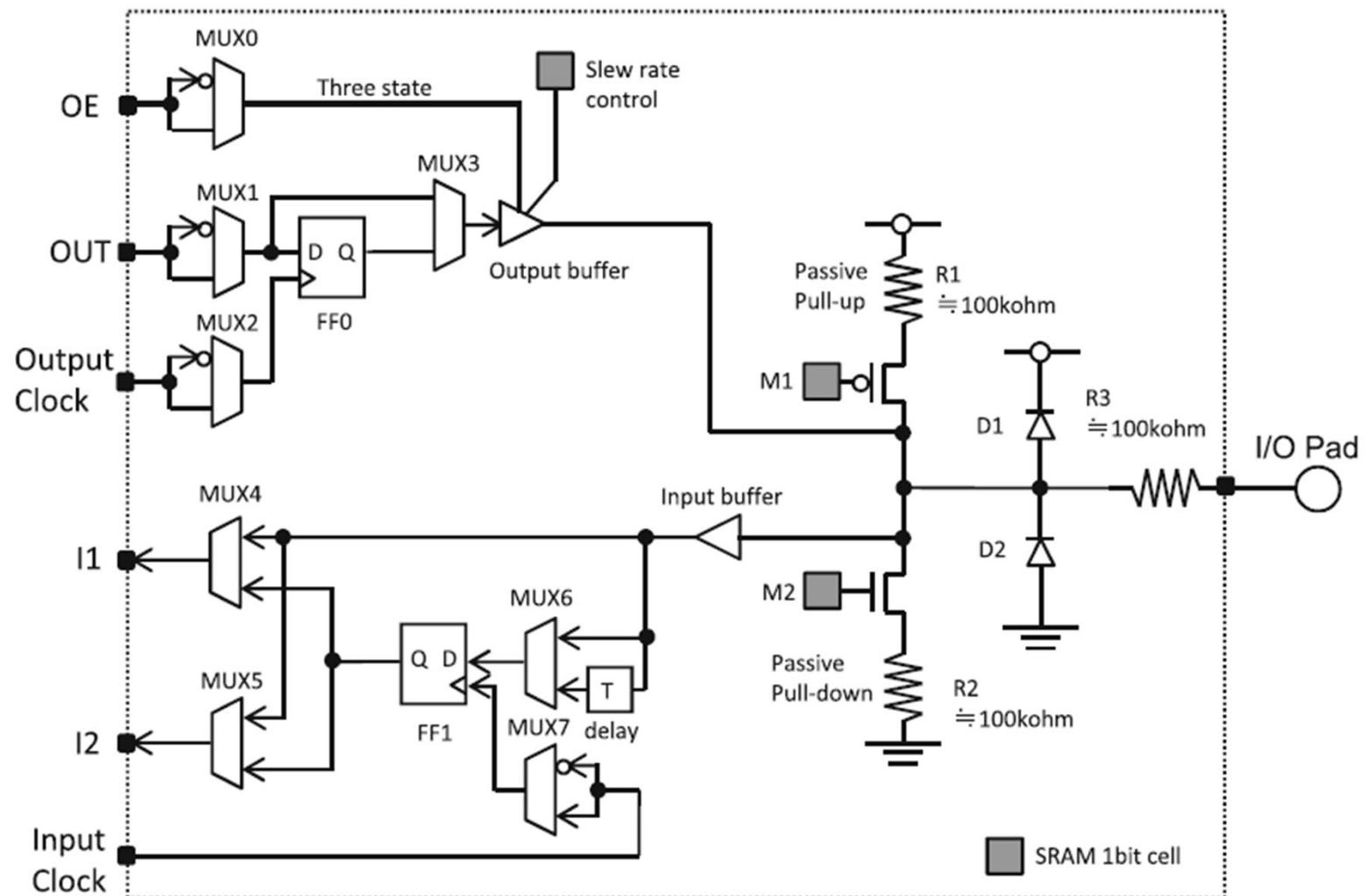


CONNECTION BLOCK

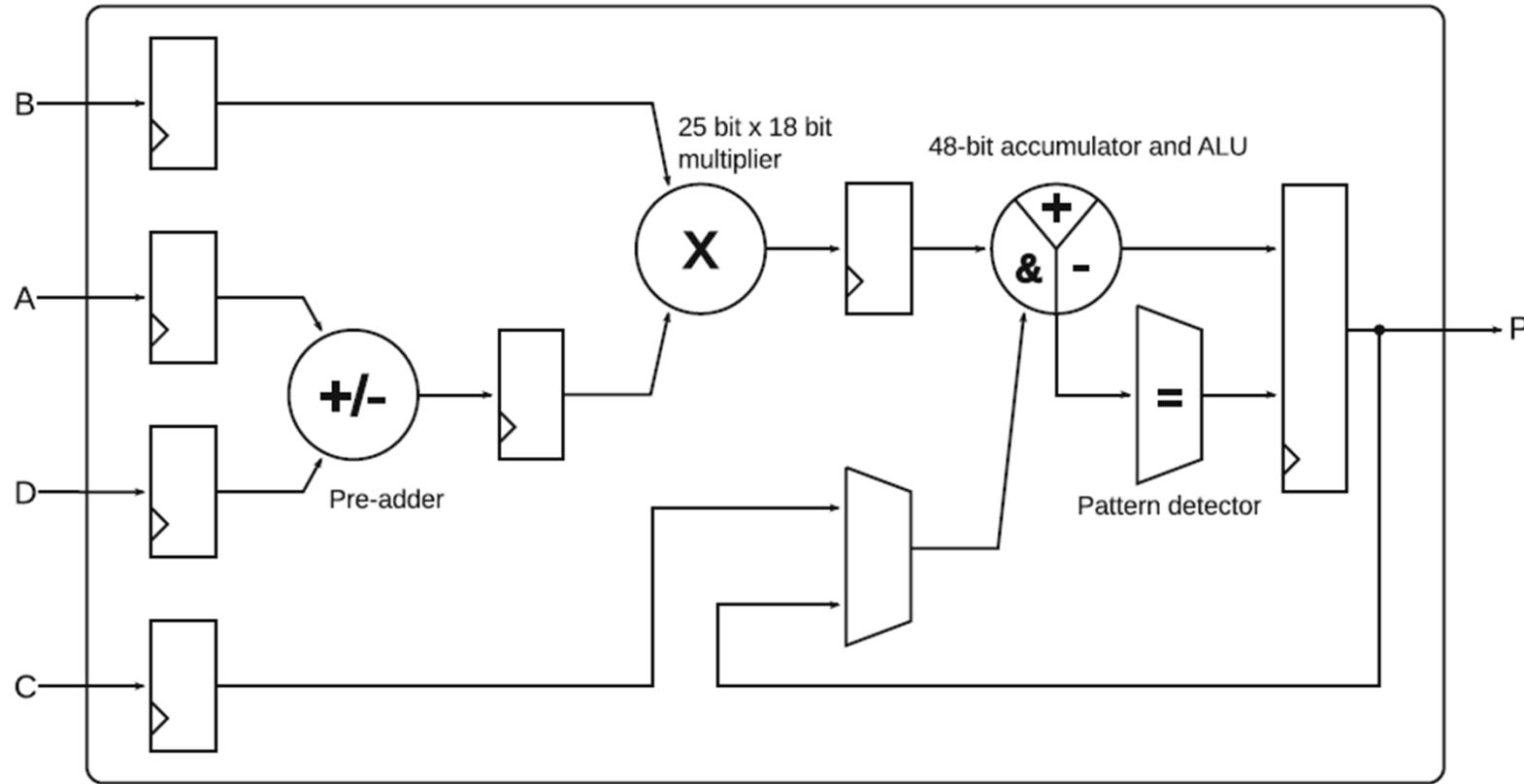


- Connecting the input and output of the routing channel and the logic block
 - Very large in the number of routing channel width
 - Use sparse crossbars with unidirectional wires

I/O BLOCK

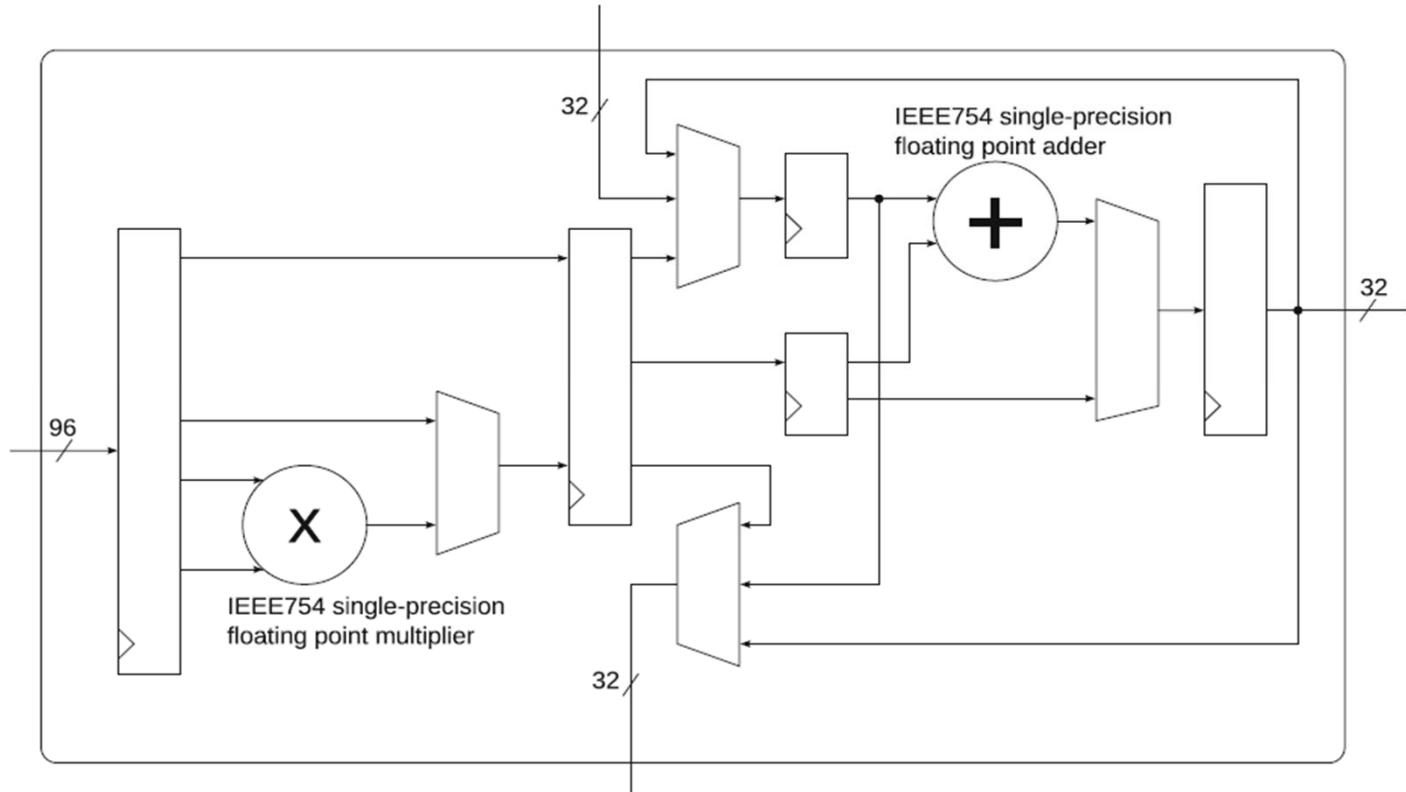


DSP BLOCK (XILINX)



- Xilinx 7-series architecture
- $Y \leftarrow A \times B + Y$

DSP BLOCK (ALTERA)



- IEEE Single-precision floating point multiplier
- $Y \leftarrow A \times B + Y$