HARDWARE DESCRIPTION LANGUAGE FOR DIGITAL DESIGN

數位設計硬體描述語言

Overview

NCKU EE
LPHP Lab

INSTRUCTOR & TEACHING ASSISTANTS

Instructor Name: 邱瀝毅 **(Lih-yih Chiou)**

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Room: EE95316

Office hours: Monday 7:00 pm-9:00 pm

Course website: http://moodle.ncku.edu.tw

Moodle for class announcements, materials, lab submissions, and Q&A.

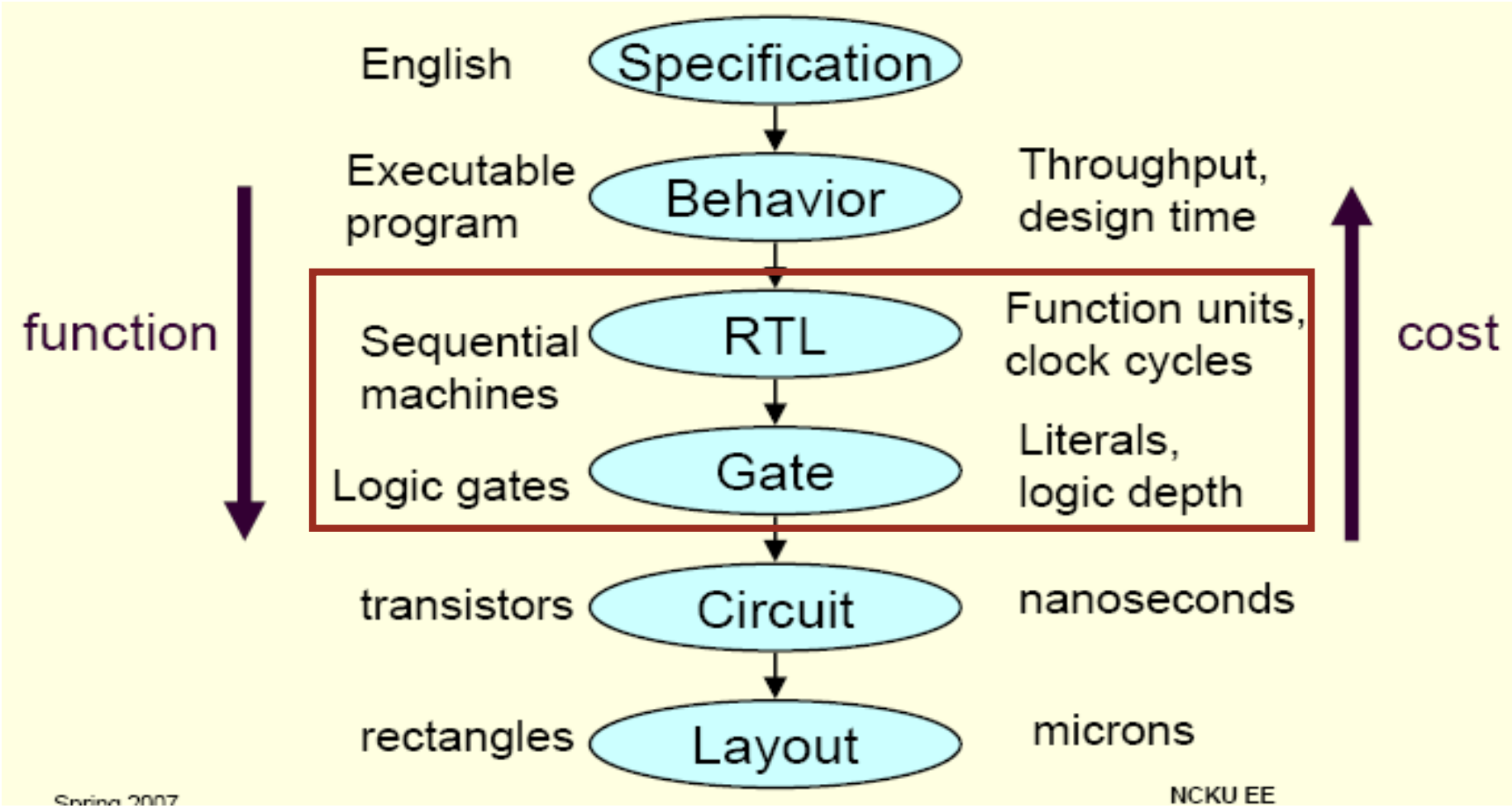
COURSE PREREQUISITES AND MATERIALS

- **Course Prerequisites**
  - Digital Logic Design (MUST).
  - Computer Organization (MUST)
  - Entry-level HDL coding, at least 500 lines and above (MUST)
  - A notebook that you can work on during class hours (MUST).
- **Materials**
  - Lecture notes/Lab manuals are on the course website.
  - *Reference books:*
    - "Digital System Designs and Practices," Ming-Bo Lin, Wiley, 2008. ISBN: 978-0-470-82323-1.
    - "Principles and Structures of FPGAs," Editor Hideharu Amano, Springer, 2018. ISBN: 978-981-13-0824-6 (eBook). Available in the library of NCKU.

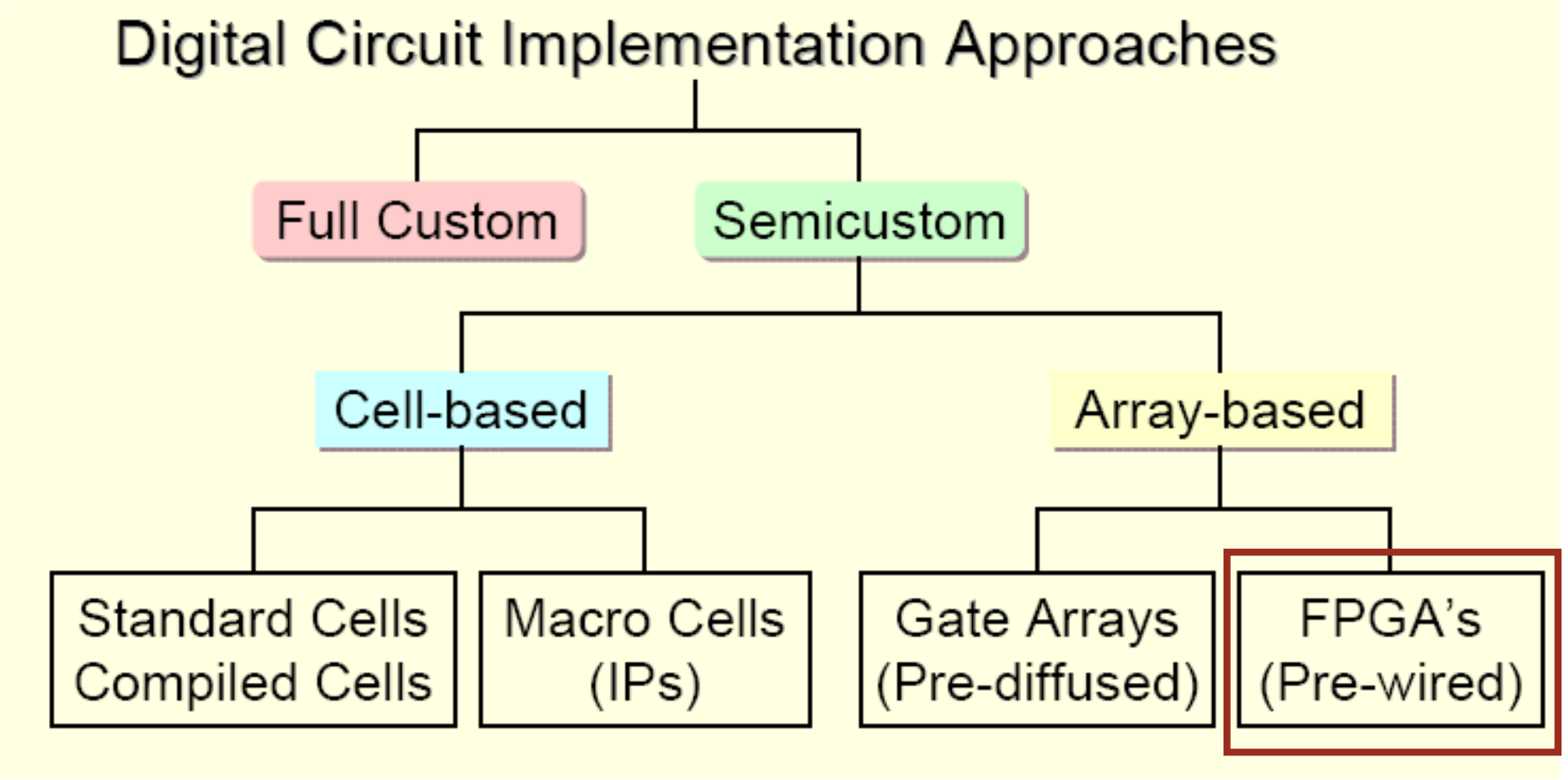
WHAT IS THE COURSE ALL ABOUT?

- This course covers modern digital system design fundamentals and provides an in-depth understanding of hardware description language. The learners will be required to use their learned knowledge to complete design challenging problems and demonstrate their learned skills in realizing digital design.
- Note that the course is designed for fresh graduate students or last-year undergraduates to know how to apply digital design to their fields; it is not intended for cell-based IC design students.
- You will learn
  - **Fundamentals of HDL and FPGAs**
  - **Compilation/Simulation Tools for HDL**
  - **FPGA Structure, Design Flow, and Tools**
  - **Applications in industrial designs**

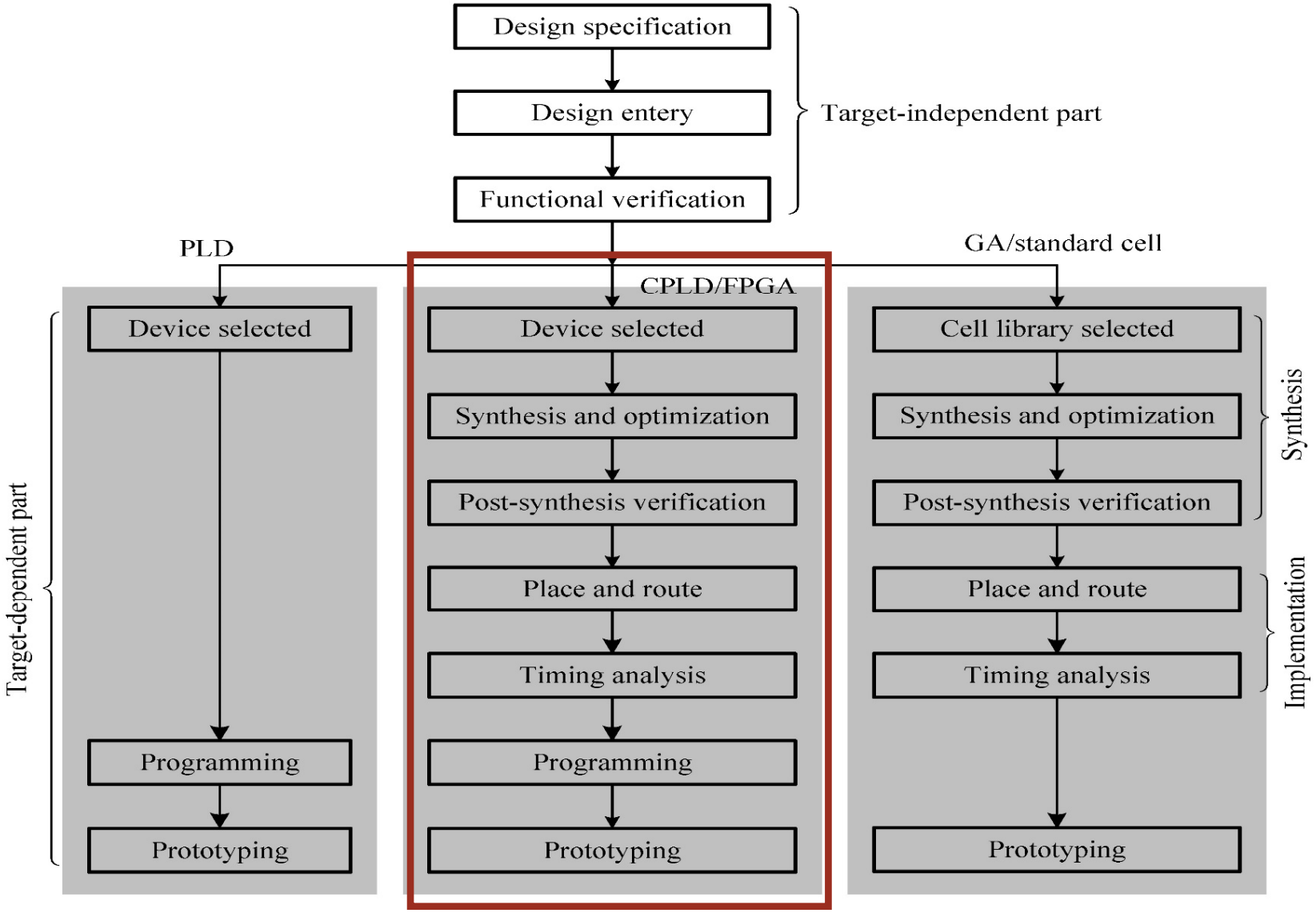
TARGET LEVELS OF DESIGN ABSTRACTIONS



TARGET DIGITAL DESIGN IMPLEMENTATION



HDL-BASED DESIGN FLOW



Adapted from "Digital System Designs and Practices Using Verilog HDL and FPGAs," M.B. Lin

OUTLINE

- Course Overview (1 week)
- Basic HDL (9 weeks)
  - Digital design flow
  - Gate and Behavioral Models
  - Finite-State Machine and Controller
  - Machines with Multicycle and Pipeline operations
- HDL on FPGAs (8 weeks)
  - FPGA Structure, Design flow, and Tools
  - Design Methodology
  - Optimize Microarchitecture for Programmable Gate Arrays
- Design Challenges (3 beginner, 4 Intermediate, and 7 Advanced Problems)

COURSE HOURS & ARRANGEMENT

- Day and Time:
  - Wednesday 3:10 pm - 6:00 pm
- Lecture and Laboratory hours (tentatively)
  - Part I: 50% lecturing and 50% in-class lab
  - Part II: 1-hr lecturing and 2-hr in-class lab
- Location:
  - Lecture:
    1. iLadder Rm (EE96112) @ChiDuan Build. 1st Floor Intelligent Ladder Room and
    2. AIT Rm (EE92119) @EE Build. 1st Floor ATI Room (Live Streaming)

HOMEWORK ASSIGNMENTS

- Take-home Problems: nearly every week except holidays, examines, and projects throughout the semester.
- Due day and deliverable will be specified in the homework handouts (usually due next week before Lab hours).
- All submissions must be made electronically through the course website before the specified deadline; submissions otherwise will not be graded. Failure to deliver on time will result in your assignment being considered **OVERDUE**. The credit reduction for late submissions is as follows:
  - Within 24 hours: **40% deduction of graded score**
  - Within 48 hours: **60% deduction of graded score**
  - Within 72 hours: **90% deduction of graded score**
  - After 72 hours: **100% deduction of graded score**
- Remember to submit your assignments on time to avoid any penalties!

GRADING AND COURSE POLICY

- **Grading Weights on Course Activities**
  - Class participation 5~10%
  - Lab assignments, Midterm Exam, and Design Challenges 90~95%
  - For advanced design challenges, the grading will be based on correctness, quality based on metrics, the order of submission, etc.
- **Course Policy**
  - Encourage to discuss homework problems with peers.
  - Must complete his/her homework independently or as specified.
- **Avoid academic misconduct**
  - Any person found to be dishonest in homework assignments, examinations, or reports, the involved person(s) will receive a zero on the evaluated instrument.
  - Unauthorized access to other people's work through third parties or unauthorized means is strictly prohibited. Those found engaging in such misconduct will face additional penalties, resulting in a deduction of **at least 50%** from their original assigned score (倒扣至少該作業原始配分的50%).

FOR THOSE ALREADY LISTED IN THE MOODLE

- To better know students' backgrounds, please fill in the information as specified.

- Please follow the link sent to you via the Moodle email list.

ATTENTION

- Confirm syllabus acknowledgment (教學課綱閱讀確認) in the "Important Announcement" on *Moodle*.
- Fill in students' **background survey** online.
- Please **submit your head photo** so I can get to know you.
- All three things need to be done **by 3/07**.

FOR THOSE WANT TO ENROLL THIS COURSE

- Before filling out the application form, please ensure you can log in to your Google account.
- Please follow the QR code link to fill in the information.
- Submit the form to add to the application list. The instructor will review the applicant's background and make a decision.

QR code. Enrollment Application to HDL