HARDWARE DESCRIPTION LANGUAGE FOR DIGITAL DESIGN

數位設計硬體描述語言

FPGA (II)

Materials partly adapted from "Principles and Structures of FPGAs," Hideharu Amano Editor.

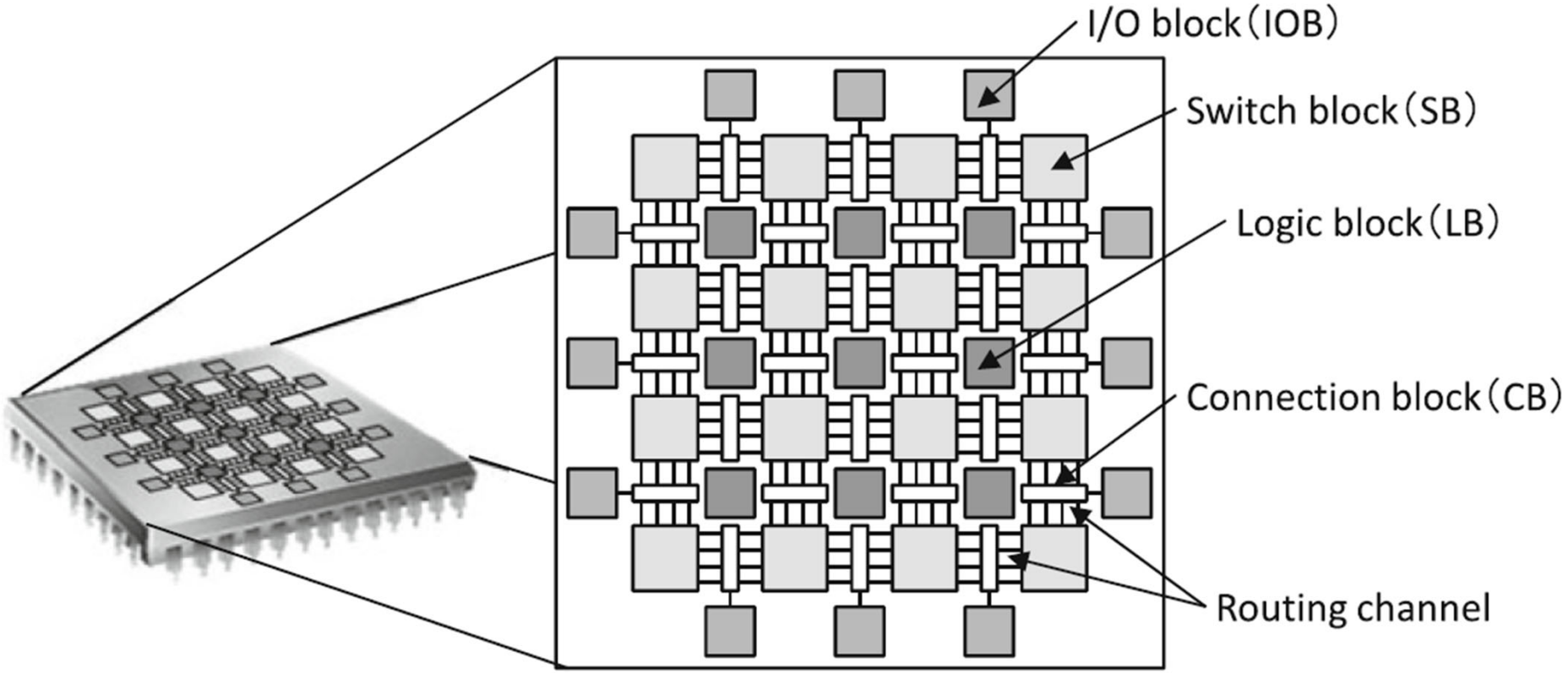
NCKU EE
LPHP Lab

OUTLINE

- FPGA Quick Review
- Example Implemented on FPGA
- FPGA Structure
- Design Flow and Design Tools
- Design Methodology
- Hardware Algorithms

FPGA QUICK REVIEW

OVERVIEW OF A TYPICAL ISLAND-STYLE FPGA



MAJOR BLOCKS

- Logic Element Schemes
  - Lookup Table (LUT)
  - Multiplexer (MUX)
  - Generic Array Logic (GAL)
- Input/Output Element
  - Connect I/O pins and internal wiring elements
- Wiring Element
  - Wiring channels
  - Connection blocks (CB)
  - Switch blocks (SB)

PROGRAMMING TECHNOLOGY

- The circuit on FPGA is controlled by a programmable switch.
- Possible semiconductor technologies
  - EPROM
  - EEPROM
  - Flash memory
  - Antifuse
  - Static memory (SRAM). Its strong point is "*being able to use COMS advanced process.*"

FEATURE COMPARISON OF PROGRAMMING TECHNOLOGY

	Flash memory	Antifuse	Static memory
Nonvolatile	Yes	Yes	No
Reconfigurability	Yes	No	Yes
Memory area	Mid (1 Tr.)	Small (none)	Large (6 Tr.)
Process Tech.	FLASH process	CMOS process+Antifuse	CMOS process
ISP[a]	Available	None	Available
Switch resistance (Ω)	500–1,000	20–100	500–1,000
Switch capacitance (fF)	1–2	<1	1–2
Programing yield (%)	100	>90	100
Lifetime	10,000	1	Infinity

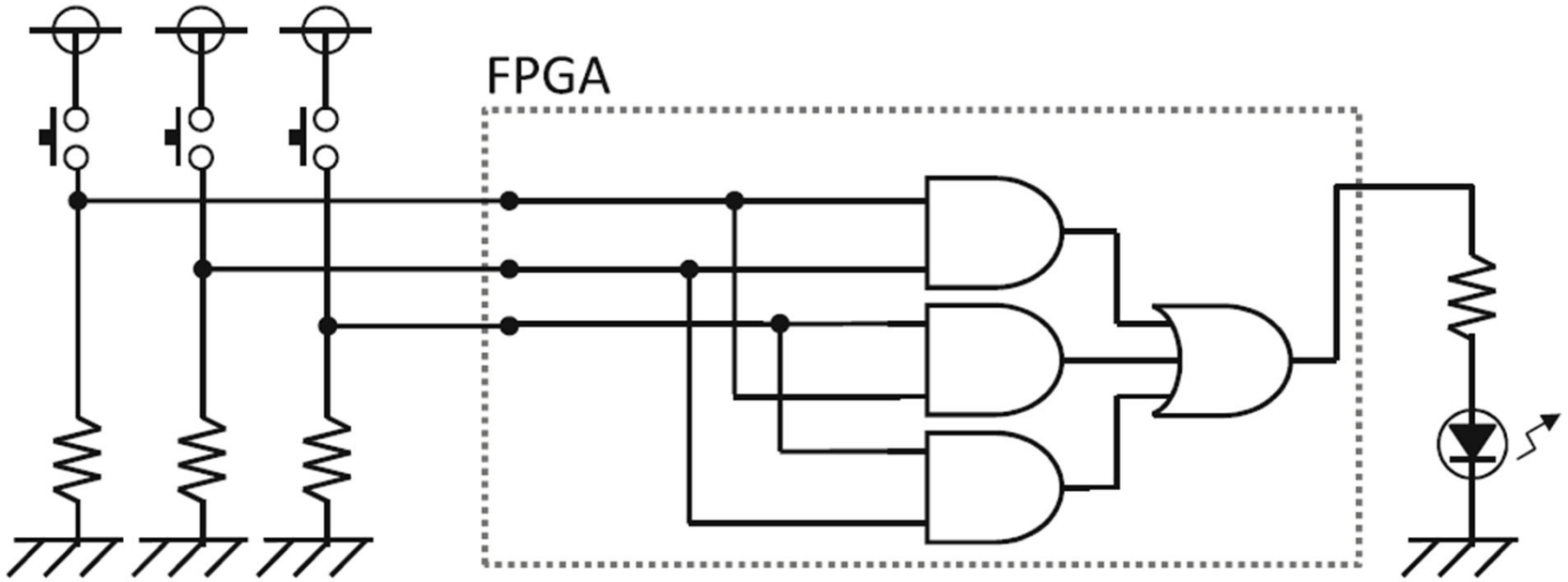
[a]In System Programmability, circuit information can be rewritten while it is mounted on an equipment

FPGA VS. CPLD

- Similarity
  - FPGA and CPLD are programmable ASIC devices
- Differences
  - CPLDs
    - Use of E2PROM or Flash. A limited number of writing.
    - Suitable for combinational logic and product terms
    - Uniform and predictable timing delay
    - No extra storage, faster, smaller, and simpler
  - FPGAs are for sequential logic
    - Use of SRAM. No limit on the number of writing. Reload every time.
    - Suitable for sequential logic with many registers
    - Timing delay depending on the routing
    - Better for complex design
    - Extra non-volatile memory needed for configuring

EXAMPLE IMPLEMENTED ON AN FPGA

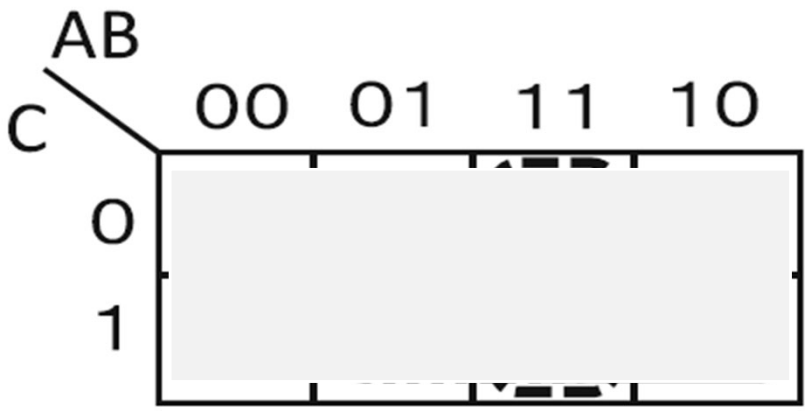
A MAJORITY VOTE CIRCUIT (MVC)



Truth Table and Karnaugh Map

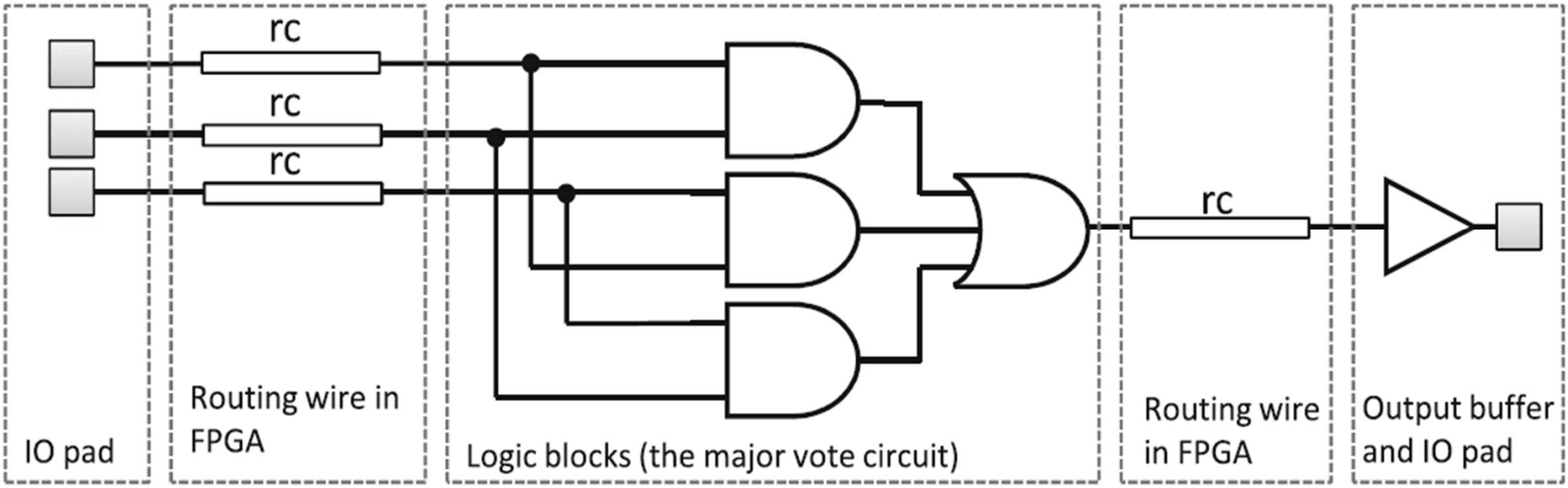
Truth table

A	B	C	M
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

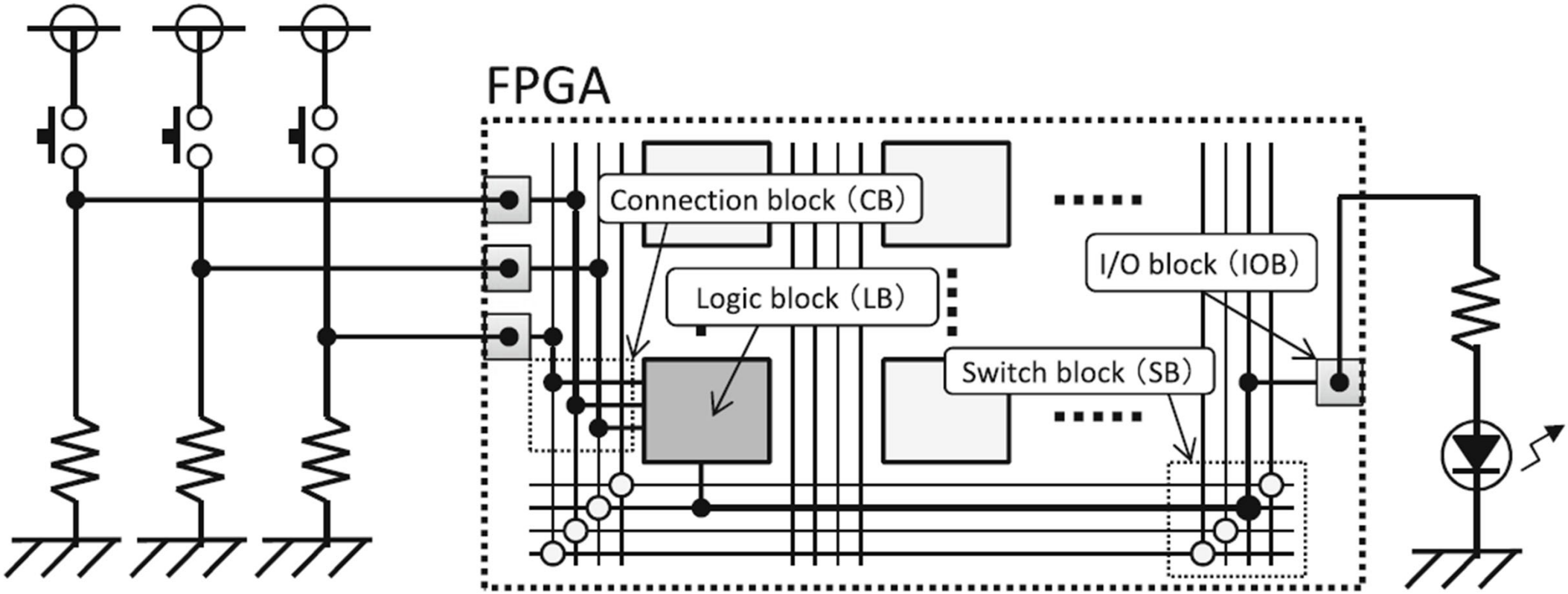


$$M =$$

Mapping of MVC for FPGA

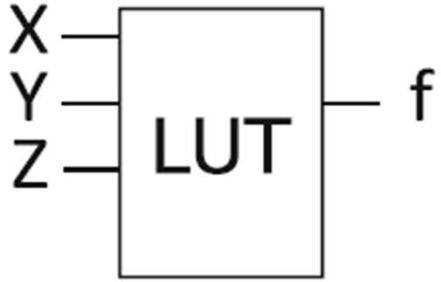


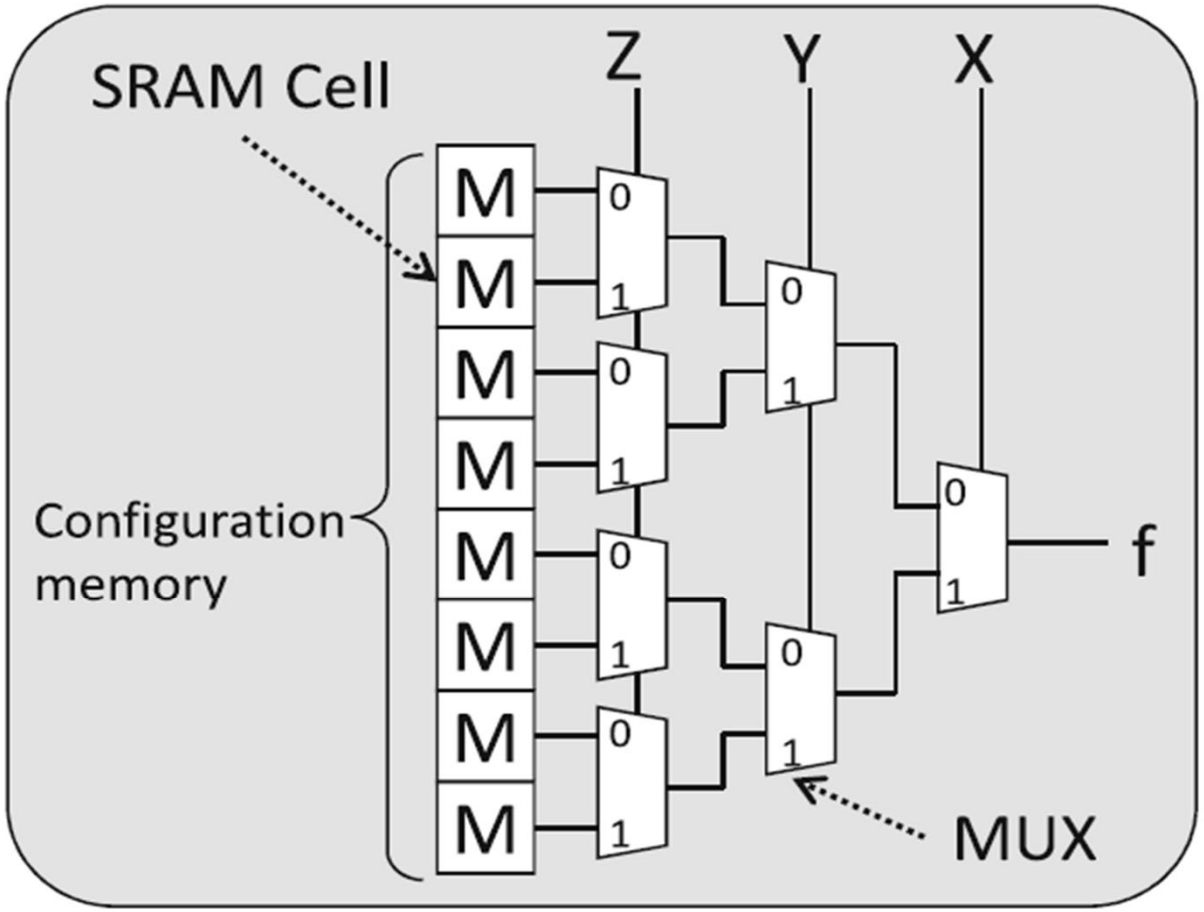
Implementation of MVC on FPGA



Overview of LUT

Example of 3-input LUT





Hardware

- 2^3 bit memory
- 2^3 input selector

Logic capability

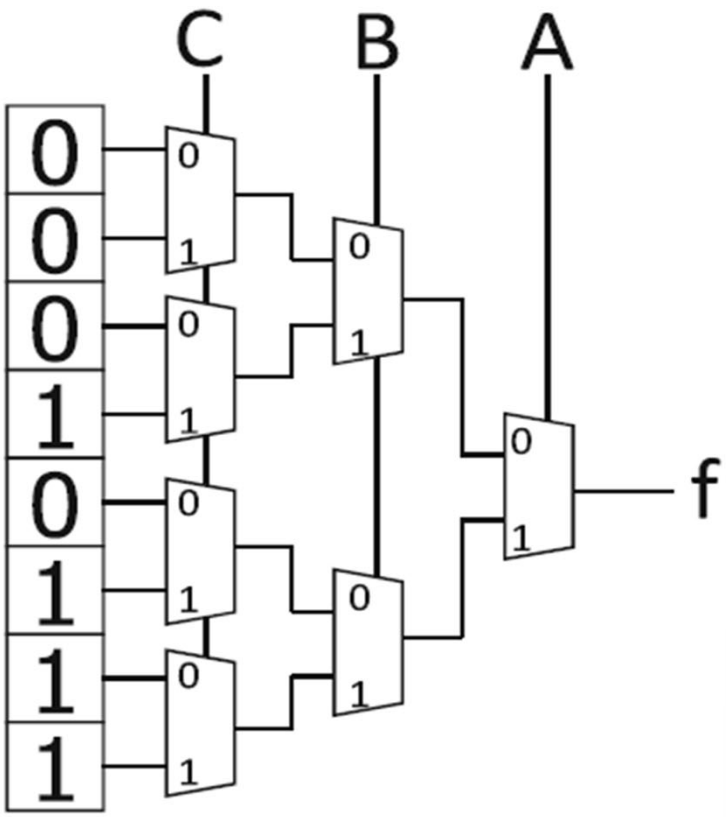
- 2^{2^3} 3-input logic functions

K input LUT has 2^K SRAM cells, 2k-input MUX

Implementation by LUT

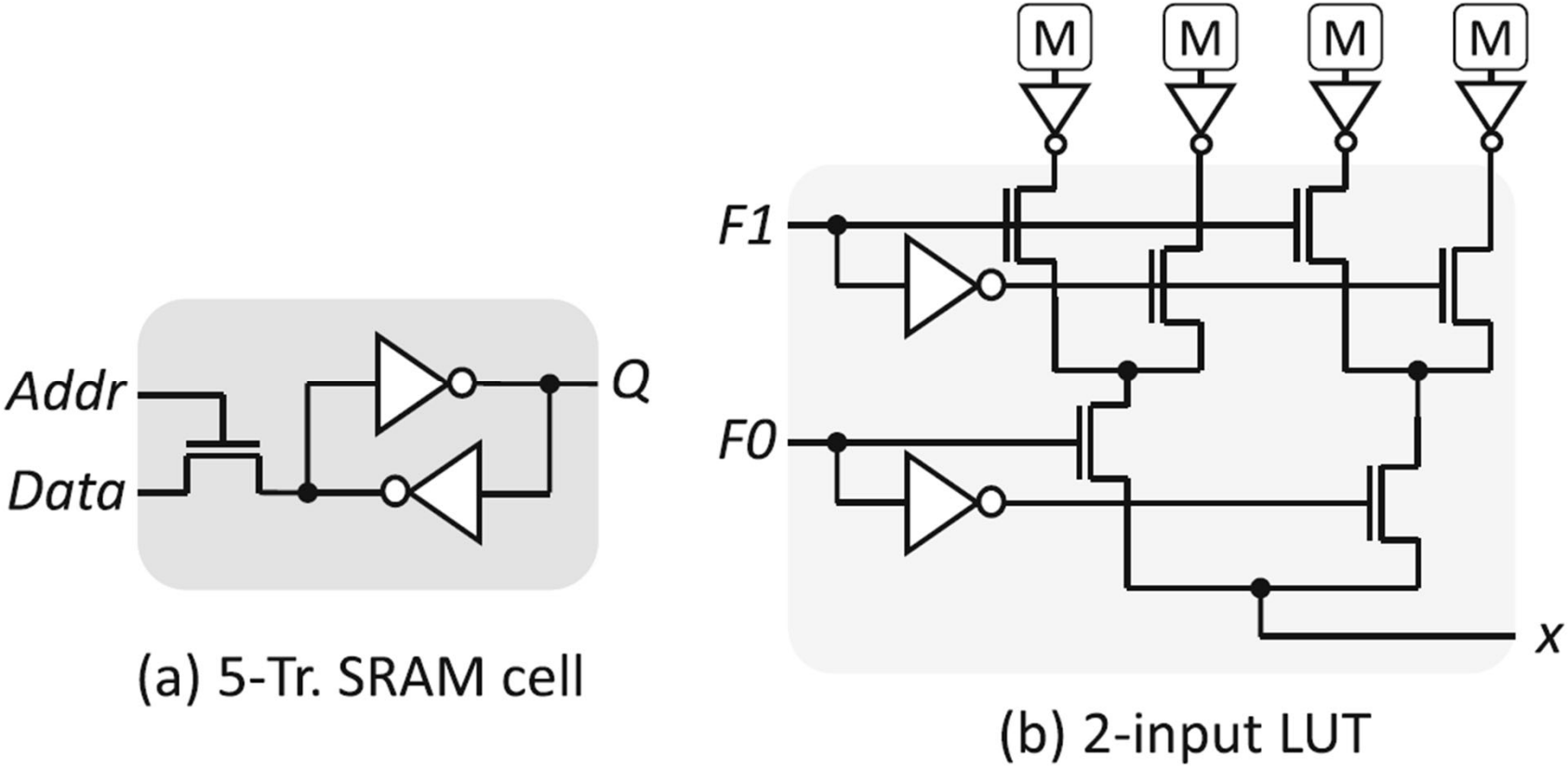
A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(a) Truth table

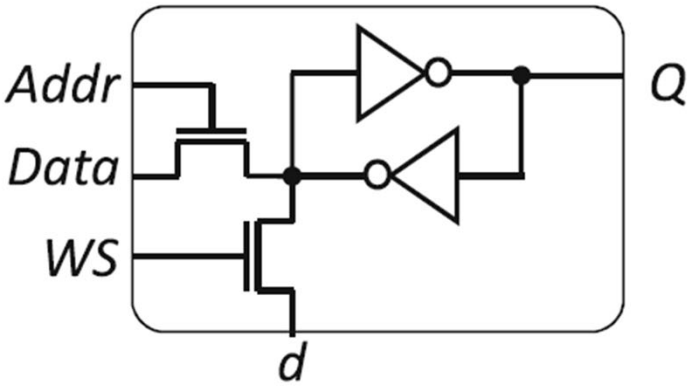


(b) LUT

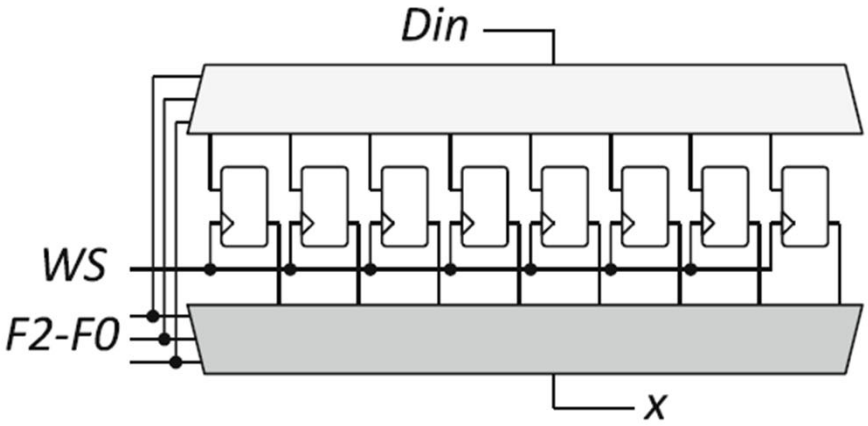
LUT in Xilinx FPGAs by Hsieh around 1980's



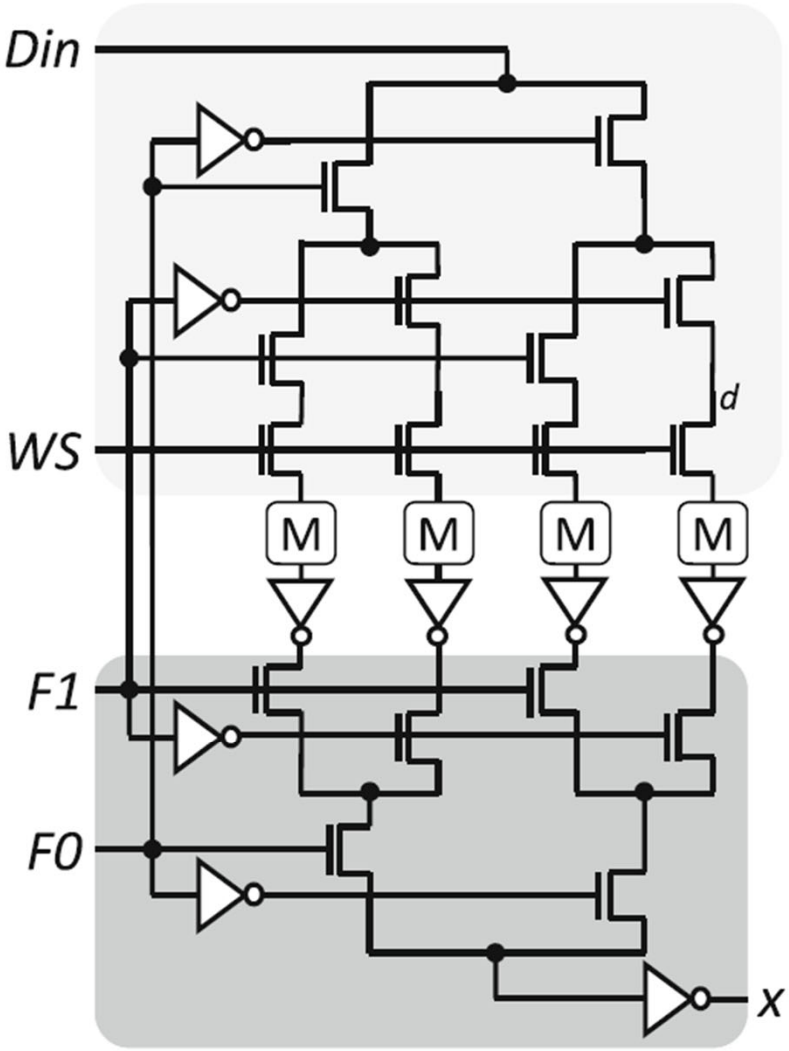
LUT in Xilinx FPGAs by Freeman around early 1990's



(a) 2 port memory cell

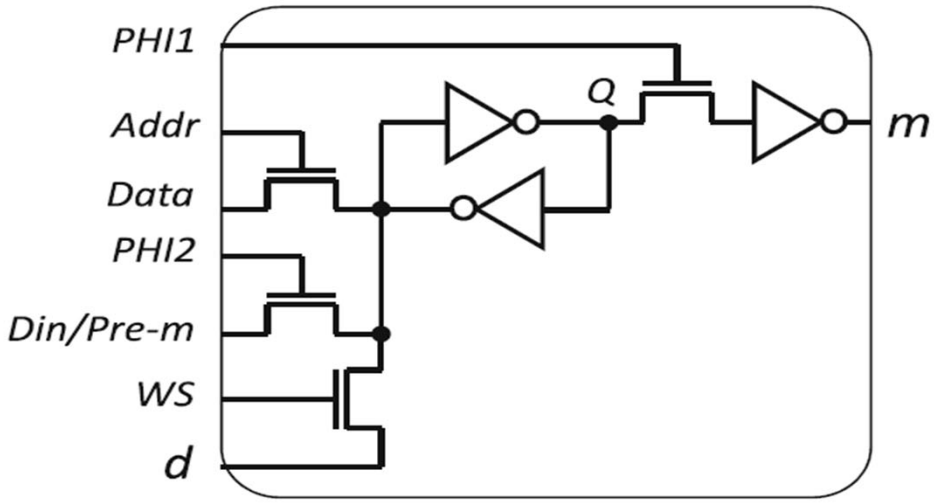


(c) 3-input LUT/8 bit RAM

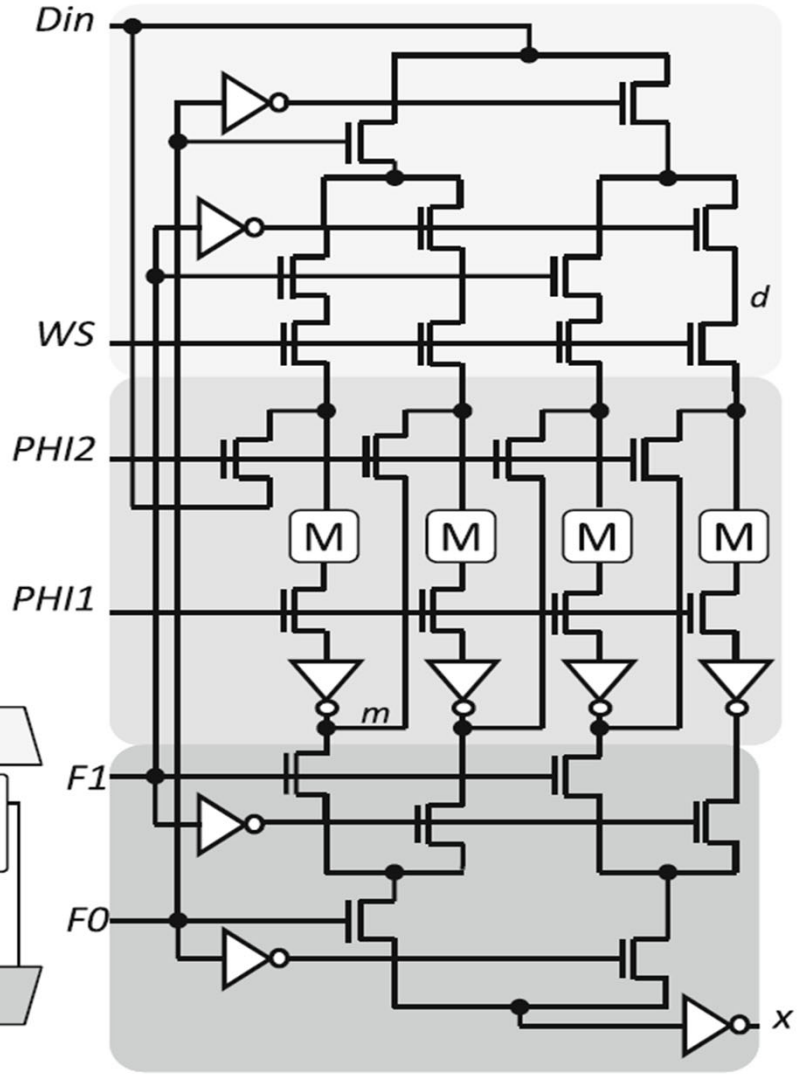


(b) 2-input LUT/4 bit RAM

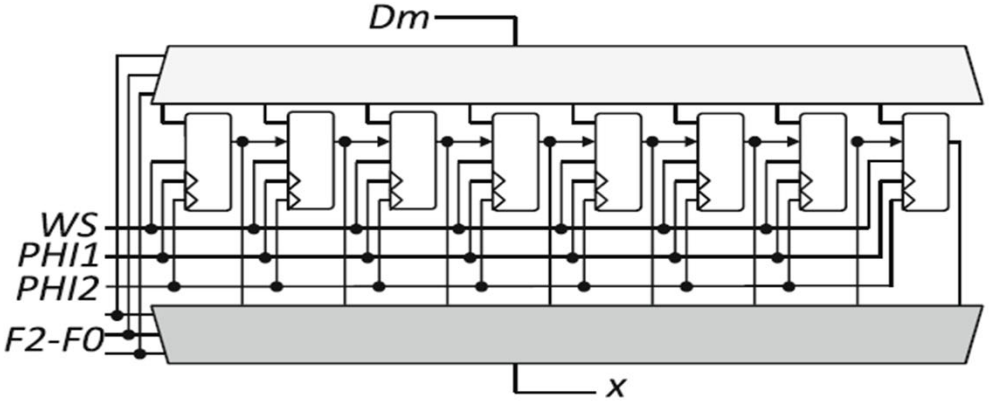
LUT in Xilinx FPGAs by Bauser around late 1990's



(a) 2 port memory cell with shifter



(b) 2-LUT/4bit RAM/4bit shifter



(c) 3-LUT/8bit RAM/8bit shifter