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Triple-junction amorphous/microcrystalline silicon solar cells: Towards industrially viable thin film solar technology

X. Multone, L. Fesquet, D. Borrello, D. Romang, G. Choong, E. Vallat-Sauvain *, M. Charrière, A. Billet, J.-F. Boucher, J. Steinhauser, J.-B. Orhan, R. Monnard, J.-P. Cardoso, G. Charitat, B. Dehbozorgi, N. Guillot, G. Monteduro, M. Marmelo, R. Semenzi, S. Benagli, J. Meier

TEL Solar-Lab SA, rue du Puits-Godet 12a, CH-2000 Neuchâtel, Switzerland

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ABSTRACT

The status of the development of triple-junction (amorphous silicon/microcrystalline/microcrystalline silicon) test cells fabricated with up-scalable PECVD processes is given. A first draft of novel rather flat scattering superstrates with an optimized high bandgap amorphous silicon top cell including a carbon-free buffer at the p/i interface is presented. The careful optimization of the interfaces (including sub-oxide doped layers and buffers) and of the bulk crystallinity of the middle and bottom microcrystalline sub-cells allowed to reach a stabilized efficiency of 13.5 % (after 1000 h light-soaking, internal measurement). Sub-cells individual developments are discussed and their specific integration into the full triple-junction device with its optimization for AM1.5G illumination relying on a partly LED supported solar simulator characterization is presented.

1. Introduction

The major issue with the thin film silicon solar cell technology is the relatively low stabilized conversion efficiency (currently around 13 %) as compared to its theoretical limit (> 20% [1]). Moreover, thin film silicon solar cells incorporating amorphous photoactive materials tend to suffer from light-induced degradation. Despite these limitations the use of these materials in multi-junction devices can pave the way towards a cost effective thin film silicon PV technology [2,3].

Amongst the different thin film silicon solar cell design structures developed throughout the years the tandem amorphous (a-Si:H)/microcrystalline (μc-Si:H) device known as "Micromorph™" is incontestably the most mature and industrially relevant. However, two other cell structures give particularly interesting high efficiencies, namely triple-junction devices [4,5]. Two kinds of triple solar cells comprise an amorphous silicon top cell and a microcrystalline silicon bottom cell, however, they differ by the middle cell which is composed of either an amorphous silicon/germanium alloy (a-SiGe:H) or of microcrystalline silicon. These triple structures are therefore a-Si:H/a-SiGe:H/μc-Si:H [4] and a-Si:H/μc-Si:H/μc-Si:H [5]. While the use of the first structure results in rather high initial state conversion efficiencies (with record cells up to 16.3% [6]), it is the triple device incorporating only microcrystalline silicon in the middle and bottom cells that gave confirmed record conversion efficiency of 13.4% [5] after light-soaking. For silicon–germanium alloy the main issue is the poor stability while the triple-junction of a-Si:H/μc-Si:H/μc-Si:H exhibits a notably improved stability behavior thanks to its reduced amorphous material content. As a result of a two years study on a-SiGe:H based triple cells together with PV-lab of EPFL [7] our last developments described in the present study are focused on the a-Si:H/μc-Si:H/μc-Si:H triple device.

This paper summarizes in detail our main developments which have contributed to steadily increase the stable efficiencies of the a-Si:H/μc-Si:H/μc-Si:H triple-junction test cell. The key challenges to overcome this triple development are namely: the improvement of the light-trapping scheme in order to achieve a total current-density up to 30 mA/cm^2, then the mastering of the bulk material and the interfaces in each sub-cell for realizing high electronic properties and, finally, the integration of each sub-components into the complete triple cell architecture.

2. Material and methods

2.1. Cell fabrication

The a-Si:H/μc-Si:H/μc-Si:H triple cells device structure is sketched in Fig. 1. Our devices are fabricated in the superstrate p–i–n

* Corresponding author. Tel.: +41 32 72 12 14.
E-mail address: evelyne.vallat@gmail.com (E. Vallat-Sauvain).

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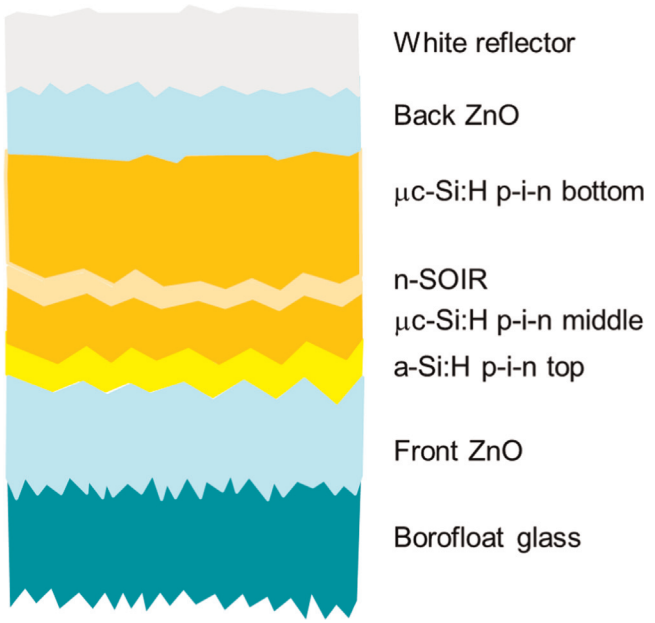

Fig. 1. Schematic design of the triple-junction device studied in this paper. The roughened interfaces are not to scale and the thicknesses of the layers are detailed in the text.

configuration (i.e. the light is impinging the solar cell through the glass) using state-of-the-art low pressure chemical vapor deposition process (LPCVD) and plasma enhanced chemical vapor deposition (PECVD) process [8–10].

For the individual optimization of the sub-cell components single-junction microcrystalline silicon cells were fabricated on similar substrates. Their detailed description is given further below.

The glass substrate is a Schott AF45 squared 50 mm × 50 mm borofloat glass with a thickness of 1.1 mm. These glass substrates undergo an etching step in a Nextral P500 reactive ion etching (RIE) system with a mixture of SF_6 and O_2 at a pressure of 5 mTorr for 20 min. This treatment in the RIE system generates a roughened glass surface as described earlier in [11] and acts as an anti-reflection treatment (ART) [10].

ZnO deposition is performed in our in-house LPCVD reactor at 165 °C with H_2O, diethylzinc (DEZ) and B_2H_6 as gas precursors and dopant gas. The H_2O/DEZ ratio is maintained close to 1 and the B_2H_6 flow is kept minimal in order to maximize near infrared transparency [12]. In order to achieve sufficient front contact conductivity (10–20 Ω/sq) a thickness of around 5 μm is chosen with a resulting as-grown haze value (ratio diffused transmission over total transmission) of 90% at the wavelength of 600 nm. The as-grown ZnO layer is subsequently treated in a reactive ion etching reactor using a mixture of O_2 and Ar, as described in [13] for a duration varying up to 150 min. This RIE step on as-grown LPCVD ZnO removes outstanding surface features and modifies V-shapes to more U-shape surface morphology which represents a more favorable geometry for subsequent thin film silicon growth [13].

The a-Si:H top sub-cells are deposited in a KAI-M reactor of 40.68 MHz plasma excitation frequency at an optimized deposition temperature of 185 °C and a deposition rate of 0.175 nm/s. The optimization of the top cell includes the use of a microcrystalline p-layer followed by a p-SiC amorphous layer. A carbon-free buffer layer at the p–i interface previously developed [14] is implemented to improve light-induced stability and the a-Si:H i-layer is chosen in a palette of materials fabricated with different ratios of the hydrogen/silane gas flows ($D = [H_2]/[SiH_4]$). Of course the thickness of the different absorber materials (D) has been adapted in the cell configuration.

The middle and bottom microcrystalline silicon sub-cells were deposited in an Oerlikon Cluster Line CLN200II reactor operating with a plasma excitation frequency of 80 MHz (inter-electrode distance of 15 mm) at 1.3 mbar and at temperature of 160 °C. For the p–i interface of each sub-cell an optimized 10 nm thick μc-SiO_x:H p-type layer [15] followed by a 7 nm thick intrinsic μc-SiOx buffer layer [16] are used. The intrinsic μc-Si:H layer was deposited in a three steps sequence. Each step (i_n) was characterized by a different hydrogen/silane gas flow ratio (dilution $D=[H_2]/[SiH_4]$) and steps of optimized durations follow each other without plasma interruption in the PECVD reactor. Each step (i_1 or i_2 or i_3) was optimized individually in a single μc-Si:H test cell while maintaining the two other i_n steps unchanged. The resulting graded i-layer was then incorporated as middle and/or as bottom sub-cell of the entire triple-junction cell to quantify the efficiency improvement.

In this study, the highest triple cell efficiency has been achieved with middle sub-cells implementing a short i_1 step at high $D22$ (corresponding to a 65% crystallinity) and a long i_2 (bulk absorber layer) at medium $D19$ (47% crystallinity) followed with a short i_3 at lower $D15$ (crystallinity lower than 30%). The resulting measured crystallinity profile of such middle cells are described further below. The bottom cell crystallinity architecture is pretty similar to the middle cell, except for a longer duration and higher dilution D22 for the i_2 step (bulk absorber of the bottom i-layer). Both microcrystalline silicon sub-cells have incorporated and optimized n-doped sub-oxide layers playing the role of the intermediate reflector [17].

The back contact consists of 3 μm thick undoped LPCVD ZnO layer deposited under the same conditions as the front ZnO except the doping by diborane. 1.05 cm^2 test cells are then defined by laser ablation of the back contact and of the silicon-based absorber to access the front electrode. A diffusive white reflector is applied onto the cells back contact.

2.2. Characterization of multi-junction thin film silicon devices

Test cells were characterized under AM1.5G illumination with a Wacom dual-source sun simulator (WXS-155S-L2 double-source simulator) at 25 °C. The AM1.5G values for V_{oc} and FF as well as J_{sc} were measured after correct settings of the spectra thanks to primary calibrated (PTB) component reference cells (Konica-Minolta) [18]. Light-induced degradation (LID) was performed under open-circuit conditions at 50 °C under one sun during 1000 h. External quantum measurements (EQE) were executed with a setup dedicated to triple-junction characterization: the top cell EQE is measured by saturating the middle and bottom cells with LED illumination at 650 nm, 875 nm and 950 nm, while the middle cell EQE is measured by saturating the top and bottom cells with 465 nm, 875 nm and 950 nm illumination. Finally, the bottom cell EQE is measured by saturating top and middle cells using 465 nm and 650 nm illumination.

Furthermore, in order to fully characterize the maximum efficiency potential of the devices a LED-based modification of the Wacom sun simulator has been developed, recently described in [19–21]. This powerful characterization method is schematically presented in Fig. 2. LED arrays of blue (465 nm), red (650 nm) and IR (875 nm) illumination were implemented to the spectrum of the steady state xenon–halogen simulator. These additional light sources are dedicated for adjusting individually the three sub-cells current densities while maintaining a constant total photocurrent (AM1.5G set-point value) thanks to a small reduction of the sun-simulator total illumination (see for details in Ref. [19]). This LED-based setup helps to find out the optimal cell design by adjusting sub-cells current as shown in Section 3.5 below.

Finally, after complete electrical device characterization, Raman crystallinity profiles were obtained as described in [22] and the

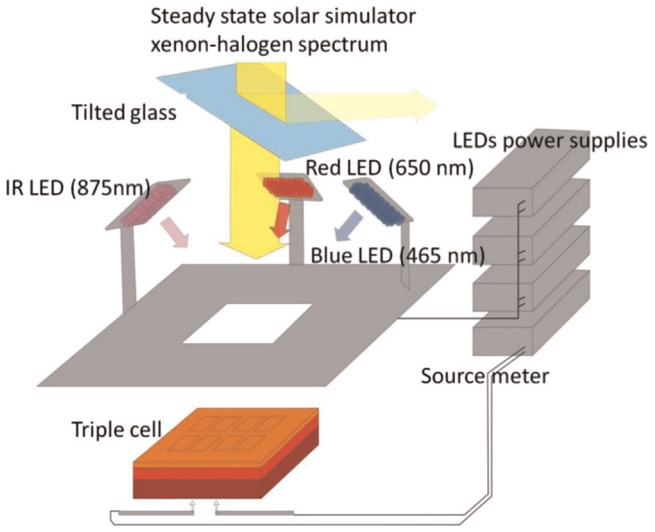

Fig. 2. Sketch of the experimental setup of the LED-based solar simulator, specifically designed for the triple-junction device optimization. Arrays of blue LED's (465 nm), red LED's (650 nm) and IR LED's (875 nm) are implemented in addition to the steady state xenon–halogen dual-source simulator, see for details in Ref. [14]. The additional LED sources are dedicated to the individual adjustment of the sub-cells current-densities [13]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

μc-Si:H bulk material compactness was qualitatively checked by scanning electron micrographs obtained on polished cross-sections of the devices [23].

3. Results

3.1. Anti-reflection treatments of glass

By implementing roughening treatments on both sides of the glass substrate minimized reflection losses are obtained both at the air/glass interface and at the glass/ZnO interface. Both rough surfaces contribute independently in increased EQE over the whole wavelength range (c.f. Figs. 3 and 4). The combination of both leads to an overall short-circuit current gain of over 5%. As the roughened interfaces are giving rise to some light-scattering, it is difficult to separate the respective contributions of the antireflective and of the light-scattering effects, especially at the glass/ZnO interface.

3.2. Front ZnO contact optimization

The as-grown 5 μm thick ZnO applied here as front contact is so rough that is completely detrimental to PECVD thin film silicon device growth [24]. The above mentioned RIE post-treatment of the very rough front ZnO allows us to tune a texture on which low crack density and high quality silicon material are possible to be grown, however, at the detriment of the light-scattering capabilities of the front contact [13]. This trend is illustrated in Fig. 5. The trade-off between improving silicon material quality (V_{oc} increase) and reduced total current-density due to decreasing light-scattering capability of the front ZnO leads to a treatment time of around 150 min. It is observed as well that longer treatment time will bring only marginal additional improvement to the device electrical performances.

3.3. Top cell optimization

The top cell development aims to optimize the a-Si:H absorber with a wide optical bandgap material to achieve maximized open-

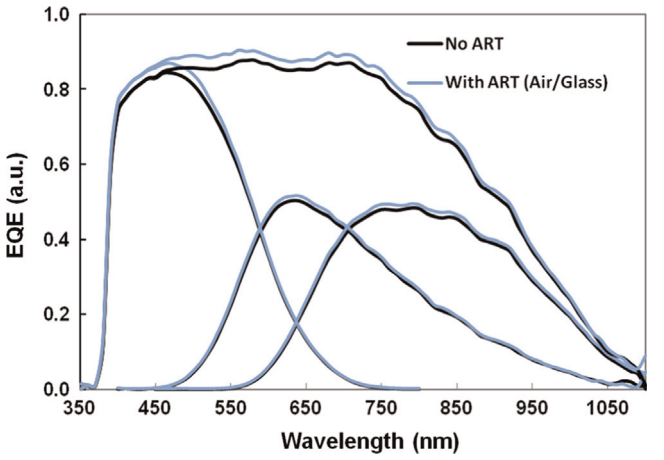

Fig. 3. External quantum efficiency of a cell with and without antireflective treatment (ART) applied at the air/glass interface of the structure. The broadband effect leads to a gain in the short-circuit current of 2.9%.

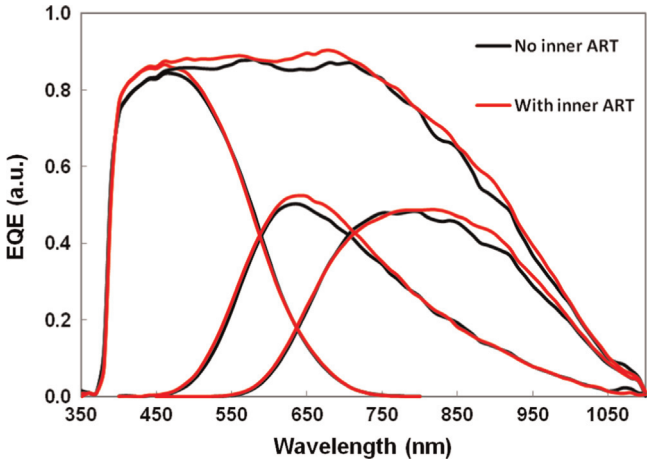

Fig. 4. External quantum efficiencies of two triple-junction cells: one consists of a diffusive antireflection characteristics at the glass/ZnO interface (inner ART), the other is the bare glass without an ART for comparison. The gain due to the "inner ART" benefits mostly in the range of 350–900 nm, the total current increase is close to 2.5%.

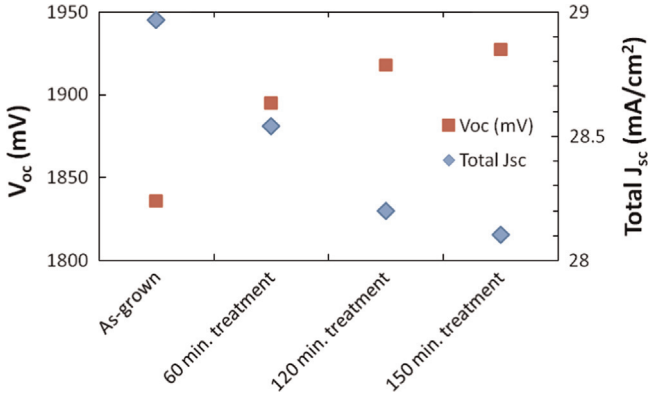

Fig. 5. Triple-junction cells (initial) open-circuit voltage (in red) and total current-density (in blue) as a function of the 5 μm thick LPCVD ZnO post-treatment duration. The overall gain in efficiency increases with treatment time up to 150 min. Note that FF is also positively affected by the ZnO post-treatment (not shown). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

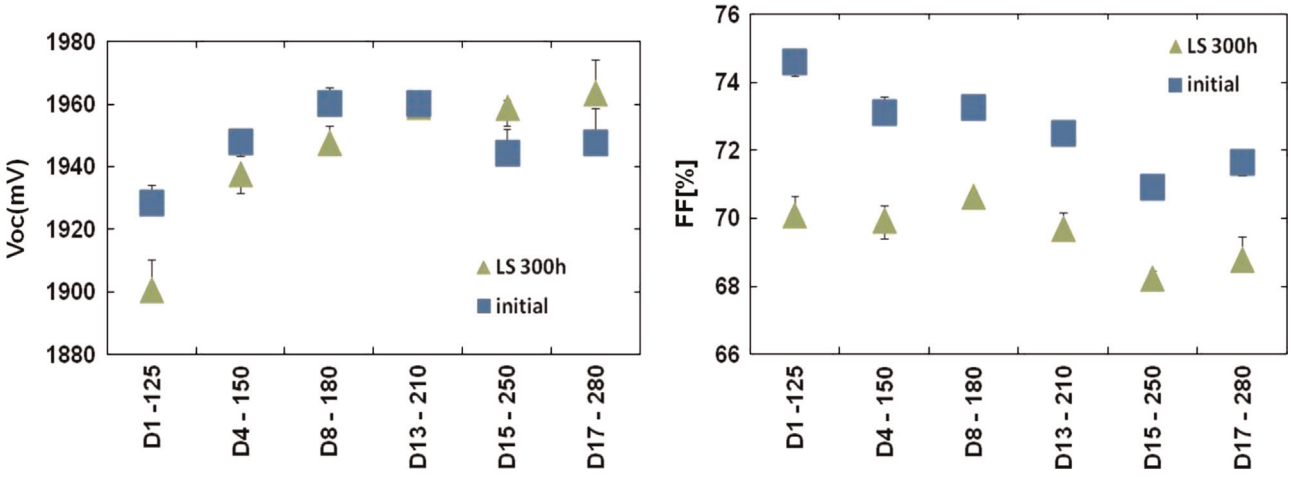

Fig. 6. Values of initial and light-soaked (300 h) V_{oc} and FF of triple cells as a function of top-cell a-Si:H material and thickness. The dilution D and i-layer thickness (in nm) are indicated (D8-180 means dilution 8 with i-layer of 180 nm thickness). The bottom and middle cells are co-deposited on the various top cells. In this series, the top-cell sub-current is kept constant at 9 ± 0.2 mA/cm^2 thanks to the adapted dilution/thickness combination. The mismatch current is thus kept constant at 0.8 mA/cm^2 in these top-limited triple cells.

circuit voltages at a reasonable current potential in a triple device. After setting the deposition temperature at 185 °C the optical bandgap of the a-Si:H is tuned by varying the hydrogen flow in the plasma gas phase resulting in hydrogen dilution series (increasing D). Within the palette of absorber materials fabricated from D1 up to D17 (c.f. Fig. 6) the i-layer thickness is chosen in order to reach 9 mA/cm^2 after light-soaking. Such top-cells are then incorporated in triple-cells whose middle and bottom cells are kept unchanged. In this experiment, the top cell is limiting the current. Finally, it has to be noted that for this experiment, the buffer layer (positioned between the p-layer and i-layer) was optimized for light-soaked state, leading to V_{oc} gains of up to +30 mV compared with standard buffer. The best buffer layer found in our development consists of a very thin (< 10 nm) state-of-the-art $D=1$ layer followed by a H_2 plasma treatment. The optimal hydrogen plasma conditions and duration are detailed in [14]. This new optimized carbon-free buffer layer (with the hydrogen plasma) was combined in a dilution series of i-layers in solar cells. These cells integrated in triple cells are given in Fig. 6 by the resulting V_{oc} and FF values. The i-layer thickness targeting the 9 mA/cm^2 increases with higher dilution D as expected for a larger bandgap material. On the other side Fig. 6 confirms as well that a-Si:H i-layers obtained at high D result in higher V_{oc} values, as expected for wider opto-electronic bandgap material. Fig. 6 also reveals that high D a-Si:H i-layers are more stable against LID, both in term of V_{oc} and FF. The smaller decay of the FF with light-soaking in this study can be attributed in a straight-forward way to the top i-layer material, as the current repartition within the 3 junctions is kept same for all cells. Generally it is believed that in terms of LID the thinner the a-Si:H absorber layer the better is the stability; however, we found in our experiments that the best compromise for the top cell is to use rather the D13 thickness=210 nm combination than the thinnest 125 nm/D1 top cell (Fig. 6).

3.4. Microcrystalline middle and bottom cells improvement

In addition to the i-layer grading described previously, it is the implementation of silicon oxide-based p-doped and buffer layers in the middle and bottom cells which helped to considerably improve the triple-junction solar cell efficiency [16]. Table 1 illustrates the impact of the incorporation of the oxide-based p-layer in comparison with simple p-doped microcrystalline layers on the V_{oc} and FF values of triple cells with otherwise similar i_n steps: both solar cell parameters are significantly increased.

Table 1
Effect of a p μc-SiO$_X$ layer instead of the standard p μc-Si layer in the middle and bottom μc-Si:H cells. This experiment is done with post-treated ZnO.

p-Layer	V_{oc} [mV]	FF [%]	J_{sc} [mA/cm^2]	Eff. [%]
p μc-Si	1923	71.2	9.1	12.5
p μc-SiO$_X$	1945	75.3	8.7	12.7

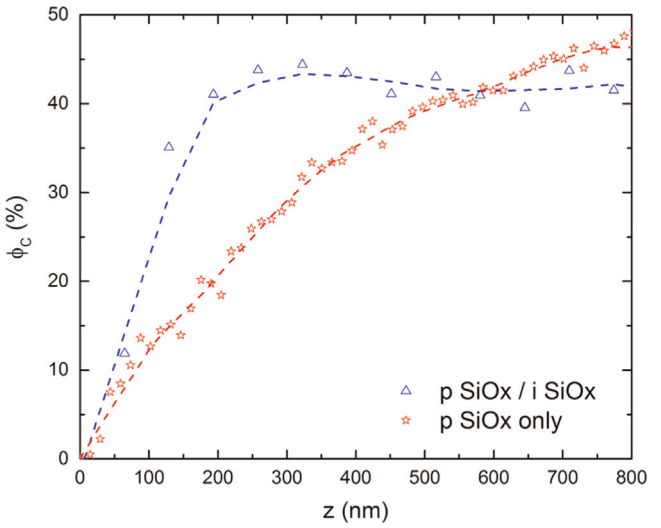

Fig. 7. Raman crystallinity profile of two identical single-junction μc-Si:H cells except for the introduction of a 7 nm thick intrinsic μc-SiO$_X$ layer at the p/i interface. The use of such a thin i SiOx buffer layer improves clearly the nucleation of the on-growing μc-Si:H layer.

Fig. 7 shows the impact of the introduction of a sub-oxide buffer layer on the Raman crystallinity profile measured on single-junction microcrystalline cells (deposited directly on treated ZnO). The crystallinity profiles of Fig. 7 indicate that the application of these oxide based buffer layers has a marked impact on the nucleation of the μc-Si:H i-layer: with the same PECVD process conditions the resulting μc-Si:H absorber material at a chosen depth is much more crystalline when oxide layers are underlying the i-layer. Fig. 8 reveals the resulting external quantum efficiency of the two cells. The broadband improvement of the current

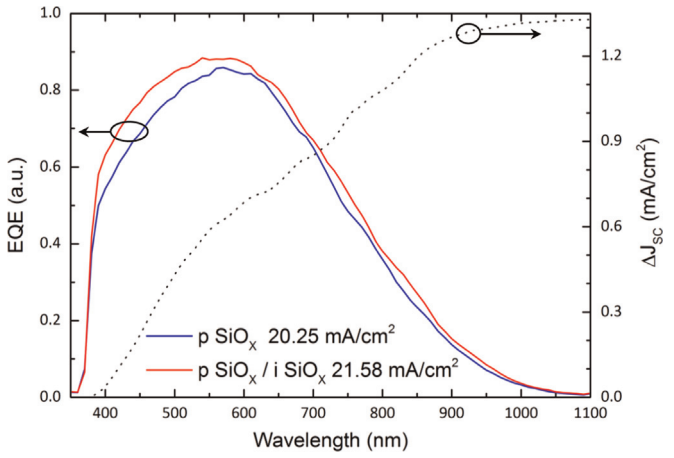

Fig. 8. EQE of two identical single μc-Si:H cells with and without a 7 nm thick i μc-SiO_X buffer layer. The spectrally increasing total gain in the current-density is given by the dashed line.

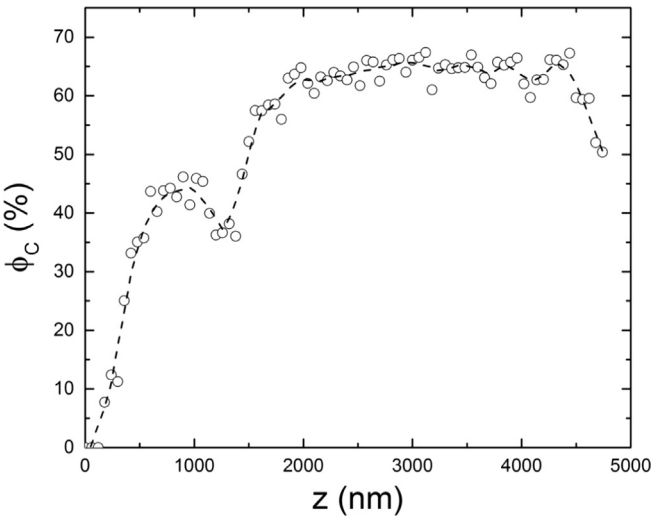

Fig. 9. Raman crystallinity profile of a high-efficiency triple-junction solar cell. The bulk crystallinity of the middle cell is about 45% while the bottom cell crystallinity is higher at around 65%. The crystallinity drop between the middle and bottom cells is due to the presence of a low crystallinity i_3 layer at the i/n interface of the middle cell and to the use of a low refraction index silicon oxide intermediate reflector material.

generation thanks to the addition of the microcrystalline oxide buffer layer is obvious and can be attributed to two phenomena: (1) for the short wavelength (from 350 to 600 nm) the enhanced EQE is attributed to an improved collection efficiency of photo-generated carriers at the p–i interface thanks to the increased microcrystalline silicon fraction close to this interface, as observed in Fig. 7. The latter can be attributed to the oxide-like chemical nature of the underlying layer [25]. The long wavelength enhancement (from 600 to 1000 nm) is linked to the overall increased crystallinity in the intrinsic μc-Si:H layer giving rise to an increased absorption. This increased absorption in long wavelength allows for a thinner middle cell. While short wavelength improvement in μc-Si:H cells will not be significant in triple cells, in which amorphous top cell absorbs most of the light in this range, the enhanced long wavelength absorption significantly helps to get higher currents in middle and bottom cells.

In summary, the optimization of the oxide-based interfaces is based first on the successive development of the silicon-oxide p-layer that results in a significant V_{oc} improvement. Then, the intrinsic oxide buffer layer is introduced to promote a high crystallinity of the following μc-Si:H i-layer.

The optimization of the three dilution and duration steps for the i-layer (i_1–i_3) results in a crystallinity profile such as depicted in Fig. 9. The middle cell has an overall thickness of 1.5 μm with a "bulk" crystallinity reaching 45%. This moderate crystallinity allows a remarkable V_{oc} increase for the middle cell. Then, the thick n-oxide/p-oxide recombination junction (between 60 nm and 120 nm) of relatively low crystallinity (30%) acts as an intermediate reflector, enhancing thereby the middle cell photocurrent and, thus, allows for a reduced μc-Si:H i-layer thickness of the middle cell. Finally, the bulk crystallinity of the bottom cell is optimized to 65% in order to reach 9 mA/cm^2 with a thickness kept below 3 μm. As described above the passivation layer i_3 with a reduced crystallinity acts as a buffer at the i/n interface and allows for further V_{oc} improvement [26].

Finally, one can see that PECVD deposition processes developed for the bottom cell lead to a rather compact μc-Si:H material. Fig. 10 shows the impact of the use of as-grown rough front ZnO on the compactness of the middle and bottom cells. While some porous zones are observed in the middle cell, no more cracks are present in the bottom cell. One advantage of using smoothened substrates as developed for our triple devices is to reduce the defective zones in the middle cell.

3.5. *Evaluation of efficiency potential*

Once the absorber materials and interfaces are optimized the maximization of the triple-junction cells efficiency relies on the fine-tuning of the sub-cells photocurrents with respect to the AM1.5G illumination. The repartition of total current to the different sub-cells influences the device conversion efficiency under the AM1.5G spectra. We have done extensive investigations with various sub-cell currents combinations to arrive to the conclusion that the most impacting characteristics are first the top cell current and second the middle/bottom mismatch. Fig. 11 shows how the triple device efficiency depends sensitively on these characteristics for one typical test cell fabricated in the course of our development. The value of top cell current has a stronger direct impact on the overall device efficiency when the current repartition between the middle and bottom cells remains within a range from $+0.2$ mA/cm^2 to -0.6 mA/cm^2. Finally, the maximum efficiency for this particular device will be reached under slightly middle and bottom sub-cells limitation.

3.6. *Improved light-induced degradation and best results*

Thanks to the high optical bandgap and the relatively thin a-Si:H top cell the average light induced degradation of the a-Si:H/μc-Si:H/μc-Si:H is rather low, only around 3.5% after 1000 h. Finally, having optimized all the design structure so as to answer the specific challenges (high gap top cell, highly diffusive structure, high performance middle and bottom cells) our overall development has led to a state-of-the-art thin film triple solar cell with a stabilized efficiency of 13.46% after 1000 h of light-soaking (Fig. 12). This cell exhibits a remarkable open-circuit voltage value of 1967 mV together with a high fill factor and short-circuit current.

4. Discussion

Thanks to the developments previously described, state-of-the-art a-Si:H/μc-Si:H/μc-Si:H triple-junction cells were fabricated with efficiency close to 13.5%. This represents roughly an absolute 1% improvement compared to state-of-the-art tandem a-Si:H/μc-Si:H cells fabricated with similar processes [8,9].

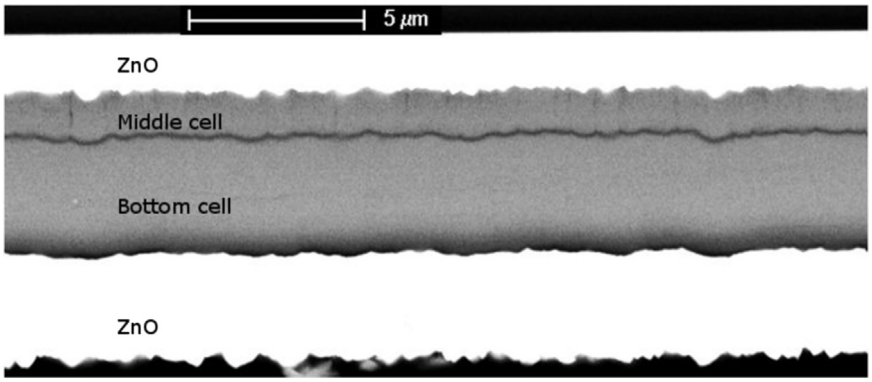

Fig. 10. SEM micrograph of the cross-section of a triple-junction cell deposited on a rough, as-grown ZnO (similar to our industrial reference TCO). Cracks are clearly visible in the middle cell but almost absent in the bottom cell although the crystallinity is much higher. The smoothening effect of both top and middle cells allows obtaining a good electrical quality in the bottom cell in spite of its larger thickness and crystallinity.

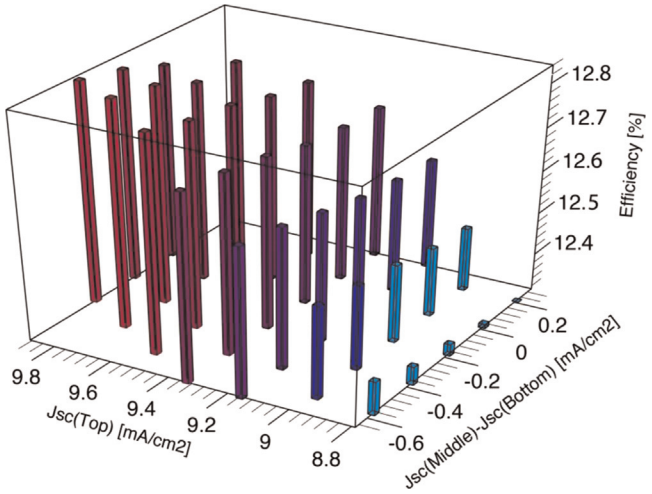

Fig. 11. Efficiency of a triple cell in function of various combinations of sub-cell current-densities as provided by the solar simulator developed in Fig. 2. These data are obtained by maintaining the total photocurrent density constant ($J_{sc}^{total}=J_{sc}^{top}+J_{sc}^{middle}+J_{sc}^{bottom}$ @AM1.5). By varying the different sub-cell current densities with the spectral illumination the optimum triple efficiency can be found for a given total short-circuit current-density value.

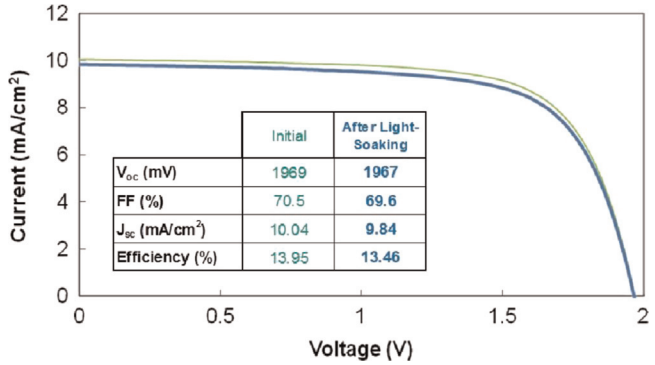

Fig. 12. AM1.5G *I*(*V*) characteristics of the best triple cell fabricated at TEL Solar-Lab after 1000 h of light-soaking (50 °C, one sun, in open-circuit conditions) and in its initial state. Note the high stability of this device (only 3.5% LID loss).

The first challenge in the path of the development of high efficiency triple-junction cells was to gather enough light to increase the current-density up to 30 mA/cm^2. As the photoactive microcrystalline material quality deteriorates above thicknesses of several μm [27] the total accumulated thickness to reach 30 mA/cm^2 is sub-divided into two μc-Si:H junctions.

Furthermore, it appeared that the newly developed superstrate is very effective in reducing parasitic reflections. The advantage of using an etched glass/etched ZnO combination is to provide a sufficiently light-scattering substrate with a rather smooth surface topography for subsequent PECVD silicon deposition; this substrate is a first draft of a type of flat-diffusing substrate as already well demonstrated in thin-film silicon n–i–p configurated devices [28,29]. The advantage of such substrates for the triple cell application is that it allows the use of very thin diluted a-Si:H layers with good conformal growth (i.e. constant i-layer thicknesses over the substrate). In fact, rough substrates limit the use of highly diluted or low temperature processes [23] as they result in non-conformal growth of the already thin top-cell layers (doped as well as intrinsic layers). Therefore, the choice to use smoothened strongly scattering substrate was a strong lever for the efficiency improvement of the triple cells in our laboratory.

The use of highly diluted more stable i-a-Si:H layers in good adequacy with the underlying roughened substrate and treated ZnO layer allowed to reduce the LID by a factor 2 with respect to state-of-the-art a-Si/μc-Si tandem devices. Such i-a-Si:H layers are not applicable to the tandem design, as they result in too low current densities (respectively, too excessive thickness and consequently too high LID). This reduced LID of the triple device comes not only from the improved stability of the amorphous top-cell material but, hence, also from the distribution of the power produced by each sub-components. In fact, the contribution of each sub-cell to the effective power in the triple junction is approximatively for the amorphous silicon cell $<1/2$ and the microcrystalline silicon cells $>1/2$ respectively (to be compared with the Micromorph™ tandem design, where the power distribution is 2/3 by the a-Si:H cell and 1/3 by the microcrystalline cell). It is a real advantage to have a larger fraction of the power produced by the stable μc-Si:H material. Furthermore, the highly diluted i-a-Si:H top-cell material allows for higher V_{oc}-values. Together with the newly developed sub-oxide silicon layers used in the middle and bottom cells the V_{oc} potential of the triple junction structure could be maximized.

Finally, the integration of the individual sub-cells in the triple-junction was optimized in terms of i-layer thicknesses with the newly developed LED-based simulator. This powerful solar cell characterization technique was determinant to the direction in which the development should be focused to maximize the efficiency under AM1.5G. In practice the optimization of triple devices is equipment-wise rather time consuming if one relies only on

device fabrication & characterization with various i-layer thicknesses combinations.

The industrial application of such multi-junction devices compared to the tandem (Micromorph™) design remains however challenging. First of all, the fabrication of low-cost strongly diffusing transparent conductive contacts adequate for subsequent PECVD layers deposition is not straight-forward. The triple device architecture involves two additional recombination junctions compared to the tandem and therefore adds complexity in the interfaces optimization: the number of process steps to be mastered is increased, as well as the specific device characterization procedures (EQE, enhanced sensitivity to spectral calibration in the $I(V)$ measurement). However, the efficiency benefit ($>$ absolute 1% in our study) is so consequent that it favors the use of μc-Si:H multiple junctions for high efficiency thin film silicon devices.

Design complexity has been tackled at the R&D level by using the newly LED-based simulator to optimize sub-cells current combination for highest efficiency from one single device measurement. Moreover, thanks to its flexibility, the same setup permits to evaluate the spectral sensitivity of such triple-junction test cells. The scaling-up of this characterization system should be a priority for a development of large-scale triple-junction solar modules.

According to our experience the microcrystalline middle sub-cell is the most critical in terms of compactness. Consequently we suggest to use two different regimes for the deposition of each microcrystalline sub-cells: the middle junction should be deposited with advanced processes (e.g. with the high pressure depletion regime [30]) resulting in compact microcrystalline i-layer material even if the regime used implies a reduction of the deposition rate. Meanwhile the bottom junction, less sensitive to substrate roughness, could be deposited in a higher deposition rate regime.

5. Conclusions

State-of-the-art thin film silicon triple-junction a-Si:H/μc-Si:H/μc-Si:H cells were fabricated thanks to careful development of each of its sub-elements. In terms of stability the advantage of using a triple-junction design compared to Micromorph™ tandem is demonstrated, as the relative degradation is remarkably reduced to about 3.5–8% after 1000 h of light-soaking. One of the main advantage of the triple-junction cell architecture is to shift the power generation from the amorphous silicon to the microcrystalline silicon absorber material and to benefit from the strong improvements in μc-Si cells development of the recent years. The triple cell allows further the possibility to increase the total thickness of the microcrystalline absorber while keeping sufficiently good microcrystalline sub-junctions.

The triple junction allows to profit from high short-circuit current potential of up to 30 mA/cm^2 and keeping high LID stability. While the design of efficient light-scattering substrates allowing for a defect-free growth of H_2-diluted a-Si:H layers is still an open challenge, triple cell will clearly benefit from this wide bandgap material that yields to a strong improvement of V_{oc} (plus 60 mV compared to a top cell necessary in the Micromorph™ tandem structure). Moreover, the use of sub-oxide p and buffer layers and dedicated crystallinity profiles in the middle and bottom microcrystalline junctions help to improve further the efficiency. By applying a new $I(V)$ metrology technique to assess the efficiency potential a fast and effective way to design sub-cells combinations for efficiency maximization has been undergone. The obtained 13.5 % triple cell conversion efficiency demonstrates that high efficiency thin film silicon devices are within reach, considering that fabrication of advanced light-trapping structures and new silicon material deposition processes could lead in the future to an industrially viable solution.

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