FABRICATION OF THE LARGE-AREA INTEGRATED a-Si SOLAR CELLS

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1. PREFACE

PIN-structure small-area solar cells using a-Si have been frequently reported on, but only a few reports are available on the study of solar cells using a large-area (10-cm square) substrate, all with a resultant conversion efficiency of above 9.0 %[1,2]. Our study has been concentrated on solar cells using a batch of ten 10-cm square substrates with an average conversion efficiency of 9.5 % or more.

As a result, without an anti-reflection coating on the surface of the glass substrate, the following values have been obtained:
average conversion efficiency (EFF)=9.63 % (standard deviation of 0.195 %)
-Open-circuit voltage (Voc)=12.668 V (standard deviation of 0.215 V)
-Short-circuit current (Isc)=78.467 mA (standard deviation of 1.619 mA)
-Fill factor (FF)=0.6672 (standard deviation of 0.009)

The process, equipment and methods for measurements through which these results were obtained are described below.

2. CELL STRUCTURE

Figure 1 illustrates a profile of our prototype solar cell. The substrate is made of soda glass. The transparent conductive film of ITO (indium tin oxide with a thickness of 800 Å) and SnO_2 (200 Å thickness) are formed on the substrate with a textured surface structure. The following amorphous semiconductor layers are also deposited on the transparent conductive film using a multi-chamber system.

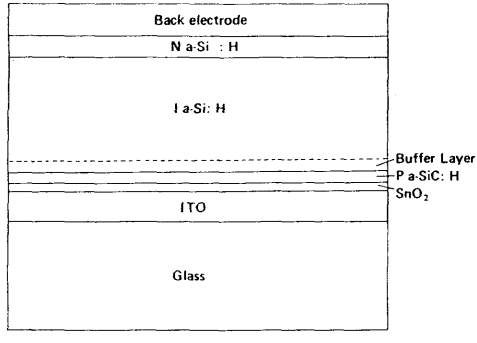

Fig. 1.
Profile of solar cell.

A P-type a-SiC:H layer (with an average thickness of 130 Å), a buffer layer (a-Si_xC_{1-x}, $0<X<1$) to provide an intentionally continuous junction, an I-type a-Si:H layer (7000Å thickness) and an N-type a-Si layer (400 Å thickness) are formed in that order. The back electrode employed is highly reflective.

The reasons for the adoption of this type of device structure are summarized as follows:

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1. To decrease the amount of C, N and O impurities in the I-type semiconductor layer, which is essential to elongate the lifetime of the drifting carriers.
2. To provide an intentionally continuous P-I junction interface, thereby decreasing the loss of holes at this interface due to recombination.
3 To provide the P-type semiconductor layer on the incident side with wider energy band width, thereby lowering the absorption loss of light.
4. To enable the use of the texture surface of conductive transparent films so as to confine the light in the semiconductor layer.

By integrating these factors, high conversion efficiency was obtained by a simple, single PIN junction solar cell using amorphous semiconductors.

3. INTEGRATION

Figure 2 illustrates the integrated module structure. Laser scribe method was used for patterning in order to fabricate the module structure. This method, which we developed, has already been reported[3].

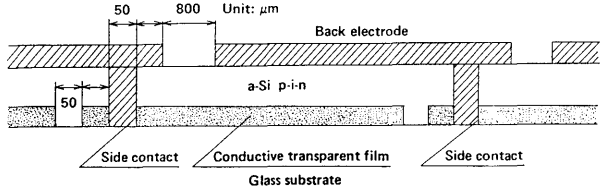

Fig. 2.
Integrated module structure.

As is shown in Fig. 2, the glass substrate is employed and front side electrode made of a transparent conductive film is formed thereover. This transparent conductive film is processed using a YAG laser (with a wavelength of 1.06 μm). To make a 15 series connection of this layer, the first laser patterning is performed to form a 50 μm-width groove. Upon this patterned films, PIN junction semiconductor layers are deposited by the use of the multi-chamber system, which will be described in the next section.

The second laser patterning is performed using the same YAG laser to form another 50 μm-width groove which enable the solar cell to connect in series. In this case, the second pattern is formed 350 μm away from the first pattern, because the YAG laser employed has a wavelength of 1.06 m, and its radiation eliminates (by vaporization) not only the semiconductor layer but also the transparent conductive film which is formed beneath the semiconductor layer.

The YAG laser processing conditions are as follows:
-Wavelength.....1.06 μm
-Q-switch frequency.....5 kHz
-Laser output.....1 W (measured at the laser beam exit)
-Scanning speed...1 cm/sec

Furthermore, the back electrode is formed by using a metal mask on the upper surface of the semiconductor layers.

In the formation of this back electrode, the electrode material makes contact with the side of the transparent conductive film (what is called the side contact structure)[4,5]. Even with this type of structure, the contact resistance at each side is not so large as to hinder 15 cells from being efficiently connected in series.

We have reported on the Laser process to make the patterning of the backside electrode on this PIN semiconductor layer[3], but the speed of the laser-process is a problem, and therefore, a metal mask was used to form this back electrode. As a result, the effective area of a 10 cm-square substrate is only 68.83 cm^2. The process to make the patterned backside electrode is performed using the vacuum evaporation method and attaching the

metal mask.

4. PROCESS AND EQUIPMENT

Figure 3 is a schematic diagram of the multi-chamber type plasma chemical vapor deposition (PCVD) equipment[6,7] which we employed. As shown, the equipment consists of:
VC1...Substrate load chamber.
VC2...Reaction chamber for the formation of P-type a-SiC:H.
VC3...Reaction chamber for the formation of both buffer layer of $a\text{-}Si_xC_{1-x}$(0<X<1) and I-type amorphous silicon layer.
VC4...Reaction chamber for the formation of N-type amorphous silicon layer.
VC5...Substrate unload chamber.

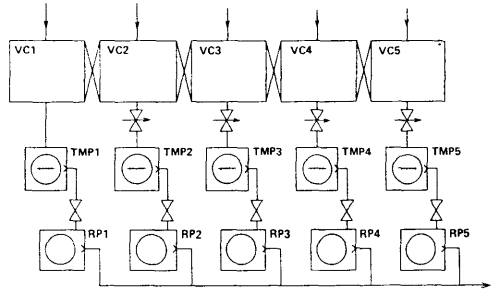

Fig. 3
Schematic diagram of the multi-chamber type PCVD equipment.

All the reaction chambers are evacuated by turbo-molecular pumps. Thus, the amount of C, N and O impurities within the chambers can be effectively reduced. As shown in SIMS depth profile in Fig. 4, the amount of C, N and O impurities in the I-type semiconductor layer are typically 5 x 10^{17} cm^{-3}, 5 x 10^{16} cm^{-3} and 1 x 10^{19} cm^{-3}, respectively[8].

To obtain the buffer layer of an intentionally continuous junction[9] at the P-I interface, the flow rates of carbon source gas at this interface are controlled by a microcomputer. Since the flow rates are controlled on a per second basis, high-precision control of the buffer layer thickness over the P-I interface can be realized with a sufficient degree of repeatability.

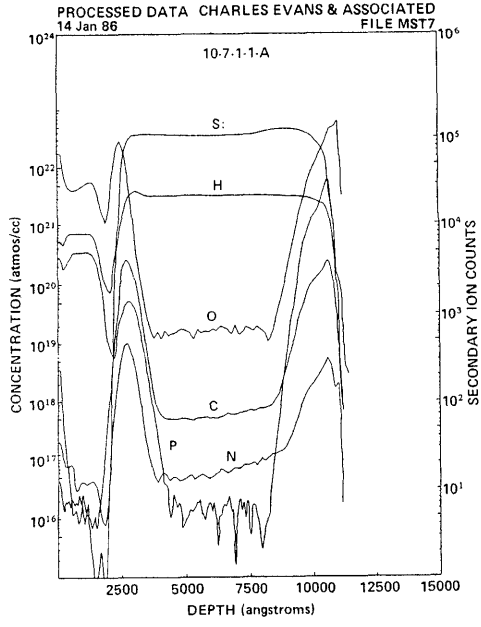

Fig. 4.
SIMS depth profile.

5. EVALUATION

The four-point probe method was used to evaluate the conversion efficiency. The light intensity of the solar simulator was calibrated as follows. The table of wavelength vs. photon number of natural sunlight (IEC [USA(AM1.5)]) was chosen as a standard[10]. The photocurrent of the photo-diode (Hamamatsu Photonix Co., S-1133 or G-1736 with special filter for solar cell) was calculated to be AM1.0 or AM1.5. In this calculation the quantum efficiency of the photo-diode was measured as a function of wavelength by the conventional constant-photon spectrometer. By the use of this photo-diode, light intensity of the solar simulator was set to be AM1.0 or AM1.5. The light intensity of the solar simulator set at AM1.0 intensity had the total light intensity of 84 mW/cm^2 when we integrated the light intensity from 0.3 to 2 μm by the use of a radio-spectrometer.

6. MODULE CHARACTERISTICS

To obtain the optimum number of solar cells which are connected in series, computer simulation was performed using the following parameters.

	A	B
-Series connection resistance for a single side contact	0.2 ohm	
-Reverse saturation current density	7.0×10^{-11} A/cm^2	
-Diode factor	1.7	
-Rsh (1 cm^2)	600 ohm	

-CTF sheet resistance	25 ohm/cm^2	10 ohm/cm^2
-CTF thickness	1000 Å	2000 Å
-Photo current density	16 mA/cm^2	15 mA/cm^2

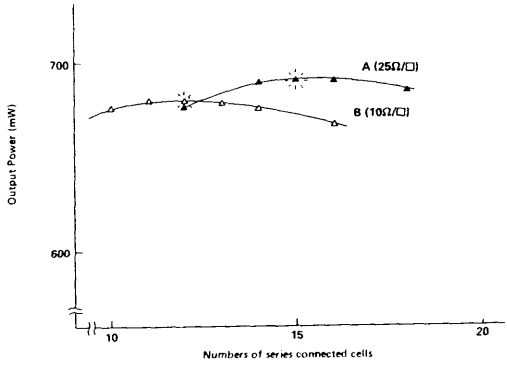

Fig. 5.
Computer simulation for the optimum number of solar cells which are connected in series.

Figure 5 is the result of the computer simulation. The 15 and 12-connection structures are preferable at a thin and thick CTFs respectively. Here a series connection of 15 cells was employed, which was expected to get the highest efficiency.

The solar cell characteristics obtained from the series-connected 15 cells are shown in Table I. As can be seen from this table an average conversion efficiency of 9.63 % was obtained with one batch of 10 substrates. Especially noted is the low standard deviation value among modules: 0.195 %. The maximum conversion efficiency attained in this sample batch is 9.90 %. The I-V characteristic is shown in Fig. 6.

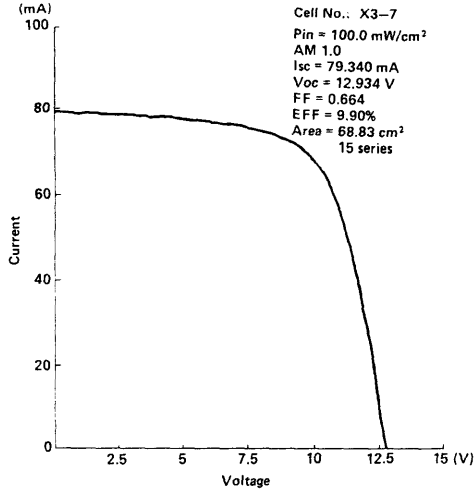

Fig. 6.
I-V characteristic of the solar cell for maximum conversion efficiency.

The parameters of our maximum efficiency solar cell are summarized as follows:

-Series resistance, Rse(ohm).....1.86E + 0.1
-Parallel resistance, Rsh(ohm).....4.01E + 0.3
-Open circuit voltage, Voc(V).....12.934
-Short circuit current, Isc(mA).....79.34
-Short circuit current density, Jsc(mA/cm^2)..17.290
-Curve factor, FF.....0.6641
-Conversion efficiency, EFF(%).....9.90
-Area(cm^2).....68.83

Table 1. Parameters of the ten integrated cells including the 9.90 % conversion efficiency cell.

CELL NO.	Voc (V)	Isc (mA)	Jsc (mA)/cm^2	FF	EFF (%)
X3-1	12.357	79.640	17.356	.6707	9.59
X3-2	12.620	80.570	17.558	.6615	9.77
X3-3	12.464	79.900	17.412	.6561	9.49
X3-4	12.389	76.540	16.680	.6796	9.36
X3-5	12.860	75.540	16.462	.6818	9.62
X3-6	12.807	77.410	16.870	.6701	9.65
X3-7	12.934	79.340	17.290	.6641	9.90
X3-8	12.630	76.950	16.770	.6575	9.28
X3-9	13.003	79.070	17.232	.6580	9.83
X3-10	12.618	69.710	17.371	.6720	9.82
Average	12.668	78.467	17.100	.6672	9.63

EFF standard deviation: 0.195%

7. CONCLUSION

We have attained an average conversion efficiency of 9.63 % with one batch of ten 100 cm^2 single junction amorphous silicon solar cells. The standard deviation of each cell is 0.195 %, which is due to the precise control of P-I interface and reliability of laser scribe process.

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