High photocurrent polycrystalline thinfilm CdS/CuInSe2 solar cella

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creases in magnetoresistance at fields predicted theoretically, including the somewhat complex yet interesting feature related to the subband dimensionality in the superlattice. Unlike the transition reported previously where semiconducting or semimetallic behaviors are obtained in different samples with different thicknesses,[5] the present one is achieved within the same sample by the use of a magnetic field as the controlling parameter.

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High photocurrent polycrystalline thin-film CdS/$CuInSe_2$ solar cell [a)]

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A polycrystalline thin-film CdS/$CuInSe_2$ heterojunction solar cell with an efficiency of 5.7% has been prepared using a simultaneous elemental evaporation technique to deposit the $CuInSe_2$ film. The cell–s short(-circuit current of 31 mA/cm^2 under 100 mW/cm^2 is the highest ever reported for a 1-cm^2 cell. Heat treatments have been found to improve cell efficiency and to also change the cell *I-V* and *C-V* characteristics.

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The heterojunction solar cell consisting of *p*-$CuInSe_2$ and *n*-CdS has been of special interest due to its demonstrated high photovoltaic conversion efficiency. A single-crystal device with an efficiency of 12% has been reported by Shay *et al.*[1] A completely vacuum deposited thin-film polycrystalline cell of this composition with characteristics of $J_{sc} = 25.1$ mA/cm^2, $V_{oc} = 0.487$ V, and efficiency $\eta = 6.6\%$ has been demonstrated by Kazmerski *et al.*[2] In this letter, we report a thin-film $CuInSe_2$/CdS cell, which was produced by a simultaneous elemental evaporation process, exhibiting an extremely high photocurrent of 31 mA/cm^2 with an efficiency of 5.7% under simulated 100 mW/cm^2 solar illumination.

Our cell is entirely prepared by vacuum evaporation and rf sputtering deposition techniques. A glazed alumina substrate is metallized with sputtered Mo (0.35 μm) and Au (0.06–0.1 μm) to serve as cell Ohmic base contact. The *p*-$CuInSe_2$ film is then deposited onto the heated metallized substrate using a simultaneous elemental evaporation process with the apparatus shown in Fig. 1. Passing the copper and indium vapor streams through a heated (1300–1400 °C) tantalum foil baffle box, leads to a mixing of the two vapors, thereby producing films of uniform composition over reasonably large substrate areas. Individual elemental evaporation rates are controlled by corresponding quartz microbalances. By appropriately adjusting the individual rates, *p*-type single-phase chalcopyrite structure $CuInSe_2$ films can be deposited. High substrate temperatures (> 450 °C) are required to form polycrystalline grain sizes of approximately 1

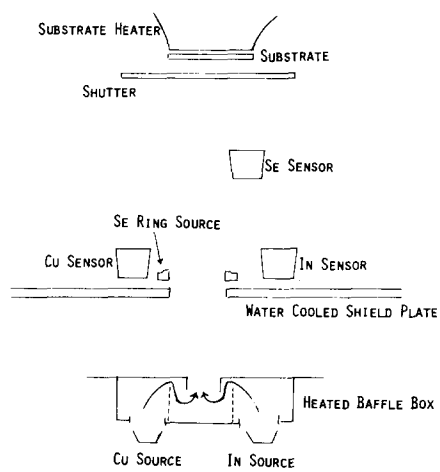

FIG. 1. Schematic drawing of elemental deposition apparatus for $CuInSe_2$ films.

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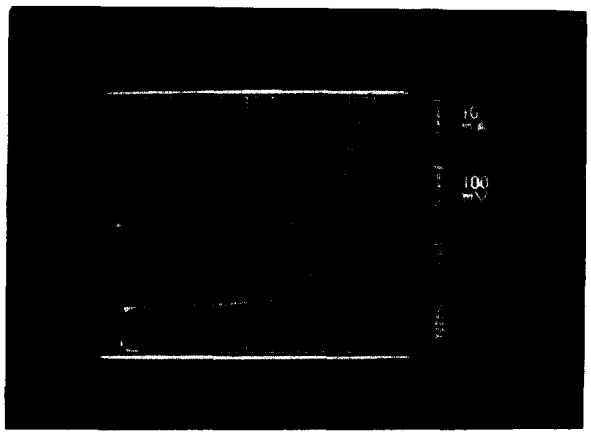

FIG. 2. Light and dark characteristics for the 1-cm^2 CdS/CuInSe$_2$ heterojunction cell. Source: 100 mW/cm^2, $V_{oc} = 0.34$ V, $I_{sc} = 31$ mA, $FF = 0.54$, and $\eta = 5.7\%$.

μm of the CuInSe$_2$ compound from the three impinging elemental species. In order to avoid creating a non-Ohmic contact by an interreaction between the selenide and gold films at the high substrate temperature, the selenide film is deposited in two steps. The first layer (1–1.5 μm) is deposited at a substrate temperature of 350 °C. This layer has low resistivity ($\sim 500\ \Omega$ cm) and small grain size ($< 1\ \mu$m). The second selenide layer is deposited at a temperature of 450 °C, which gives resistivity of approximately 1000 Ω cm and grain size of approximately 1 μm in diameter. Following the two-step selenide deposition, the substrate temperature is lowered to 150 °C for the *in situ* deposition of the 2–4-μm-thick CdS film. The CdS is evaporated from a quartz wool baffled source, and the last half (1–2 μm) is coevaporated with In ($\sim 1.5\%$) to achieve the low-resistivity material needed for low series resistance solar cell devices. Finally, a top grid contact is formed by vacuum depositing aluminum (1 μm) through a metal stencil mask. Cell area, as defined by the area of the CdS film, is 1 cm^2 and the Al grid is approximately 95% transparent.

The light and dark *I-V* curves for the polycrystalline thin-film cell after short-duration vacuum heat treatment are shown in Fig. 2. The light characteristics were obtained under 100 mW/cm^2 illumination from a tungsten-halogen source (GE type ELH lamp) calibrated with a NASA standard silicon cell. Values for the light characteristics of this cell, which did not have any antireflection coating, are: $J_{sc} = 31$ mA/cm^2, $V_{oc} = 0.34$ V; $FF = 0.54$; and efficiency $\eta = 5.7\%$. This light response was found consistent with results obtained by testing in sunlight on a clear day with an intensity of 90 mW/cm^2. The cell has a series resistance of 1 Ω and a shunt resitance of 430 Ω.

The 1-cm^2 device had an initial (before a short vacuum heat treatment) efficiency of 3.4% as shown in the detailed light characteristics (Fig. 3). After a 5-min 100 °C heat treatment in a $\sim 10^{-2}$ Torr vacuum environment, the efficiency increased to 4.8%. An efficiency of 5.7% was then achieved after an additional 90 °C 5-min treatment. The low temperature annealing dramatically increased the short-circuit current and the fill factor although a small increase in open-circuit voltage was also noted. The final short-circuit current achieved, i.e., 31 mA/cm^2, was comparable to the value of the single cell reported by Shay *et al.*, whereas the open-circuit voltage of 0.34 V was considerably smaller.[1]

The dependence of the dark current on voltage of the cell is shown in Fig. 4 before and after the heat treatment. The forward current, which was not appreciably affected by the heat treatment, varies as $\exp(qV/AkT)$ where $A = 2$, in-

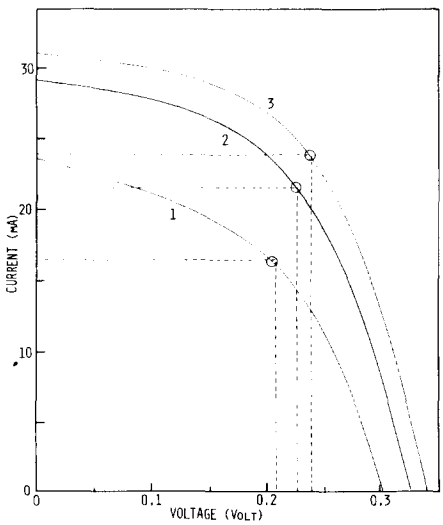

FIG. 3. Heat Treatment effects on the light characteristic of the 1-cm^2 cell. (1) Initial cell, $\eta = 3.4\%$. (2) After 5-min 100 °C, $\eta = 4.8\%$. (3) After additional 5-min 90 °C, $\eta = 5.70\%$, $FF = 0.54$, for 100-mW/cm^2 source.

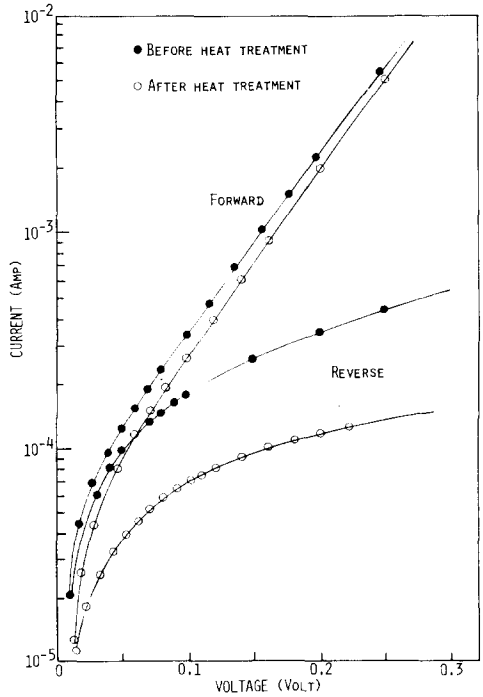

FIG. 4. Dependence of the dark current on voltage of the 1-cm^2 cell before and after heat treatment.

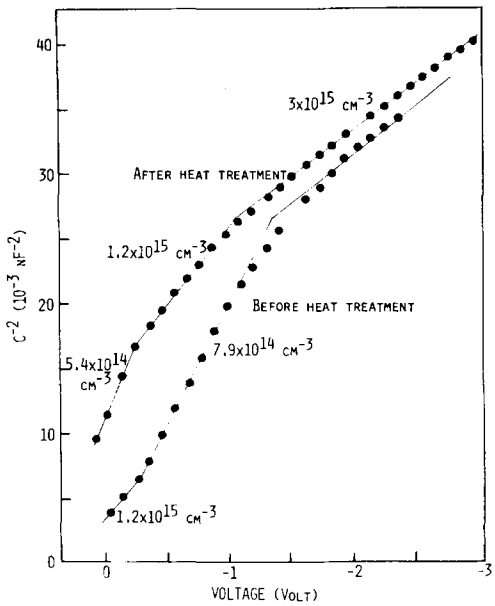

FIG. 5. Dark capacitance ($1/C^2$)-voltage characteritics of the 1-cm^2 cell before and after heat treatment. Frequency = 1 MHz.

dicating the apparent domination of the generation-recombination process for these thin-film diodes. As shown, the reverse current was greatly reduced by the mild heat treatment.

Results of C-V measurements before and after heat treatment are shown in Fig. 5 as plots of $1/C^2$ versus the bias voltage. Since the resistivity of the $CuInSe_2$ ($\sim 1000\,\Omega$ cm) is much higher than the CdS ($\sim 20\,\Omega$ cm) near the junction, most of the depletion region can be considered to be on the $CuInSe_2$ side. Further away from the junction, the net acceptor concentration in the $CuInSe_2$ is 3×10^{15} cm^{-3} and is not affected by the heat treatment. This is the low deposition temperature (350 °C) $CuInSe_2$ layer. Toward the junction, i.e., within the high deposition temperature layer, two concentration levels are observed. Both levels change with the brief low-temperature heat treatment. The greatest change occurs near the junction where the acceptor concentration decreases from an initial value of 1.2×10^{15} cm^{-3} to $\sim 5.4\times10^{14}$ cm^{-3} with heat treatment.

The specific reason for the marked improvement in cell efficiency and noticeable change in acceptor concentration near the junction following a short-period low-temperature vacuum heat treatment is yet unknown. Since the CdS deposition was performed at a higher temperature (150 °C) and for a longer duration of time (~ 15 min) than that used in the heat treatment, any interdiffusion between $CdS/CuInSe_2$ should have previously occurred during the device fabrication. Furthermore, the differences cannot reasonably be attributed to a change in the stoichiometry of the selenide film during the heat treatment, as proposed in the Cu_2S/CdS cell, because the selenide film is well protected by the CdS film. A possible explanation is that the heat treatment anneals out acceptor states (stress-induced defect states) near the junction created during high temperature deposition.

In conclusion, a polycrystalline thin-film $CdS/CuInSe_2$ heterojunction cell has been prepared with an efficiency of 5.7% by using simultaneous elemental evaporation techniques to deposit the $CuInSe_2$ film. The short-circuit current 31 mA/cm^2 under 100 mW/cm^2 is the highest ever reported for a 1-cm^2 cell. The high short-circuit current is due to a combination of the Fermi position and band bending in the high-resistivity $CuInSe_2$ which would also reduce, as observed, the open-circuit voltage (0.34 V).

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New rectifying semiconductor structure by molecular beam epitaxy

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A new unipolar rectifying semiconductor structure is demonstrated. Rectification is produced by an asymmetric potential barrier created by an MBE-grown sawtooth-shaped composition wave of $Al_xGa_{1-x}As$ between layers of n-type GaAs. Single and multiple barriers as well as doped and undoped barriers were studied and showed rectification. This is the first structure in which rectification has been produced directly by compositional grading.

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Semiconductor diodes generally achieve rectification by means of asymmetric potential barriers created by carrier-depleted charge distributions (p-n junctions) or by electron affinity discontinuities at interfaces (Schottky barriers). The shape of these barriers cannot be controlled independently of charge carrier distributions, and cascading of series

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