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Raising the one-sun conversion efficiency of III–V/Si solar cells to 32.8% for two junctions and 35.9% for three junctions

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Today's dominant photovoltaic technologies rely on single-junction devices, which are approaching their practical efficiency limit of 25–27%. Therefore, researchers are increasingly turning to multi-junction devices, which consist of two or more stacked subcells, each absorbing a different part of the solar spectrum. Here, we show that dual-junction III–V//Si devices with mechanically stacked, independently operated III–V and Si cells reach cumulative one-sun efficiencies up to 32.8%. Efficiencies up to 35.9% were achieved when combining a GaInP/GaAs dual-junction cell with a Si single-junction cell. These efficiencies exceed both the theoretical 29.4% efficiency limit of conventional Si technology and the efficiency of the record III–V dual-junction device (32.6%), highlighting the potential of Si-based multi-junction solar cells. However, techno-economic analysis reveals an order-of-magnitude disparity between the costs for III–V//Si tandem cells and conventional Si solar cells, which can be reduced if research advances in low-cost III–V growth techniques and new substrate materials are successful.

The cost of photovoltaic (PV) modules has decreased dramatically in recent years, while their efficiency has increased steadily, resulting in a stronger economic competitiveness compared with traditional energy sources and grid parity in many locations. However, without further increases in cell and module efficiency, the potential for future reductions in module costs per watt and total installed system costs is limited. Especially in small or space-constrained systems, balance-of-system costs significantly exceed module costs, such that improved efficiency can substantially lower overall system costs[1]. Today, the optimization of Si solar cells—the dominant photovoltaic technology—focuses mainly on the minimization of shadow losses caused by the front metallization and on the reduction of recombination losses at the surfaces and below metal contacts. Thereby, cell efficiencies exceeding 25.0% have been achieved by different research institutes and companies (25.2%, Sunpower[2]; 25.7%, Fraunhofer ISE[3]; 25.6%, Panasonic[4]), and a new record of 26.7% cell efficiency[5] was set by Kaneka in early 2017. However, this record efficiency is only 2.7% lower than the theoretical efficiency limit for silicon-based single-junction devices of 29.4% under one-sun illumination[6], suggesting that the efficiency potential of Si single-junction solar cells will soon be fully exploited. Other cell technologies, such as CdTe, CIGS and perovskites, typically rely on single-junction architectures as well and have demonstrated efficiencies exceeding 22% (ref. 5), but their theoretical efficiency is also limited to 30–33%, due to thermodynamic principles.

One way to overcome these efficiency limitations is to stack several solar cells on top of each other in a multi-junction design. In these devices, each junction is optimized to absorb and convert a different part of the solar spectrum at different voltages, reducing thermalization losses. Indeed, the highest conversion efficiency of solar energy into electricity has been reached with III–V semiconductor multi-junction solar cells enabling cell efficiencies up to 38.8% (ref. 7) under one sun and up to 46% (refs 8,9) under concentrated sunlight. Despite these impressive efficiencies and their application on satellites, the currently high costs of III–V solar cells have precluded their use for terrestrial, non-concentrator applications. To utilize multi-junction architectures for one-sun terrestrial PV, tandem-cell devices with Si bottom cells appear on the roadmap of many Si PV companies. The transition from Si single-junction to Si-based multi-junction solar cells will allow manufacturers to achieve module efficiencies over 30%, while still benefiting from their expertise and well-established Si cell production lines. A key challenge in this cell development is to prove that the inclusion of a subcell cheaper than III–V leads to a comparable or superior multi-junction cell performance.

Numerical simulations have predicted theoretical one-sun efficiencies exceeding 40% for Si-based dual-junction (2J) solar cells whose subcells are electrically isolated and operated independently (four-terminal) but optically coupled, for top cells with bandgap energies E_g of 1.4–2.3 eV (ref. 10). Various wide-bandgap top-cell materials have been discussed in the literature[10,11] but current research focuses mainly on III–V (refs 12–15) or perovskite[16,17] semiconductors. III–V solar cells are known to be highly efficient and have excellent proven reliability, which translates to less perceived investment risk and thus lower interest rate loans for installations. Furthermore, the maturity of the III–V solar cell technology also allows the investigation of Si-based triple-junction (3J) solar cells in which the short-wavelength light is

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Table 1 | Summary of the characteristic solar cell parameters.

	V_{OC} (mV)	J_{SC} (mA cm^{-2})	FF (%)	Cell efficiency (%)	Tandem-cell efficiency (%)
GaInP//Si dual junction					
GaInP top cell	1,453.8 (±8.7)	15.78 (±0.21)	87.0 (±0.3)	19.95 (±0.28)	
Si bottom cell#	694.3 (±4.2)#	23.11 (±0.30)#	77.9 (±0.2)#	12.50 (±0.18)#	32.45 ± 0.33
Si bottom cell*	696.0 (±4.2)*	24.44 (±0.32)*	78.0 (±0.2)*	13.26 (±0.19)*	
GaAs//Si dual junction					
GaAs top cell	1,092.1 (±6.6)	28.90 (±0.38)	85.0 (±0.3)	26.83 (±0.38)	
Si bottom cell#	682.8 (±4.1)#	11.07 (±0.14)#	79.2 (±0.2)#	5.99 (±0.08)#	32.82 ± 0.39
Si bottom cell*	697.0 (±4.2)*	17.54 (±0.23)*	79.2 (±0.2)*	9.68 (±0.14)*	
GaInP/GaInP//Si triple junction					
GaInP/GaAs 2J top cell	2,520.0 (±25.2)	13.61 (±0.20)	87.5 (±0.7)	30.01 (±0.42)	
Si bottom cell#	681.1 (±4.1)#	11.03 (±0.14)#	78.5 (±0.2)#	5.90 (±0.08)#	35.91 ± 0.43
Si bottom cell*	687.6 (±4.1)*	13.47 (±0.18)*	78.4 (±0.2)*	7.27 (±0.10)*	
GaInP/GaInP//Si 3J (two-terminal)	3,206.8 (±28.9)	10.78 (±0.14)	89.4 (±0.6)	n/a	30.93 ± 0.43

NREL-certified cell characteristics of the four-terminal GaInP//Si and GaAs//Si dual-junction and GaInP/GaAs//Si triple-junction solar cells measured under AM1.5g spectral conditions at 25 °C. The bottom-cell *J*–*V* curves were measured while the III–V top cells were either at open-circuit condition (data labelled with *) or biased close to the maximum power point P_{mpp} (data labelled with #); the latter simulates operating conditions in the field. The tandem-cell efficiency is the cumulative efficiency of the III–V top cell and the Si bottom cell measured while the top cell is operated at P_{mpp} (#). The GaInP/GaAs//Si 3J device was additionally characterized when all cells were connected in series (two-terminal). The numbers in the brackets are the estimated measurement uncertainties of each parameter (V_{OC}, J_{SC}, FF, cell efficiency). The uncertainties given for the tandem-cell efficiencies are the cumulative uncertainties of the two subcells, assuming uncorrelated measurements. The illuminated areas of the GaInP//Si, GaAs//Si and GaInP/GaAs//Si cells were 1.005(±0.002) cm^2, 1.003(±0.002) cm^2 and 1.002(±0.002) cm^2, respectively. These areas include the metal grids but not the surrounding busbars.

converted by two instead of one subcell with $E_g > 1.12$ eV, leading to higher theoretical one-sun efficiencies over 49% (ref. 10).

The fabrication of two- and four-terminal III–V/Si tandem solar cells, and in particular the integration of III–V and Si subcells, has been investigated for over two decades[18]. Recently, there has been great progress in the metalorganic vapour phase epitaxy (MOVPE) of III–V solar cells[19–21] on Si; however, their efficiencies are still limited by growth defects in the top cell and degradation of the Si bottom cell during the III–V epitaxy. Thus, tandem cell efficiencies exceeding 25% could so far be achieved only when the two cells were fabricated separately and joined at low temperature by wafer bonding[14,22,23] or mechanical stacking[12,15,24]. In contrast to wafer bonding, mechanical stacking eliminates the need for tunnel junctions and requires neither polished wafer surfaces nor a clean room environment, and hence offers a lower-cost solution. In addition, this architecture is amenable to a wide variety of different top-cell materials, which can be fabricated on the module front cover glass and integrated with a rear Si cell without major changes to the module design.

In this paper, we demonstrate several four-terminal III–V//Si tandem cells with efficiencies similar to or exceeding purely III–V-based devices, proving for the first time that lower-cost cell technologies can be viable for multi-junction applications. The double slash (//) denotes that the subcells were integrated by stacking, rather than monolithically grown. Record one-sun conversion efficiencies of 32.5% and 32.8% (AM1.5g) were achieved for III–V//Si 2J solar cells based on mechanical stacking of 1.81 eV GaInP and 1.42 eV GaAs top cells, respectively, on silicon heterojunction bottom cells. In addition, we present a 35.9%-efficient Si-based 3J solar cell featuring a monolithic GaInP/GaAs 2J top cell. To evaluate the near- and long-term economic competitiveness, we performed a detailed cost analysis of mechanically stacked four-terminal III–V//Si solar cells including a pathway towards a future cost reduction of III–V/Si multi-junction devices.

Above 32% efficiency for III–V//Si dual-junction solar cells

Our dual-junction solar cells consist of a III–V single-junction top cell stacked on top of a narrower-bandgap Si bottom cell. For maximum tandem-cell efficiency, the Si bottom cell needs an excellent spectral response for long-wavelength light and should generate a high open-circuit voltage (V_{OC}). Both are provided by a-Si:H/c-Si heterojunction solar cells (SHJ)[25] whose main limitation, the parasitic absorption losses in the short-wavelength region, becomes negligible when applied as a bottom cell. The optimum top cell in a four-terminal Si-based dual-junction solar cell has a bandgap of 1.7–1.9 eV (refs 10,24) and a high external radiative efficiency (ERE), which describes the fraction of radiative recombination compared with the total recombination current in a solar cell[26,27]. In the desired top-cell bandgap energy range, the highest cell efficiencies of 21.4% (refs 5,28) and 20.8% (ref. 27) have been achieved by 1.8 eV GaInP cells with metallic reflectors underneath the III–V layers, boosting the cell voltage through photon recycling[27,29]. The ERE of these record GaInP cells equals about 10% (ref. 10). While this is considerably lower than the 32% ERE (ref. 10) reached by the record 28.8% efficient 1.42 eV GaAs single-junction solar cell from Alta Devices[5,30], the GaInP cell has a more optimal bandgap for a tandem cell. Taking both of these considerations into account, ref. 10 suggests that with state-of-the-art technology, slightly higher tandem-cell efficiencies may be achieved with GaAs//Si 2J solar cells (four-terminal), despite the imperfect bandgap matching. The same conclusion was drawn in ref. 11 by comparing the spectral efficiencies of different top-cell candidates. Consequently, the development of both GaInP//Si and GaAs//Si 2J solar cells is relevant.

Schematic cross-sections and photos of the 1.0-cm^2-sized GaAs//Si and GaInP//Si 2J solar cells are shown in Fig. 1. The GaInP top cells show bright red photoluminescence under illumination (Fig. 1d), indicative of good ERE. The external quantum efficiencies (EQEs), reflectance (*R*) and light *J*–*V* curves of the 2J devices are shown in Fig. 2 and summarized in Table 1. The 1.81 eV GaInP top cell has a rear-heterojunction design similar to ref. 27 and is transparent to some visible light close to the bandgap of GaInP (see EQEs in Fig. 2a). With a fill factor (FF) of 87.0% (Table 1) and ERE[26] of 5%, it reaches a one-sun efficiency of 19.95%, which is only 1.4% lower than the 21.4% record GaInP cell with metallic back reflector from LG Electronics[28]. It should be noted that a high angle-averaged reflectance from intermediate layers, such as the glass slide used here, can contribute to significantly enhanced photon recycling[31]. The SHJ bottom cell in the GaInP//Si device reaches an efficiency of 12.5%, leading to a cumulative 2J cell efficiency of (32.5 ± 0.3)% (Table 1). This efficiency is 2.7% absolute higher

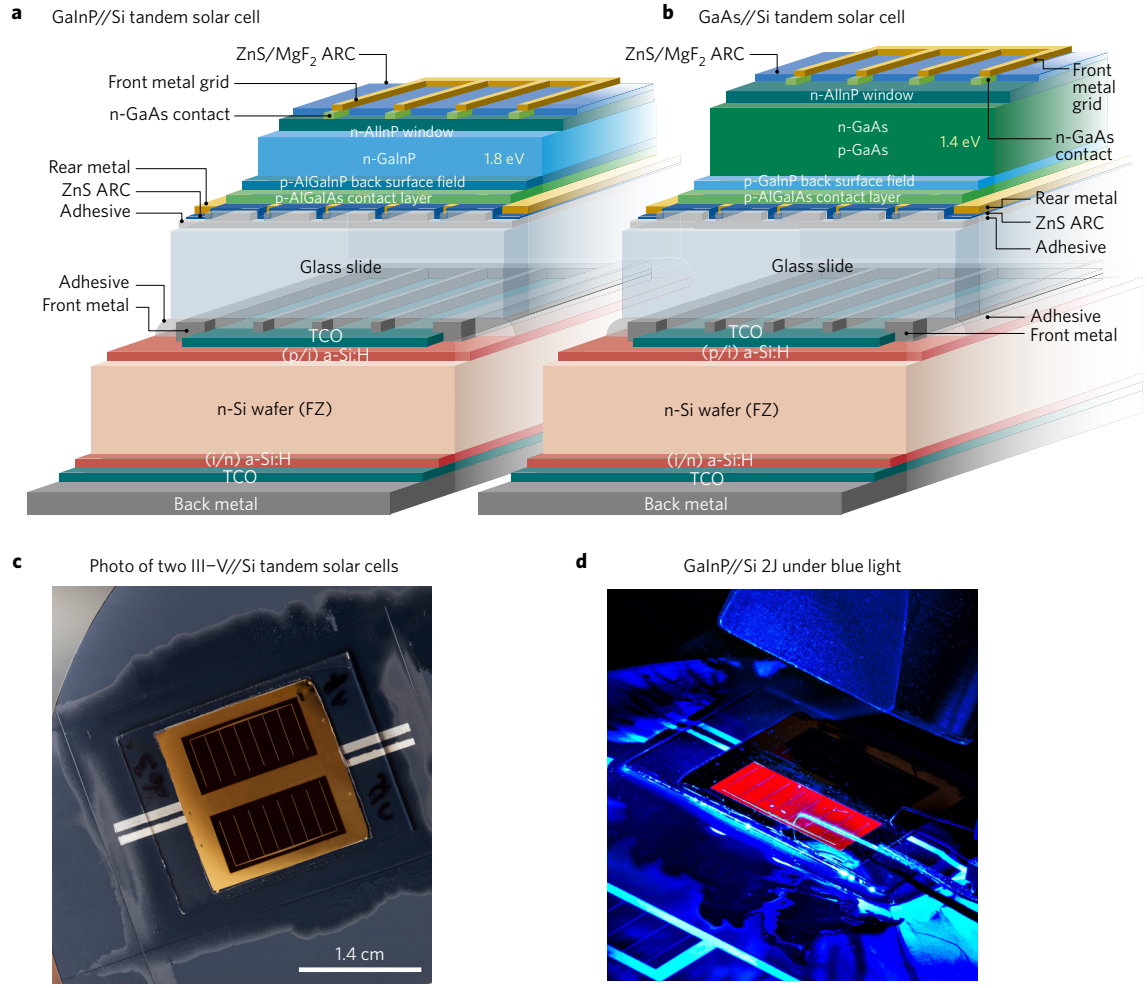

Figure 1 | Design of the III–V//Si tandem solar cells. a,**b**, Schematic cross-sections (not to scale) of the four-terminal GaInP//Si and GaAs//Si dual-junction solar cells. Each III–V top cell has aligned metal grids and antireflection coatings (ARCs) on the front and rear side, and is attached to a glass slide, which is stacked on the separately fabricated SHJ cell using a transparent adhesive. **c**, Photo of two III–V//Si tandem solar cells with 1.01 cm^2 designated illumination areas. The long silver metal bars are used to contact the front metal grid of the bottom cell. **d**, Photo of a GaInP//Si tandem solar cell under illumination with blue light and at open-circuit conditions. Due to a high ERE, the top cell emits red light.

than previously reported with a similar GaInP//Si 2J cell design[12] of 29.8%; an EQE comparison of the old[12] and our new record devices is shown in Fig. 2c. The GaInP top cells in both devices have the same structure, which is based on the cell developments described in detail in ref. 27. The improvements in the GaInP top cell are mainly due to improved interface quality through more rapid MOVPE valve switching by replacing leaking solenoids, and the ultimate device reported here is quite similar in performance to our previous single-junction record cell reported in ref. 27. The EQE and dark J–V of the GaInP cell reported here can be modelled with the Hovel model[32] using minority hole emitter diffusion length (L_p) of 2.2 μm, interface recombination velocity (S_p) of 200 cm s^{-1}, mobility of 40 cm^2 V^{-1} s^{-1}, and lifetime of 130 ps. While the lower EQE of our previous result[12] could be modelled either by inferior bulk properties (L_p = 1.5 μm) or interface quality (S_p = 1,700 cm s^{-1}), the fact that the V_{OC} did not change significantly points strongly towards the interface quality rather than bulk quality. Compared with ref. 12, reflection losses in the tandem device were reduced by better control of the antireflective coating (ARC) layer thicknesses. We also mitigated the impact of various loss mechanisms in the SHJ bottom cell. Firstly, the overlapping area between the transparent conductive oxide (TCO) and Ag front contact has been minimized to reduce the non-illuminated area of the pn junction to 0.016 cm^2 and the resulting dark saturation current[24]. Secondly, in contrast to ref. 12, the tandem cells were not separated from the neighbouring devices, which lowers the edge recombination losses. Finally, the overall bottom-cell performance was improved by using wafers with higher bulk lifetime and superior a-Si:H passivation, resulting in an effective minority carrier lifetime boost from 4.2 ms to 11.1 ms at an injection level of 5 × 10^{14} cm^{-3}. The SHJ bottom cells had front and rear TCO layer thicknesses adjusted for optimum red response, tailored to their top cells, to maximize performance in a tandem architecture.

As predicted, the GaAs//Si tandem cell performed slightly better than the GaInP//Si cell despite imperfect bandgap matching. The EQEs of our four-terminal GaAs//Si 2J cell are shown in Fig. 2b. The 1.4 eV GaAs top cell has an ERE of ~10%, slightly higher than the GaInP cell, and achieves a cell efficiency of 26.8% (Table 1). It transmits only light with a wavelength longer than 870 nm to the SHJ cell, whose front TCO was 30 nm thicker than in the GaInP//Si tandem device to increase the EQE in the long-wavelength range (see Fig. 2b). With a J_{SC} of 11.1 mA cm^{-2}, the SHJ bottom cell contributes 5.99% efficiency to the tandem device, significantly lower than the Si cell contribution in the GaInP//Si device (12.5%) due to the top cell's lower bandgap. The resulting cumulative one-sun efficiency of our GaAs/Si tandem solar cell equals (32.8 ± 0.4)%, slightly higher than the GaInP//Si device, mainly due to the relatively better performance of GaAs compared

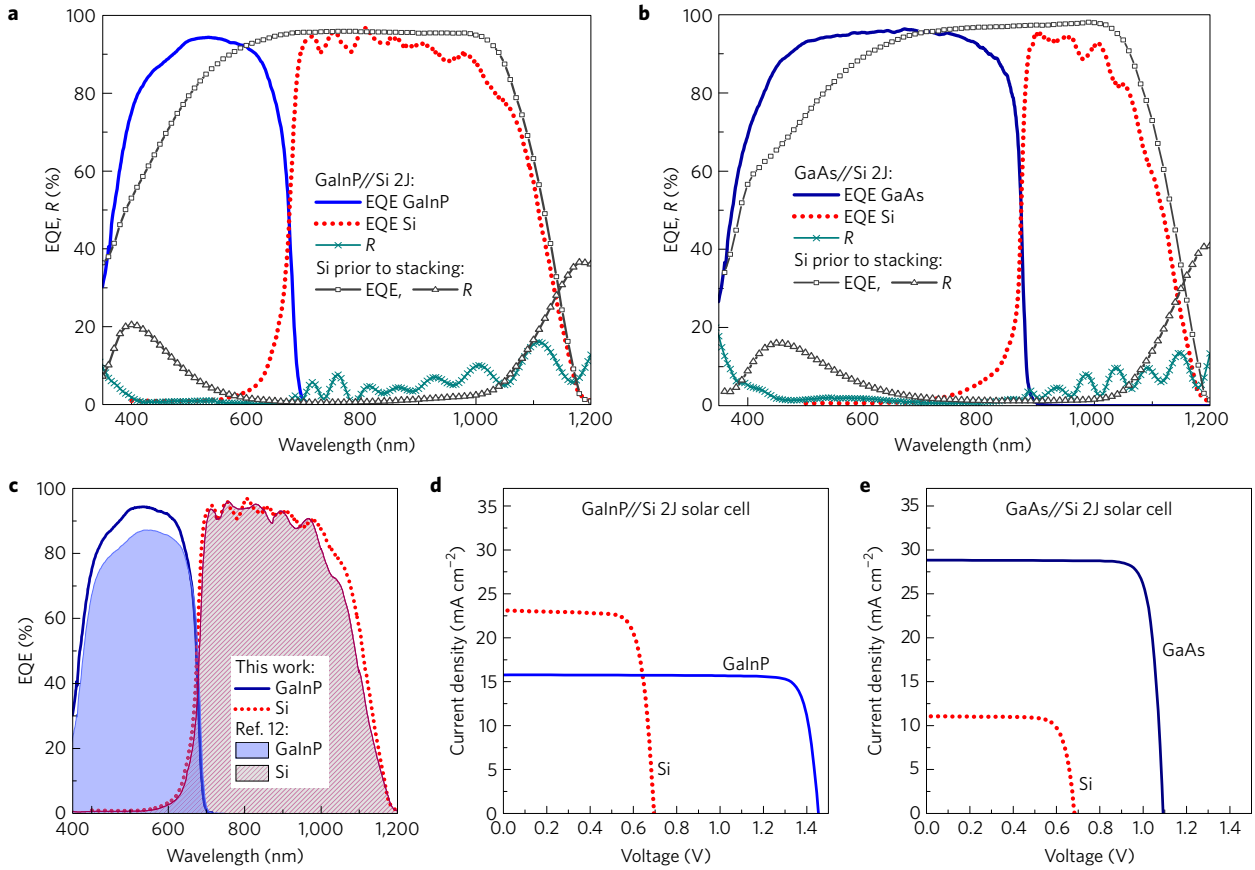

Figure 2 | Photovoltaic performance of the mechanically stacked III–V//Si 2J devices. a, External quantum efficiency (EQE) and reflection (*R*) curves of the GaInP//Si dual-junction solar cell and the Si heterojunction solar cell before stacking. **b**, EQE and *R* curves of the GaAs//Si dual-junction solar cell and the used Si heterojunction solar cell before stacking. **c**, EQE comparison of the 29.8%-efficient GaInP//Si dual-junction solar cell from ref. 12 (shaded area) and the improved 32.5% device presented here. **d**, NREL-certified *J*–*V* characteristics of each subcell of the GaInP//Si dual-junction solar cell when illuminated under AM1.5g spectral conditions at 25 °C. To simulate operation under load, the bottom-cell *J*–*V* curve was measured while the top cell was biased at its maximum power point (see Methods). This provides a realistic accounting for the effect of luminescent coupling, which leads to a very significant increase in the generation of carriers when the top cell is at V_{OC} (see Table 1 and ref. 12). **e**, NREL-certified *J*–*V* characteristics of each subcell of the GaAs//Si dual-junction solar cell when illuminated under AM1.5g spectral conditions at 25 °C. The bottom-cell *J*–*V* curve was measured while the top cell was biased at its maximum power point.

with GaInP for its absorbed spectral range. This efficiency is the highest one-sun efficiency ever reported for Si-based 2J solar cells; it is slightly higher than the record one-sun efficiency of 32.6% (ref. 33) recently achieved by NREL with a monolithic all III–V two-terminal device with current-matched 1.1 eV and 1.7 eV subcells, and significantly higher than the 31.6% record efficiency[34] achieved with lattice-matched dual-junction GaInP/GaAs cells by Alta Devices.

III–V//Si 3J solar cells approaching 36% efficiency

Replacing the GaAs top cell in the Si-based tandem cell with a GaInP/GaAs dual-junction solar cell can further reduce the thermalization losses, and thus leads to an even more efficient conversion of the short-wavelength light. Tuning of the top-cell bandgap energies and thicknesses may also enable fully current-matched 3J devices in which each subcell generates the same photocurrent density. To realize a GaInP/GaAs//Si 3J solar cell, we stacked monolithic GaInP/GaAs 2J solar cells on SHJ bottom cells with a thicker front TCO (see Fig. 3) using the same technology as for the aforementioned 2J devices. The III–V cells are connected in series by a tunnel diode and generate a photocurrent density of 13.6 mA cm^{-2} (Table 1 and Fig. 4b). When operated under this 30.0% efficient III–V tandem cell, the SHJ bottom cell achieves an efficiency of 5.9%, leading to a cumulative 3J cell efficiency of (35.9 ± 0.4)%; this is only 2.0% lower than the 37.9% (ref. 35) record efficiency achieved with inverted metamorphic III–V 3J devices, but does not require metamorphic layers. When connecting all subcells in series, our III–V//Si 3J cell reaches a lower efficiency of (30.9 ± 0.4)% due to photocurrent limitation by the bottom cell (see Fig. 4a). In comparison, wafer-bonded GaInP/AlGaAs//Si 3J solar cells developed by Fraunhofer ISE[23], which were optimized for two-terminal operation and in which the III–V and Si subcells are connected by tunnel junctions, recently reached record one-sun efficiencies up to 32.3%, as presented at a conference[36]. The comparison of our two- and four-terminal efficiencies clearly shows that independent operation of the subcells is more tolerant to the variations in the bandgap energy and solar spectrum.

Future optimization of the subcells and their optical coupling may enable even higher III–V/Si tandem-cell efficiencies. The GaAs-top-cell efficiency of 26.8% is still lower than the 28.8% efficient record cell from Alta Devices[30,34]. Improved growth conditions of the GaAs cell could therefore increase the GaAs//Si 2J efficiency by ~1–1.5%, assuming some loss due to the absence of a back reflector on the top cell. Further research may also enable improvements of the GaInP top cell, which has received significantly less research attention than GaAs; this could ultimately result in a superior performance of GaInP//Si compared with GaAs//Si 2J solar cells. Turning to the SHJ bottom cell, simulations in ref. 12

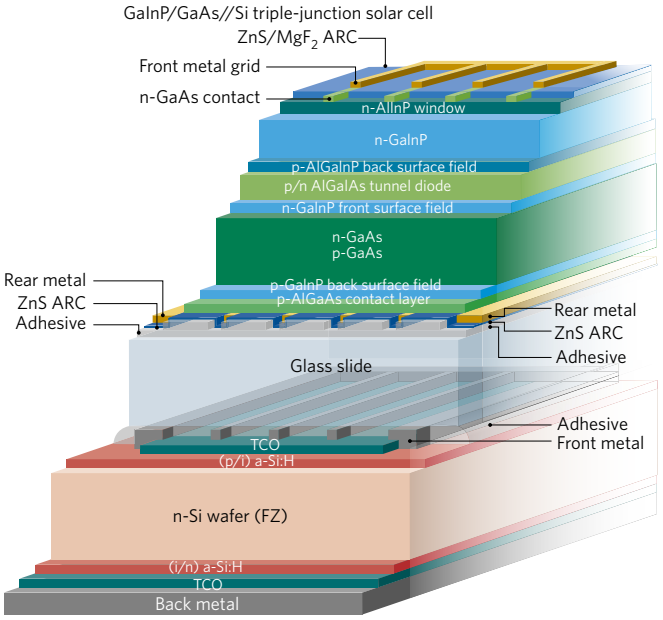

Figure 3 | Design of the four-terminal GaInP/GaAs//Si triple-junction solar cell. The GaInP top and GaAs middle cell are connected via a tunnel junction and stacked on a Si heterojunction solar cell (the schematic is not to scale).

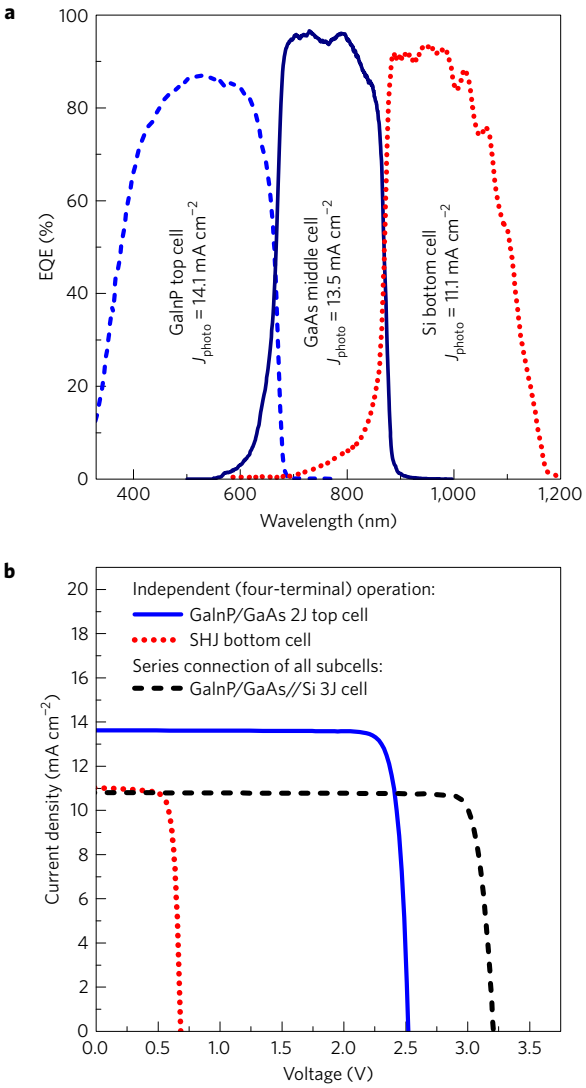

Figure 4 | Photovoltaic performance of our best four-terminal GaInP/GaAs//Si triple-junction solar cell. a, EQE of the three subcells; the GaInP top and GaAs middle cell are connected via a tunnel junction. The photocurrent densities J_{photo} generated by each subcell were calculated for AM1.5g spectral conditions. **b**, NREL-certified *J*–*V* characteristics of the GaInP/GaAs top cell and the Si bottom cell when illuminated under AM1.5g spectral conditions at 25 °C. The bottom-cell *J*–*V* curve was measured while the top III–V tandem cell was biased at its maximum power point.

have shown that with the present cell architecture the J_{SC} could be improved to 23.4 mA cm^{-2} in GaInP//Si tandem cells, provided that the red response can be further improved. When characterizing our SHJ cells as single-junction devices under filtered light with J_{SC} of 23.1 mA cm^{-2}, we achieved a V_{OC} of 709 mV and efficiency of 13.1%, which is 0.6% higher than in our current record GaInP//Si 2J device. The performance drop is attributed to a degradation induced by mechanical stress during the stacking process and handling. Larger device sizes should also help to reduce edge effects, which lowers the FF of small crystalline Si cells with effective diffusion lengths of several millimetres. This indicates that 34–35% efficiency could be possible with mature two-junction cell technologies and up to 40% with 3J devices.

Costs of III-V//Si multi-junction solar cells

To assess the viability of this tandem-cell concept for industrial applications, we have performed bottom-up techno-economic analysis. Cost analysis of the III–V//Si multi-junction solar cells is based on models developed by NREL that explore all of the processing used to manufacture III–V and silicon-based solar cells. Both process steps and cost inputs are constantly evolving, and this process flow and analysis represent costs to the best of our knowledge at the present date. The baseline process flow envisioned for industrial-scale fabrication is sketched in Fig. 5 for the case of a GaInP//Si 2J device with similar architecture to our record device, assuming slight modifications to enhance manufacturability (see Supplementary Fig. 1 for GaAs top cells).

We explored the US dollar per watt costs associated with near-term, mid-term and long-term scenarios, which assume successive advances in processing and engineering of the III–V cell as well as increasing production volumes (from 50 MW yr^{-1} in the near term to 1 GW yr^{-1} in the long term, detailed assumptions summarized in Supplementary Table 1). Any additional decreases in the cost of the silicon bottom cell will further reduce the cost of the tandem device and are not included here.

Our modelled near-term fabrication process (details described in Methods) leads to cell costs of US$4.85 W^{-1} and US$7.17 W^{-1} for 30% efficient mechanically stacked GaInP//Si and GaAs//Si 2J solar cells (Fig. 6 and Supplementary Fig. 2) and US$8.24 W^{-1} for 35% efficient four-terminal GaInP/GaAs//Si 3J solar cells (Supplementary Fig. 3). These numbers are one order of magnitude higher than for commercially available silicon cells, and than the typical modelled cost of US$0.3–0.35 W^{-1} (ref. 37) for the SHJ bottom solar cells. The disparity in cost is driven by the high cost of the GaAs wafer and epitaxy of the III–V solar cell stack. The III–V PV industry has focused on developing device epitaxial lift-off (ELO)[38] and substrate reuse techniques to reduce the impact of the expensive substrate[39]. While this approach has been implemented by several companies, the ability to achieve the very high (>100) number of substrate reuses required to achieve low costs while maintaining high manufacturing yields has not yet been publicly demonstrated, and may be challenging. Recreating an epi-ready surface for additional MOVPE growth after ELO is critical, but the cost of chemo-mechanical polishing (CMP) is extremely large (~US$30 per CMP step). In our near-term scenario, we consider 50

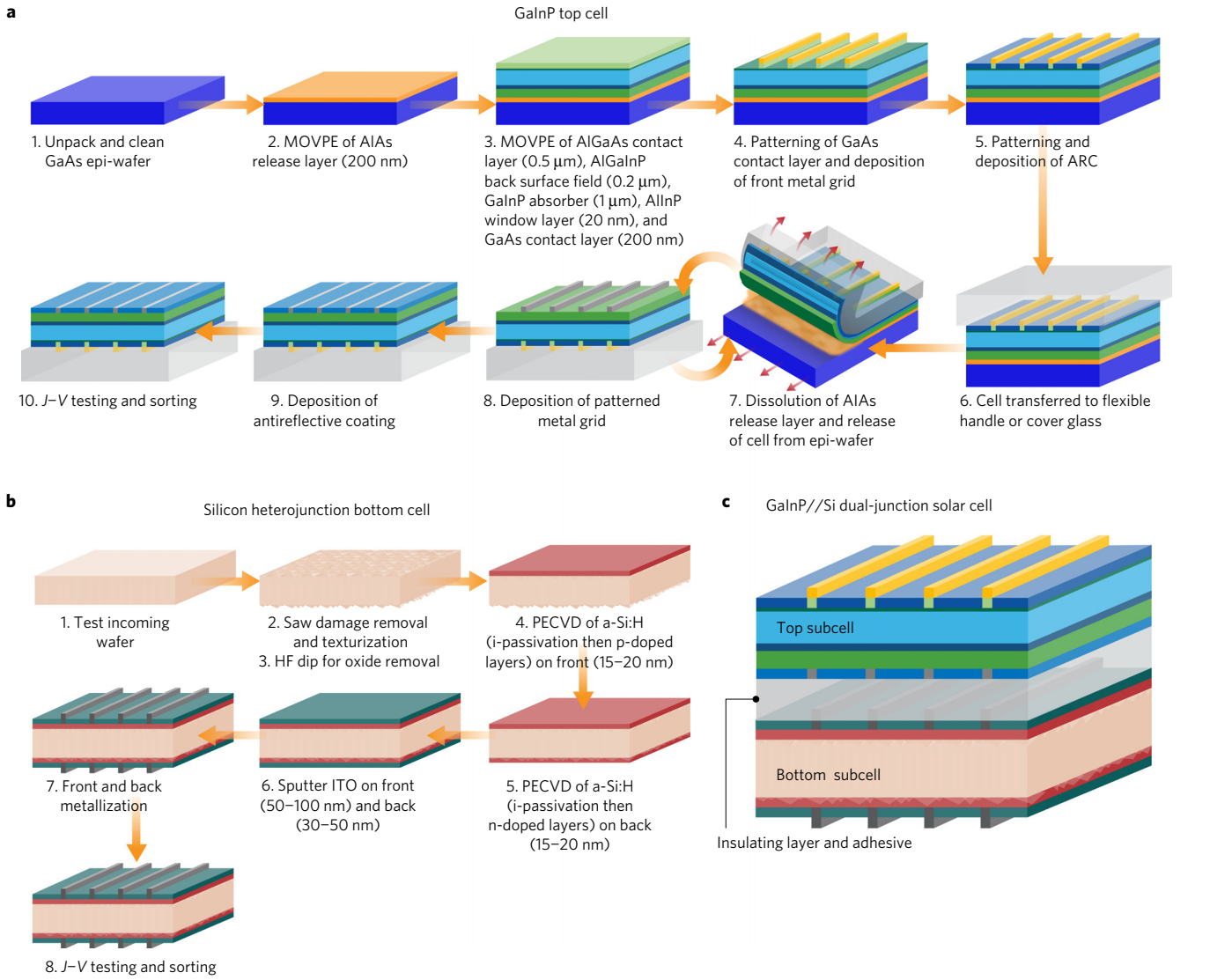

Figure 5 | Fabrication process flow considered in our techno-economic analysis (near term). a, Process steps for fabrication of GaInP top cells: an AlAs sacrificial layer and the upright (not inverted as in our experiment) III–V device structure are deposited on a GaAs growth substrate. Next, front metal contacts are applied by electroplating, the GaAs contact layer is patterned and an antireflective coating (ARC) is deposited by plasma-enhanced chemical vapour deposition (PECVD). The solar cell stack is released from the growth substrate by an ELO process[38], followed by rear metallization and ARC deposition. Finally, the III–V solar cells are tested and sorted. **b**, Process flow for the fabrication of bifacial SHJ bottom cells: after testing, cleaning and texturing 180-µm-thick silicon wafers, the cell processing continues with PECVD of a-Si:H layers and sputtering of TCOs, which is followed by metal screen printing and *J–V* characterization. **c**, GaInP//Si dual-junction solar cell after stacking of the top and bottom cells using an insulating transparent adhesive.

substrate reuses with one CMP step per 10 reuses. In the long-term scenario, we assume that low-cost substrates with a cost similar to silicon will be available that do not need to be reused. This could be achieved by growing the III–V cell directly on silicon, lowering the cost of GaAs or similar substrates by improving manufacturing methods, or by developing a new substrate material. Any of these solutions would require further research and development. Ideally, this new substrate material would be etched away, mechanically separated[40] or included in the device, depending on its properties.

Low-cost III–V epitaxy has also been identified in our analysis as an important factor in driving down the cell costs. The growth costs of 2-µm-thick 1.4-eV GaAs top cells are, in the near-term scenario, 1.7 times higher than the costs of the 1-µm-thick 1.8-eV GaInP top cell, accounting for two-thirds of the total tandem-cell costs. Several groups have reported impressive progress in the development of low-cost growth techniques by high-growth-rate MOVPE[41], close-space vapour transport[42] and hydride vapour phase epitaxy (HVPE)[43]. Our mid- and long-term scenarios assume HVPE growth, but alternative techniques may result in similar cost reductions, assuming they address the critical factors of tool throughput and precursor cost. Further reductions (beyond the long-term case) in deposition costs may also be possible—since HVPE is not yet a commercial process, its long-term cost potential is still uncertain. Bringing these advances together, along with the expected improvements in process yields, scaled-up manufacturing, and improvements in tandem-cell efficiency from 30% (near term) to 35% (long term), we project a long-term cost of US$0.66 W^{-1} (US$0.85 W^{-1} for GaAs//Si case) for a complete GaInP//Si dual-junction cell. Correspondingly, the cost of the GaInP/GaAs//Si 3J cell with long-term efficiency of 40% decreases to US$0.79 W^{-1} (Supplementary Fig. 3), which equals ~10% of the near-term costs. This price drop seems large; however, it is not unrealistic considering the history of PV: within only five years, from 2006 to 2011, the costs of PV modules manufactured in China decreased from US$4.5 W^{-1} to US$1 W^{-1} (ref. 44), and since 1980, the costs of photovoltaic modules have decreased on average about 10% per year[45].

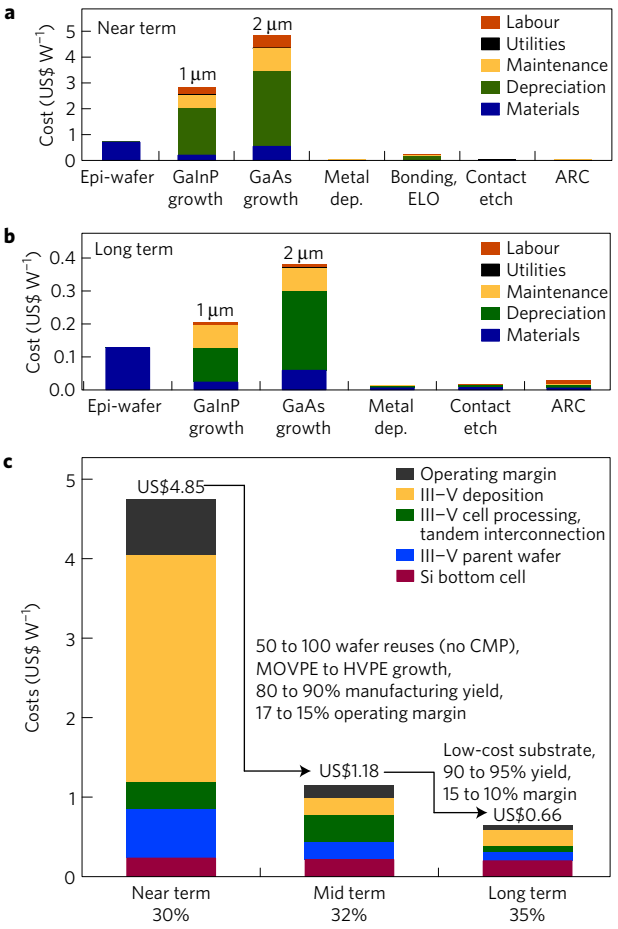

Figure 6 | Modelled costs of the III-V//Si dual-junction solar cells assuming an increase in tandem-cell efficiency from 30% (near term) to 32% (mid term) and 35% (long term). Further assumptions are explained in the text and summarized in Supplementary Table 1. **a**, Near-term costs for the fabrication process of GaInP and GaAs top cells. In each case, either the GaAs growth cost or GaInP growth cost would be included, depending on the cell. All other costs are identical for both types of cell. **b**, Long-term costs for the fabrication process of GaInP and GaAs top cells considering HVPE growth and low-cost growth substrates. Like in **a**, either the GaAs growth cost or GaInP growth cost would be included, depending on the cell. **c**, Roadmap towards cost-effective III-V//Si dual-junction solar cells, based on the GaInP top-cell case (see Supplementary Fig. 2 for the GaAs case).

While the long-term costs of the III–V//Si tandem cells are still higher than that of single-junction Si cells, the higher efficiency enables reductions in balance-of-system (BOS) costs[1]. In the United States, current module costs comprise only 20–40% of the total system cost, depending on the sector. Increasing cell efficiency from 18% (typical for standard c-Si cells today) to 35% could reduce BOS costs by US$0.22 W^{-1}, US$0.45 W^{-1} and US$0.44 W^{-1} for utility-scale (100 MW), commercial (200 kW) and residential (5.6 kW) installations respectively[1]. The higher efficiency would also enable additional reductions in balance-of-module costs, or the non-cell module costs (for example, the cost of glass, back sheet, EVA and so on). If the module configuration and manufacturing process were identical to that of standard c-Si modules today, balance-of-module savings would be approximately US$0.09 W^{-1}, thus about 6% of the total system costs. These cells could be particularly applicable in markets where performance is highly valued and/or area is constrained. They may also be applicable to low-concentration systems, providing a higher efficiency than single-junction c-Si cells at a lower cost than dual-junction III–V cells.

If III–V cell costs can be reduced to the levels shown in our long-term scenario, costs associated with the silicon subcell approach up to 40% of the total tandem-cell cost, and thus the inclusion of both Si and III–Vs is justified[46]. If the III–V costs cannot be brought to these levels, alternative top-cell materials that are cheaper, yet still very efficient and reliable, will be required to achieve cost competitiveness in general power markets. Promising alternative top-cell materials include perovskites[47] and CdZnTe[48], which are emerging technologies that require improvements in efficiency and stability to rival the III–Vs presented here. The mechanically stacked architecture that is presented here is agnostic to top-cell type, and simply requires that the top cell is attached to the module front glass in a superstrate configuration. Since no tunnel junctions are required, and the devices are not current-matched, a wide variety of options are available. These configurations circumvent concerns about materials compatibility for monolithic growth, as well, and enable the use of fully textured Si bottom cells. Importantly, mechanically stacked modules are modular, enabling new cell designs to be straightforwardly swapped out as both top- and bottom-cell technologies and manufacturing processes evolve.

Conclusions

The work presented here shows that silicon-based dual-junction solar cells are capable of reaching >32% efficiency under one-sun illumination. An efficiency of 35.9% was demonstrated using a GaInP/GaAs//Si triple-junction solar cell. Our cost analysis emphasizes the urgent need for expanded research efforts on inexpensive yet efficient and reliable top-cell technologies. For III–V top cells, a path to economic viability rests on the future development of low-cost deposition methods as well as alternative substrate materials or growth directly on Si. These research challenges are significant, but not insurmountable; if they are addressed, future PV installations will be able to provide nearly twice as much power per area as today's installations, and deliver lower-cost solar power by reducing BOS costs.

Methods

Fabrication of III–V//Si tandem solar cells. The III–V layers were grown inverted at NREL by metalorganic vapour phase epitaxy (MOVPE) on single-crystal GaAs substrates ((100), 2° off toward (111)B) and processed into thin, semi-transparent solar cells on glass as described in ref. 12. On the top-cell front side, a dual-layer ZnS/MgF_2 (~41 nm/97 nm) film acts as antireflective coating, whereas a single layer of ZnS (~105 nm for GaAs cell, ~82 nm for GaInP cells) is used on the rear side to enhance the transmission of normally incident sub-bandgap light into the silicon cell. The optimum ARC film thicknesses were determined by modelling the photocurrents in each cell. The Au metal grid lines on the front and rear side are aligned and have a width of ~10 µm, height of 2–2.5 µm and spacing of 1.8 mm, and metal was deposited using electroplating. A photo of the design is shown in Fig. 1c.

For the SHJ-bottom-cell fabrication at CSEM, ~230 µm-thick, n-type float-zone Si wafers (100) were textured and cleaned. Then intrinsic and doped hydrogenated amorphous silicon (a-Si:H) layers with a total thickness of ~12 nm were deposited by plasma-enhanced chemical vapour deposition on both sides of the wafer. A stack of hydrogenated indium oxide IO:H (65 nm or 95 nm) and ITO (10 nm) were sputter-deposited through shadow masks on ~1.1 cm^2 rectangular areas on the front side. A full-area ZnO/Ag rear contact was deposited before the 16-µm-thick front metal grid and extended busbars were applied by screen printing. Both the finger width (40 µm) and the distance (2.1–2.4 mm) between the fingers of the SHJ front grid lines were larger than for the III–V top cells, which prevented their alignment. When operated as single-junction devices under one sun, our SHJ cells obtain a V_{OC} of ~720–730 mV and efficiency of 23% (uncertified). The EQE curves of the bottom cells shown in Fig. 2 were measured at CSEM before stacking.

The glass slide with the III–V top cell was attached to the bottom cells with a transparent, electrically insulating adhesive (LOCTITE ECCOBOND 931-1 from Henkel). The alignment of the III–V and SHJ cell areas was checked optically using an infrared camera before the epoxy was cured at room temperature. The active multi-junction cell area is defined by the gold back contact of the III–V cell, which surrounds the III–V solar cell and determines the illuminated area of the bottom cell.

Solar cell characterization. The III–V//Si multi-junction solar cells were characterized in NREL's certified device performance laboratory at 25 °C. The EQE of the bottom cell was measured while the III–V cells were short-circuited to reduce the effect of luminescent coupling between the subcells to a minimum. The $J-V$ characteristics were measured under AM1.5g spectral conditions and additional shadow masks prevented carrier generation in the Si wafer outside the active cell area. The bottom-cell $J-V$ curves were measured while the III–V cells were at open-circuit condition and when voltage-biased close to its maximum power point; the latter simulates operating conditions in the field. The reflection curves of the tandem cells were measured at NREL in a Cary 5000 spectrophotometer system using an integrating sphere.

Techno-economic analysis. Our cost analysis is based on a bottom-up costing of the significant factors in each of the cells' fabrication steps. The assumptions for current cost are based on extensive NREL research of current market and industry data. The process flow is developed on the basis of literature review, interviews with industry and subject experts, and other secondary sources (for example, company websites, news articles and market reports). A total cost of ownership model is then created for each step in this process flow. The total cost of ownership model includes the costs associated with materials, labour, utilities, facilities, equipment and equipment maintenance. The costs assume that all equipment is purchased new at full price. Process-specific input data—for example, labour requirements, throughputs/cycle times, material and electricity usage, material pricing—are collected from industry members, material suppliers, equipment manufacturers and market reports. The common goal of NREL and the industry collaborators is to identify key barriers to market growth. Companies, researchers and consumers alike benefit from identifying these cost reduction paths. Most data from industry members and equipment manufacturers are collected via interview, and data from material suppliers are obtained via request for quotes or interviews. The ability of NREL to collect this input data relies on our ability to build trust with industry and protect proprietary or business-sensitive information from individual companies. Often, this can be achieved by collecting data from many different sources and providing only aggregated anonymized information. However, in cases where only a small number of data points (or only one data point) can be obtained for a given input, and thus the data cannot be sufficiently anonymized, we are unable to publish specific input assumptions. For these reasons, more detailed information on III–V cell contacts and substrate reuse processes unfortunately cannot be shared. Key input assumptions for the cost models that can be publicly disclosed are included in Supplementary Table 1.

Near-term cost model. There are several items of note on our near-term cost model. First, while we assume processes that are commercially available, further development may be required to achieve high efficiencies and yields using these processes. For example, we assume high growth rates for MOVPE that have been demonstrated in the literature on commercially available tools, but with a small degradation in efficiency[41]. We also assume that the III–V cell contacts can be made using plating and without the need for Ag or Au. Plating is used in the literature for fabricating high-efficiency III–V solar cells, but Au or Au and Ag (prohibitively expensive materials), along with lithography (an expensive process) are typically used. Our interviews indicate that Au- and Ag-free plated contacts can be used for III–V solar cells in commercial processes, but we have very limited data on whether any additional processing is required and no information on how the use of these contacts might impact cell efficiency, reliability and process yield; these questions are still being answered for c-Si cells as well, and options with and without a thin Ag seed layer exist[49]. As an approximation, the near-term numbers assume costs similar to that of Cu-plated contacts emerging for c-Si cells could be achieved at high efficiency.

Si bottom cell considered in techno-economic analysis. For the bottom cell, we intentionally consider bifacial SHJ cells, potentially also used in monofacial modules using white back sheets to collect extra light from the back. The choice of the cell bifaciality and the thinner initial wafer thickness is motivated by the current/emerging industrial SHJ standards, although they have not been implemented in the record devices for reasons of process compatibility with laboratory type equipment. Parallel studies have shown the positive effect on efficiencies of such bifacial cells when encapsulated with a white back sheet thanks to an increased current. Also, similar or lower costs are achievable with this second approach due to lower Ag mass deposition per wafer and the low cost of screen printing technology.

Data availability. The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

S.E. developed the tandem-cell design and, together with A.T., led the tandem-cell development and optimization. D.L.Y. and J.S.W. contributed to initial stages of tandem-cell design development. J.F.G., M.A.S. and A.T. developed the III–V top-cell layer structure and optimized the growth conditions. A.T. characterized the III–V solar cells, and is the project PI at NREL. C.A. and M.D. led the Si-bottom-cell fabrication at CSEM and C.A. provided characterization of the Si cells before stacking. S.E., M.S. and A.T. carried out the tandem-cell stacking process and the uncertified characterization. L.B. and A.D. from CSEM assisted with the Si-bottom-cell fabrication and optimization. C.B. is the heading the SHJ and tandem-cell activities at CSEM. The cost analysis was performed by K.H., T.R. and M.W. from NREL and discussed in detail with A.T., S.E., C.A., M.D. and C.B. S.E. wrote the manuscript, and all other authors provided feedback.

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Competing interests

The authors declare no competing financial interests.