# DEVELOPMENTS ON CdS/CdTe PHOTOVOLTAIC PANELS AT PHOTON ENERGY, INC.

S. P. ALBRIGHT, J. F. JORDAN, B. ACKERMAN and R. R. CHAMBERLIN
*Photon Energy, Inc., El Paso, TX 79924 (U.S.A.)*

## Summary

Photon Energy, Inc. has been developing a prototype production line that produces 1 $ft^2$ and 4 $ft^2$ photovoltaic modules based on polycrystalline thin films of CdS and CdTe. A 1 $ft^2$ module has been measured at SERI with 7.3% aperture area and a corresponding output of 6.11 W. A 4 $ft^2$ module delivered to SERI is the largest known single substrate CdS/CdTe module in the world to date. Active area efficiency has increased from 6.1 to 8.1% on 1 $ft^2$ substrates delivered to SERI since June 1987. An efficiency of 12.3% has recently been achieved on a small cell (0.302 $cm^2$ area). Higher efficiencies (over 13%) are expected as a more transparent window layer is developed. Research and development efforts have focused on stability and efficiency issues. Areas studied include electroding, encapsulation, doping, small cell as well as 1 $ft^2$ and 4 $ft^2$ module performance optimization, and accelerated as well as real-time life testing.

## 1. Introduction

PEI has been developing CdS/CdTe devices and modules since 1984. A 2-year cost-sharing subcontract through SERI starting in 1987 has helped address common objectives between PEI and DOE on large-area low-cost terrestrial photovoltaics. Specifically, the objective of this research effort has been directed towards development of an improved materials technology and fabrication processes for limited-volume production of 1 $ft^2$ and 4 $ft^2$ CdS/CdTe photovoltaic modules, with stability and efficiency goals being the most significant milestones.

To achieve the efficiency and stability goals, the research program has been separated into tasks which include

(1) doping of p-CdTe,
(2) surface chemistry studies of CdTe,
(3) analyses and characterization of CdS/CdTe devices,
(4) encapsulation and stability testing,
(5) performance optimization on small cells, and
(6) panel efficiency optimization.

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The major technical results and milestones for each of these tasks are reviewed and future development plans are discussed.

Using the results of these tasks, PEI has produced and delivered samples to SERI with efficiencies very close to the original objectives, including a 1 $ft^2$ module with an output of 6.1 W (measured at SERI) and an active area of 754 $cm^2$. For this module, the active area efficiency was 8.1% and the aperture efficiency was 7.3%.

A functioning 4 $ft^2$ module has already been delivered to SERI. Further developmental work is under way to attain the efficiency goals required on 4 $ft^2$ modules.

## 2. Device description

On commercial 3-mm float glass is deposited a 0.5 - 1.2 $\mu$m film of tin oxide by spray pyrolysis. The deposition temperature is ca. 480 °C. A typical resistivity for the tin oxide film is 5 - 6 $\times 10^{-4}$ $\Omega$ cm, and a typical extinction coefficient is 1500 $cm^{-1}$. The tin oxide films generally measure 5 - 10 $\Omega/\square$ sheet resistance and 87% transmission in the wavelength range from 520 to 850 nm, with a variation of 10 - 50% in sheet resistance across a 1 $ft^2$ substrate.

A CdS film of 6-$\mu$m thickness is deposited on top of the tin oxide, with a carrier concentration of the order of $1 \times 10^{19}$ $cm^{-3}$ as measured by biased capacitance using Shottky diodes. Approximately 6 $\mu$m of CdTe is deposited onto the CdS, and the measured hole concentration in the CdTe (when not intentionally doped) is of the order of $1 \times 10^{15}$ $cm^{-3}$. A scanning electron micrograph is shown in Fig. 1. It should be noted that the porosity of the

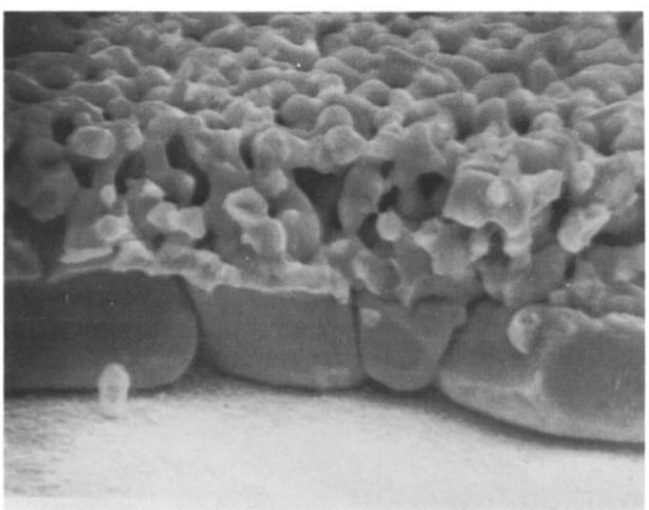

Fig. 1. Scanning electron micrograph of an edge view of the tin oxide, CdS, and CdTe films.

CdTe film decreases as one moves closer to the metallurgical junction between the CdS and CdTe.

After an etch to remove the surface oxide a graphite electrode is deposited on top of the CdTe to a thickness of ca. 10 $\mu$m. A more-conductive electrode containing tin is then evaporated on top of the structure to complete the device.

## 3. Efficiency improvement

The DOE and PEI objectives for future large-area terrestrial photovoltaics call for efficiencies greater than 15%. The theoretical efficiency of a CdTe-based photovoltaic device calculated from the band-gap alone exceeds 27%. Efficiencies have been projected up to 18% for well-optimized CdTe-based polycrystalline thin-film devices by further reductions in series resistance, reflection, and window absorption, completely external to the junction part of the cell [1].

A small-area cell (0.302 $cm^2$) cut from a full 1 $ft^2$ module at PEI has been measured by SERI at 12.3% efficiency [2]. The current–voltage performance curve for that cell is shown in Fig. 2. Window layer improvements for such a device should allow us to achieve over 14%

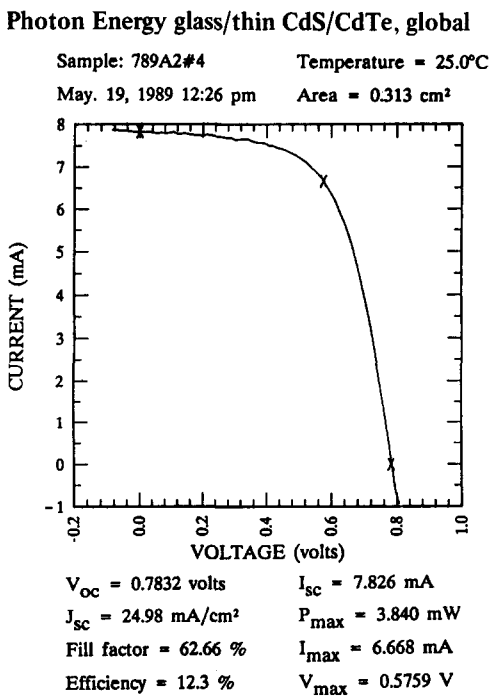


Fig. 2. Current–voltage response for the best cell to date at PEI (area = 0.302 $cm^2$).

efficiency in the mid-1990s. Window-layer materials are currently being developed at PEI based on very thin CdS layers; it is realistic to project that 15% efficient single-junction CdTe devices and modules will be realized before the year 2000 with completely optimized device structure and process control.

## Material improvement

### *4.1. Doping*

CdTe can be made conductive with suitable doping. Heating phosphorus (or copper) and CdTe in a closed quartz container at temperatures above 750 °C results in reproducible resistivities below 100 Ω cm. Neither arsenic nor antimony has provided similar results when these procedures are used.

It has been reported [3] that phosphorus-doped CdTe can result in devices with measured hole concentrations as high as $2.8 \times 10^{16}$ cm$^{-3}$. Using copper-doped CdTe, measured hole concentrations are actually lower than undoped CdTe. CdTe which is not intentionally doped generally measures $0.9 - 2.0 \times 10^{15}$ cm$^{-3}$.

The best device which has yet been produced using the phosphorus-doped CdTe had 7.3% efficiency, a short-circuit current of 17.5 mA cm$^{-2}$, an open-circuit voltage of 734 mV, a fill factor of 57%, and a hole concentration of $2.3 \times 10^{15}$ cm$^{-3}$. Another device similarly produced with a measured hole concentration of $2.8 \times 10^{16}$ cm$^{-3}$ had low $J_{ac}$ (12.9 mA cm$^{-2}$), low $V_{oc}$ (692 mV), and a poor fill factor (46%). A statistical comparison of six phosphorus-doped and six undoped samples indicate that an increase in measured hole concentration from $2.5 \pm 0.4 \times 10^{15}$ cm$^{-3}$ to only $5.1 \pm 0.7 \times 10^{15}$ cm$^{-3}$ already results in lower $I_{sc}$ (15.0 - 13.0 mA cm$^{-2}$), $V_{oc}$ (694 - 684 mV), and efficiency (6.3 - 5.9%). For polycrystalline devices doped in this manner, there appears to be a hole concentration threshold above which cell parameters suffer, especially $J_{oc}$ and $V_{oc}$.

The results on devices produced by copper-doped CdTe were much less promising, because of very low open-circuit voltages (593 mV at best). It appears that during deposition and processing, the copper in the doped CdTe may have some tendency to diffuse into the CdS and also to self-compensate.

### *4.2. Contact chemistry*

The condition of the CdTe surface affects the resulting device efficiency as a result of its contribution to contact resistance. Therefore, treatment of the surface, using various chemical rinses and etches, is of major importance for good device efficiency and stability. Understanding the growth and removal steps of the oxide at the surface is both a performance and stability issue.

ESCA analyses have been carried out [4] on CdTe surfaces treated by our laboratory. The ESCA results on material after various steps of a bromine etch are given in Table 1. The bromine solution, 0.5 vol.% in methanol, is followed by a 6 M NaOH soak. The raw data showing the tellurium peak positions are also indicated.

By the method used, one cannot distinguish between Cd° cadmium in CdTe, or cadmium in $Cd(OH)_2$. Nor can this method distinguish between Te° and tellurium in CdTe. However, some valid comments can be made, even without further experimentation.

It is observed that there is a great difference in the measured composition of the surface growth for the 530 °C (Cd/Te = 0.95) air-heated sample and sample given the 200 °C air heat treatment (Cd/Te = 1.7).

After the 200 °C air anneal, measurements indicate an excess of Cd° or a cadmium compound on the surface probably made up chiefly of an oxide mixture of CdO, $TeO_2$ and $CdTeO_3$. However, no CdO peak near the published 404.0-eV mark was observed on any sample except for a very small side peak on the 530 °C, air heat-treated sample. The high Cd/Te ratio on CdTe after an air anneal has been claimed to be due to cadmium outdiffusion by Danaher *et al.* [5] and Bryant *et al.* [6].

After a subsequent $Br_2$/MeOH etch which removes 0.5 μm of CdTe, measurements indicate no lattice cadmium or tellurium. The only peak observed is the $Te^{4+}$ peak. It is not certain from this work whether this $Te^{4+}$ peak is due to residual insoluble $TeBr_4$ or to $TeO_2$ (or $CdTeO_3$). Further work needs to be done to determine the exact species.

However, in any case, a subsequent soak in the NaOH solution removes the $Te^{4+}$ peak entirely. Both $TeO_2$ and $TeBr_4$ are soluble in NaOH solution. The Cd/Te ratio after the NaOH soak is higher than expected for a stoichiometric CdTe. In addition, the shift of the Cd peak by 0.4 - 0.7 eV away from the supposed CdO peak occurrence during the NaOH soak may indicate that some residual Cd° did exist at the point before NaOH treatment even though no CdO peak was observed directly. Further work should include direct measurement of the CdO peak.

Similar results are seen for the NaOH soak alone after the 200 °C air anneal, but the final Cd/Te ratio is higher if the $Br_2$ etch is done first. Residual Na was found after the NaOH soak in both cases.

Further analyses need to be done to be sure of the exact species present after the NaOH soak and to confirm the high Cd/Te ratio at that stage. It is, however, qualitatively apparent that the oxide can be controllably removed and that the CdTe stoichiometry can be adjusted by this and similar etches. Improved electrical contact development should follow as a result of these preliminary, but useful efforts.

### *4.3. Device analysis and characterization*

Electrical and optical measurements of the CdS/CdTe devices have been performed to characterize the effect of process variations on the cell behavior and to improve our understanding of the mechanism of current

TABLE 1

ESCA data at various stages of a $Br_2$ etch

| | | *Corrected peak ratios* | | | *Peak positions* | | |
|---|---|---|---|---|---|---|---|
| | | *Cd/Te* | *$Te^0/Te^{4+}$* | *Cd/Te after sputter* | *Te* | *Cd* | *$Te^{4+}$* |
| No. 1: | 200 °C, air | 1.7 | ~1.9 | 1.1 (10 min) | 572.6 | 405.3 | 576.4 |
| No. 2: | 200 °C, air + $Br_2$ | 0.04 | <0.02 | 0.03 (5 min) | — | 405.6 | 576.6 |
| No. 3: | 200 °C, air + $Br_2$ + NaOH | 2.6 | >100 | 1.3 (5 min) | 572.2 | 404.9 | Very small |
| No. 4: | 200 °C, air + NaOH only | 1.9 | >100 | 1.0 (5 min) | 572.4 - 572.5 | 404.9 | — |
| No. 5: | 530 °C, air | 0.95 | ~0.02 | 1.3 (5 min) | 572.2 | 405.7 | 576.4 |

flow at the junction. Of particular interest here is the role played by the interface states.

It was found previously [7] that interface states affect not only the diode reverse saturation current ($J_0$) but also the junction collection efficiency and hence the light-generated current ($J_L$). A set of equations has been derived to calculate the effect of interface states on $J_0$ and $J_L$. A preliminary model describing the junction current flow in terms of tunneling and interface recombination was developed and presented earlier [3]. $J_{sc}$ was found to increase with reverse bias and to decrease with forward bias.

The highest efficiency measured by SERI on a CdS/CdTe solar cell made at PEI, with a cell area of 0.302 $cm^2$, is 12.3%. The best values (measured at SERI or PEI) for individual cell parameters are $V_{oc}$ = 830 mV, $J_{sc}$ = 25.0 mA $cm^{-2}$ and $FF$ = 72%.

As reported earlier [8], cells analyzed by EBIC showed the existence of a shallow homojunction with a peak response 0.7 - 0.8 $\mu$m into the CdTe. The diffusion length was measured as 0.7 $\mu$m for the p-CdTe, 1.3 $\mu$m for the n-CdTe, and 1.2 $\mu$m for the CdS [9].

It was also found [8] that under a white light intensity of 16 mW $cm^{-2}$ a typical cell (0.302 $cm^2$ in area) capacitance is 2.9 nF (corresponding to a depletion layer width of 0.95 $\mu$m). Carrier concentration ($N_A$) in CdTe from voltage-biased junction capacitance measurement was found to be $1 \times 10^{15}$ $cm^{-3}$.

Results from capacitance measurements at various frequencies have indicated [10] that the dispersion effects due to interface states and/or the midgap states in the depletion layer persist at frequencies as high as 100 kHz.

Photoluminescence results are shown in Fig. 3 [11]. The position of the peak and the peak width would seem to indicate good electronic quality for this CdTe sample.

Spectral response measurements have indicated [8] that the reduction of $J_{sc}$ with forward bias appears to be relatively insensitive to the wavelength of monochromatic radiation. This insensitivity suggests that the major loss mechanism is likely to be a reduced electric field at the junction, causing an increased trapping of the light-generated electrons by midgap recombination centers and/or interface states. Absolute measurements of quantum efficiency corrected for all absorptions and reflections remain to be done. A generally weaker spectral response at longer wavelengths may indicate that the short-circuit current of these devices could be improved by increasing the diffusion lengths in the CdTe and/or by achieving more heterojunction character, thereby increasing the field at the metallurgical interface.

Practically, these diffusion length and electric field improvements are to be achieved through further optimization of the alloying and doping of the CdTe and through improvement of the morphology of the crystal near the junction.

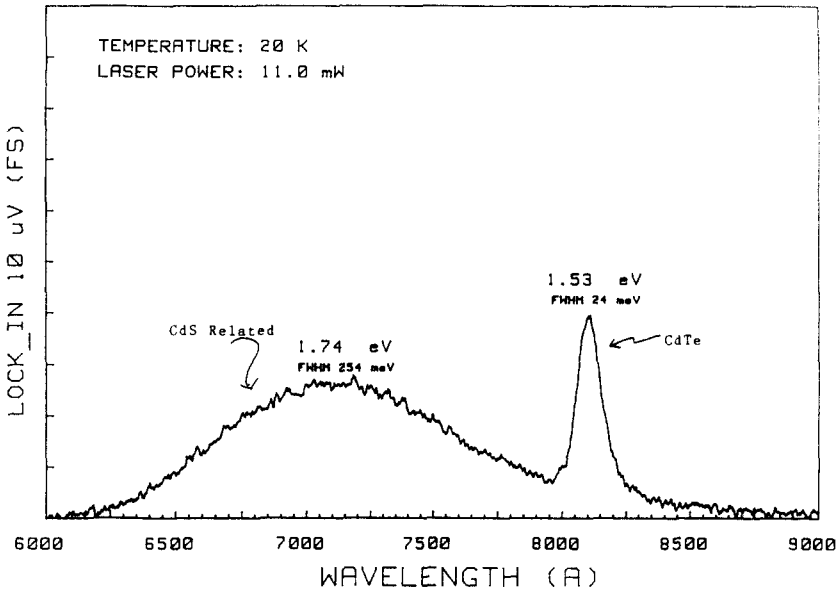


Fig. 3. Photoluminescence spectrum for a CdTe device.

## 5. Stability, encapsulation and life testing

Considerable work has been done on electroding, encapsulation, and life-testing of cells and modules.

As reported at an earlier conference [12] PEI had abandoned development of an electrode based on tellurium, as a result of stability problems. It was found, in life-testing such cells, that their primary mode of degradation was a loss of open-circuit voltage. This voltage loss occurs at a decreasing rate, but the rate is strongly dependent on temperature. The loss of voltage was not reversible. Figure 4 shows an example of voltage degradation of this type of electrode at two elevated temperatures. Similar results were obtained using gold or nickel electrodes.

Present work focuses on a graphite electrode, which indicates good stability when adequately encapsulated. The principal mode of degradation which an unencapsulated cell using this improved electrode can exhibit is an increase in $R_{se}$ due to an overexposure to humidity. This electrode provides excellent long-term stability if the encapsulation is adequate to protect it from being subjected to excessive humidity. No significant degradation has been observed in the outdoor El Paso environment for over 9 months on some encapsulated samples, as shown in Fig. 5. No degradation mode due to light effects has been observed.

One encapsulation method explored was a lamination of a foil to the active substrate using a vacuum bag laminator of known design [13]. Foils

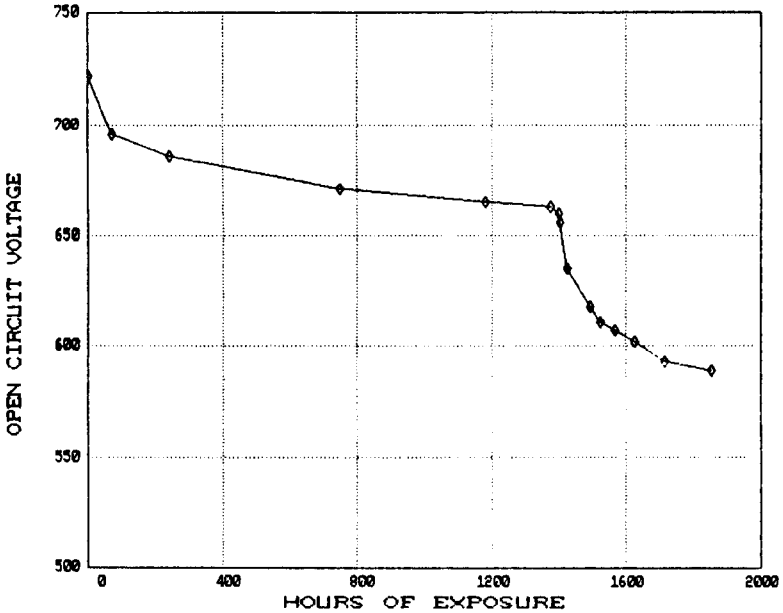


Fig. 4. Graph of open-circuit voltage degradation with temperature for a tellurium electrode on CdTe.

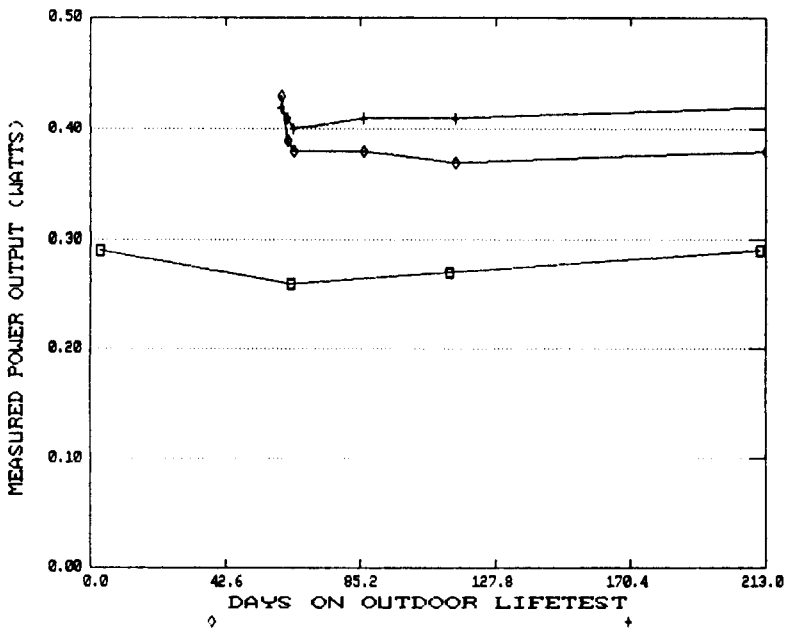


Fig. 5. Long-term life-testing results done at Photon Energy, Inc.

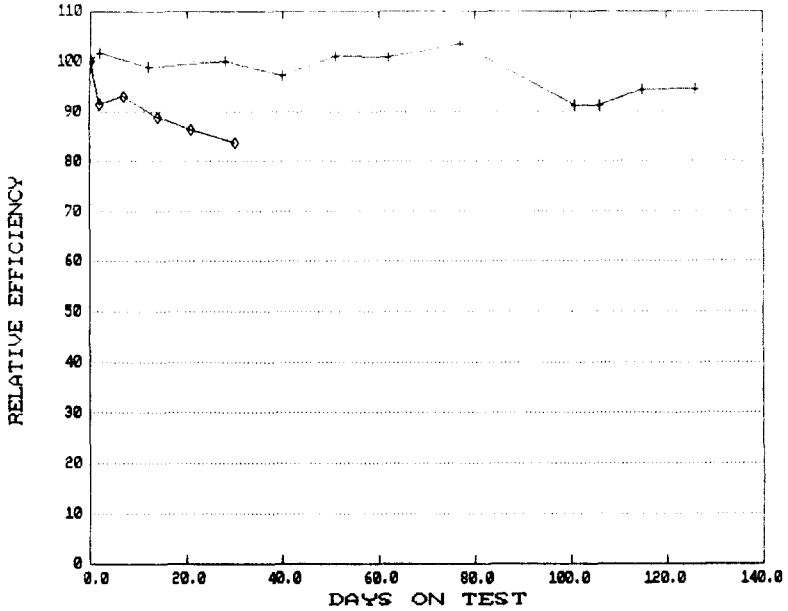


Fig. 6. Performance life-testing of two types of encapsulation (testing done at SERI).

were used primarily because of their cost advantages. The thermoplastic and thermoset adhesives explored by this method have generally been EVA-based. The EVA application was followed by an edge seal with high-performance epoxy. Although this method was satisfactory from a manufacturing standpoint, the results shown by the dashed line in Fig. 6 [14] indicate that the stability of early encapsulations was not acceptable and that good stability can be observed when panels are properly sealed. Collaborative efforts between PEI and JPL [15] are addressing long-term module degradation issues.

## 6. Module development

### *6.1. Module description*

A 1 $ft^2$ module is prepared as described above. An interconnection step such as is shown in Fig. 7 allows one to match optimally the maximum power point of a single module to a 12 V storage battery. Figure 8 shows an unencapsulated module with such an interconnection.

### *6.2. Progress of 1 $ft^2$ modules*

Significant progress has been made since 1987. As seen in Table 2, an increase of over 35% in aperture area efficiency was attained in only 16 months. The 8.1% active-area efficient module with an output of 6.1 W delivered to SERI in October 1988 is a world record output for CdTe

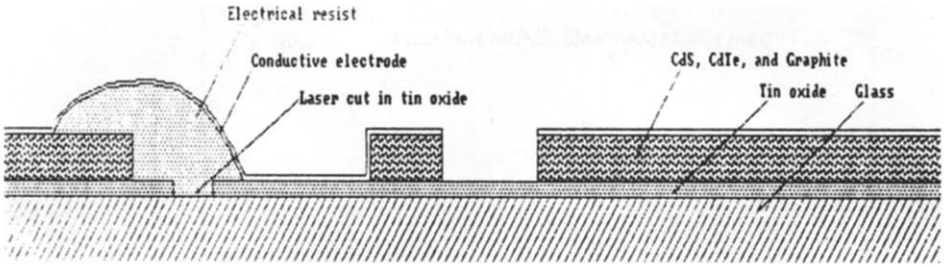


Fig. 7. Cross-sectional view of interconnection structure.

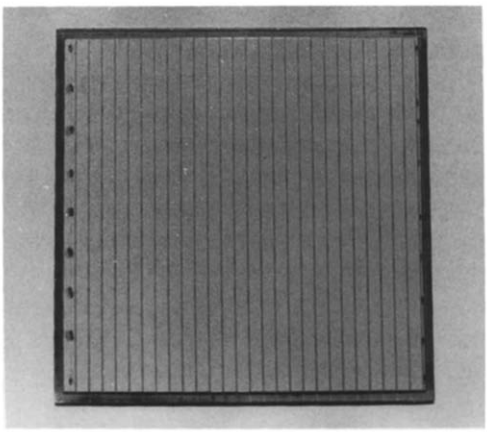

Fig. 8. Current–voltage response for a 1 $ft^2$ module delivered to SERI as measured on the spire simulator at SERI.

TABLE 2

Performance of modules delivered to SERI

| *Date* | *Output* (W) | *Active area* ($cm^2$) | *Active area efficiency* (%) | *Aperture area efficiency* (%) |
|---|---|---|---|---|
| June 1987 | 4.0 | 660 | 6.1 | 5.4 |
| Nov. 1987 | 4.4 | 660 | 6.6 | 5.8 |
| March 1988 | 4.7 | 686 | 6.8 | 6.1 |
| June 1988 | 5.3 | 760 | 7.0 | 6.3 |
| Oct. 1988 | 6.1 | 754 | 8.1 | 7.3 |

modules of this size. The current–voltage performance curve for a 6.1 W module is shown in Fig. 9 [16].

### *6.3. Description of 4 $ft^2$ module*

The Department of Energy (DOE) objectives for photovoltaic development call for PV modules larger in area than 1 $ft^2$, to address properly the

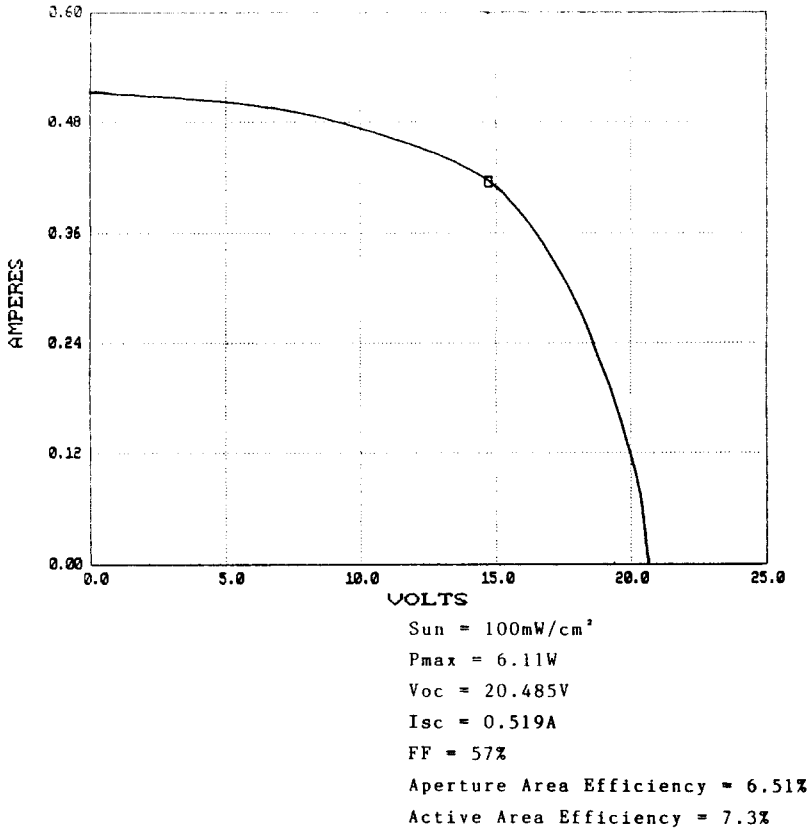


Fig. 9. Current–voltage response for a 1 $ft^2$ module delivered to SERI as measured on the Spire simulator at SERI.

future of large-capacity terrestrial photovoltaic installations. With this in mind, a 4 $ft^2$ module was produced and delivered to SERI in 1988.

The 4 $ft^2$ module to be produced at PEI will be 2 ft × 2 ft and will yield 23 W in the early stages.

Further improvement of the percentage of active area on a given module can be realized. The portion of the active area lost at the division (interconnection) can practically be reduced from ca. 12% to less than 6%. Increasing the size of the module to 4 $ft^2$ allows an aperture area of 3413 $cm^2$ with a 1/2 in border. At 7% aperture area efficiency of nearly 24 W can be expected on the 4 $ft^2$ modules. Considerable work is needed to optimize the output of these larger modules.

The interim goal for overall module active area efficiency of 11.6% corresponds to an output of 9.3 W per $ft^2$ or 37.2 W on a 4 $ft^2$ module. This increase is to be accomplished by improving the fill factor, the window layer, and the active area to total area ratio. After full optimization of device structure, materials, and processing, a 15% aperture area module will be able to produce over 50 W.

## 7. Conclusions and future objectives

The efficiency and stability objectives at PEI on CdS/CdTe modules are being addressed. The feasibility of producing 4 $ft^2$ modules of CdS/CdTe has been shown and requires further effort to realize the overall potentials.

The ability to reduce the resistivity of CdTe through proper doping has been shown. Self-compensation of dopants is an issue; however, only a slight change from present hole concentrations in the CdTe is indicated for device improvement. An optimum carrier concentration appears to exist. Work must continue towards the understanding of CdTe surface chemistry, but has already improved the understanding of oxide growth and removal on CdTe.

EBIC, capacitance, spectral response, photoluminescence, and $I-V$ curve analyses have proven to be beneficial characterization tools and have resulted in useful device models which have supported the direction of research.

Properly encapsulated modules produced at PEI have been observed to be stable in the outdoor environment for life-testing periods of up to 9 months duration at last testing.

Present power outputs per square foot and expected power outputs in the future have been reviewed. More development work remains on both 1 $ft^2$ and 4 $ft^2$ modules with most efficiency, output, and stability improvements to be gained by

(1) window material optimization,
(2) uniformity improvement by process control and optimization,
(3) addressing long-term encapsulation issues,
(4) material alloying and improved understanding of defect significance,
(5) morphology improvement and device structure optimization,
(6) modelling, optimization and characterization of layers for an optimum device structure,
(7) improvement of active area to total area ratio.

## Acknowledgments

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