

IITB RISC 2022 MULTICYCLE IMPLEMENTATION

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1 INFORMATION ABOUT THE DESIGN

Owing to the fixed encoding in RISC architecture we have made the PC move 2 bytes at a time. To command the PC to stop we added a state with state id 111111 which serves as an infinite loop. The instruction register IR stores the current instruction. Eight 16-bit registers from R0-R8 were implemented using an array in regs.vhdl. The writing operation for all memory elements was done on the negative clock edge. Sign extender and shifters are used as required to send the input to ALU in the required format. ALU was made using behavioral modeling and it can perform addition, subtraction, NAND, and compare operations as well as check the zero and carry flags. An FSM was made to control the flow of states depending on the current instruction. A state signal has been sent to every component to control which operation is performed by them in that state. A clock of frequency 100MHz has been used.

2 FEEDING INSTRUCTIONS

IITB-RISC-22 is a 16-bit microprocessor having 64 bytes of data memory and 64 bytes of instruction memory. Instructions can be given to the processor using the mem.vhdl file in which the instructions can be directly fed into the instruction memory array.

```

17
18 architecture working of mem is
19     type mem_array is array (0 to 31) of std_logic_vector (15 downto 0);
20     signal mem_data: mem_array :=(
21         x"0000",x"0000", x"0000", x"0000",
22         x"0000",x"0000", x"0000", x"0000",
23         x"0000",x"0000", x"0000", x"0000",
24         x"0000",x"0000", x"0000", x"0000",
25         x"0000",x"0000", x"0000", x"0000",
26         x"0000",x"0000", x"0000", x"0000",
27         x"0000",x"0000", x"0000", x"0000",
28         x"0000",x"0000", x"0000", x"0000"
29     );
30
31
32     signal mem_ins: mem_array := (
33         b"1101000000011011", x"FFFF", x"0000", x"0000",
34         x"0000",x"0000", x"0000", x"0000",
35         x"0000",x"0000", x"0000", x"0000",
36         x"0000",x"0000", x"0000", x"0000",
37         x"0000",x"0000", x"0000", x"0000",
38         x"0000",x"0000", x"0000", x"0000",
39         x"0000",x"0000", x"0000", x"0000",
40         x"0000",x"0000", x"0000", x"0000"
41     );

```

Figure 2.1: Instruction feeding

It is important to note that an end instruction, given by x"FFFF", has to be input at the appropriate location the program is expected to end as seen in the above example. Also the project statement had the same OP CODE for LHI and ADI. Hence we have taken the OP CODE for LHI as 0011 and kept the OP CODE for ADI as 0000.

3 ALTERING DATA MEMORY

Data memory, similar to instruction memory, is also of 64 bytes and can be accessed in the mem.vhdl file.

The picture shown has value 1,2,3,4,5 stored at addresses 0,1,2,3,4 respectively. Every element in the array is of 2 bytes, making the array of size 32.

4 REGISTER ACCESS

Eight 16-bit registers from R0-R8 were implemented using an array in regs.vhdl. They can be accessed from the same.

```

mem.vhd*
6 port( t1_addr: in std_logic_vector(15 downto 0);
7 t3_addr: in std_logic_vector(15 downto 0);
8 state: in std_logic_vector(5 downto 0);
9 data_t1: in std_logic_vector(15 downto 0);
10 data_t2: in std_logic_vector(15 downto 0);
11 data_2: out std_logic_vector(15 downto 0);
12 ir_data: out std_logic_vector(15 downto 0);
13 ins_addr: in std_logic_vector(15 downto 0);
14 clk: in std_logic;
15 );
16 end entity;
17
18 architecture working of mem is
19 type mem_array is array (0 to 31) of std_logic_vector (15 downto 0);
20 signal mem_data: mem_array :=(
21 x"0001",x"0002", x"0003", x"0004",
22 x"0005",x"0006", x"0007", x"0008",
23 x"0009",x"000a", x"000b", x"000c",
24 x"000d",x"000e", x"000f", x"0010",
25 x"0011",x"0012", x"0013", x"0014",
26 x"0015",x"0016", x"0017", x"0018",
27 x"0019",x"001a", x"001b", x"001c",
28 x"001d",x"001e", x"001f", x"0020",
29 );
30
31
32 signal mem_ins: mem_array := (
33 b"1101000000011011", x"FFFF", x"0000", x"0000",
34 x"0000",x"0000", x"0000", x"0000",

```

Figure 3.1: Altering data memory

```

regs.vhd
12 t1_in: in std_logic_vector(15 downto 0);
13 t2: out std_logic_vector(15 downto 0);
14 t2_in: in std_logic_vector(15 downto 0);
15 t3: in std_logic_vector(15 downto 0);
16 shift7: in std_logic_vector(15 downto 0);
17 pc_in: in std_logic_vector(15 downto 0);
18 pc_out: out std_logic_vector(15 downto 0);
19 clk: in std_logic;
20 state: in std_logic_vector(5 downto 0);
21 );
22 end entity;
23
24 architecture working of registers is
25 type mem_array is array (0 to 7) of std_logic_vector (15 downto 0);
26 signal regs: mem_array :=(
27 x"0001",x"0002", x"0003", x"0004",
28 x"0000",x"0000", x"0000", x"0000"
29 );
30
31 begin
32
33 regs_read: process(reg_a1, reg_a2, state)
34 begin
35 if (state = "000010") then
36 t1 <= regs(to_integer(unsigned(reg_a1)));
37 t2 <= regs(to_integer(unsigned(reg_a2)));
38 elsif (state="001000" or state="100100") then
39 t1 <= regs(to_integer(unsigned(reg_a1)));
40 t2 <= regs(to_integer(unsigned(reg_a1)));

```

Figure 4.1: Register

The picture shown has value 1,2,3,4 stored in R0,R1,R2,R3 respectively.

5 CHECKING VALUES IN RTL SIMULATION

After compiling successfully, we run RTL simulation. This is where we check if our program has given the output expected out of it.

The value stored in any storage component or any signal can be accessed in RTL simulation.

5.1 CHECKING VALUE STORED IN DATA MEMORY

Instance	Design unit	Design unit type	Name	Value	Kind	Mode
testbench	testbench(b...	Architecture	mem_data	{0000000000000000} {...	Signal	Internal
+	dut_instance	dut(dutwrap)	(0)	0000000000000000	Signal	Internal
+	+	+	(1)	0000000000000001	Signal	Internal
+	+	+	(2)	0000000000000010	Signal	Internal
+	+	+	(3)	0000000000000000	Signal	Internal
+	+	+	(4)	0000000000000100	Signal	Internal
+	+	+	(5)	0000000000000101	Signal	Internal
+	+	+	(6)	0000000000000000	Signal	Internal

Figure 5.1: RTL Simulation - Memory data

5.2 CHECKING VALUE STORED IN REGISTERS

Instance	Design unit	Design unit type	Name	Value	Kind	Mode
testbench	testbench(b...	Architecture	t2_in	UUUUUUUUUUUU...	Signal	In
+	dut_instance	dut(dutwrap)	t3	UUUUUUUUUUUU...	Signal	In
+	+	+	shift7	UUUUUUUUUUUU...	Signal	In
+	+	+	pc_in	UUUUUUUUUUUU...	Signal	In
+	+	+	pc_out	UUUUUUUUUUUU...	Signal	Out
+	+	+	clk	0	Signal	In
+	+	+	state	111111	Signal	In
+	+	+	regs	{0000000000000001} {...	Signal	Internal
+	+	+	(0)	0000000000000001	Signal	Internal
+	+	+	(1)	0000000000000010	Signal	Internal
+	+	+	(2)	0000000000000011	Signal	Internal
+	+	+	(3)	0000000000000100	Signal	Internal
+	+	+	(4)	0000000000000101	Signal	Internal
+	+	+	(5)	0000000000000110	Signal	Internal
+	+	+	(6)	0000000000000111	Signal	Internal
+	+	+	(7)	0000000000001000	Signal	Internal

Figure 5.2: RTL Simulation - Registers

5.3 CHECKING VALUE STORED IN INSTRUCTION MEMORY

Instance	Design unit	Design unit type	Name	Value	Kind	Mode
testbench	testbench(b...	Architecture	mem_data	{0000000000000000} {...	Signal	Internal
+	dut_instance	dut(dutwrap)	mem_ins	{1101000000011011} {...	Signal	Internal
+	+	+	(0)	1101000000011011	Signal	Internal
+	+	+	(1)	1111111111111111	Signal	Internal
+	+	+	(2)	0000000000000000	Signal	Internal
+	+	+	(3)	0000000000000000	Signal	Internal
+	+	+	(4)	0000000000000000	Signal	Internal
+	+	+	(5)	0000000000000000	Signal	Internal
+	+	+	(6)	0000000000000000	Signal	Internal
+	+	+	(7)	0000000000000000	Signal	Internal

Figure 5.3: RTL simulation - Memory instruction

5.4 CHECKING VALUE OF PROGRAM COUNTER

As seen in the instruction memory the second instruction is the end instruction and hence the value of program counter is set to 2.

Instance	Design unit	Design unit type	Name	Value	Kind	Mode
testbench	testbench(b...	Architecture	alu_c	0000000000000010	Signal	In
dut_instance	dut(dutwrap)	Architecture	reg	UUUUUUUUUUUUUU...	Signal	In
stateTrans...	ins_decoder...	Architecture	alu_a	0000000000000001	Signal	Out
stateSet_i...	ins_setter(w...	Architecture	data_1	0000000000000001	Signal	Out
ir_instance...	ir(working)	Architecture	reg_out	UUUUUUUUUUUUUU...	Signal	Out
mem_inst...	mem(working)	Architecture	state	111111	Signal	In
reg_instan...	registers(wo...	Architecture	clk	0	Signal	In
t1_instanc...	temp_1(wor...	Architecture	pc	0000000000000010	Signal	Internal
t2_instanc...	temp_2(wor...	Architecture				
t3_instanc...	temp_3(wor...	Architecture				
alu_instan...	alu(working)	Architecture				
pc_instanc...	pc(working)	Architecture				
shift1_inst...	shifter_1(wo...	Architecture				
shift7_inst...	shifter_7(wo...	Architecture				
sign_ex10...	sign_extend...	Architecture				

Figure 5.4: RTL Simulation - Program Counter