SINGAPORE UNIVERSITY OF TECHNOLOGY AND DESIGN

Term 7- Sept 2025

Nanoelectronics and Technology (01.119/99.503)-Week 2 Class 2

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25-Sept- 2025

Outline

- MOSFET structure
- CMOS Inverter
- CMOS Based Digital Circuits
- Noise Margin

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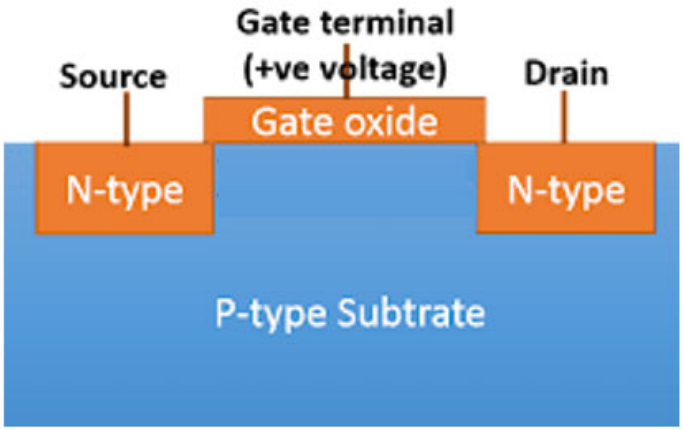
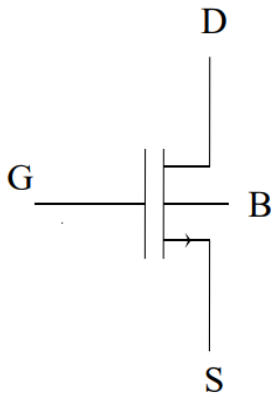
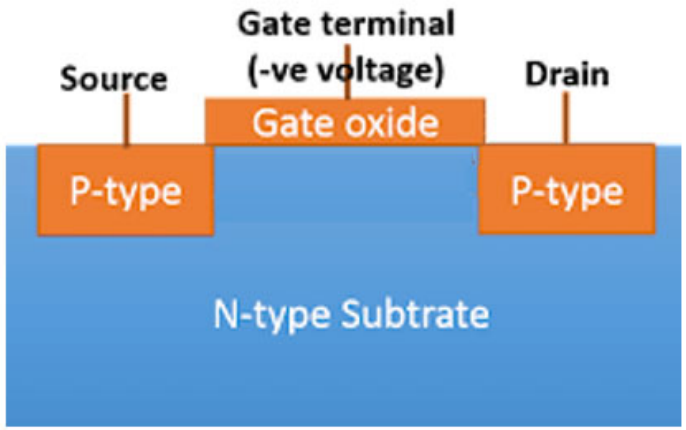
Review of MOSFETs

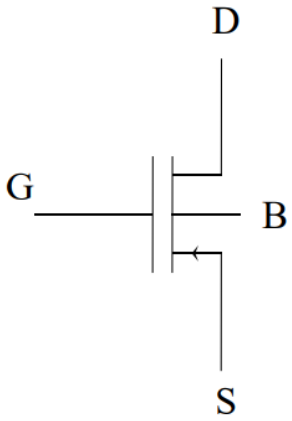


n-channel MOS
Transistor





p-channel MOS
Transistor



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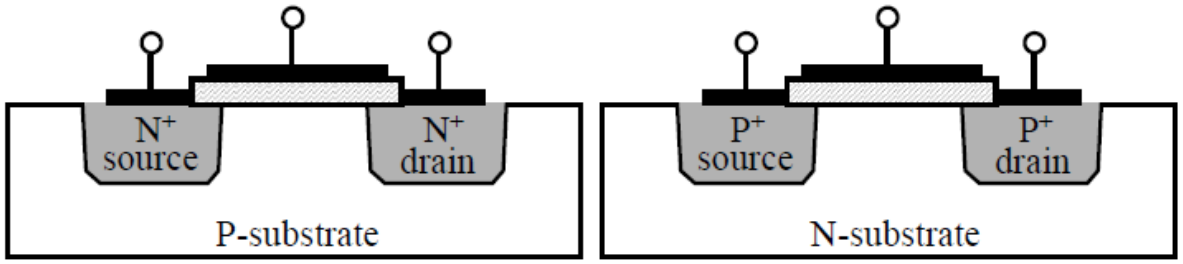
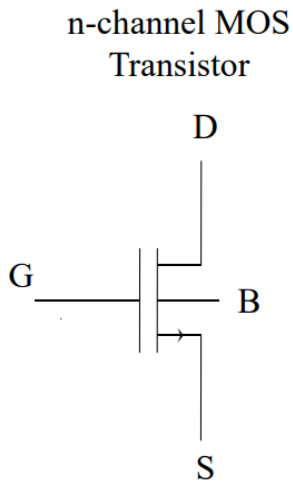
Review of MOSFETs

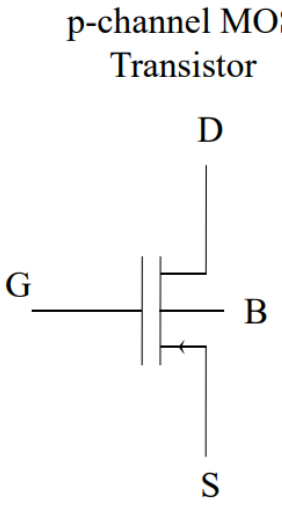
MOS Transistor

- Add "source" and "drain" terminals to MOS capacitor
- Transistor types
  - NMOS: p-type substrate, n^+ source/drain
  - PMOS: n-type substrate, p^+ source/drain



NMOS PMOS





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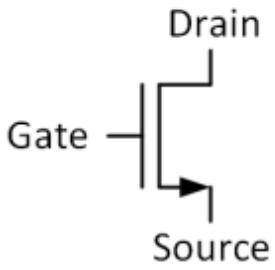
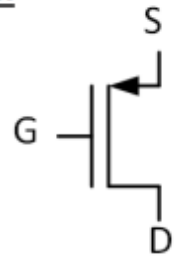
Review of MOSFETs

- We now turn our attention to another type of transistor, the **MOSFET**:
  - **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
- Many similarities to the BJT:
  - Three terminals
  - Voltage at one terminal controls current between the other two
    - A transconductance device
  - Two polarities: N-channel and P-channel MOSFETS
    - Our focus will primarily be N-channel MOSFETs (NMOS devices)

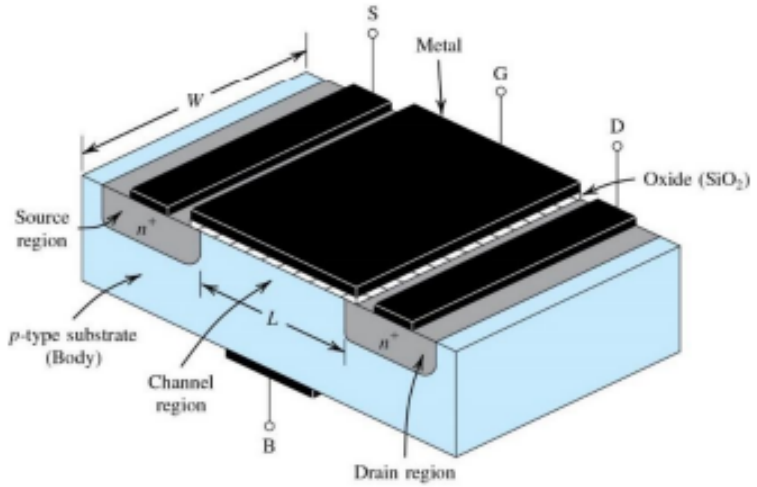
N-Channel (NMOS):

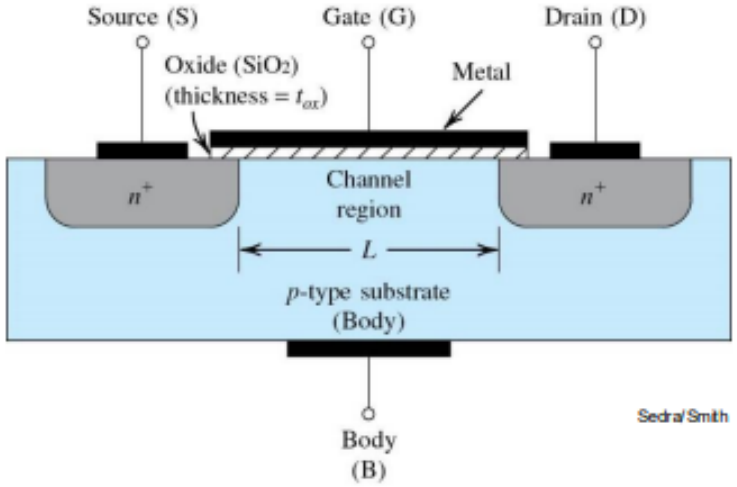


P-Channel (PMOS):



Review of MOSFETs





- P-type substrate
- N+ source and drain
- ***Metal gate electrode***, and source/drain/body contacts
- Thin ***oxide*** insulates the gate from the rest of the device
- Region of substrate between the drain and source is the ***channel***
  - Channel dimensions: W and L

Review of MOSFETs

- Terminal voltages and currents named as shown
  - Again, lower-case v/i and upper-case subscript represents ***total*** (AC and DC) voltage and current
- For an NMOS device in typical operation:

$$v_{GS} \geq 0$$

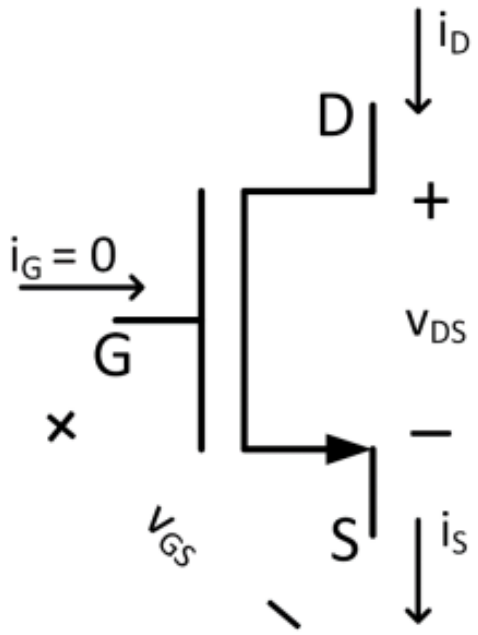
$$v_{DS} \geq 0$$

- Gate oxide does not allow current to flow, so

$$i_G = 0$$

and

$$i_D = i_S$$



Review of MOSFETs

Cut-Off Region

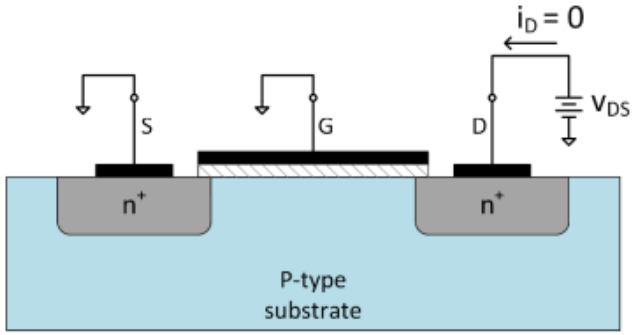
- Gate and source both grounded

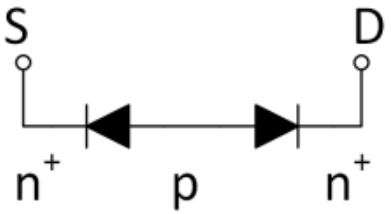
$$v_{GS} = 0$$

- Drain-to-source pathway looks like two back-to-back diodes
  - Very high drain-source resistance ($r_{DS} = \infty$)
- Even for $v_{DS} > 0$, no current will flow

$$i_D = 0$$

- Looks like an open switch

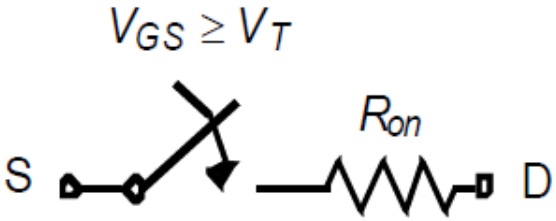


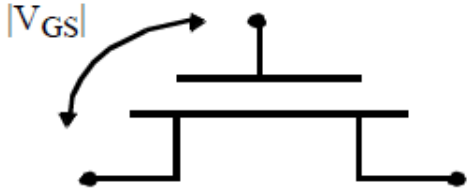


Review of MOSFETs

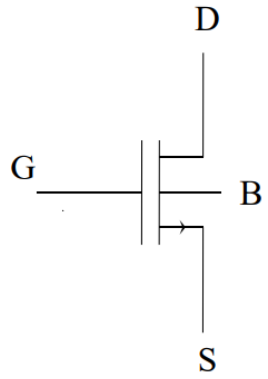
What is a Transistor?

A Switch! ⟷ An MOS Transistor

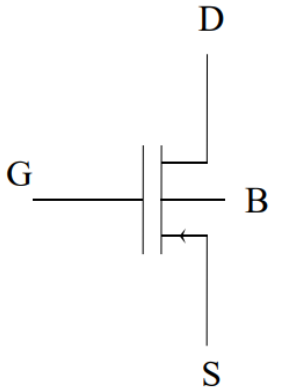




n-channel MOS Transistor



p-channel MOS Transistor



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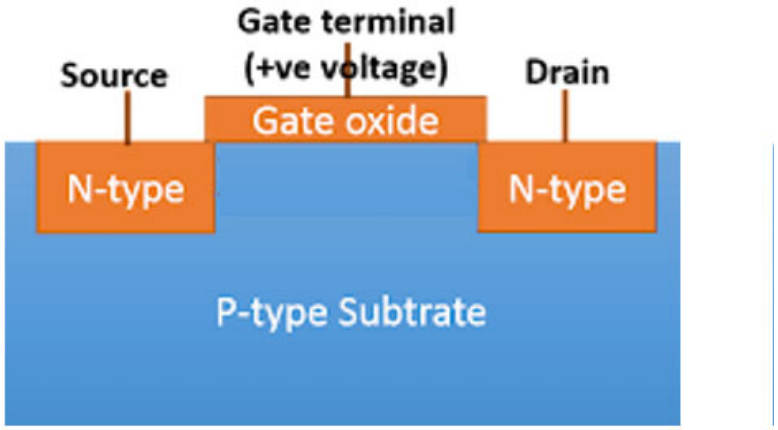
Review of MOSFETs



n-channel MOS
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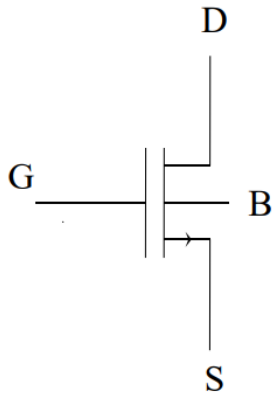

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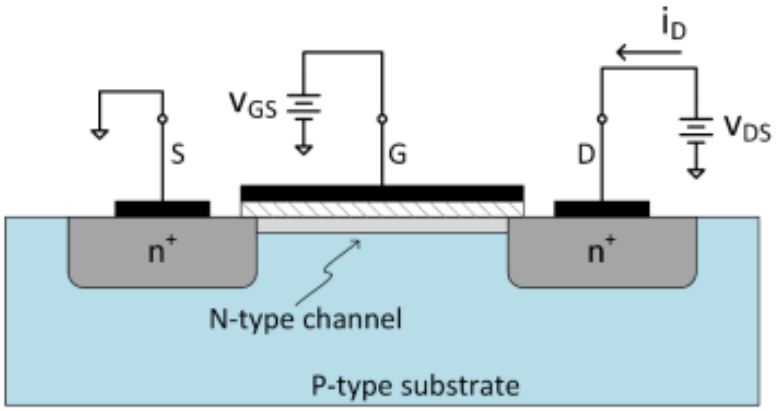
Review of MOSFETs

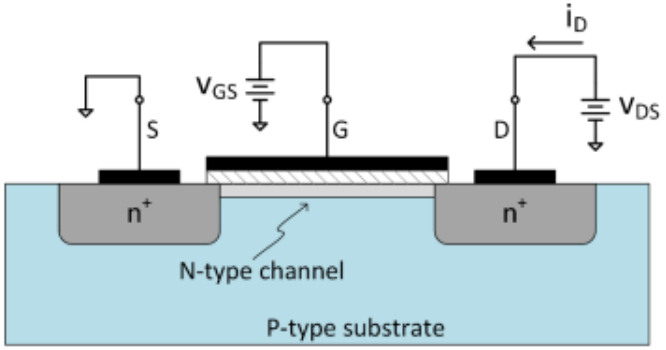
Inversion



- Now, v_{GS} is increased, while v_{DS} is kept small
  - Electric field established across gate oxide
  - Holes in p-type substrate repelled deeper into substrate
  - Electrons from drain and source attracted to region below the gate
- For large enough v_{GS}, p-type material below the gate is ***inverted*** to n-type
  - An ***inversion layer***
  - ***Induced n-type channel connects drain to source***
  - Now, current can flow in response to v_{DS}, $i_D > 0$

Review of MOSFETs

Threshold Voltage



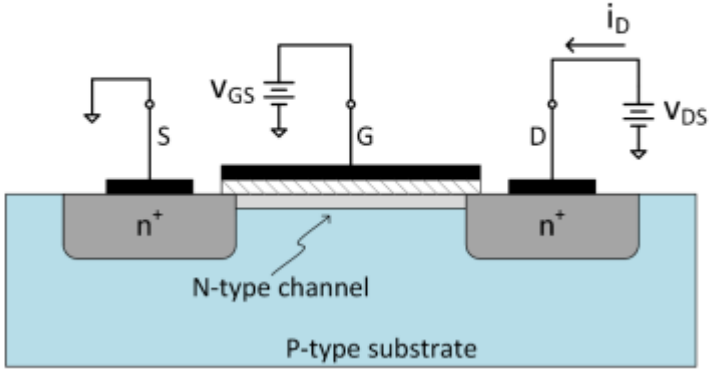
- Channel is induced once v_{GS} exceeds a certain voltage:
  - The ***threshold voltage***

$$v_{GS} \geq V_t$$

  - A device parameter
  - Typically, $V_t = 300\ mV \ldots 1\ V$
- As v_{GS} increases beyond V_t, the induced channel gets deeper
- As long as v_{DS} is small ($v_{DS} \ll V_t$), channel depth is uniform

Review of MOSFETs

Overdrive Voltage

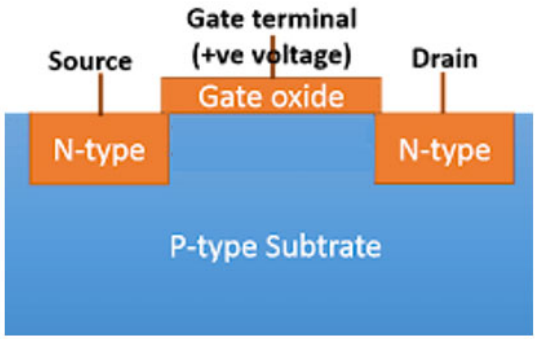


- A channel is induced once v_{GS} exceeds the threshold voltage
- v_{GS} in excess of the threshold voltage is called the ***overdrive voltage*** or ***effective voltage***:

$$v_{OV} = v_{GS} - V_t$$

- As we will soon see, v_{OV} plays an important role in determining device behavior

Review of MOSFETs



Channel formation basics

- A channel forms when

$$V_{GS} > V_T$$

because inversion charge appears under the gate.

- Along the channel, the local inversion charge is

$$Q_n(x) \;\propto\; V_{GS} - V_T - V(x),$$

where $V(x)$ is the channel potential at position x.

- At the source end, $V(0) = 0 \implies Q_n(0) \propto V_{GS} - V_T$ (strong channel).
- At the drain end, $V(L) = V_{DS} \implies Q_n(L) \propto V_{GS} - V_T - V_{DS}$.

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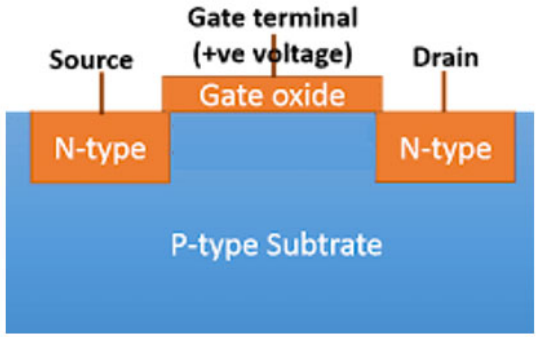
- At the source end, $V(0) = 0 \implies Q_n(0) \propto V_{GS} - V_T$ (strong channel).
- At the drain end, $V(L) = V_{DS} \implies Q_n(L) \propto V_{GS} - V_T - V_{DS}$.

Condition for pinch-off

- If $V_{DS} < V_{GS} - V_T$:
  Channel charge is positive all along the channel → continuous inversion path from source to drain. MOSFET is in **linear/triode region**.
- If $V_{DS} = V_{GS} - V_T$:
  At the **drain end**,

$$Q_n(L) = 0$$

  → the inversion channel just disappears at the drain edge → **onset of pinch-off**.
- If $V_{DS} > V_{GS} - V_T$:
  No inversion possible near the drain. Instead:
  - Channel terminates at a "pinch-off point" before the drain.
  - Beyond this, a depletion region carries the extra potential drop.
  - Current saturates since the effective voltage across the channel is clamped at $V_{GS} - V_T$.



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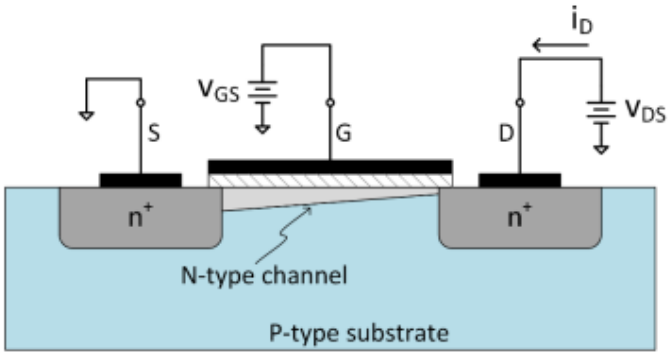
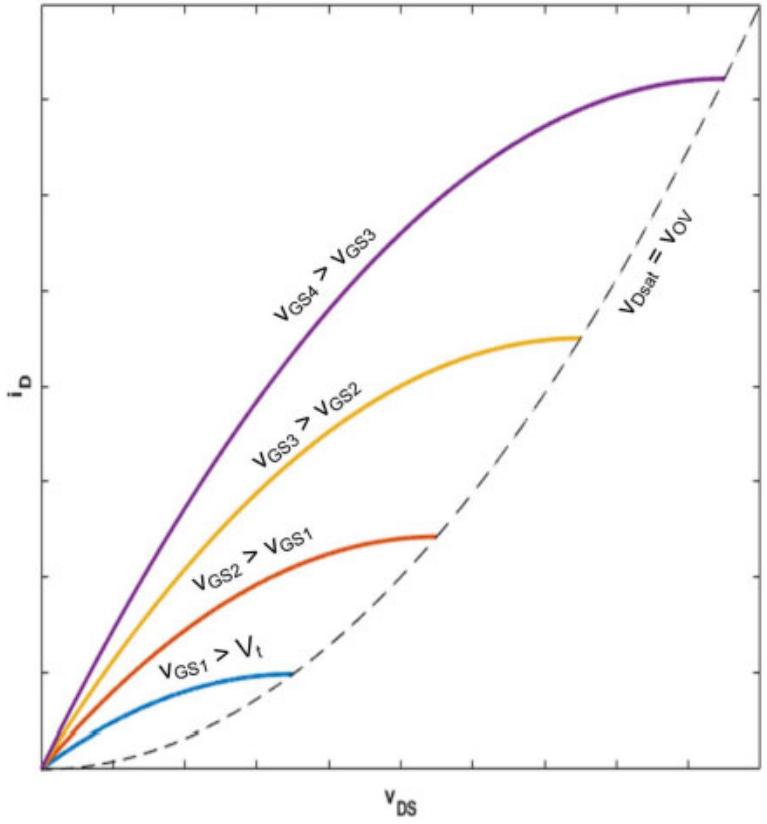
Review of MOSFETs- Linear Region





- As v_{DS} increases:
  - Voltage varies along the channel
    - v_S near the source, v_D near the drain
  - Gate-to-channel voltage decreases closer to the drain
  - Channel depth decreases closer to the drain
    - Channel is tapered
- More current flows with increasing v_{DS}, but channe. resistance increases as channel becomes more tapered

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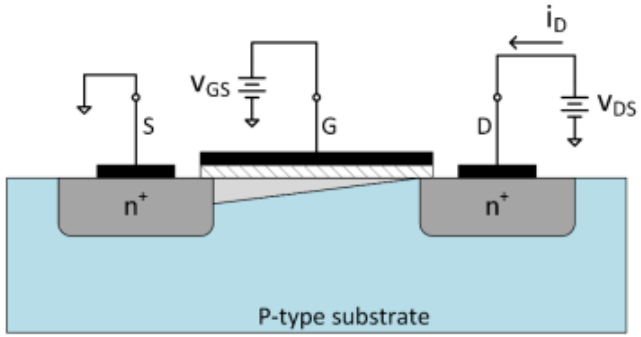
Review of MOSFETs- Linear Region

Channel Pinch-Off



- Eventually, for large enough v_{DS}
  - Gate-to-channel voltage near the drain no longer exceeds V_t
  - Channel ***pinch-off*** occurs
  - Channel disappears at the edge of the drain
- Pinch-off occurs when:

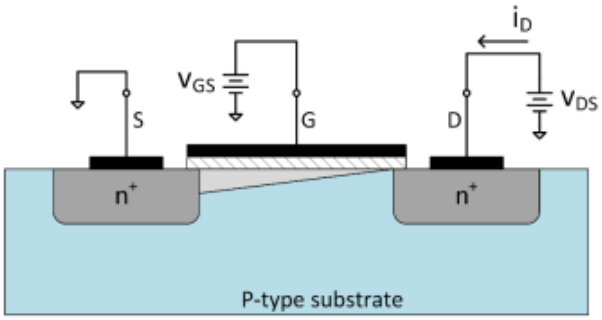
$$v_{GD} = V_t = v_{GS} - v_{DS}$$

$$v_{DS} = v_{GS} - V_t$$

Review of MOSFETs- Linear Region

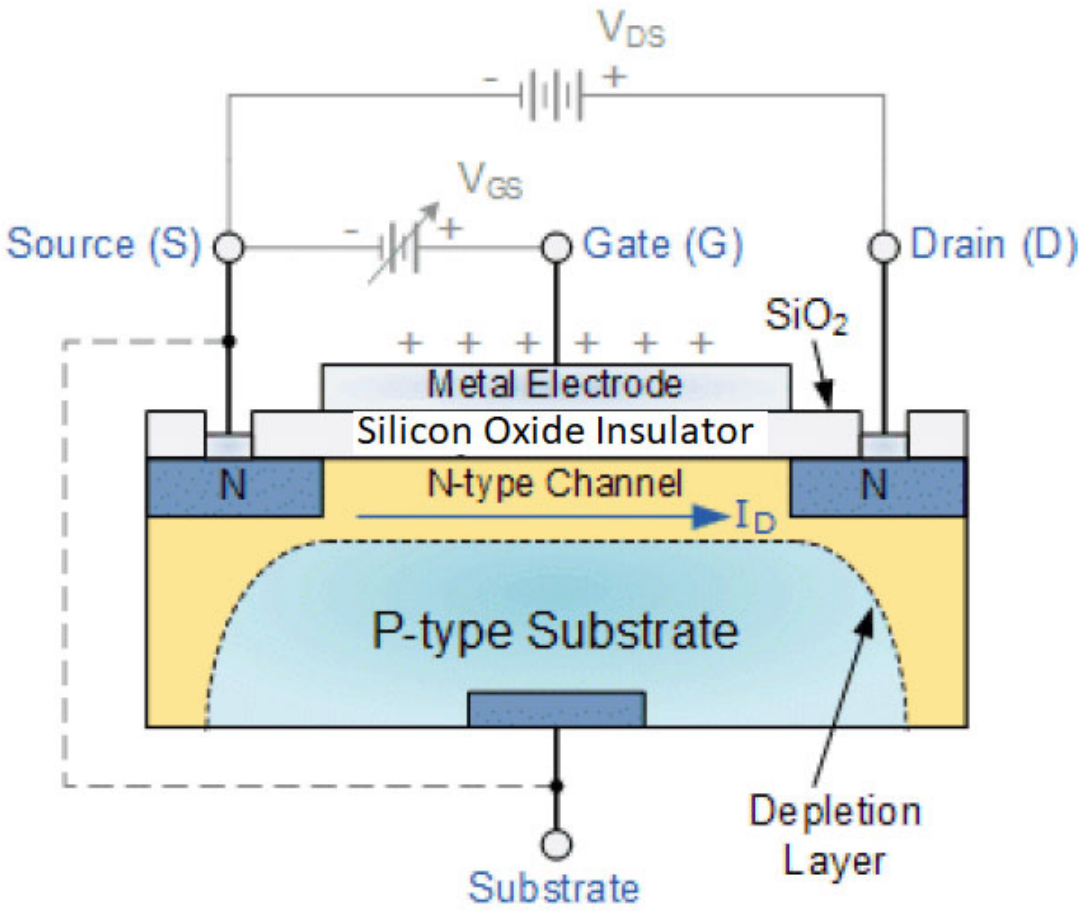
Saturation Region

- Once channel pinch-off occurs:
  - Voltage at the drain-end of the channel remains v_{OV}, even as v_{DS} increases
  - Any increase in v_{DS} beyond v_{OV} is dropped across the depletion region surrounding the drain

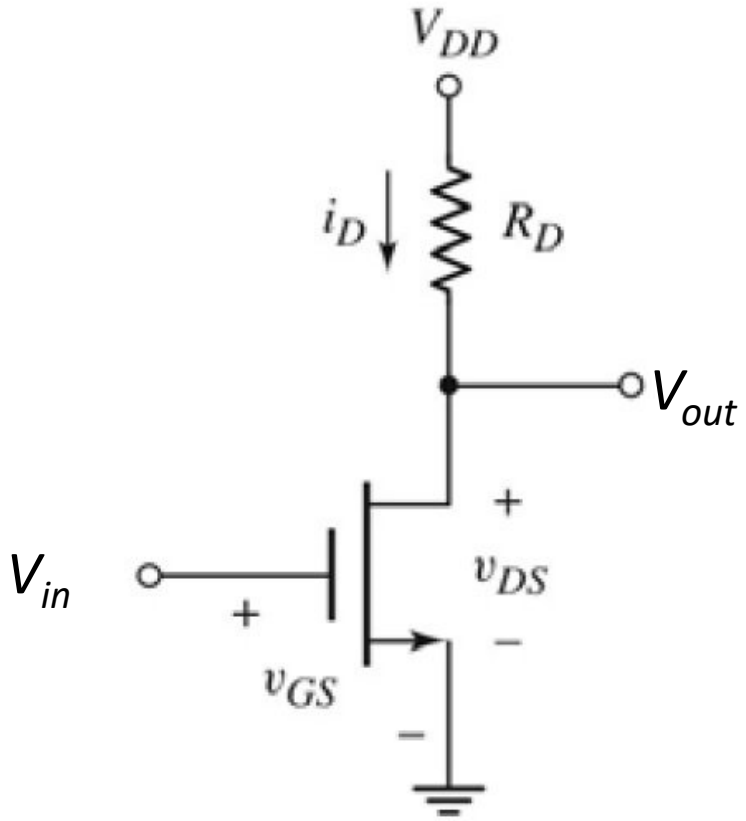


  - Voltage across the length of the channel is fixed at v_{OV}
  - Pinched-off channel shape does not change with v_{DS}
  - Drain current ***saturates*** at a constant value for constant v_{GS}

Review of MOSFETs- Linear Region



Review of MOSFETs: DC load line of n-MOSFET



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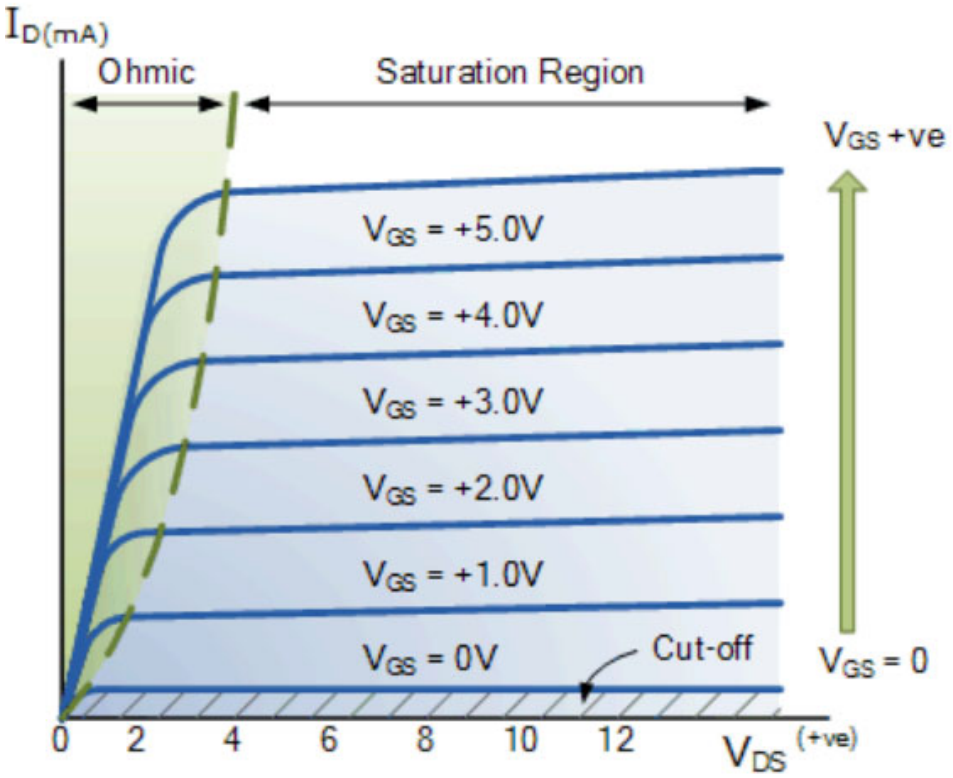
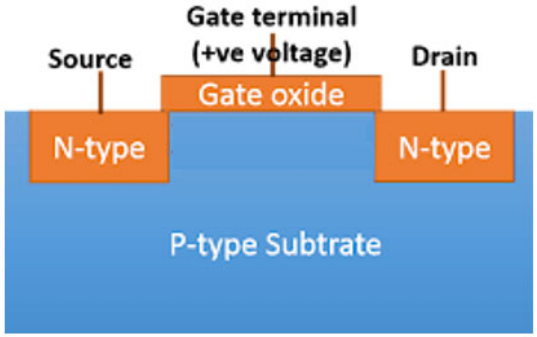
Review of MOSFETs





Relation between V_{DS} & V_{GS}

Case	V_T	Channel condition
Linear region	$V_{DS} < V_{GS} - V_T$	Continuous inversion from source to drain
Pinch-off onset	$V_{DS} = V_{GS} - V_T$	Channel just disappears at drain end
Saturation	$V_{DS} > V_{GS} - V_T$	Pinch-off near drain, depletion region forms, current saturates

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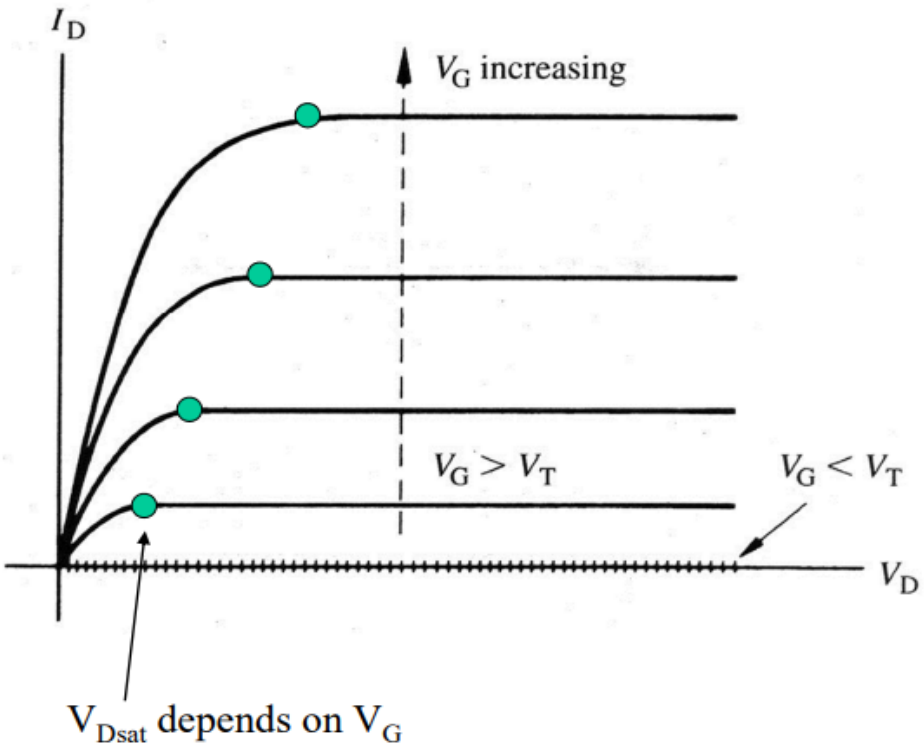
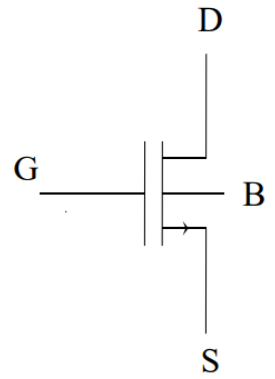
Review of MOSFETs

I_D-V_{DS} curves for various V_{GS}:



$$\beta = \mu C_{ox} \frac{W}{L}$$

n-channel MOS Transistor



$$_s = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

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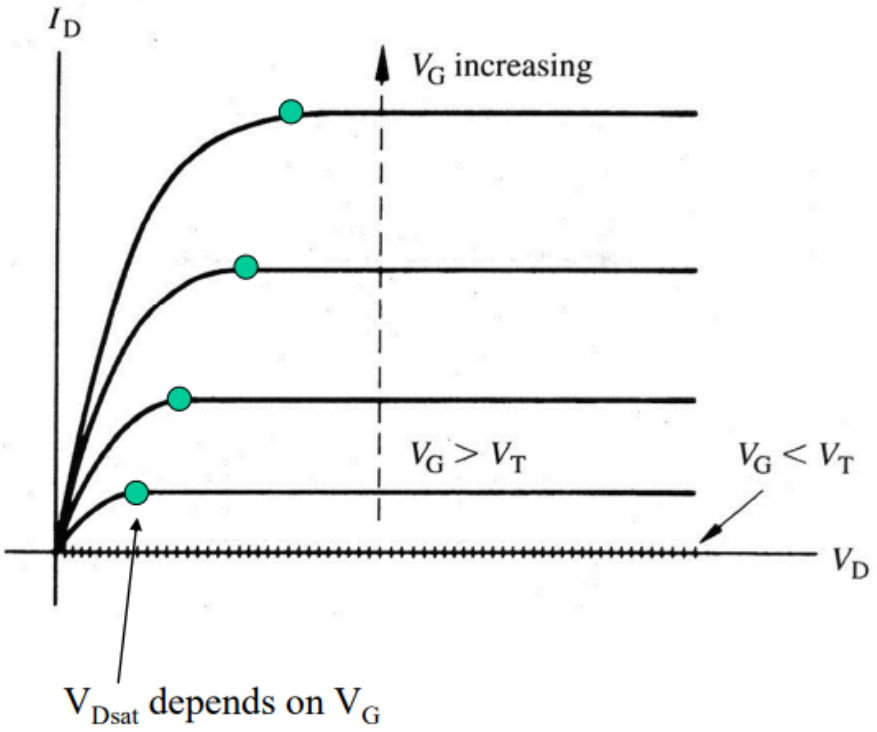
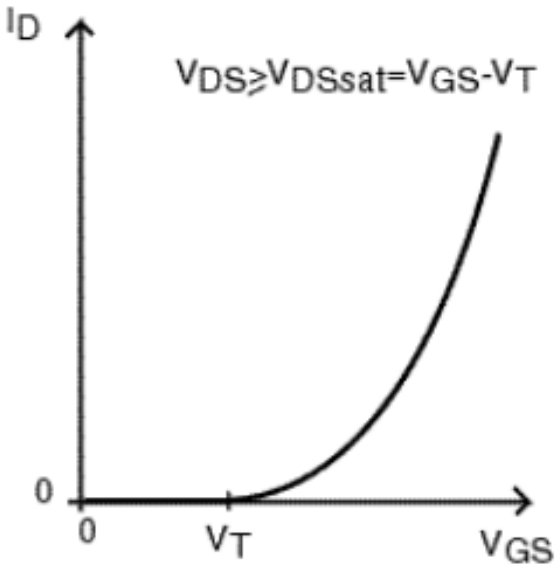
Review of MOSFETs: DC load line of n-MOSFET

I_D-V_{DS} curves for various V_{GS}:



Transfer characteristics:



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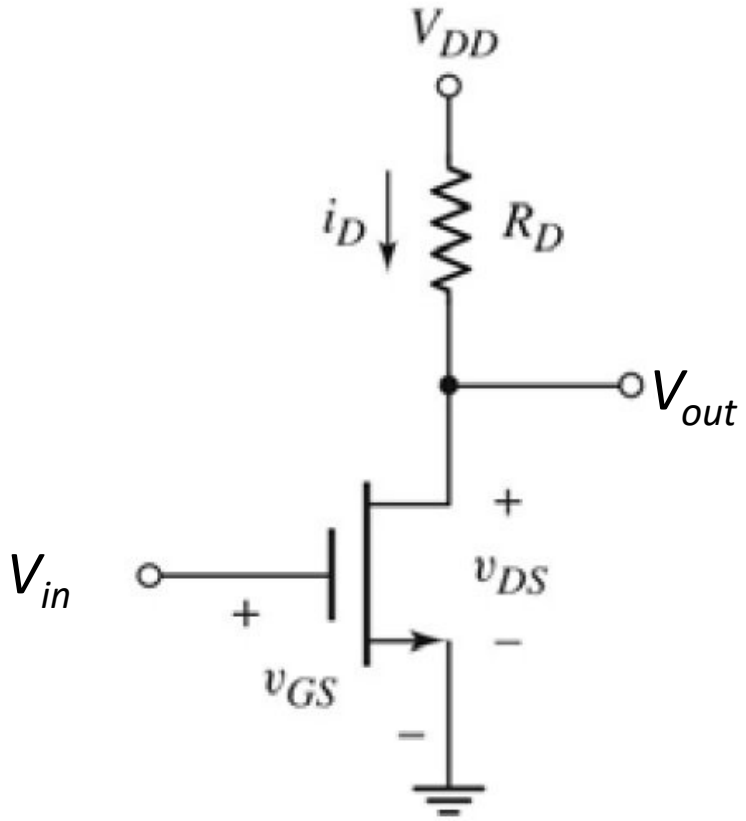

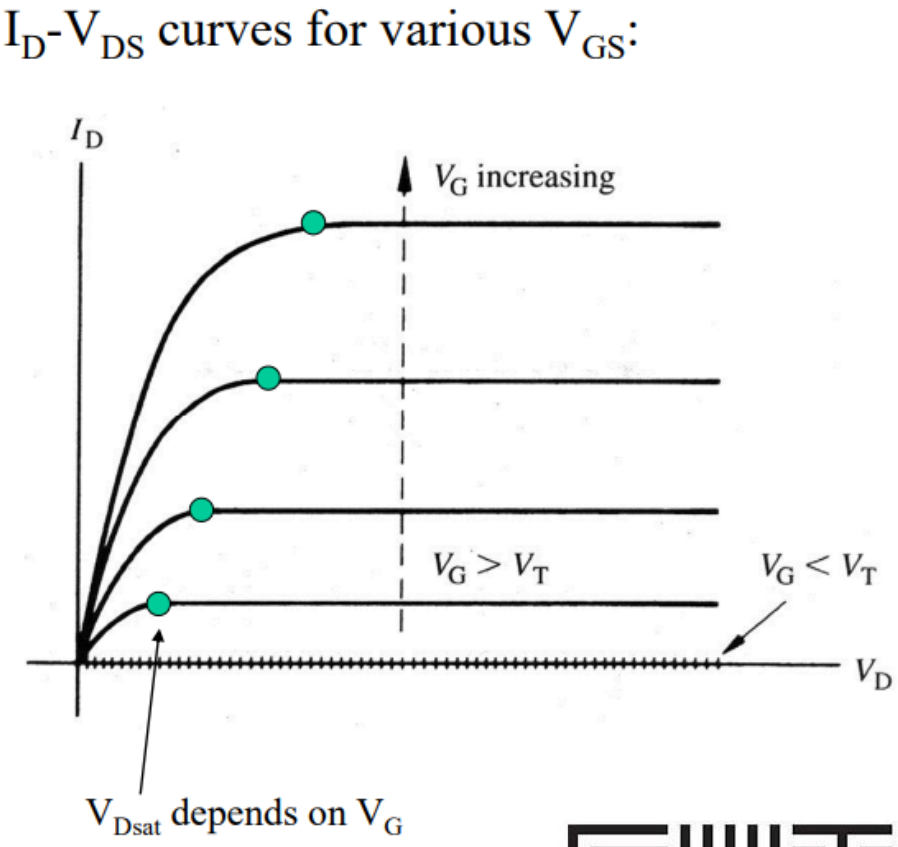

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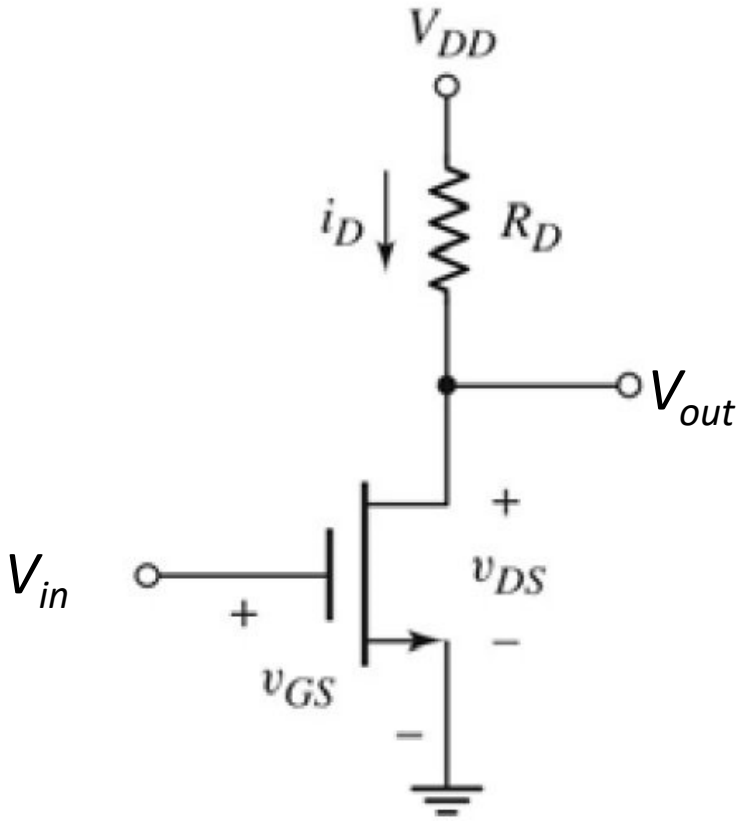

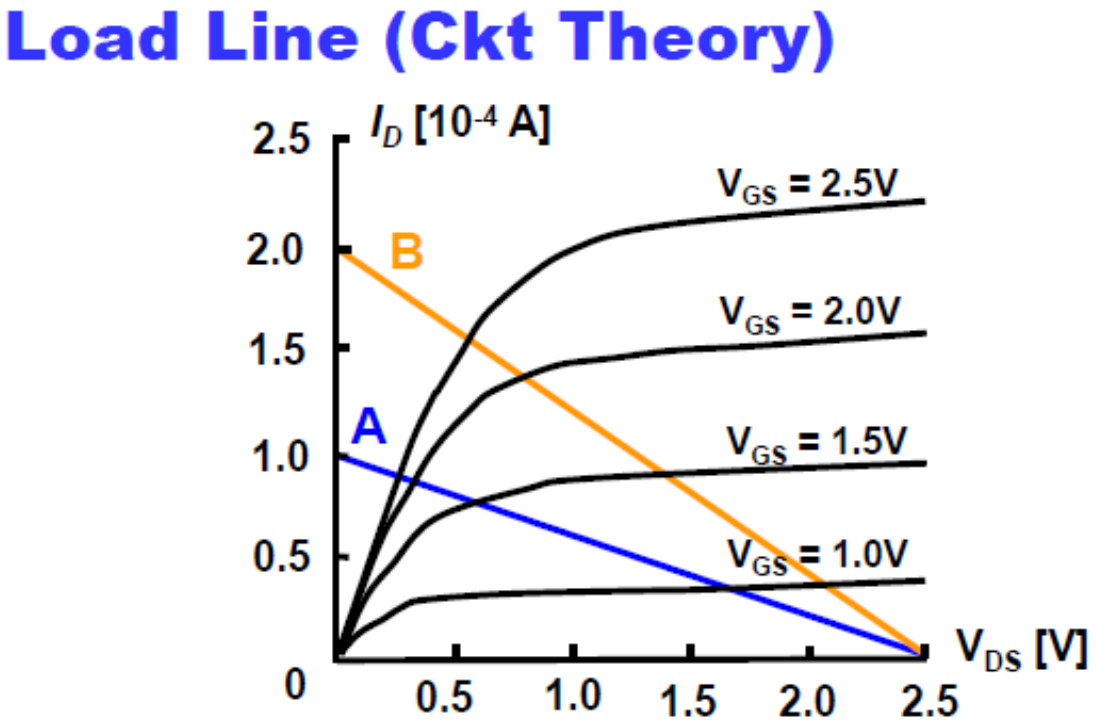

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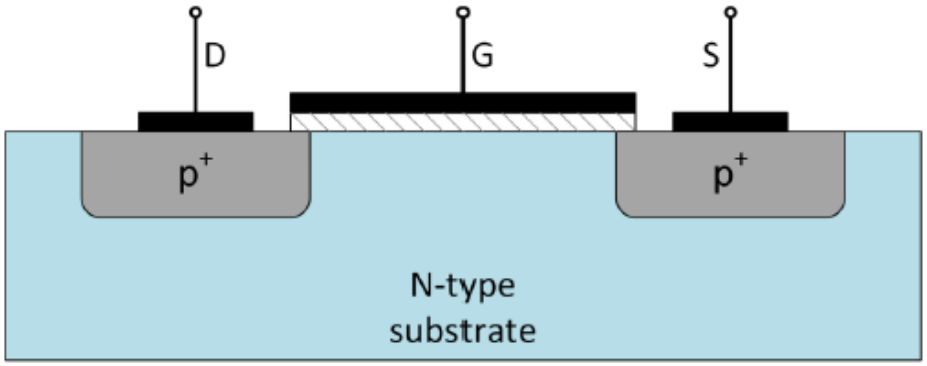
Review of MOSFETs

P-Channel MOSFETs

- Voltage polarities and doping types reversed relative to NMOS
  - N-type substrate
  - P+ drain and source
  - Negative threshold voltage: $V_{tp} < 0$
  - Negative overdrive voltage: $v_{OV} = v_{GS} - V_{tp} < 0$
  - Channel induced for $v_{GS} \leq V_{tp}$
  - Substrate connected to source or most positive circuit voltage



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Review of MOSFETs

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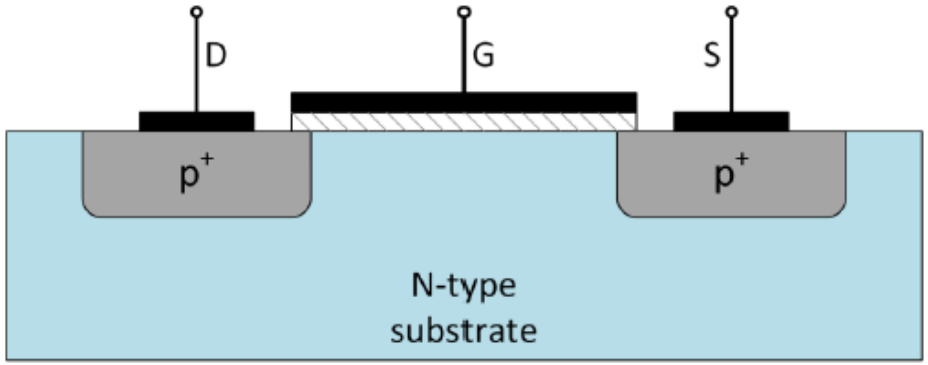
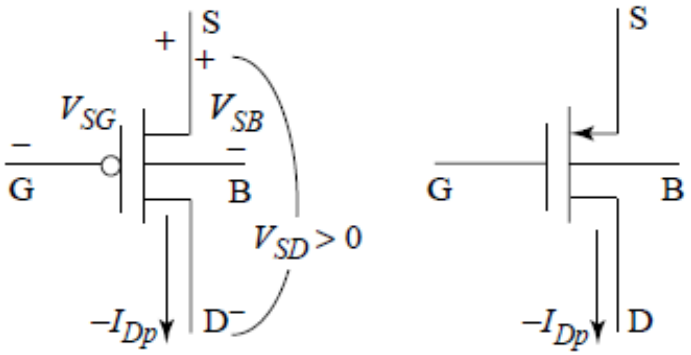
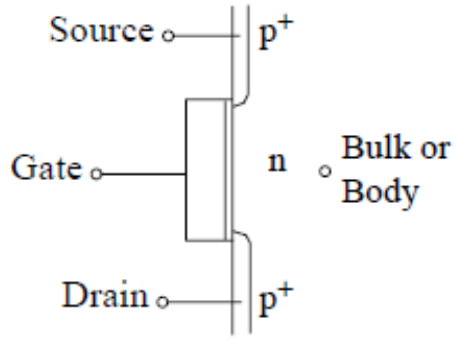




(b) p-channel MOSFET



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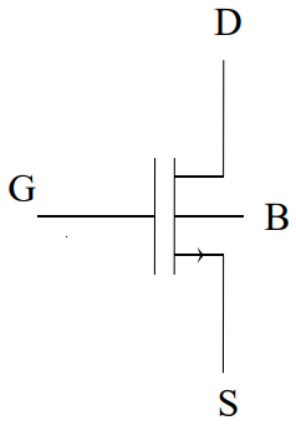
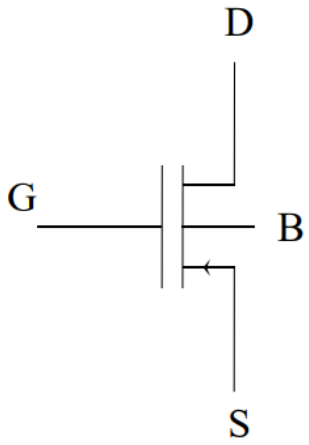
Review of MOSFETs

n-channel MOS Transistor



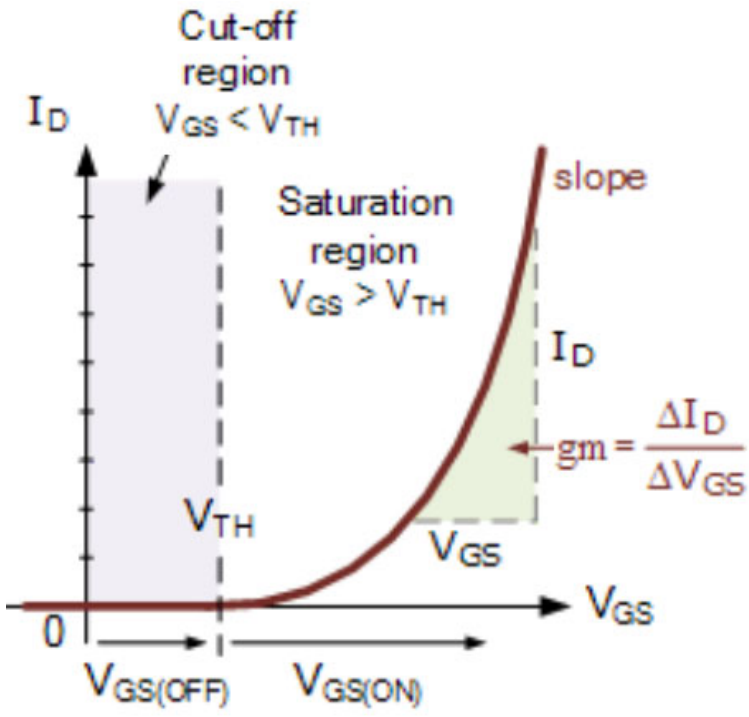
p-channel MOS Transistor



MOSFET type	V_{GS} = +ve	V_{GS} = 0	V_{GS} = -ve
N-Channel	ON	OFF	OFF
P-Channel	OFF	OFF	ON

MOSFET: Threshold Voltage (V_{th})

- The voltage needed on the Gate terminal of the MOSFET to form a thin channel beneath the gate electrode (between Source & Drain terminals).
- The current can flow between S and D terminals through the channel.
- So threshold voltage is the voltage needed to turn on the device.
- As the MOSFET is voltage controlled current source, the output current will depend on the gate voltage applied.



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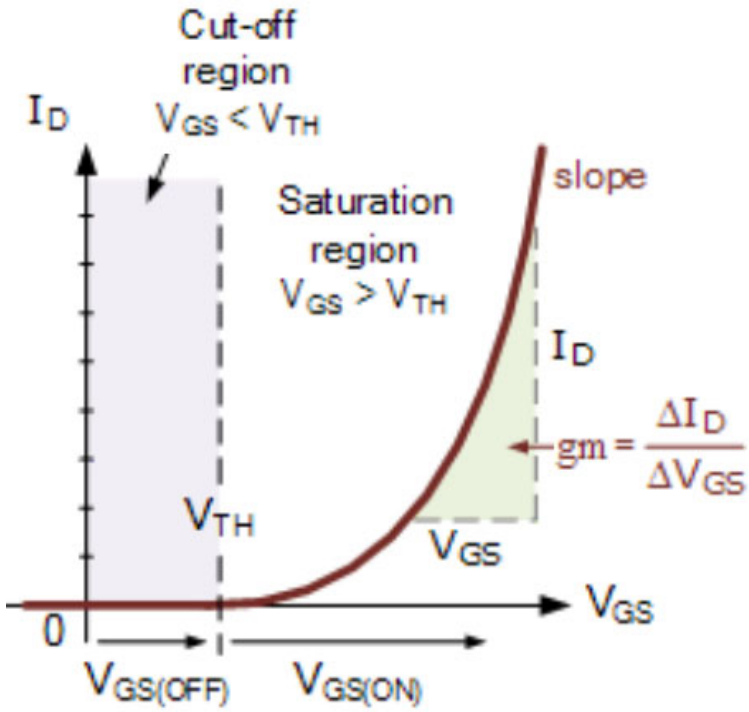
MOSFET: Threshold Voltage (V_{th})

- Lower Vth:
  - Faster in timing
  - Higher subthreshold current
- Higher Vth:
  - Less leakage
  - Higher delay
- V_{th} scales with MOSFET scaling



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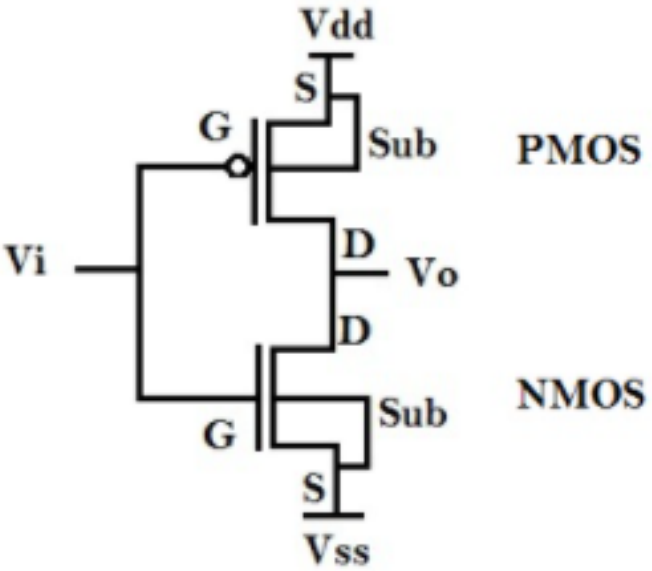
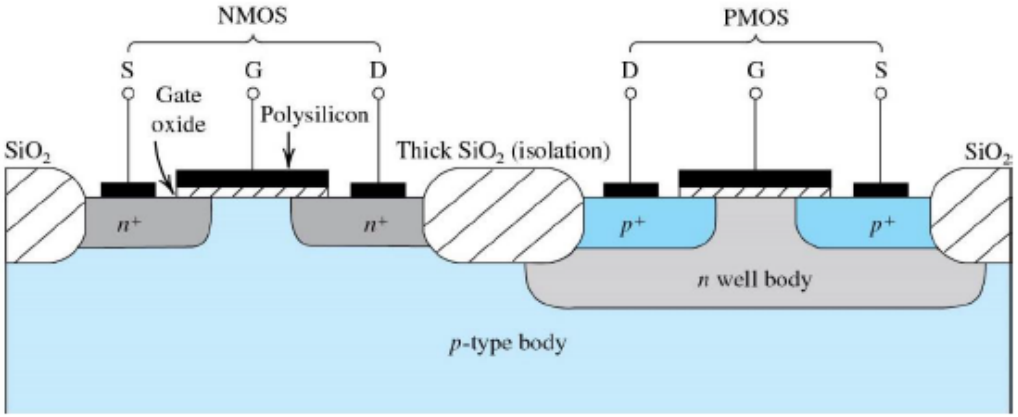
CMOS circuit



G = Gate Terminal
S = Source Terminal
D = Drain Terminal
Sub = Substrate Terminal

CMOS

- Complementary MOS or ***CMOS***
  - Both NMOS and PMOS fabricated on the same chip
- P-type substrate
- PMOS devices fabricated in ***n wells***
- Most modern MOS chips are fabricated using CMOS technology



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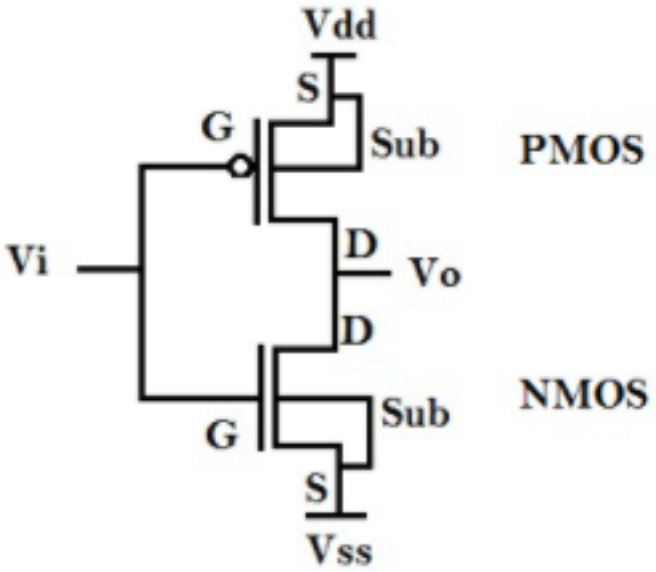
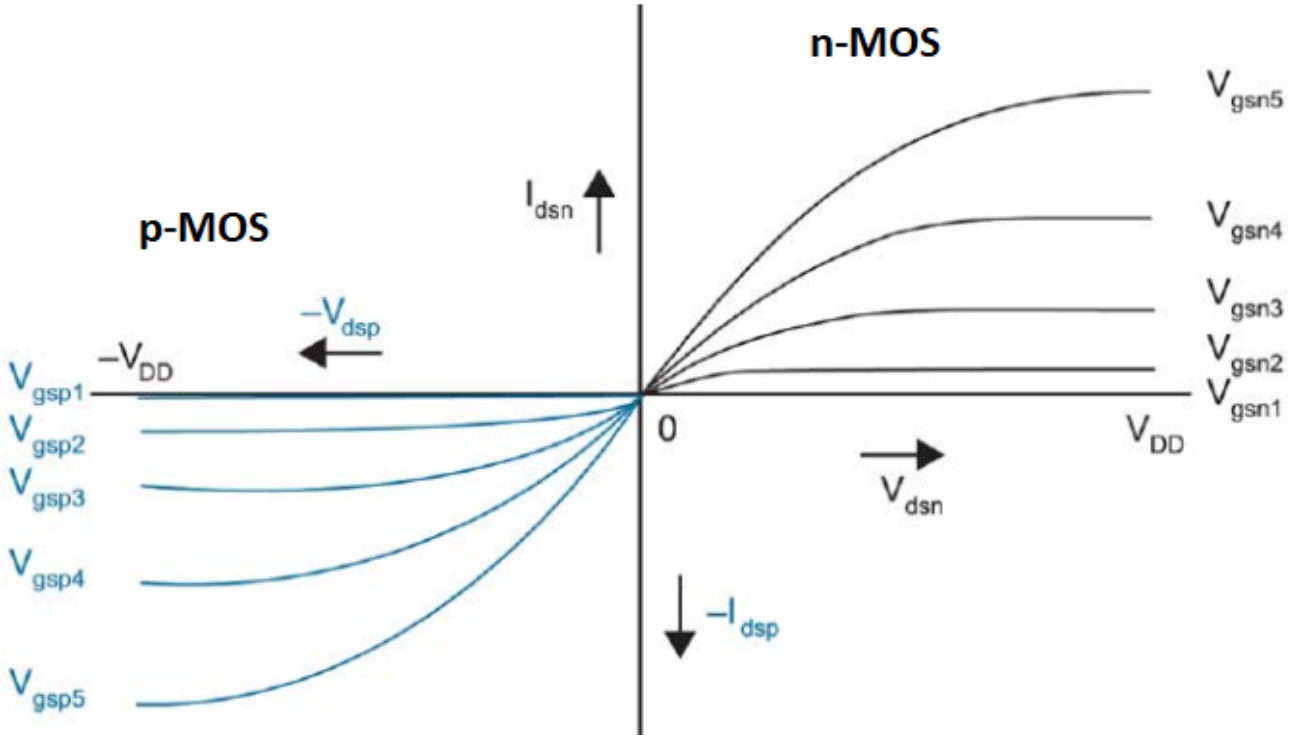
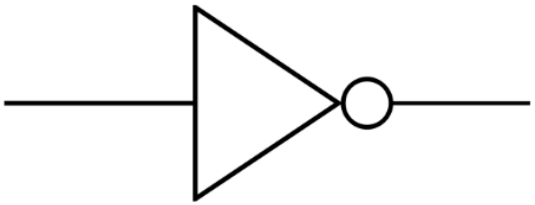
CMOS circuit







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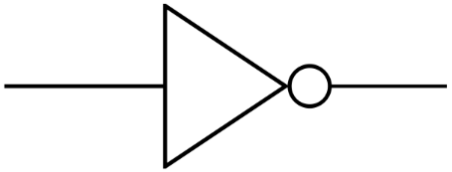
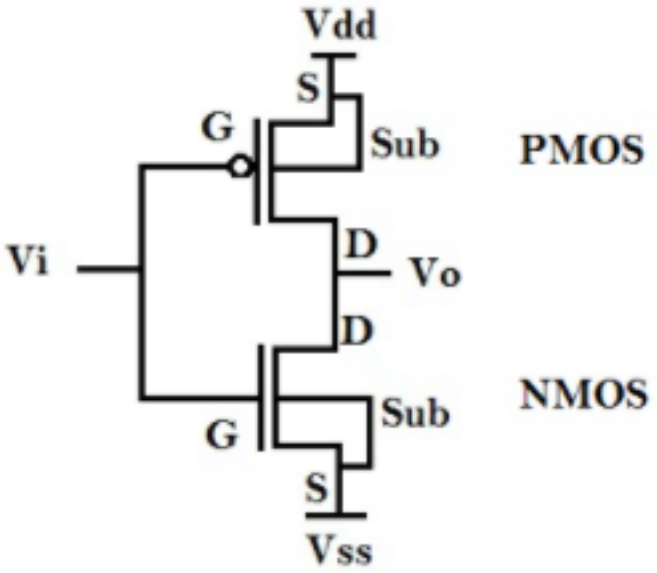
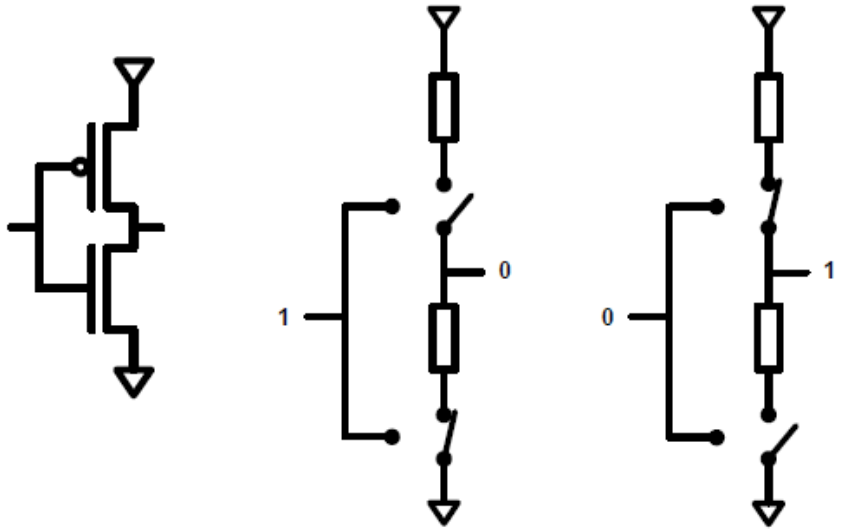
CMOS circuit





CMOS Inverter Operation Principle



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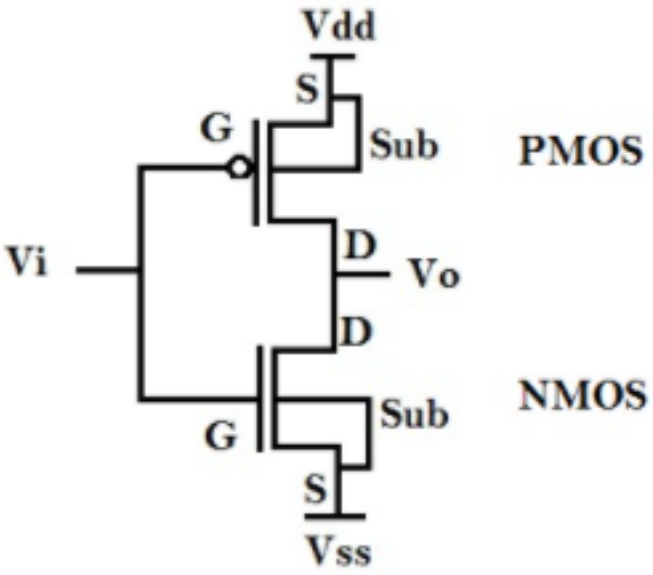
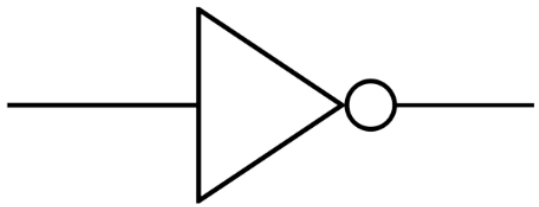
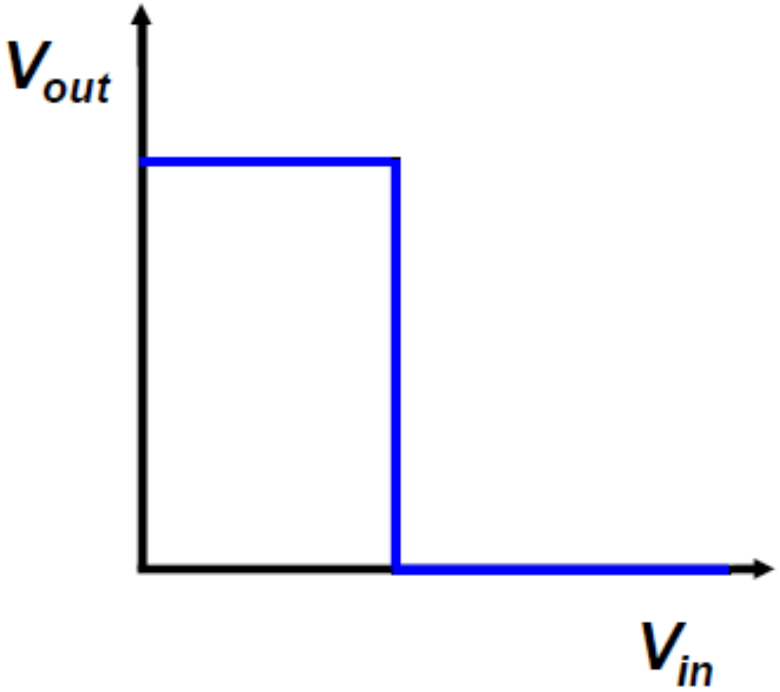
CMOS circuit





The Ideal Inverter



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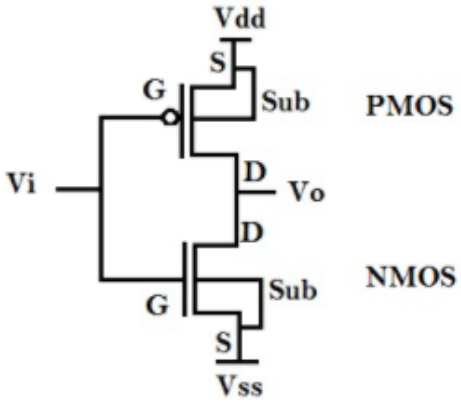
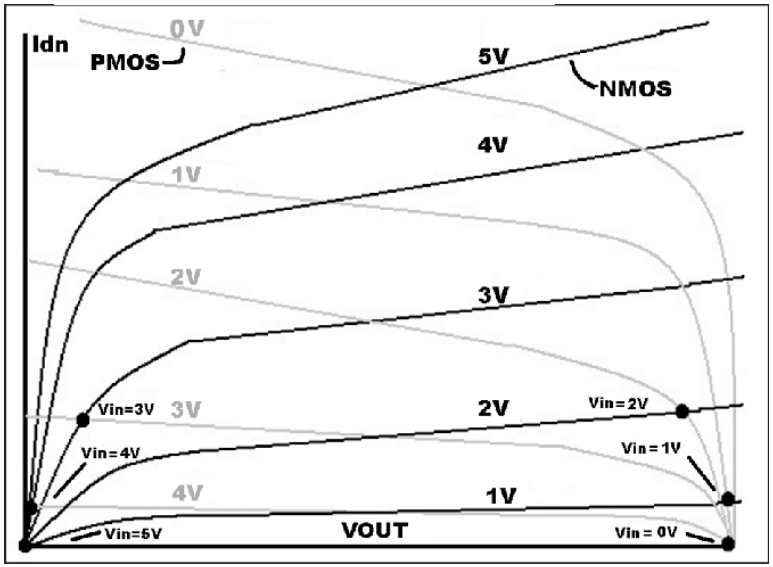
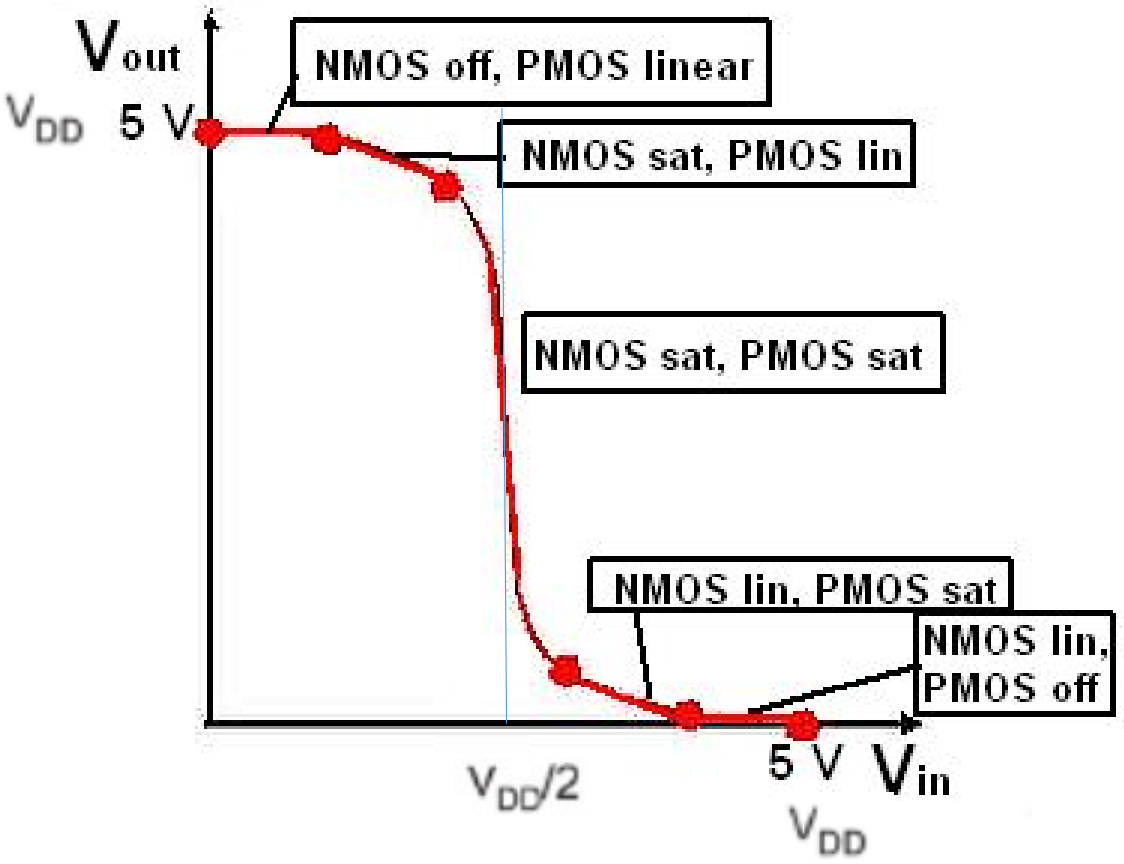
CMOS circuit





CMOS inverter transfer function



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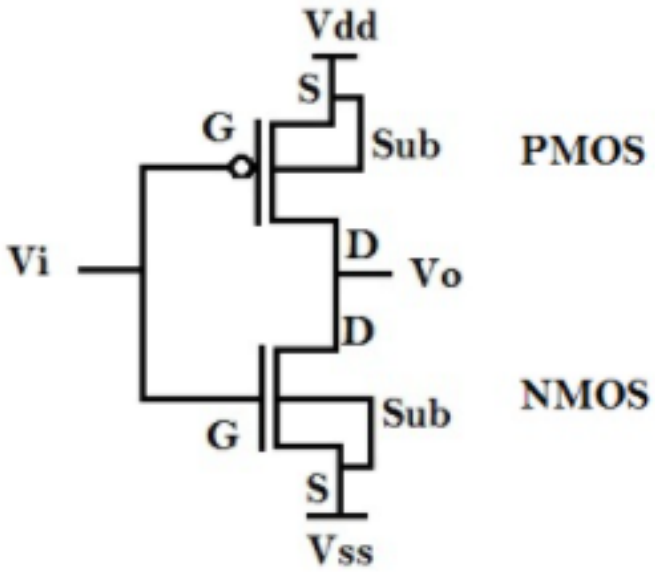
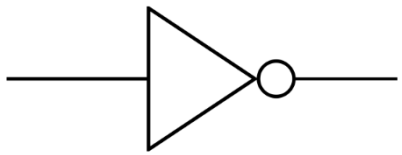
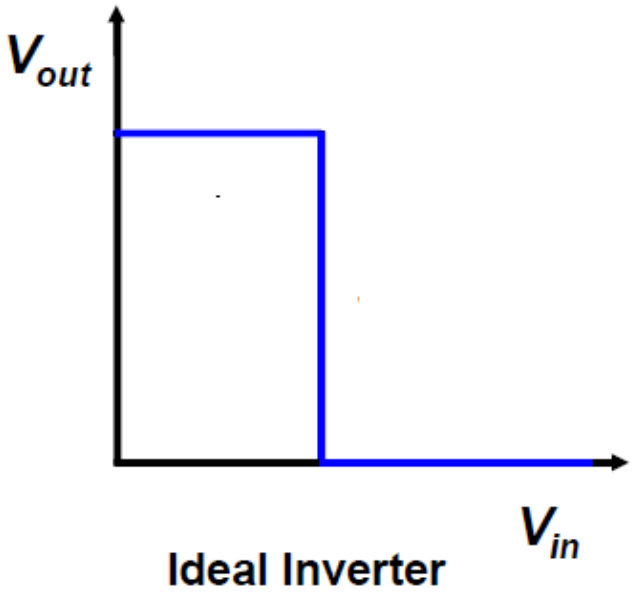
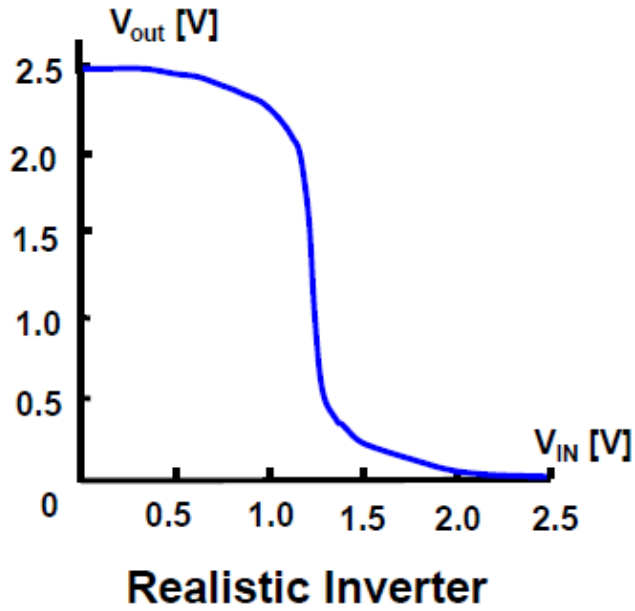
CMOS circuit





The Realistic Inverter





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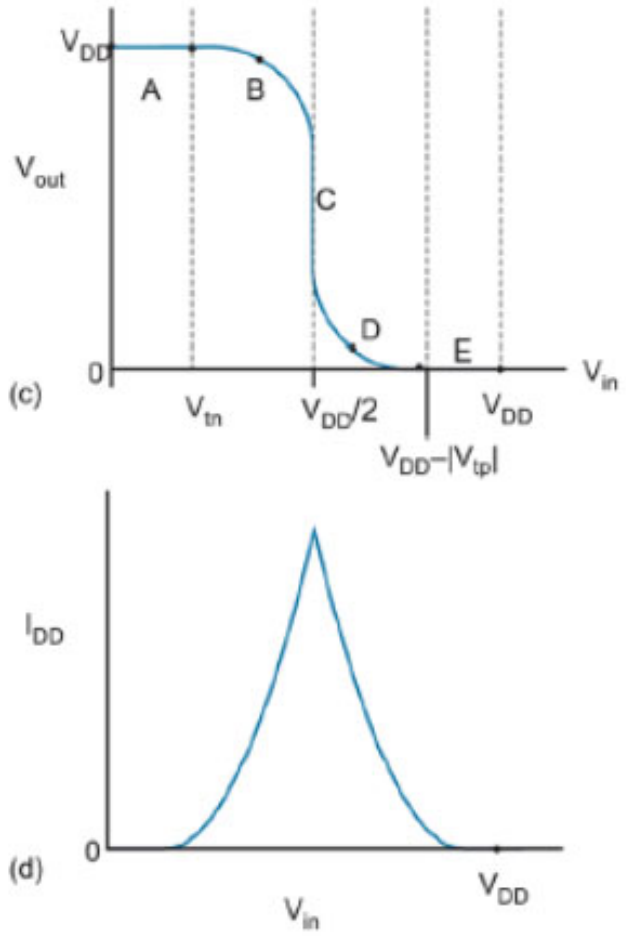
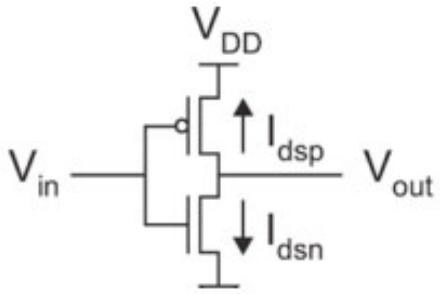
CMOS circuit





A CMOS inverter

Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \|V_{tp}\|$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \|V_{tp}\|$	cutoff	linear	$V_{out} = 0$

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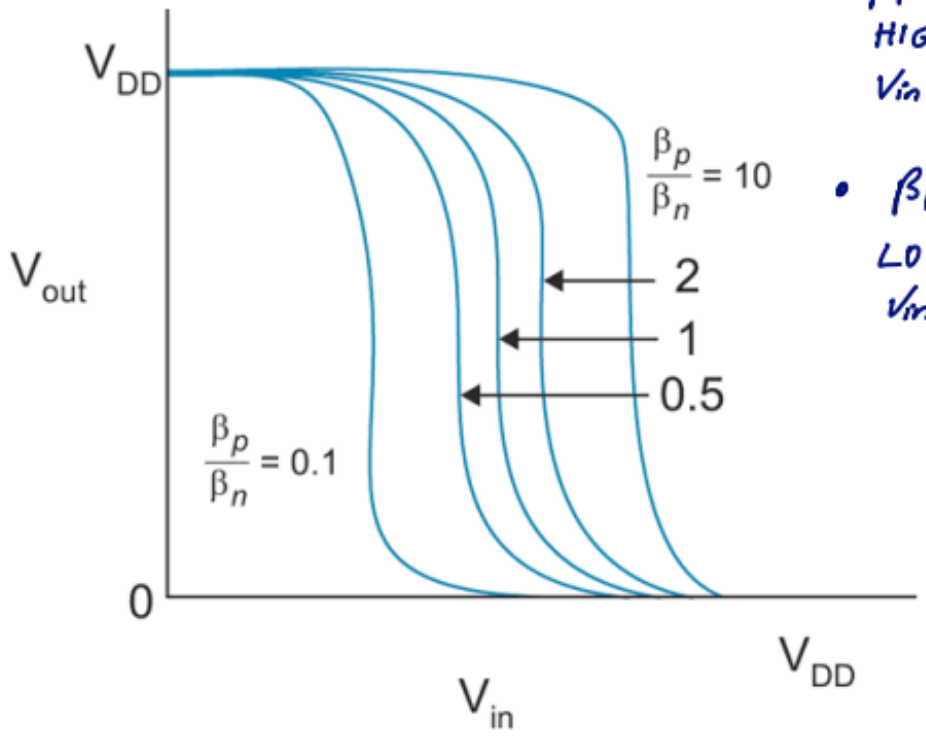
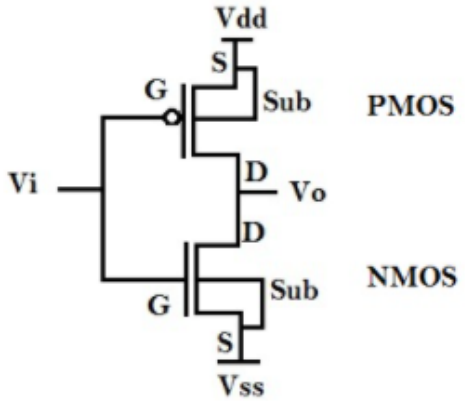
CMOS circuit

$$\beta = \mu C_{ox} \frac{W}{L}$$

If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$



- $\beta_p > \beta_n$
  HIGH SKEWED inverter
  $V_{in} = \frac{V_{DD}}{2} \rightarrow V_{out} > \frac{V_{DD}}{2}$
- $\beta_p < \beta_n$
  LOW SKEWED inverter
  $V_{in} = \frac{V_{DD}}{2} \rightarrow V_{out} < \frac{V_{DD}}{2}$



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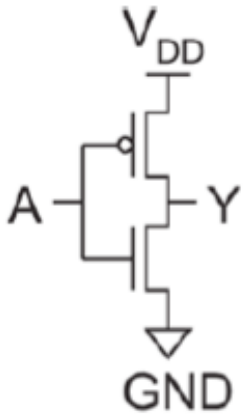
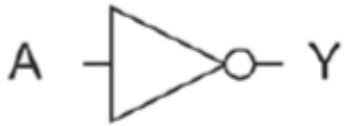
CMOS circuit

CMOS Inverter (= NOT gate)

Table 1.1 Inverter truth table

A	Y
0	1
1	0





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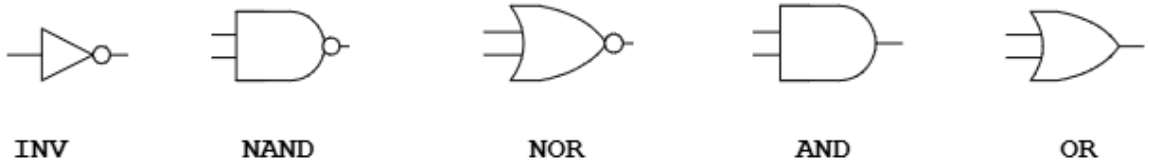
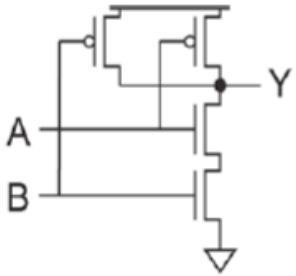
CMOS circuit



CMOS Logic NAND

Table 1.2 NAND gate truth table				
A	B	pull-down network	pull-up network	Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

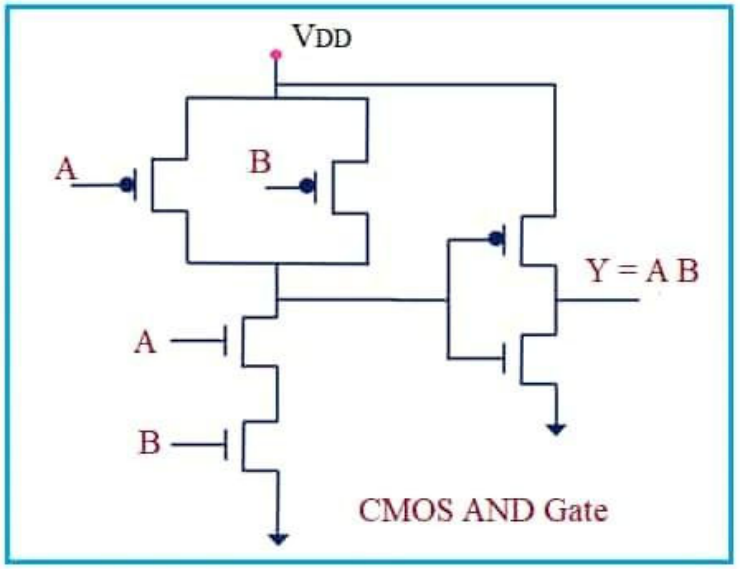


(a)

$$Y = \overline{A \bullet B}$$

(b)

AND Gate



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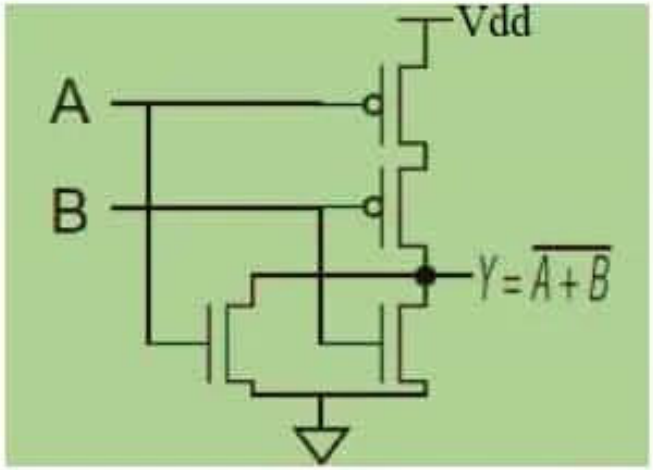
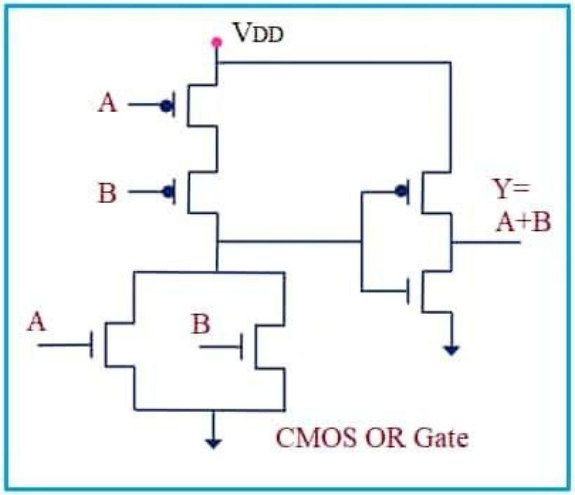
CMOS circuit

NOR Gate



A	B	A **NOR** B
0	0	1
0	1	0
1	0	0
1	1	0

OR Gate



A	B	Output (A OR B)
0	0	0
0	1	1
1	0	1
1	1	1

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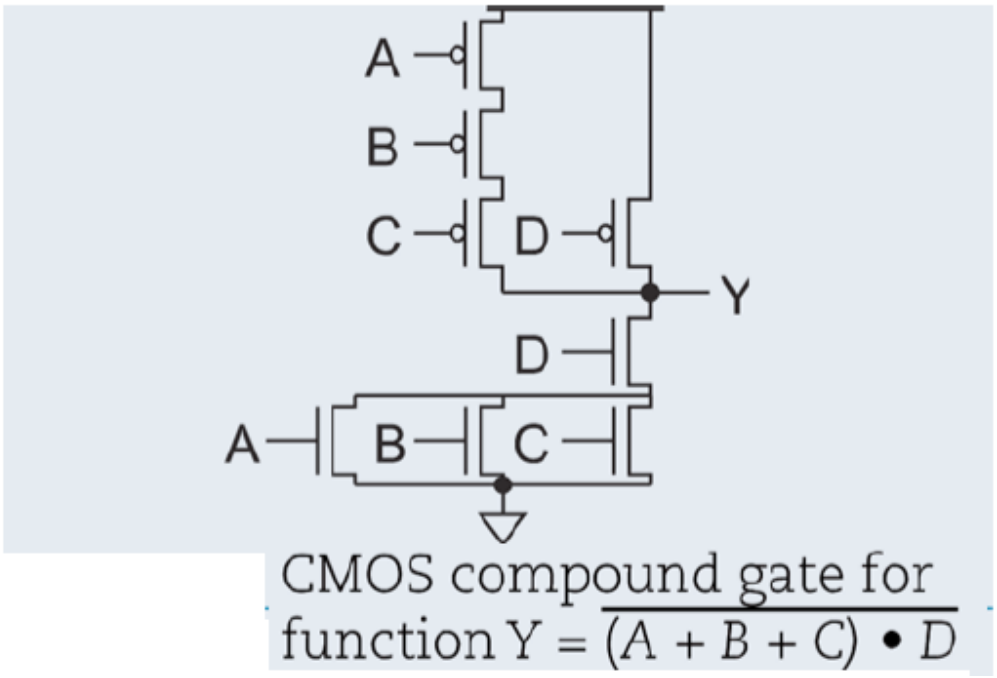
CMOS circuit

Compound gates



CMOS compound gate for function $Y = \overline{(A + B + C) \bullet D}$

CMOS circuit: Noise Margin

- Noise margin is the ratio by which the signal exceeds the minimum acceptable amount.
- It explains up to what extent IC allows noise in the transmission of logic ‘0’ and logic ‘1’.
- Logic ‘0’ and ‘1’ – represent the range of input values
- Hence, for error free digital signal transmission noise margin is required

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CMOS circuit: Noise Margin

- **Noise margin** refers to how much unwanted noise (disturbance in voltage levels) a circuit can tolerate without misinterpreting logic levels. It essentially defines the safety "buffer" between valid logic-0 and logic-1 signals.
- Noise margin is critical in digital IC design because it ensures reliable operation in the presence of crosstalk, supply fluctuations, or electromagnetic interference.
- Higher VDD gives bigger absolute noise margins, but modern technology scales VDD down, so circuit design must ensure sufficient margins.

CMOS circuit: Noise Margin

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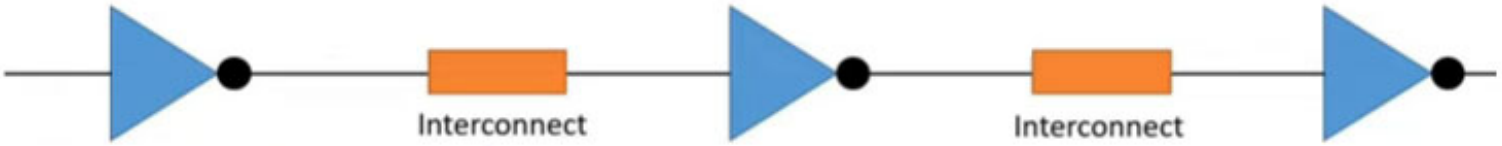

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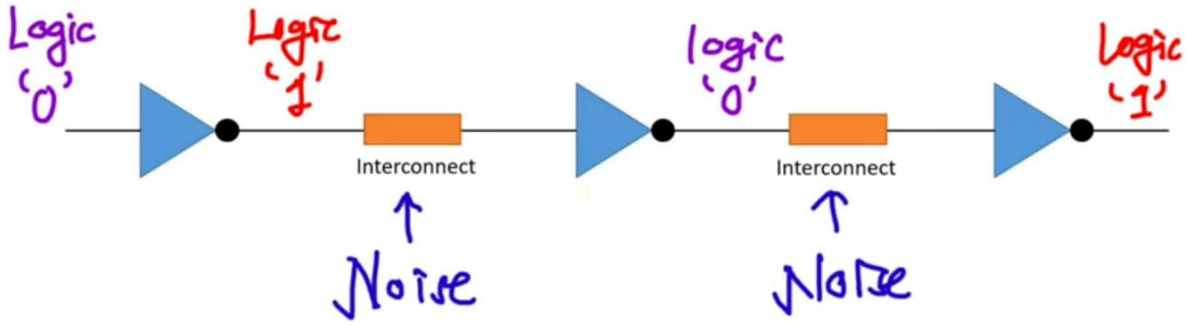

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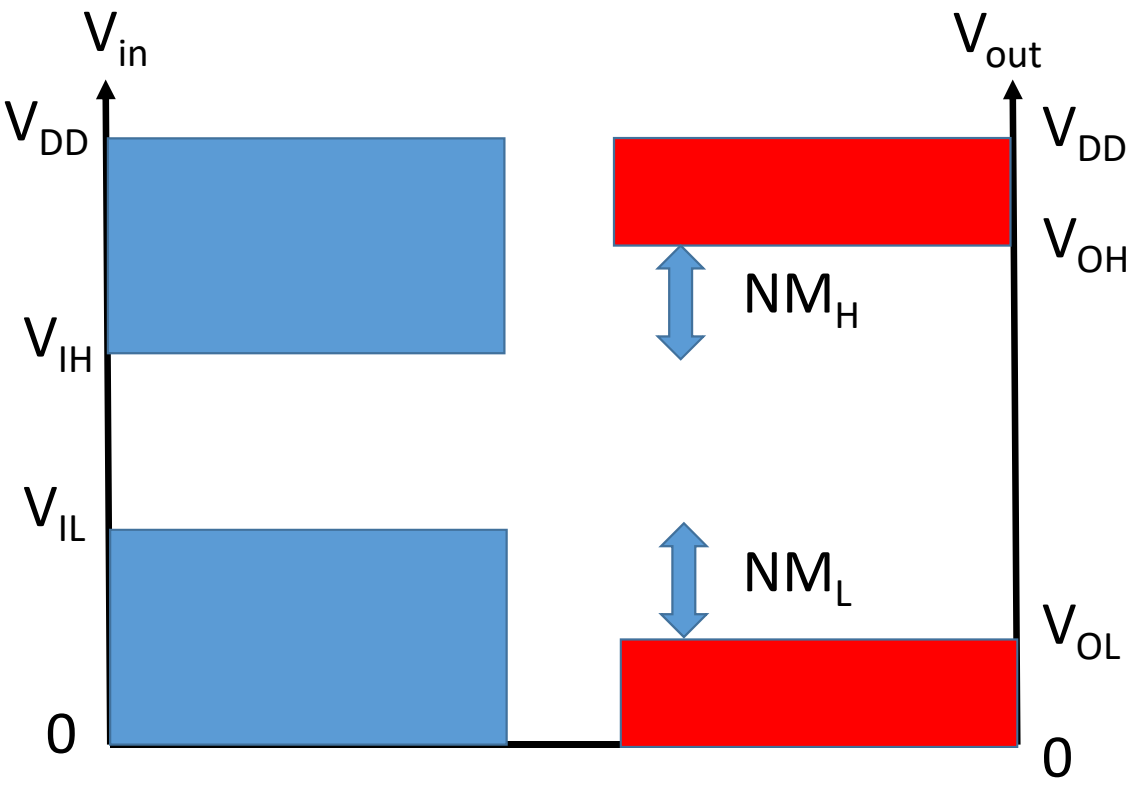
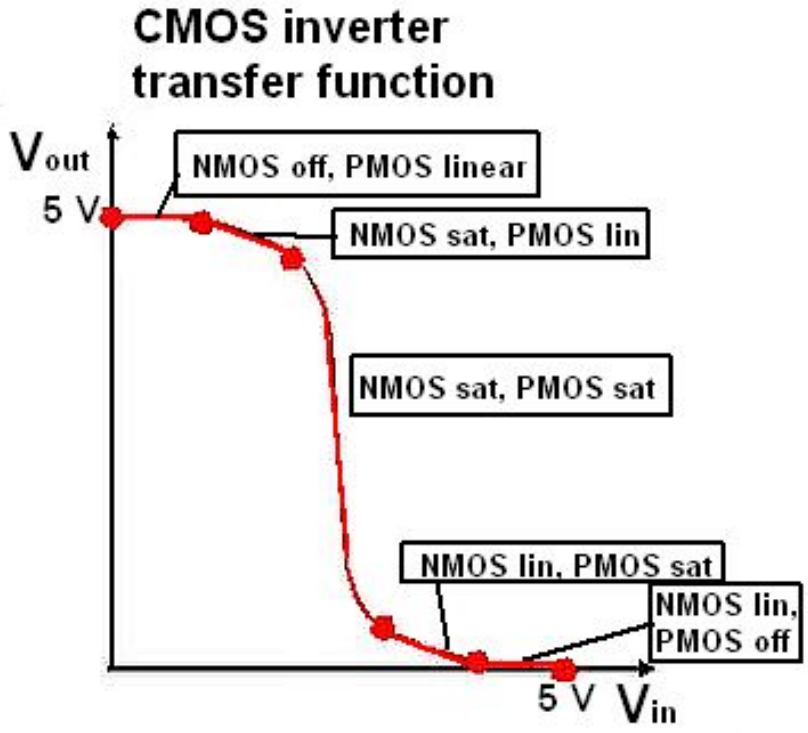
CMOS circuit: Noise Margin





$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

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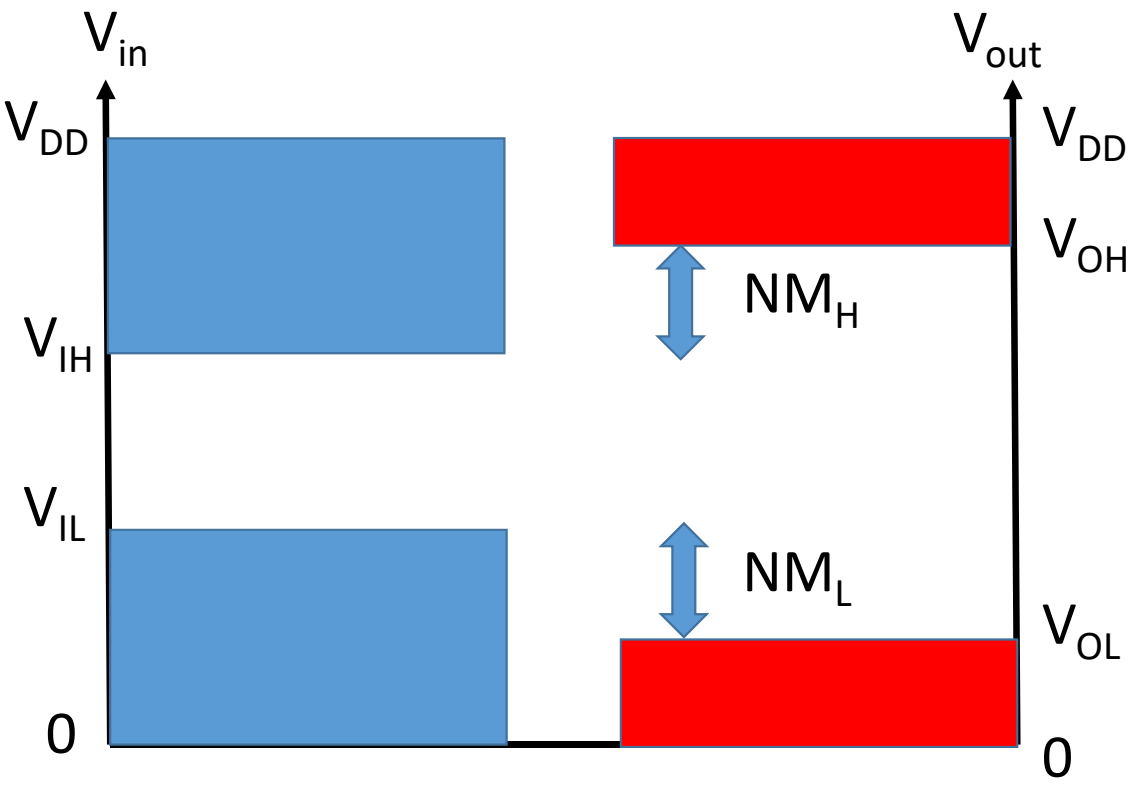
CMOS circuit: Noise Margin



$$NM_H = V_{OH} - V_{IH}$$

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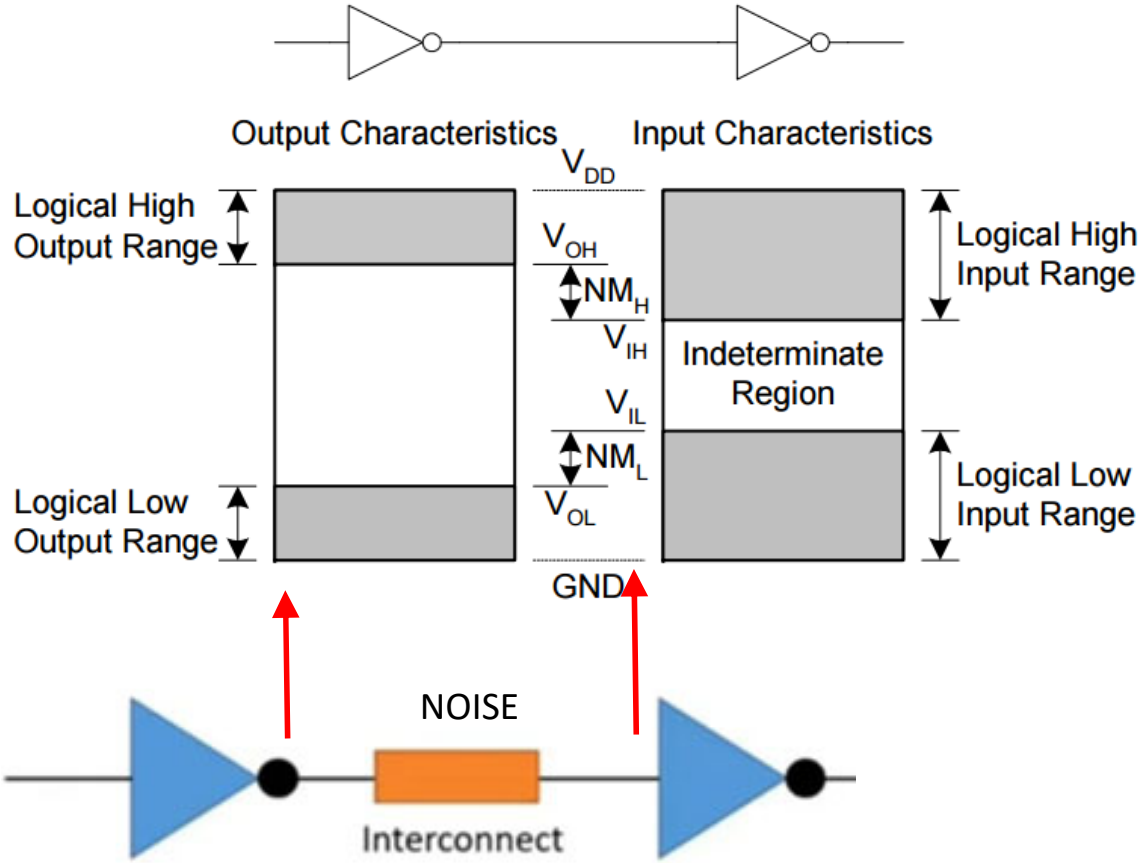
CMOS circuit: Noise Margin



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