SINGAPORE UNIVERSITY OF TECHNOLOGY AND DESIGN

Term 7- Sept 2024

Nanoelectronics and Technology (01.119/99.503)

Week 1 Day 2 (19-Sept 2024)

Outline

- Review of P and N type semiconductors
- Review of P-N junction, Metal-semiconductor (Schottky/Ohmic) junction
- Review of MOS Capacitors
- Review of MOSFETs
- CMOS Inverter circuit
- CMOS scaling

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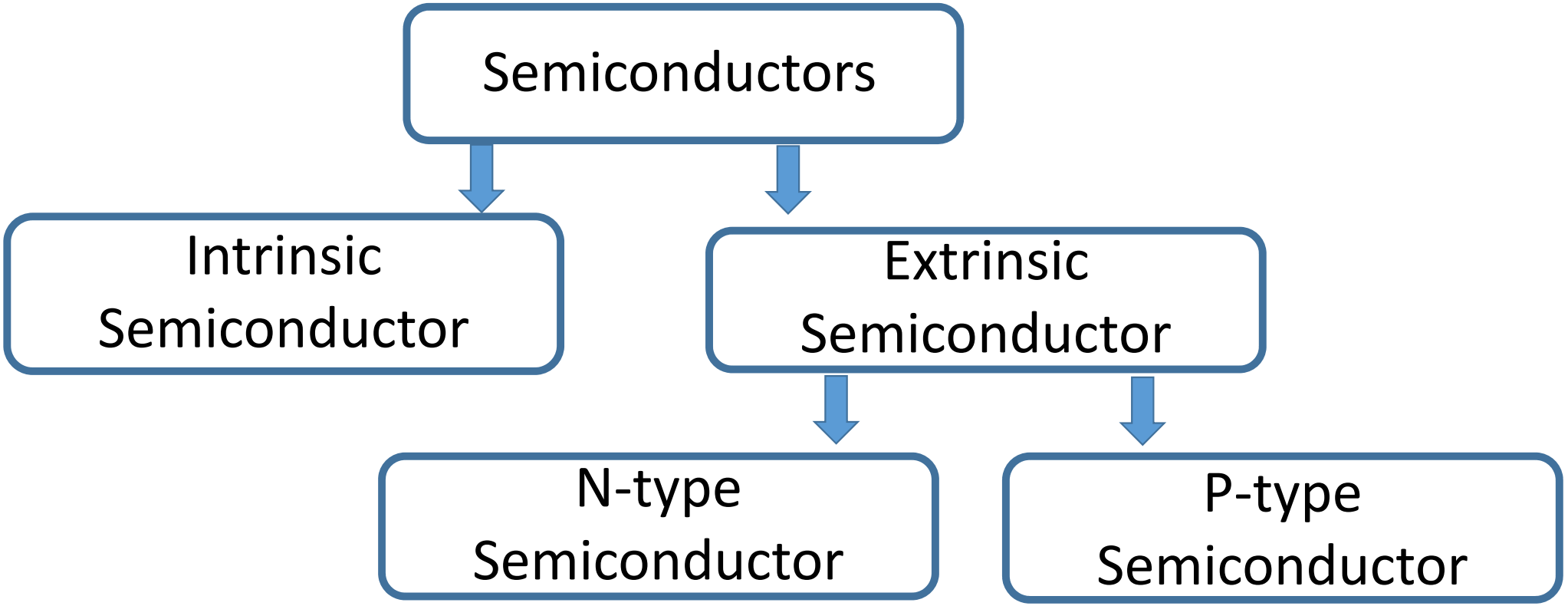
Review of Semiconductors



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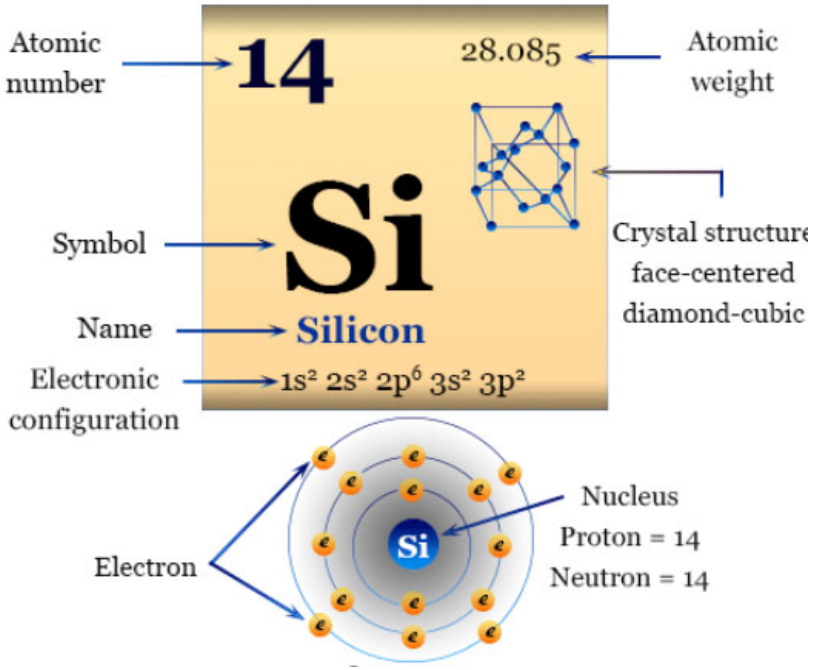
Silicon Material

Silicon: basic information and properties.

Atomic Weight	28.09
Crystal structure	Diamond
Lattice constant (Angstrom)	5.43095
Density: atoms/cm^3	4.995E+22
Energy gap (eV) at 300K	1.12
Melting point (C)	1415



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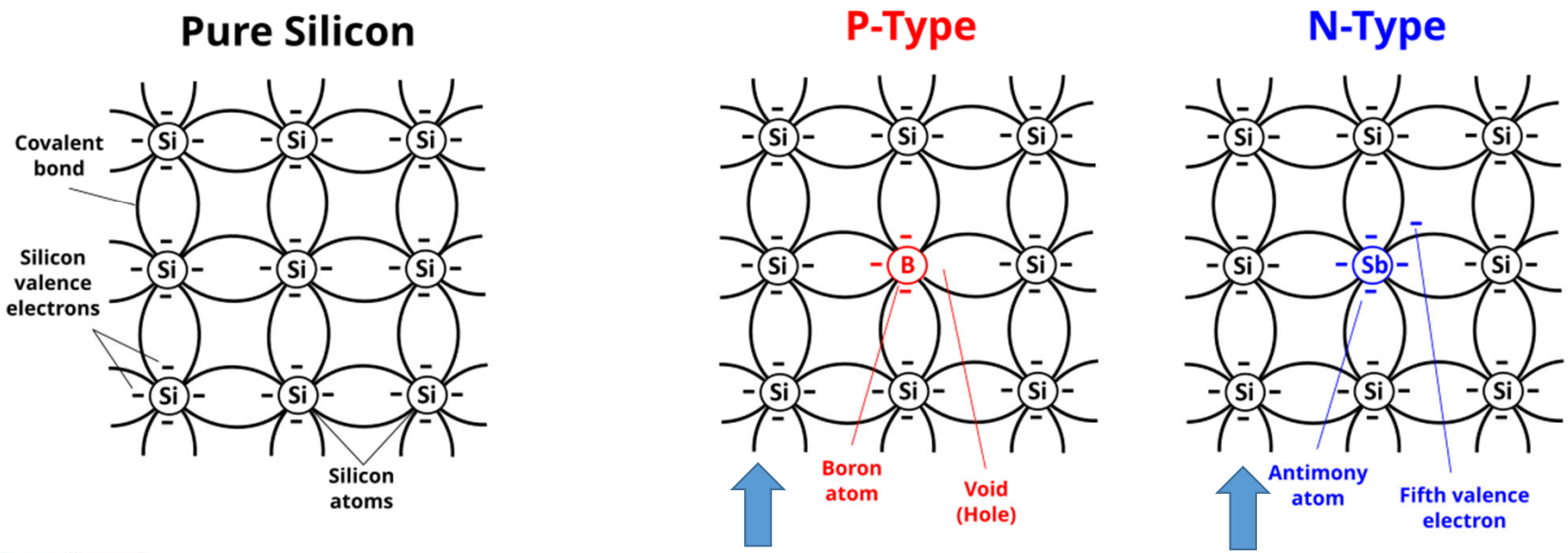
Doped Silicon

Ion Implantation and diffusion process (these topics will be studied in detail later)

Intrinsic (Undoped)

Extrinsic (Doped)



Boron (B), Indium (In), Gallium (Ga)

Phosphorus (P), Arsenic (As), Antimony (Sb)

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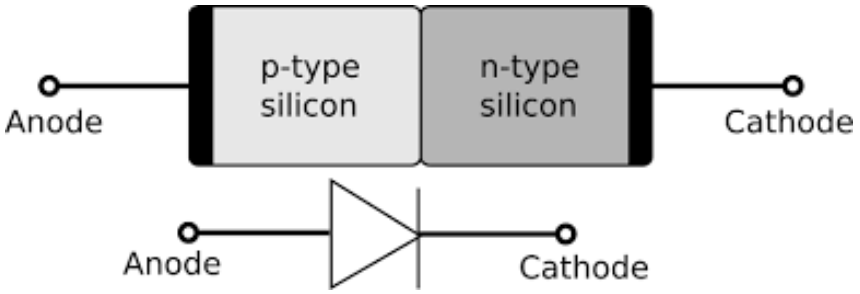
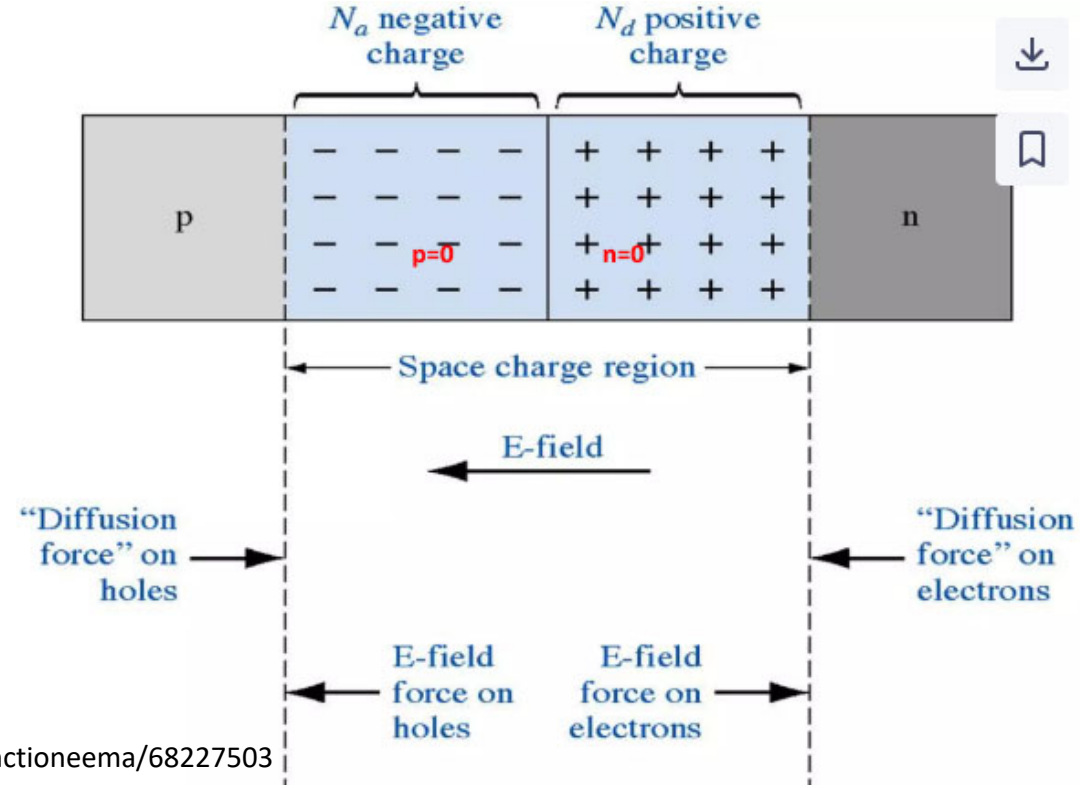
P-N Junction (Diode)

A p-n junction diode is a basic semiconductor device that controls the flow of electric current in a circuit. It has a positive (p) side and a negative (n) side created by adding impurities to each side of a silicon semiconductor.





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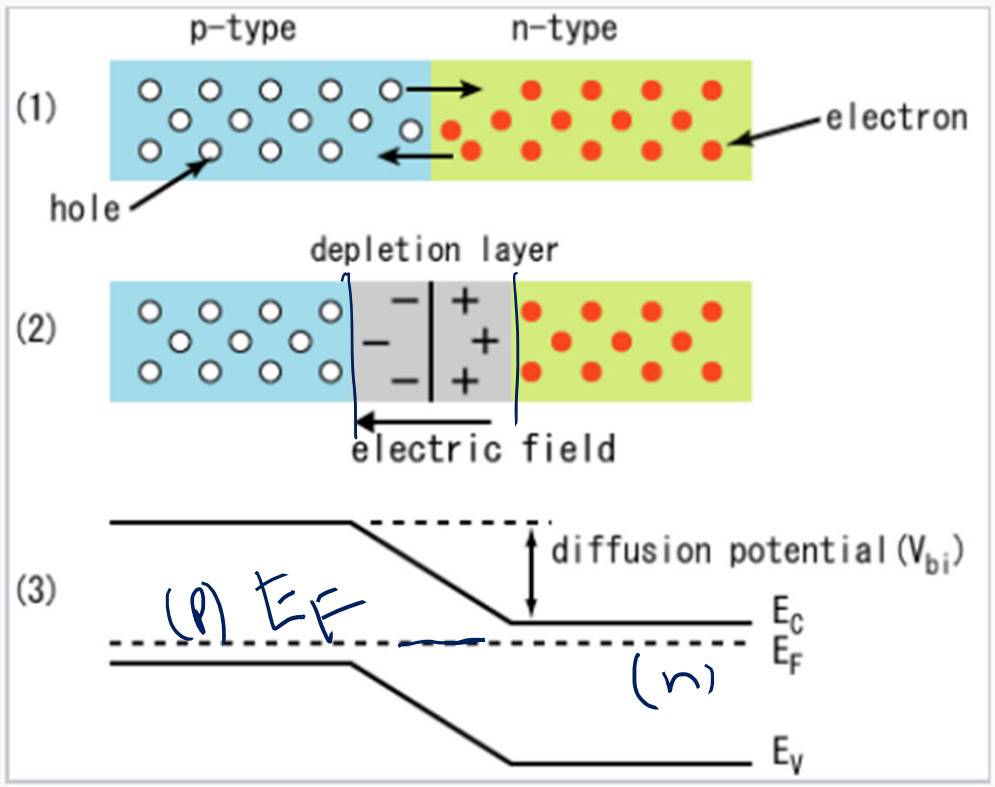
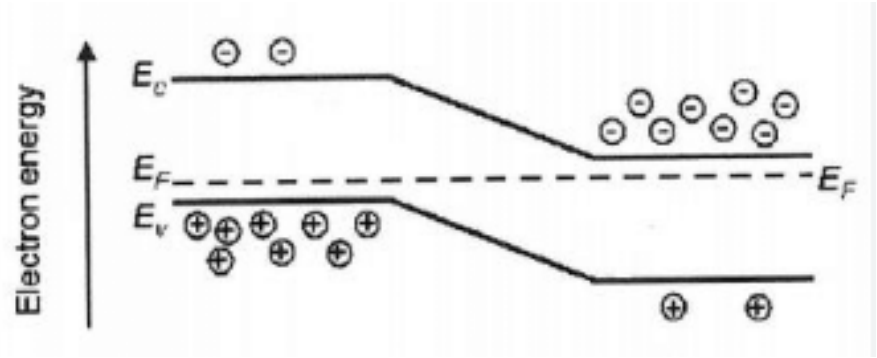
https://www.slideshare.net/slideshow/p-n-junctioneema/68227503

P-N Junction (Diode)-Built in potential



The built-in potential of a P-N junction is the potential difference that develops at the intersection of its p-type semiconductor material and n-type semiconductor material. This built-in potential develops in the depletion region.



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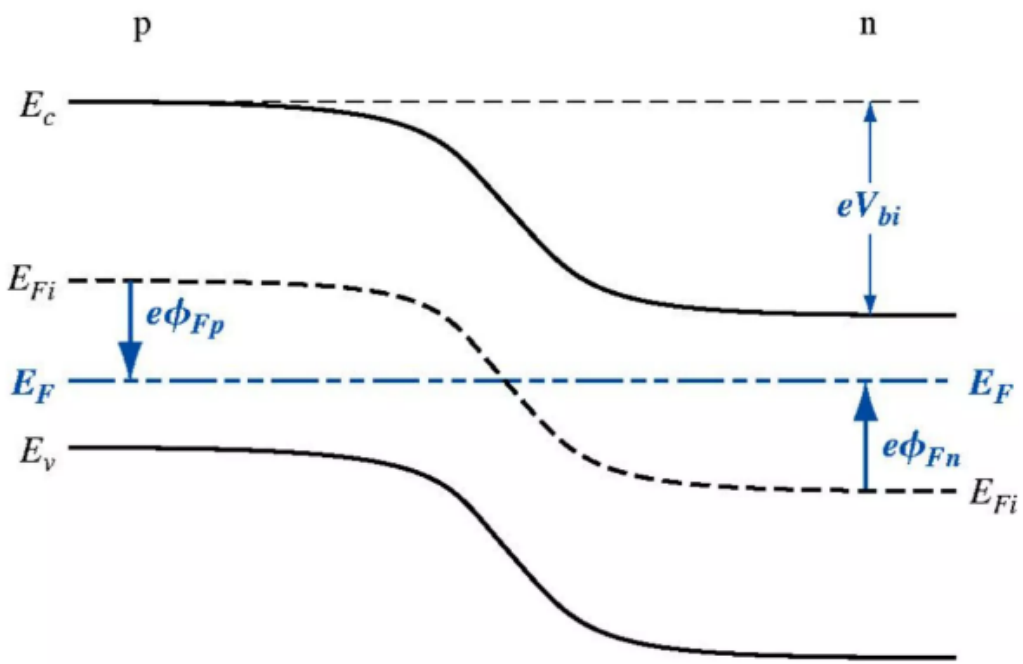
P-N Junction (Diode)-Built in potential



$$\phi_{bi} = \frac{kT}{q} \ln \frac{N_d N_a}{n_i^2}$$

The built-in potential of a P-N junction is the potential difference that develops at the intersection of its p-type semiconductor material and n-type semiconductor material. This built-in potential develops in the depletion region.

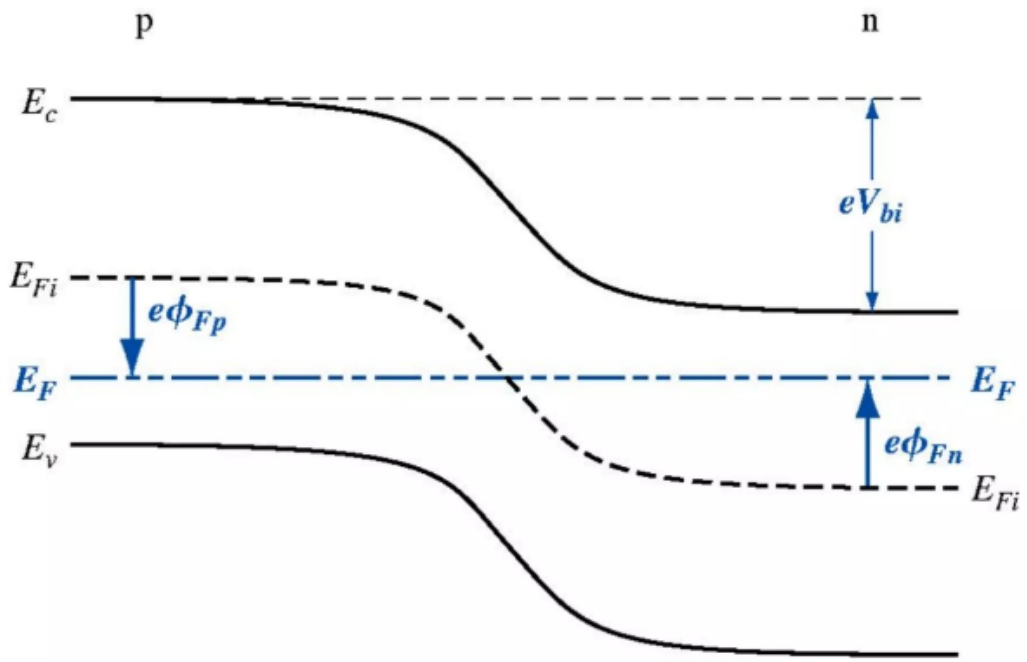
Formula

PN Junction Built-in Potential

$$V_{built\text{-}in} = \frac{kT}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

$V_{built\text{-}in}$	→	Built-in potential in volts
N_D	→	n type - donor atoms concentration
N_A	→	p type - acceptor atoms concentration
n	→	concentration of electrons
kT/q	→	thermal voltage
T	→	temperature in Kelvin
q	→	charges in coulombs

P-N Junction (Diode)-Built in potential



$$\phi_{Fn} = \frac{-kT}{e} \ln\left(\frac{N_d}{n_i}\right)$$

$$\phi_{Fp} = +\frac{kT}{e} \ln\left(\frac{N_a}{n_i}\right)$$

$$V_{bi} = \frac{kT}{e} \ln\left(\frac{N_a N_d}{n_i^2}\right)$$

$$W_{\text{dep}} = \sqrt{\frac{2\varepsilon_s \phi_{\text{bi}}}{q}\left(\frac{1}{N_{\text{a}}} + \frac{1}{N_{\text{d}}}\right)}$$

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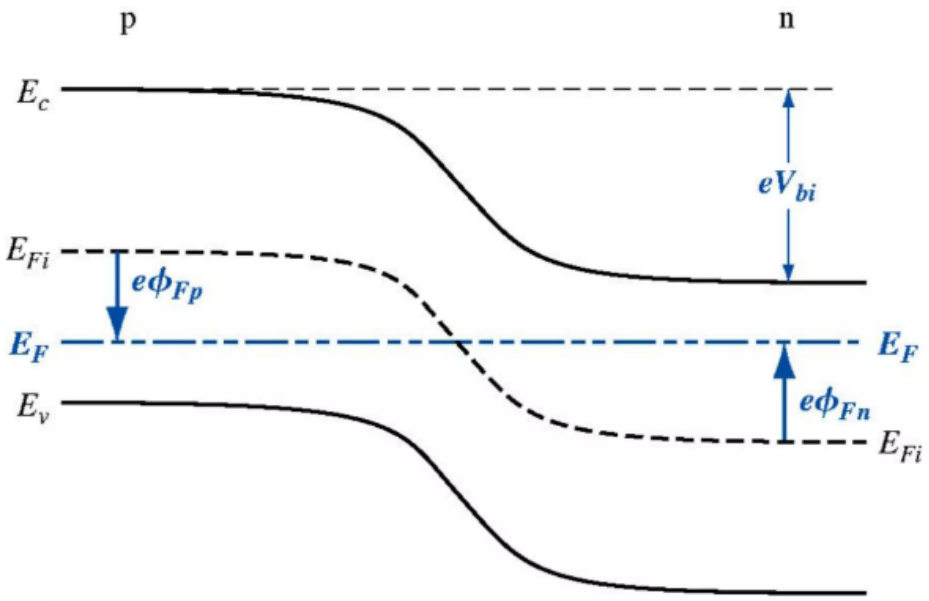
P-N Junction (Diode)-Built in potential



$$W_{\text{dep}} = \sqrt{\frac{2\varepsilon_s \phi_{\text{bi}}}{q}\left(\frac{1}{N_{\text{a}}} + \frac{1}{N_{\text{d}}}\right)}$$

If $N_{\text{a}} >> N_{\text{d}}$, as in a P^+N junction,

$$W_{\text{dep}} \approx \sqrt{\frac{2\varepsilon_s \phi_{\text{bi}}}{qN_{\text{d}}}} \approx |x_{\text{N}}|$$

If $N_{\text{d}} >> N_{\text{a}}$, as in an N^+P junction,

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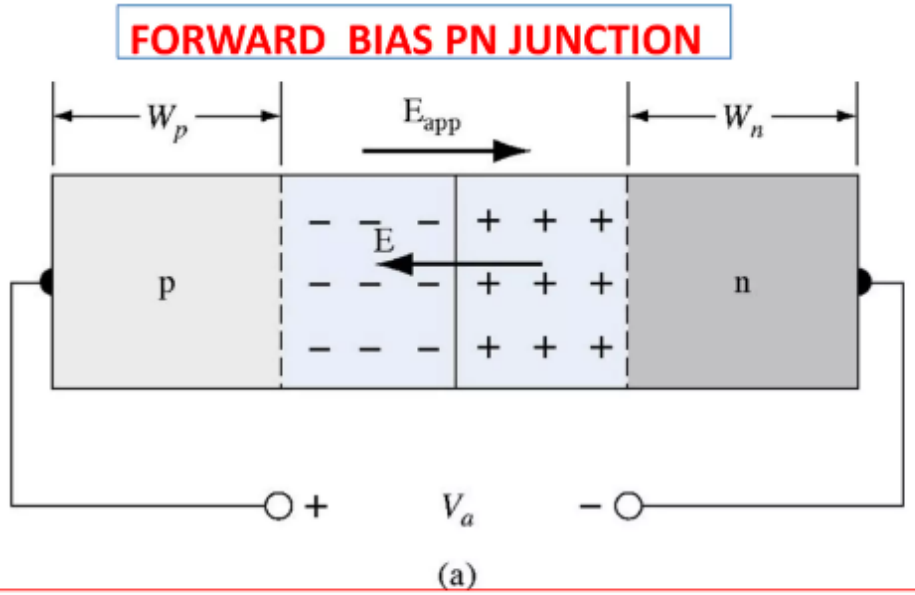
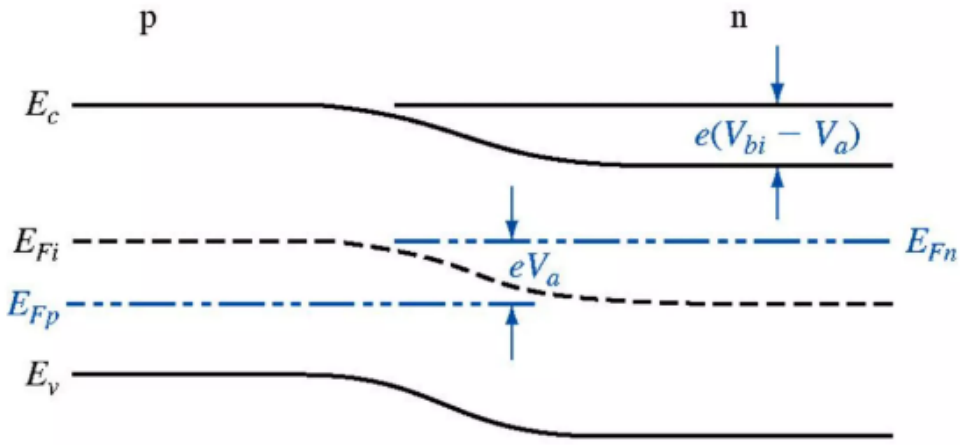
P-N Junction (Diode)-Forward Bias

When positive terminal of the source is connected to the P side and the negative terminal is connected to N side then the junction diode is said to be connected in forward bias condition.





- Injection of holes into the n region means these holes are minority carriers there.
- Injection of electrons into the p-region means these electrons are minority carriers there.
- The behavior of these minority carriers is described by the ambipolar transport equations.

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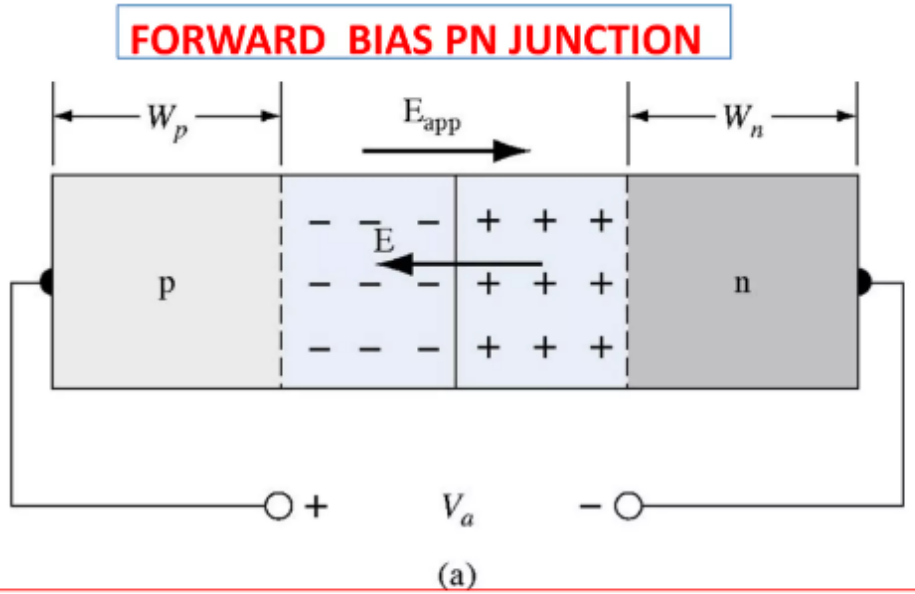

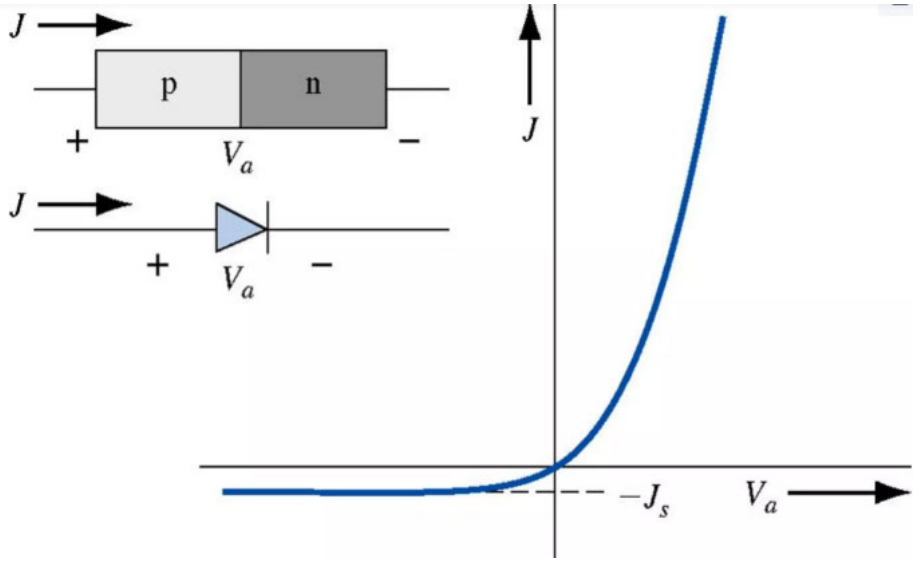

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$$J \simeq J_s \left[\exp\left(\frac{eV_a}{kT}\right) - 1 \right]$$

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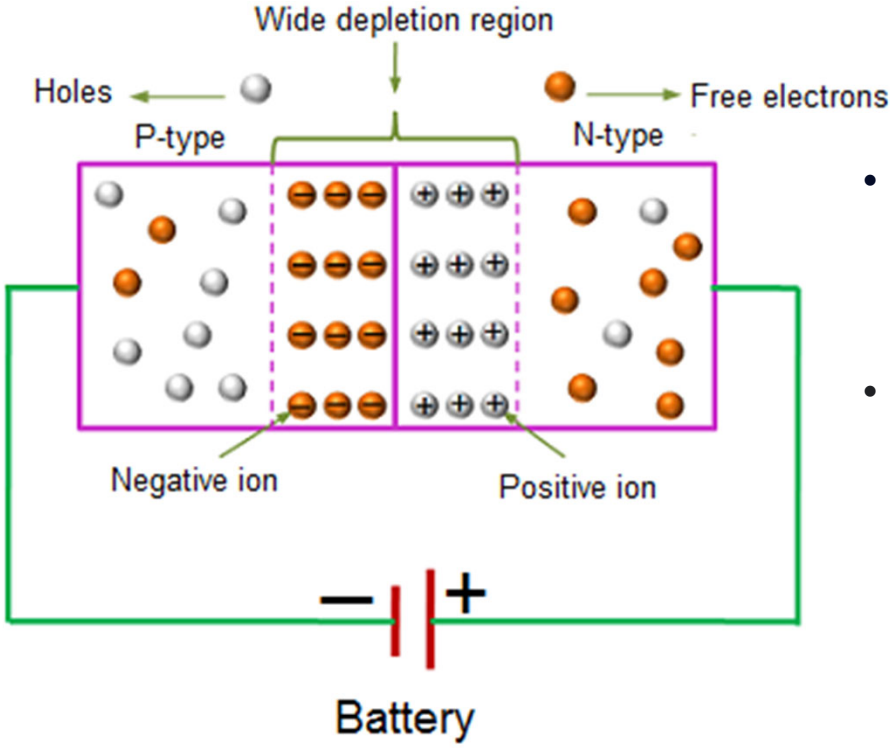
P-N Junction (Diode)-Reverse Bias



- Positive terminal attracts the electrons away from the junction in N side and negative terminal attracts the holes away from the junction in P side.
- As a result of it, the width of the potential barrier increases that impedes the flow of majority carriers in N side and P side.

https://www.physics-and-radio-electronics.com/electronic-devices-and-circuits/semiconductor-diodes/reversebiaseddiode.html

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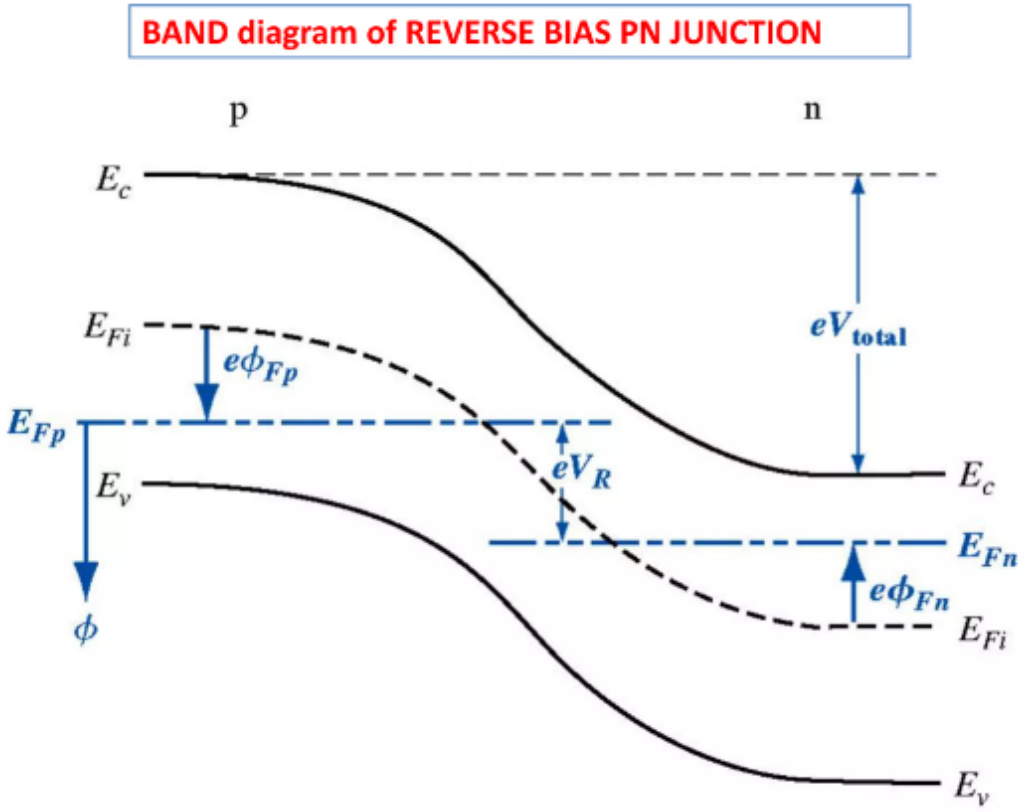
P-N Junction (Diode)-Reverse Bias



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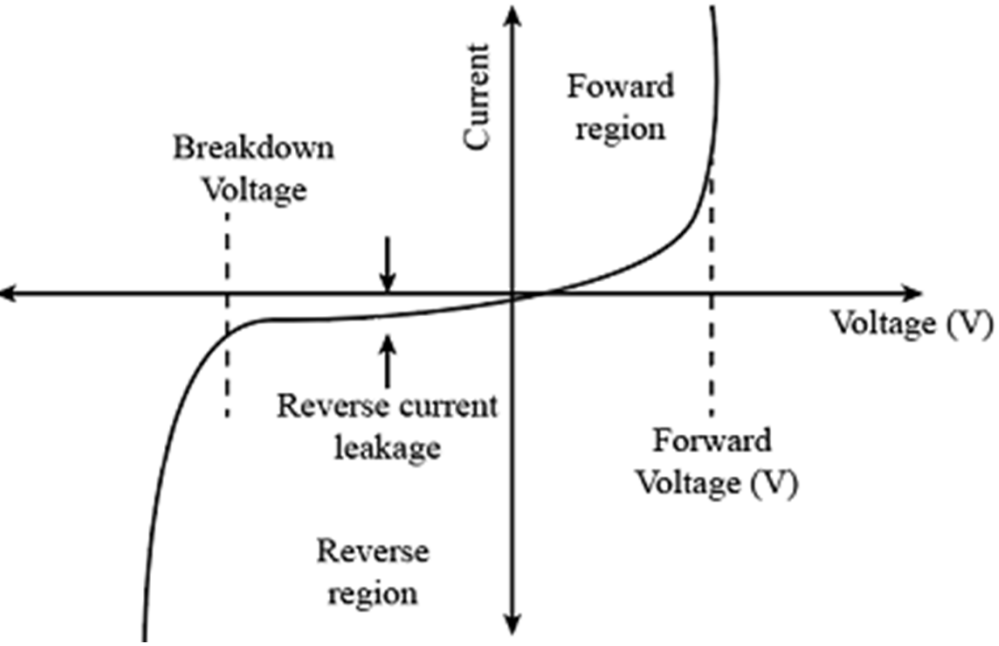
P-N Junction (Diode)-Reverse Bias



Breakdown occurs by two mechanisms.

- **Avalanche Breakdown**
  Energetic carriers ionize host atoms and there is carrier multiplication leading to breakdown.

- **Zener Breakdown**
  Electrons from p-region can tunnel to the conduction band in the n-region causing breakdown.

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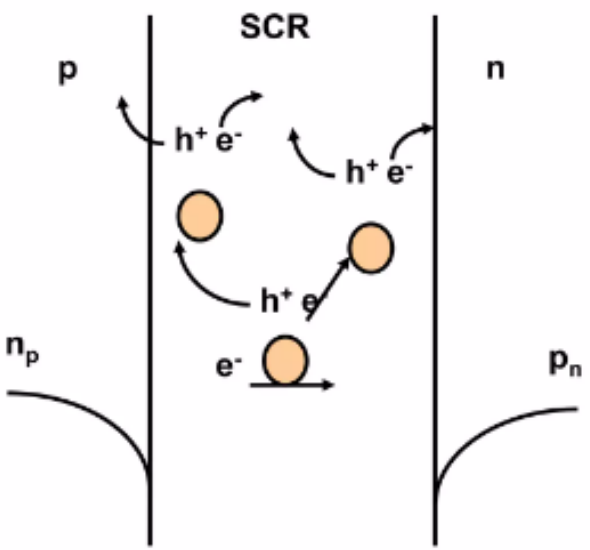
P-N Junction (Diode)-Reverse Bias

Avalanche Breakdown : in high electric field

- Electrons or holes traveling inside the SCR attain high velocity when reverse bias is high and collide with atoms dislodging an electron from the atom and causing an electron-hole pair to form, the process continues.
- This is known as **Avalanche multiplication,** resulting in a large reverse bias current leading to breakdown



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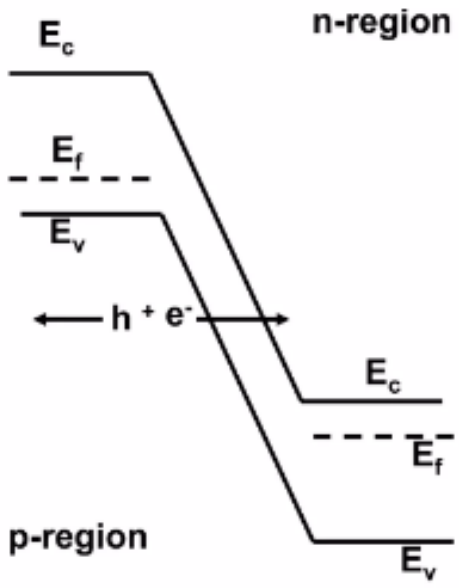
P-N Junction (Diode)-Reverse Bias

Zener Breakdown : Heavily doped junction

- the valence band edge of p-region will be at a higher potential than the conduction band edge of the n-region. Due to heavy doping depletion layer will be thin.
- Breakdown occurs due to electron tunneling between the valence band of the p-region and conduction band of the n-region. A large reverse current flows. This is known as **Zener Breakdown.**



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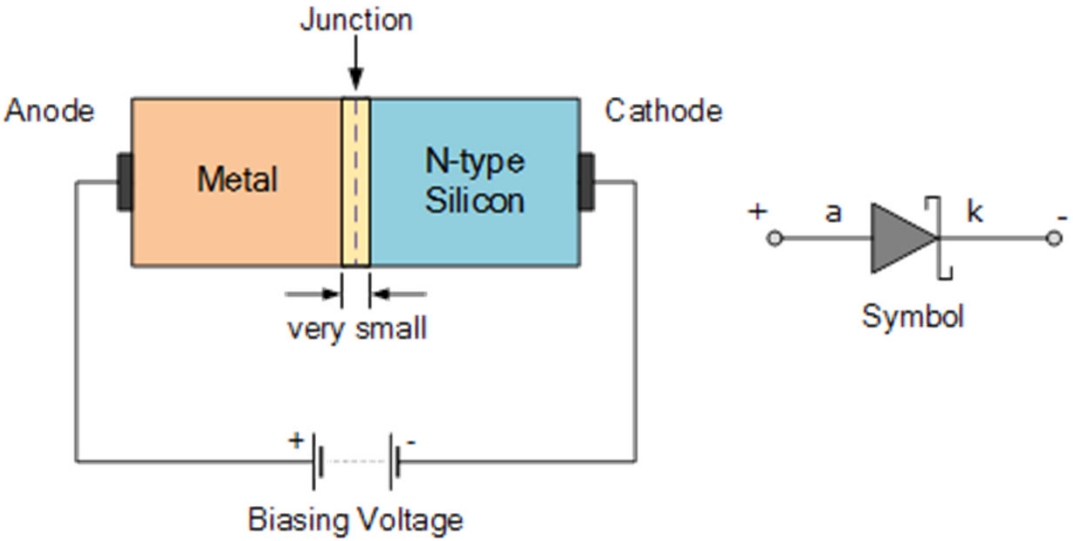
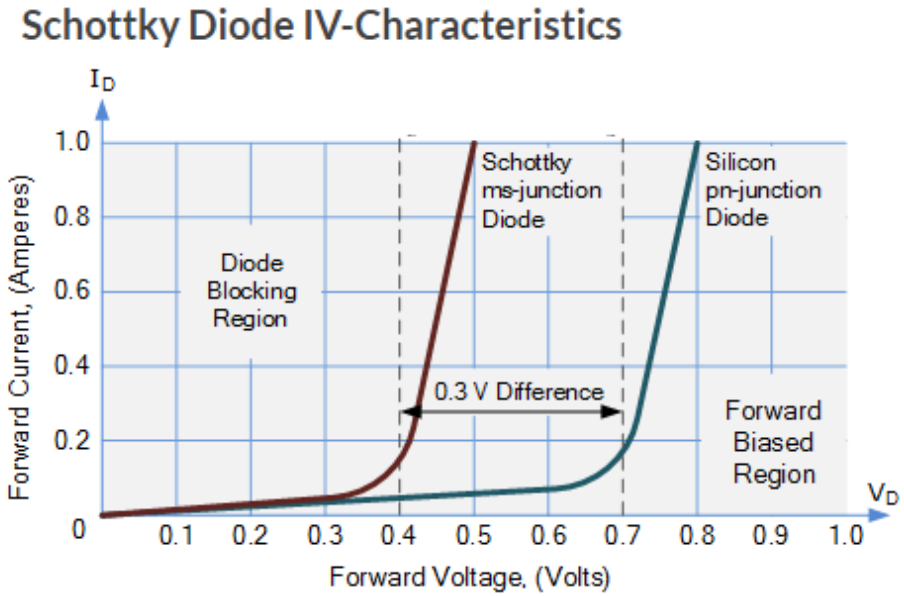
Schottky Diode-Metal-Semiconductor Junction

- The Schottky diode is a semiconductor diode formed by the junction of a semiconductor with a metal.
- It has a low forward voltage drop and a very fast switching action.
- The most common contact metal used for Schottky diode construction is “Silicide” which is a highly conductive silicon and metal compound.





https://www.electronics-tutorials.ws/diode/schottky-diode.html

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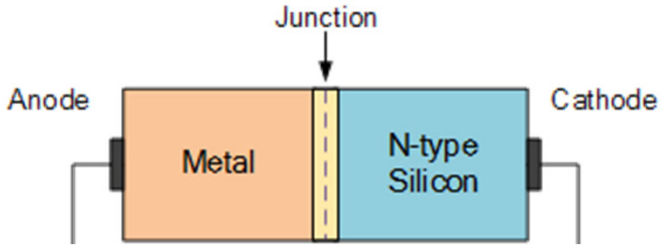
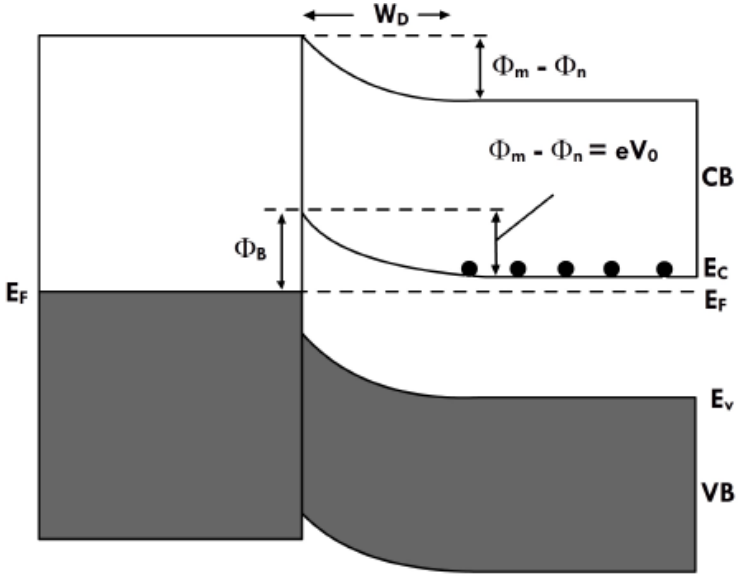
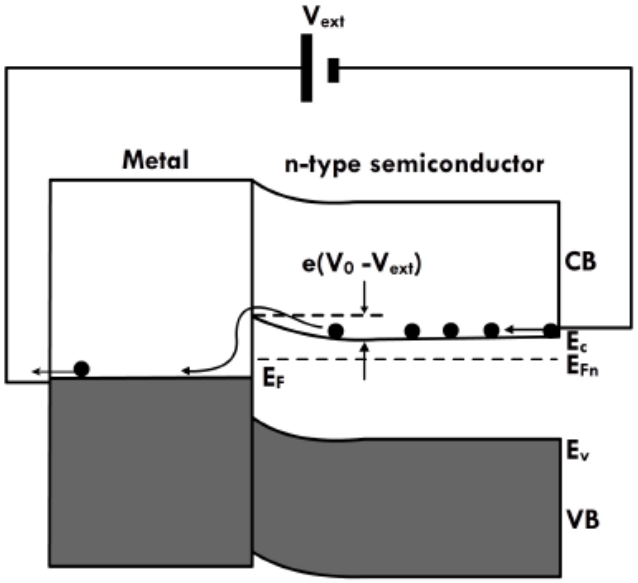
Schottky Diode-Metal-Semiconductor Junction





Equilibrium condition



Forward Bias

https://www.electronics-tutorials.ws/diode/schottky-diode.html

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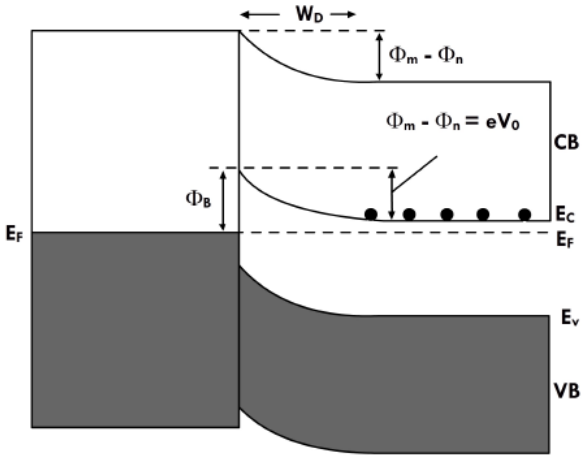
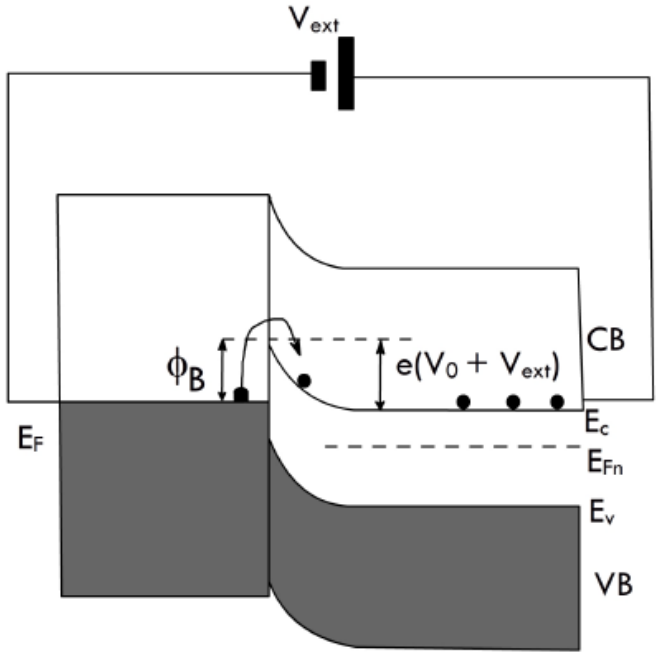
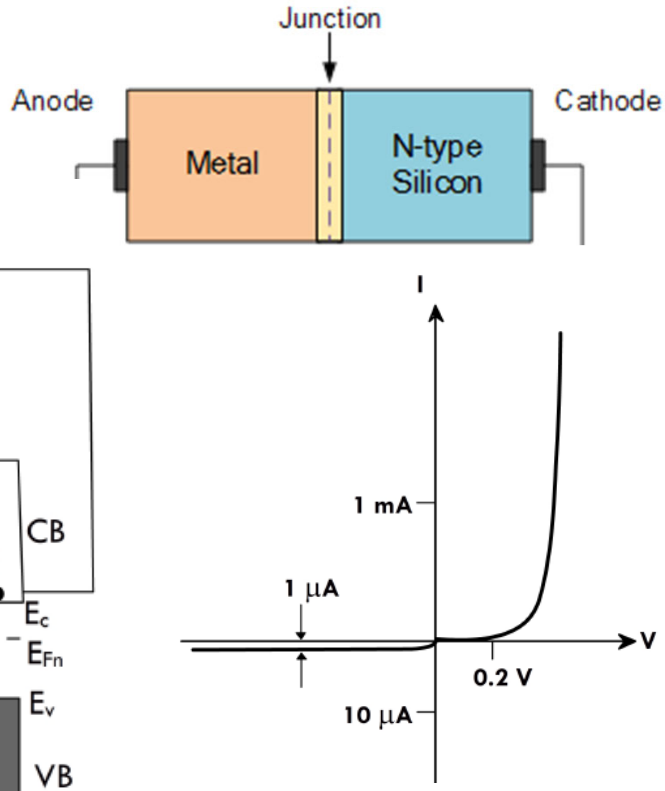
Schottky Diode-Metal-Semiconductor Junction



Equilibrium condition



Reverse Bias



https://www.electronics-tutorials.ws/diode/schottky-diode.html

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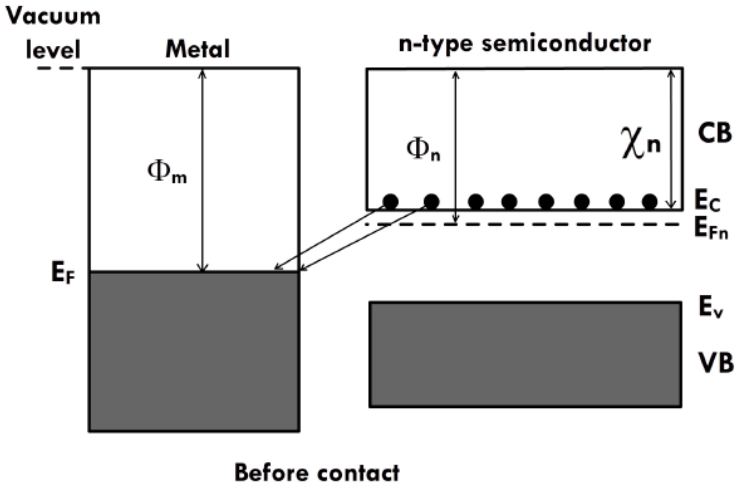
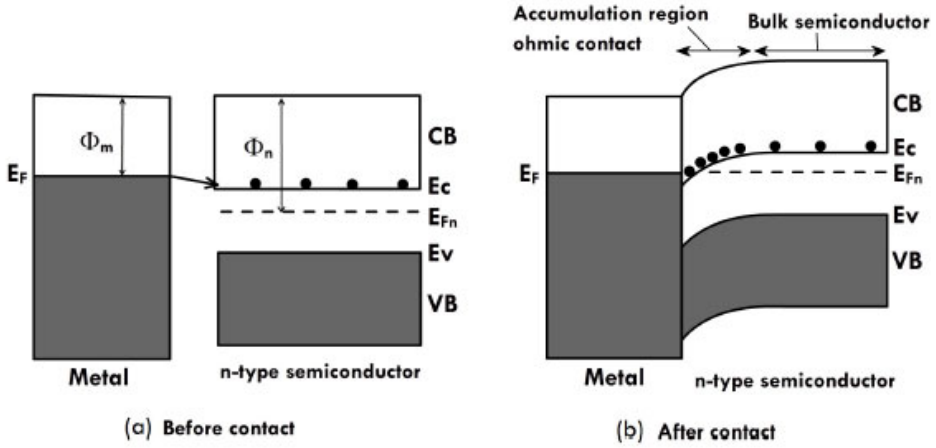
Schottky contact and Ohmic Contact

- A Schottky junction is formed when the semiconductor has a lower work function than the metal. When the semiconductor has a higher work function the junction formed is called the Ohmic junction.

- Ohmic junction behaves as a resistor conducting in both forward and reverse bias. The resistivity is determined by the bulk resistivity of the semiconductor.



Schottky contact



Ohmic Contact

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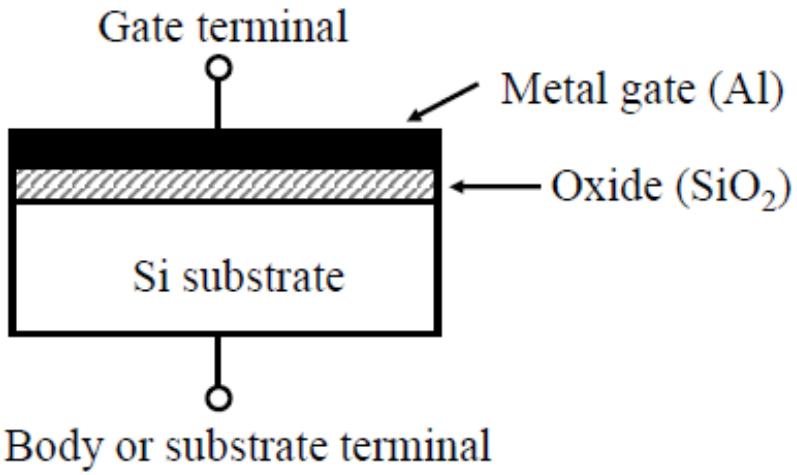
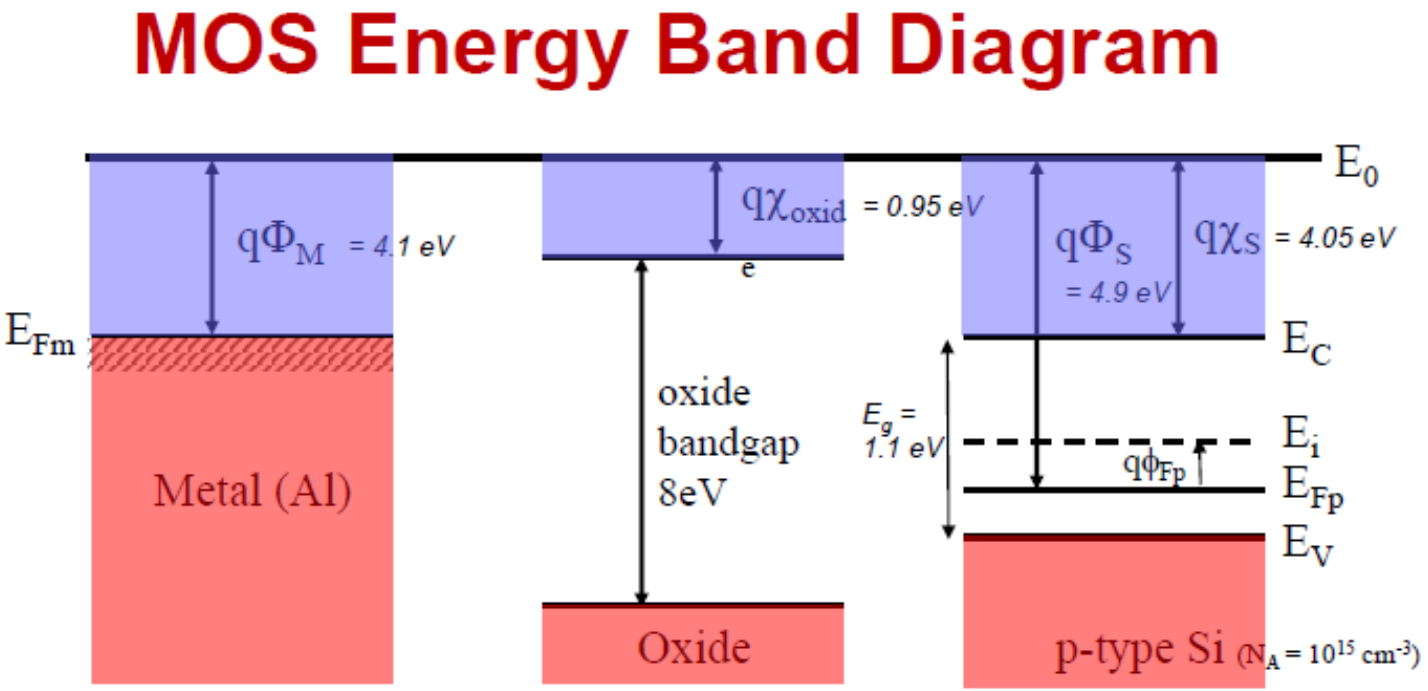
MOS Capacitors

- MOS: Metal-oxide-semiconductor
  - Gate: metal (or polysilicon)
  - Oxide: silicon dioxide, grown on substrate
- MOS capacitor: two-terminal MOS structure



MOS Capacitors



- Work function ($q\Phi_M$, $q\Phi_S$): energy required to take electron from Fermi level to free space
- Work function difference between Al and Si = 0.8V

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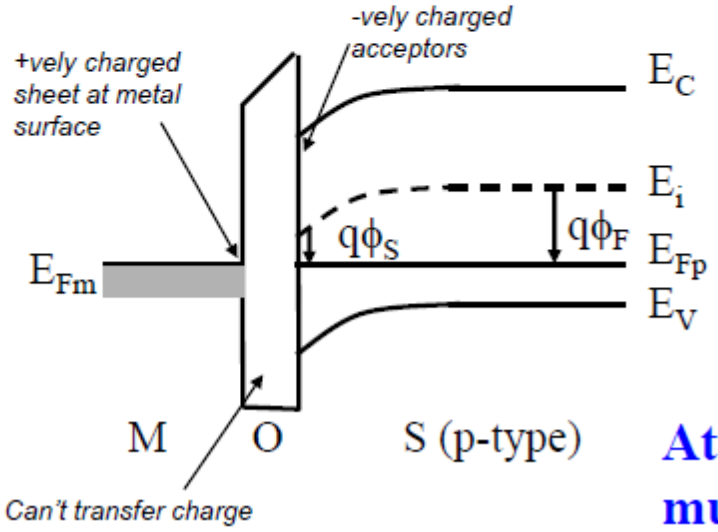
MOS Capacitors- Energy band diagram

- Bands must bend for Fermi levels to line up
- Amount of bending is equal to work function difference: $q\Phi_M - q\Phi_S$
- Fermi levels equalized by transfer of –ve charge from materials with higher E_F (smaller work functions) across interfaces to materials with lower E_F
- **Part of voltage drop occurs across oxide, rest occurs next to O-S interface**



ϕ_F = Fermi potential (difference between E_F and E_i in bulk)

ϕ_S = surface potential

At equilibrium, Fermi levels must line up!!

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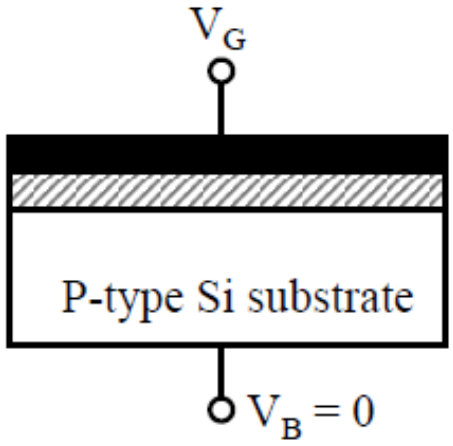
MOS Capacitors- Operation

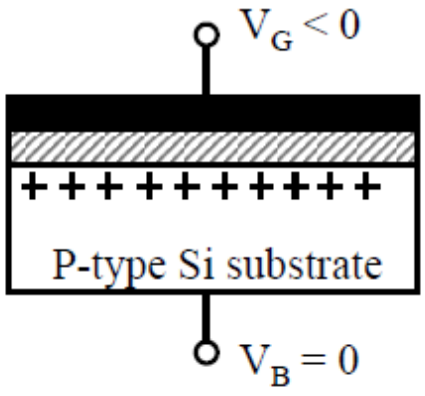
- Assume p-type substrate
- Three regions of operation
  - Accumulation ($V_G < 0$)
  - Depletion ($V_G > 0$ but small)
  - Inversion ($V_G >> 0$)

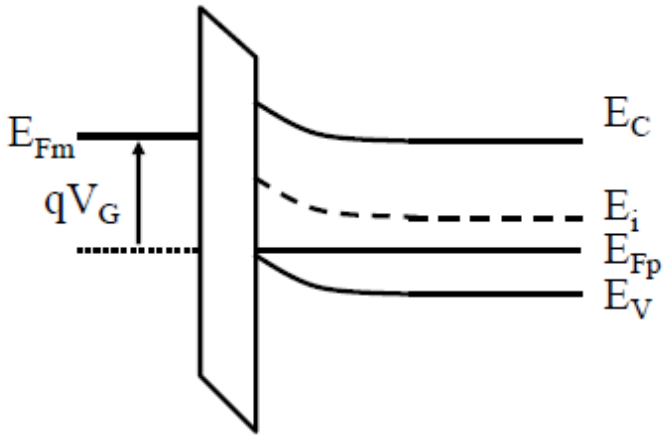


MOS Capacitors- Operation

Accumulation

- Negative voltage on gate: attracts holes in substrate towards oxide
- Holes "accumulate" on Si surface (surface is more strongly p-type)
- Electrons pushed deeper into substrate

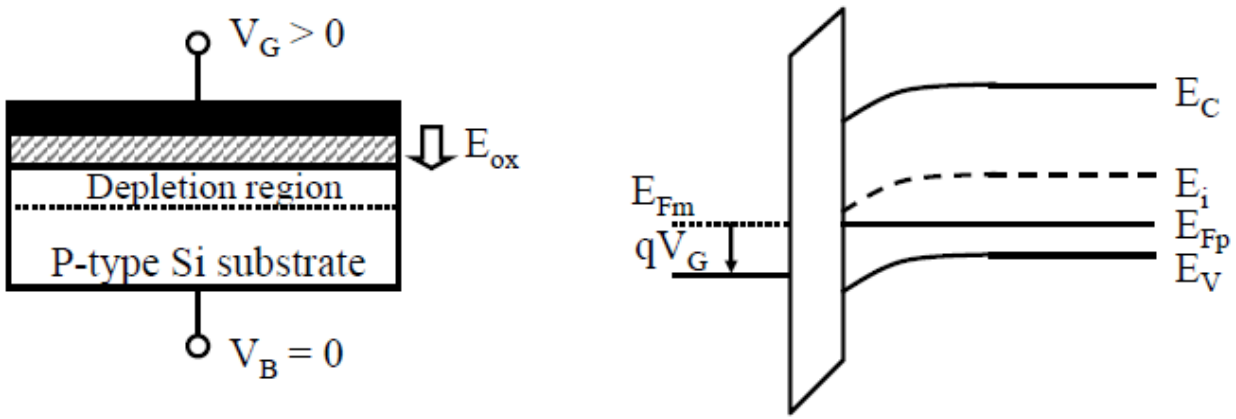




MOS Capacitors- Operation

Depletion

- Positive voltage on gate: repels holes in substrate
  - Holes leave behind negatively charged acceptor ions
- Depletion region forms: devoid of carriers
  - Electric field directed from gate to substrate
- Bands bend downwards near surface
  - Surface becomes <u>less</u> strongly p-type (E_F close to E_i)

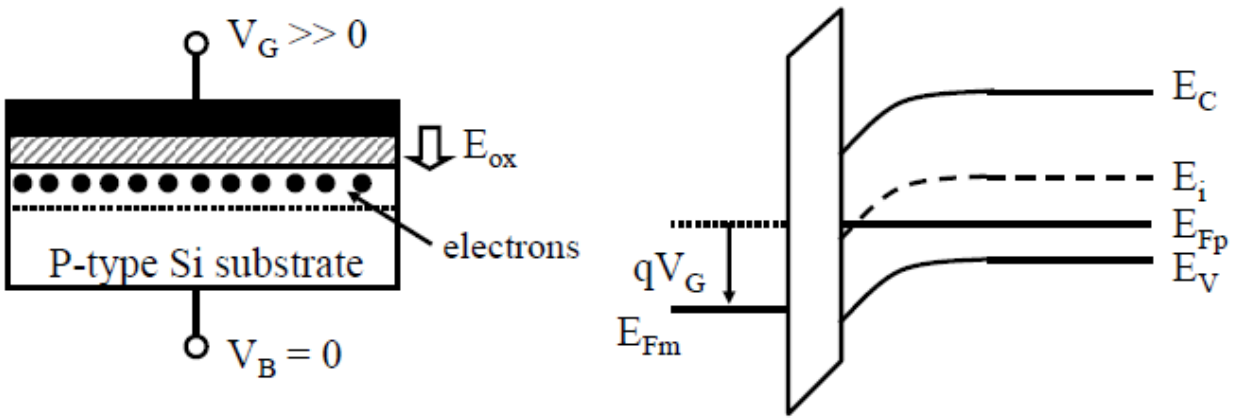


MOS Capacitors- Operation

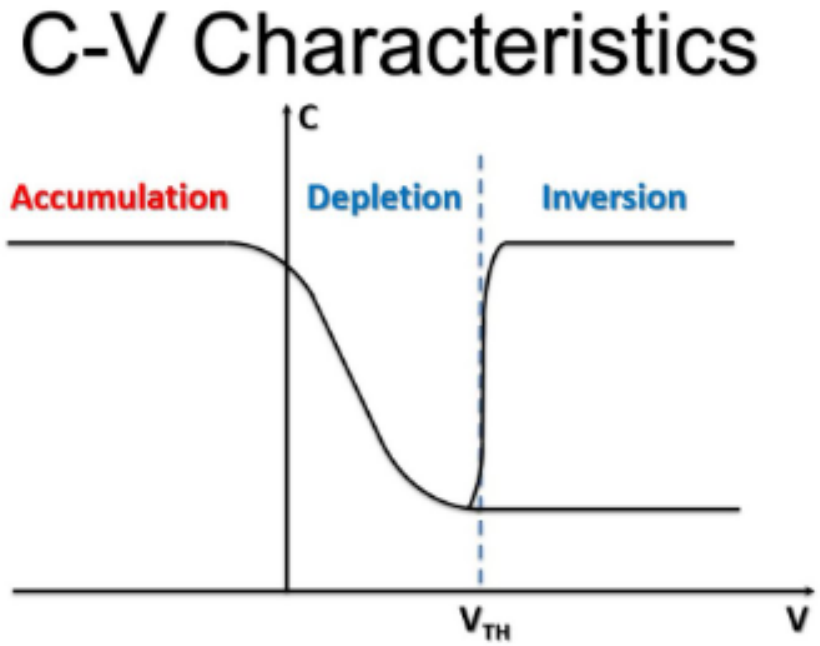
Inversion

$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}}$$

- Increase voltage on gate, bands bend more
- Additional minority carriers (electrons) attracted from substrate to surface
  - Forms "inversion layer" of electrons
- Surface becomes n-type



MOS Capacitors- C-V Characteristics



$$C_{dep} = \frac{\varepsilon_s}{W_{dep}}$$

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

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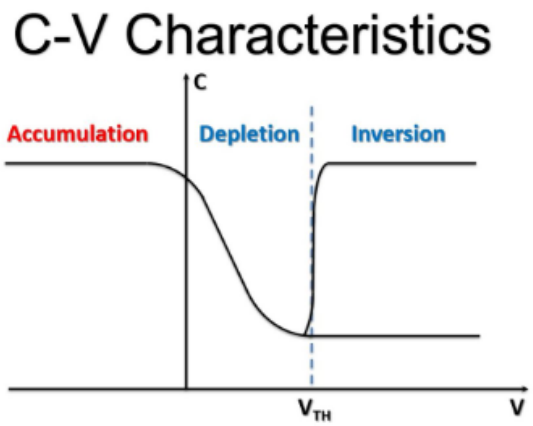
MOS Capacitors- C-V Characteristics



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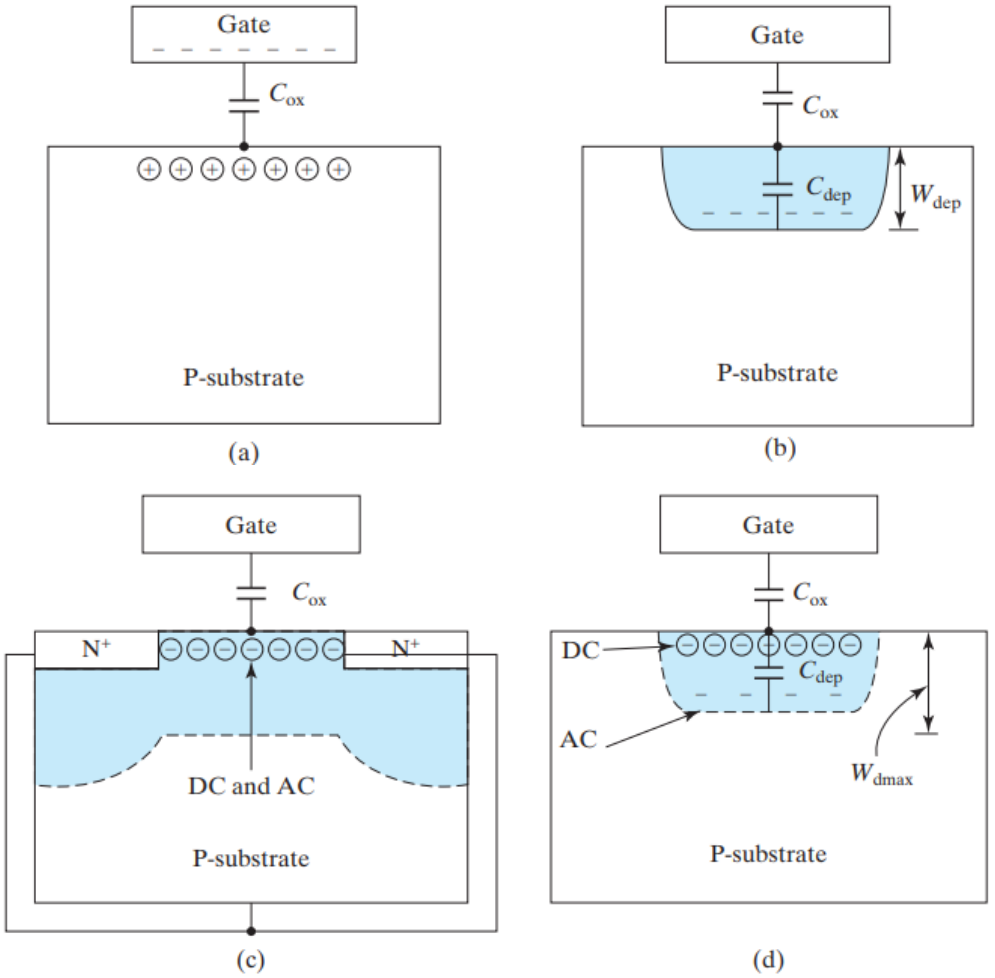

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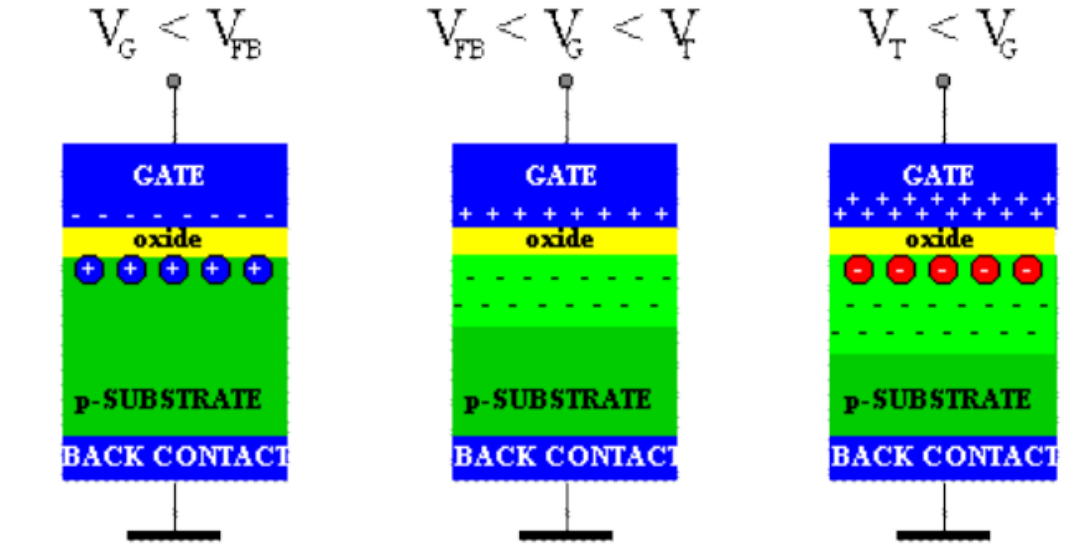
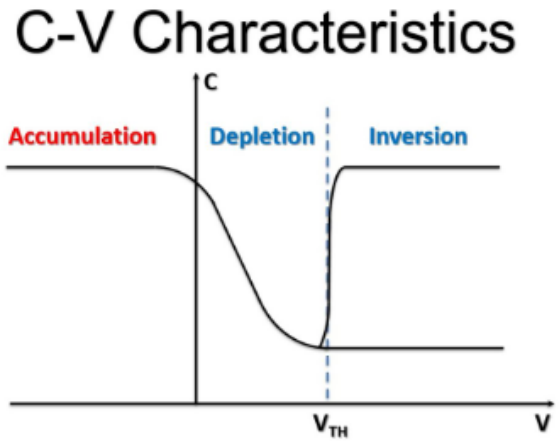
MOS Capacitors- C-V Characteristics





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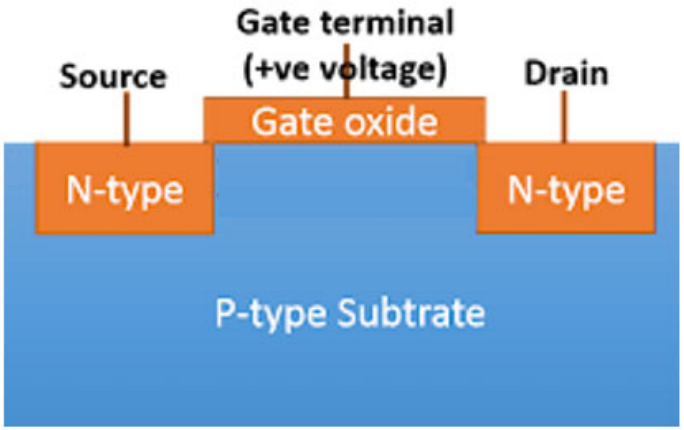
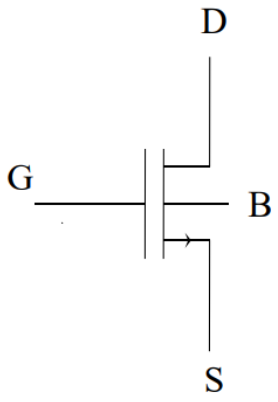
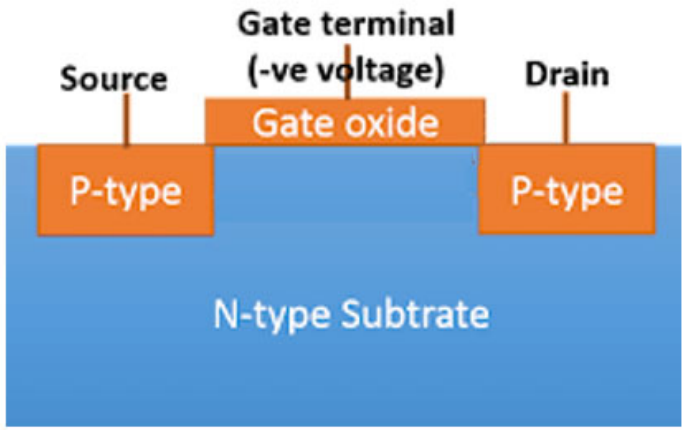
Review of MOSFETs

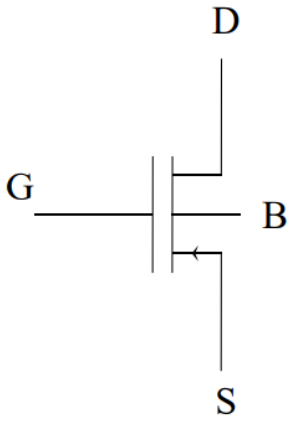


n-channel MOS
Transistor





p-channel MOS
Transistor



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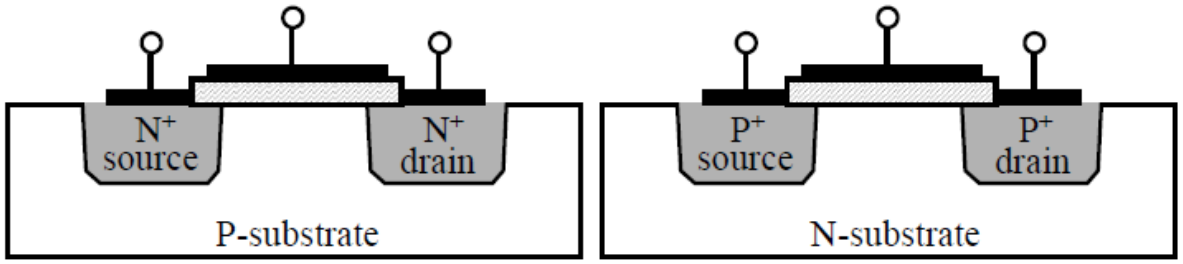
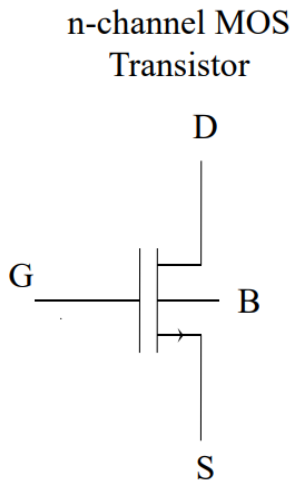
Review of MOSFETs

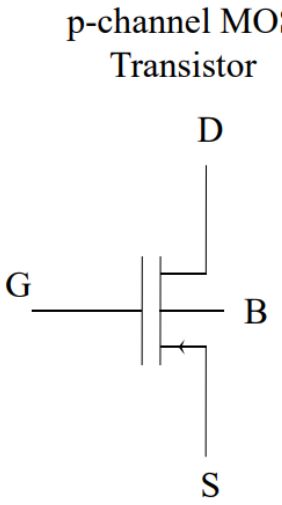
MOS Transistor

- Add "source" and "drain" terminals to MOS capacitor
- Transistor types
  - NMOS: p-type substrate, n^+ source/drain
  - PMOS: n-type substrate, p^+ source/drain



NMOS PMOS





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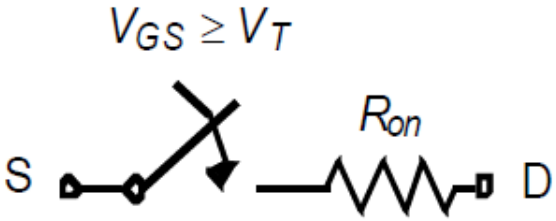
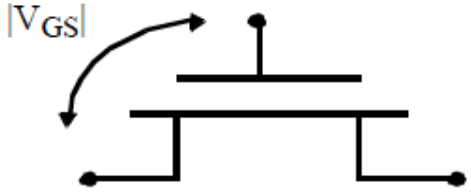
Review of MOSFETs

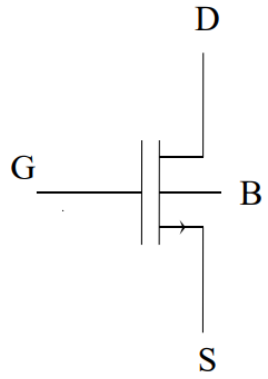
What is a Transistor?

A Switch! ⟷ An MOS Transistor

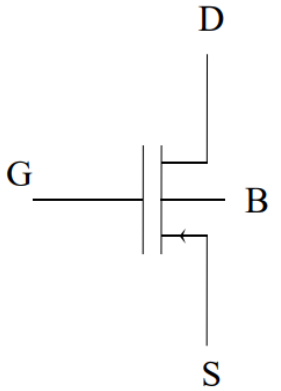




n-channel MOS Transistor



p-channel MOS Transistor



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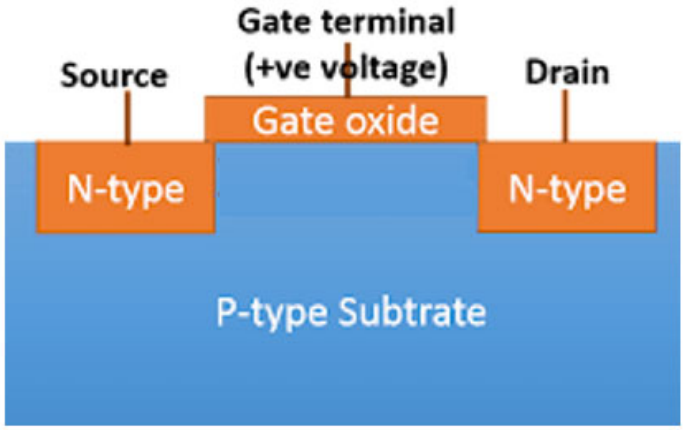
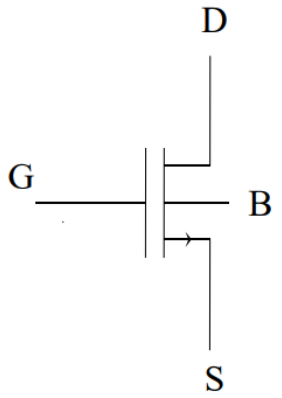
Review of MOSFETs



$$\beta = \mu C_{ox} \frac{W}{L}$$

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

n-channel MOS Transistor



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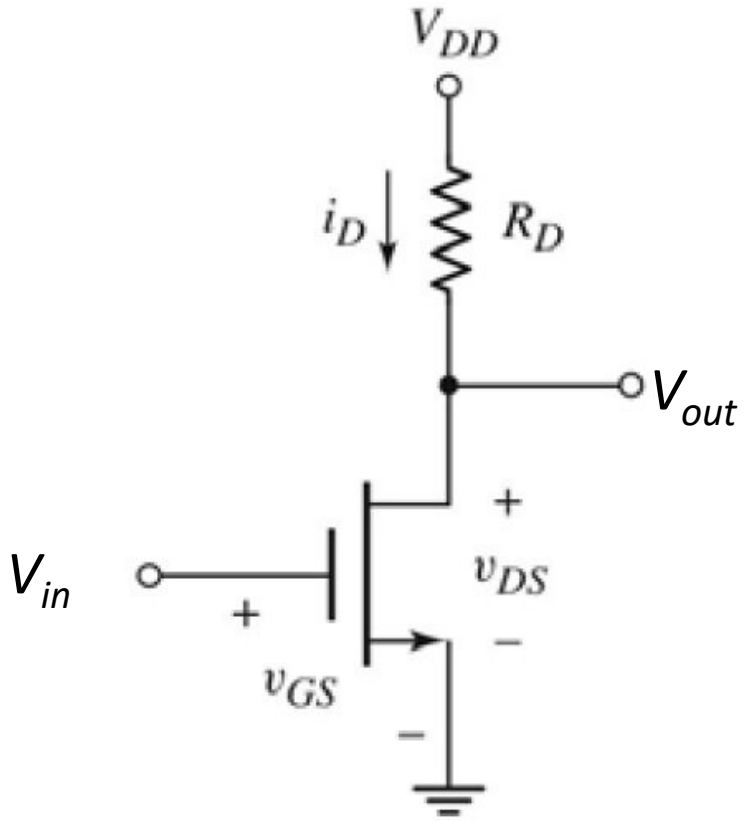
Review of MOSFETs: DC load line of n-MOSFET



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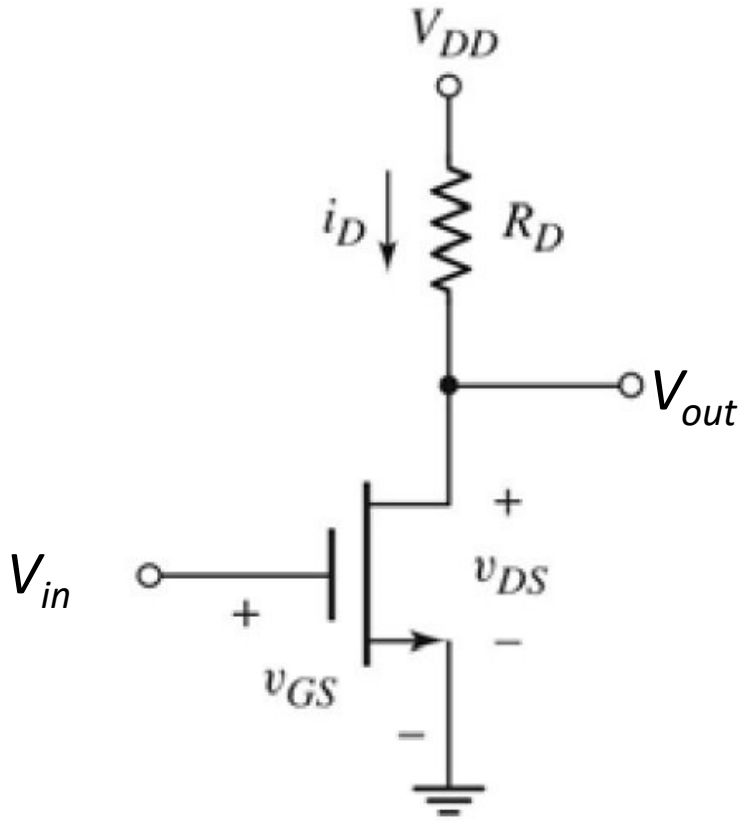

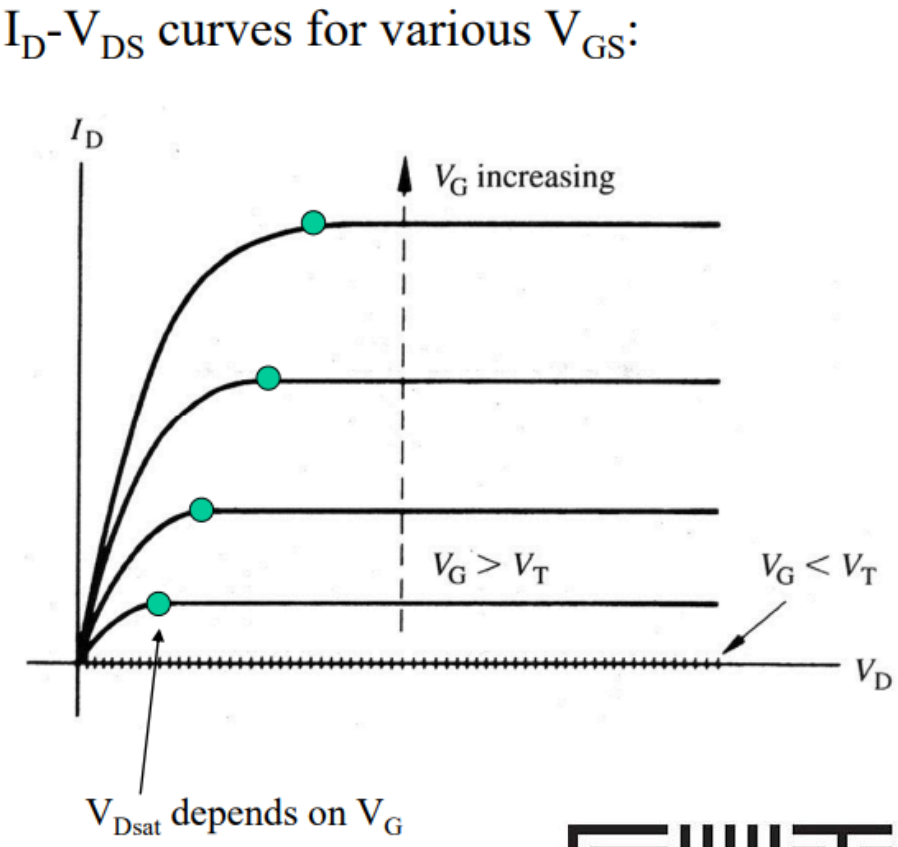

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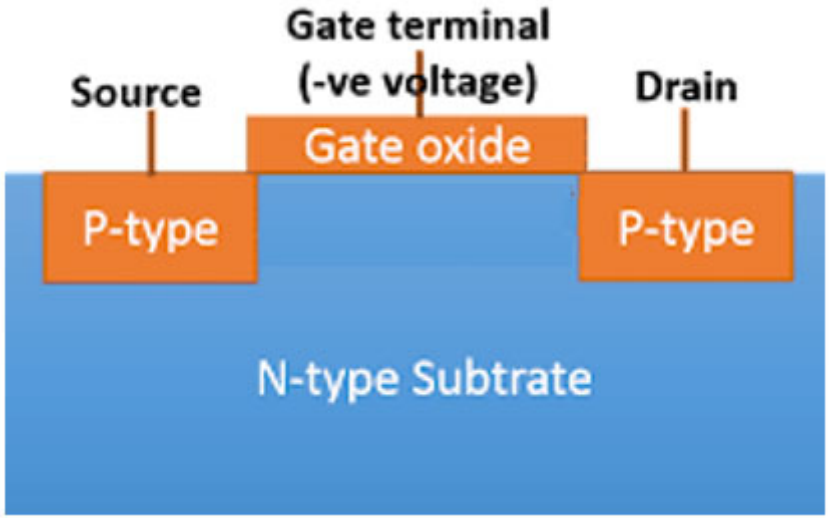
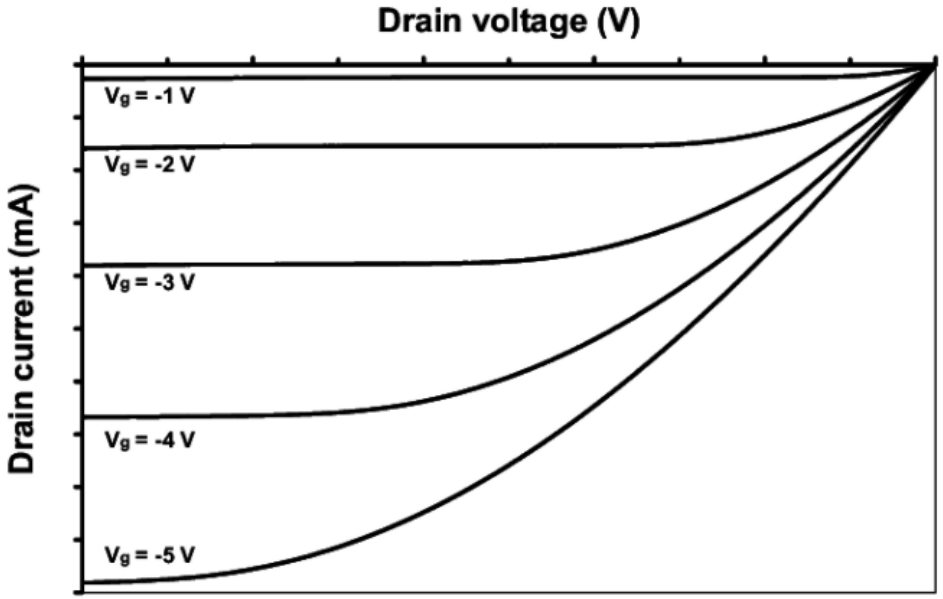
Review of MOSFETs

p-MOSFET





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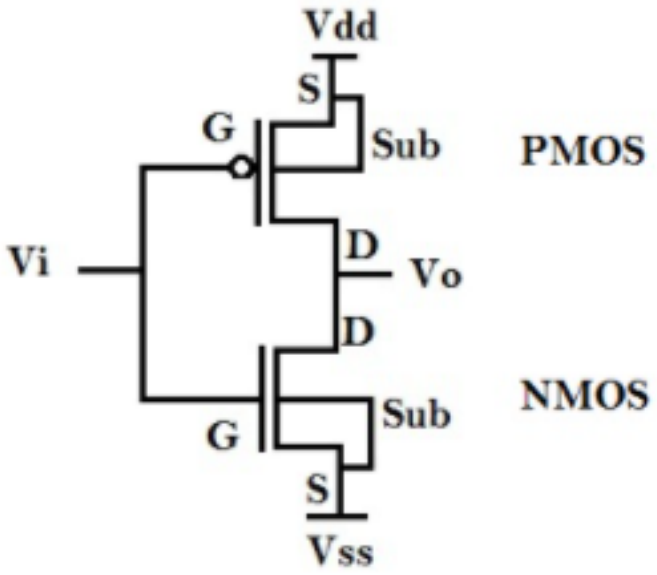
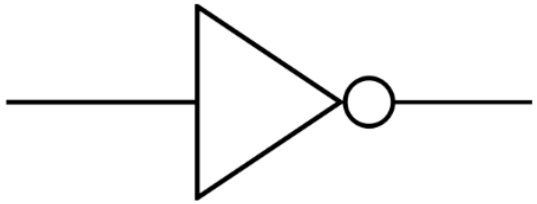
CMOS circuit





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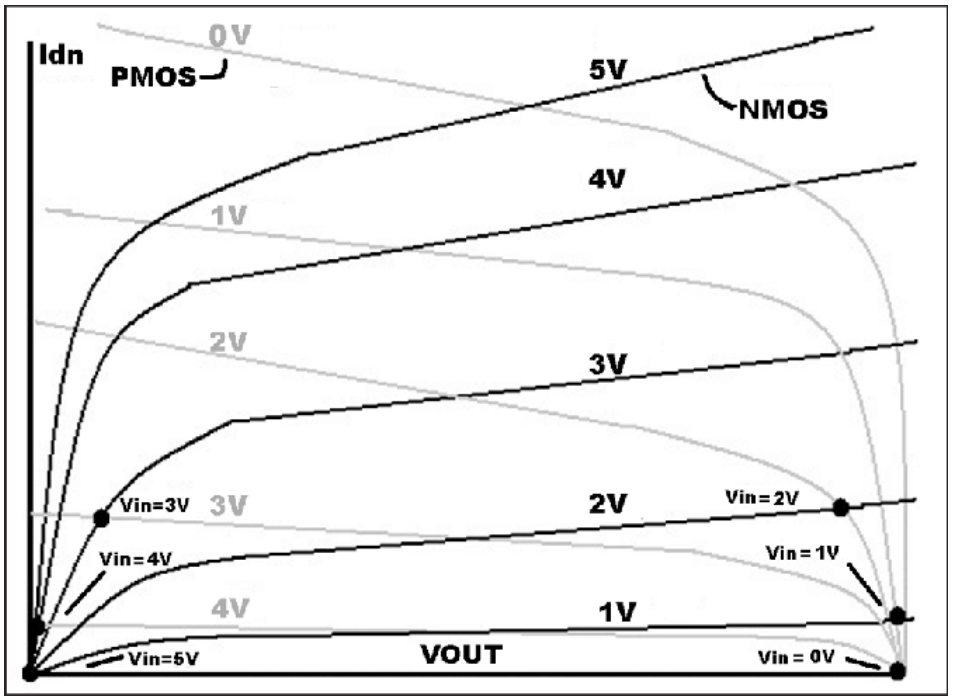

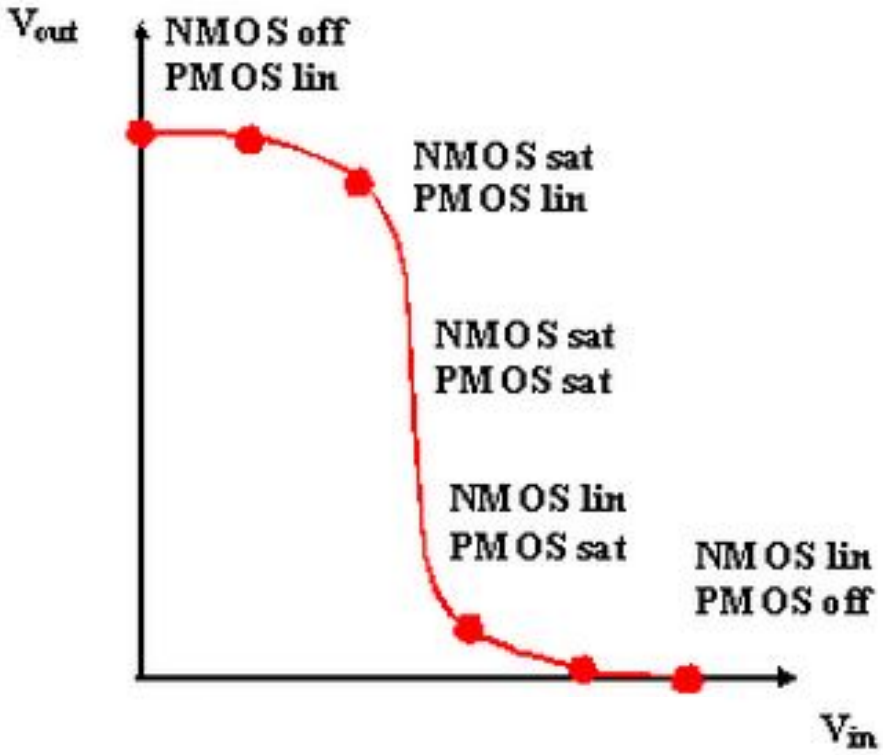

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CMOS circuit: Noise Margin

- Noise margin is the ratio by which the signal exceeds the minimum acceptable amount.
- It explains up to what extent IC allows noise in the transmission of logic ‘0’ and logic ‘1’.
- Logic ‘0’ and ‘1’ – represent the range of input values
- Hence, for error free digital signal transmission noise margin is required

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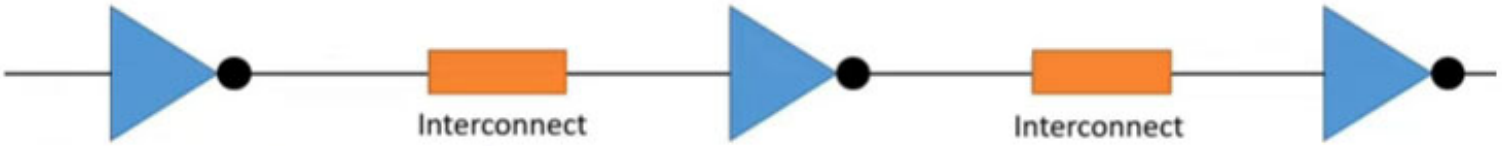

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