SINGAPORE UNIVERSITY OF TECHNOLOGY AND DESIGN

Term 7- Sept 2024

Nanoelectronics and Technology (01.119/99.503)

Week 2 Day 1 (24-Sept 2024)

Outline

- Review of MOSFETs
- CMOS Inverter circuit
- CMOS scaling

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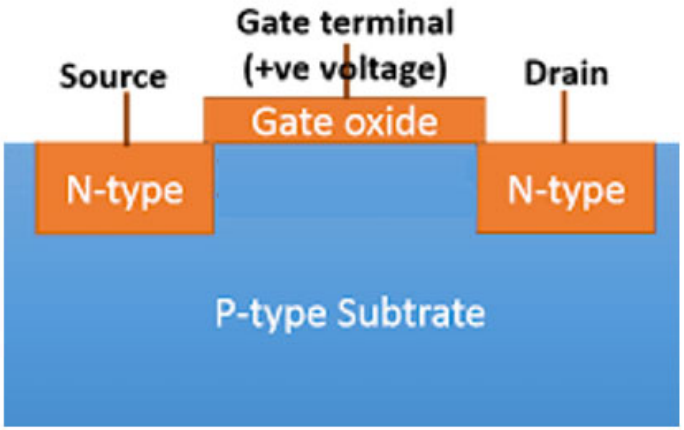
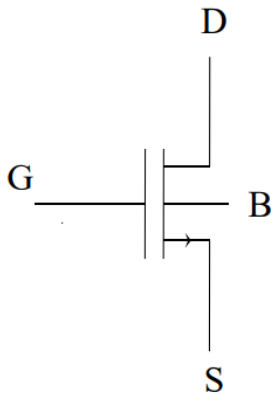
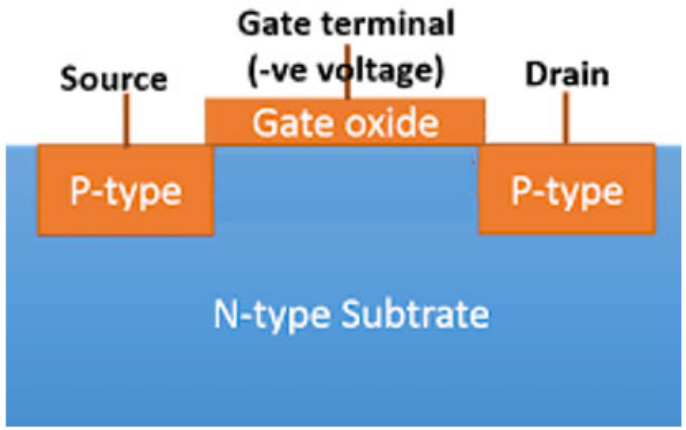
Review of MOSFETs

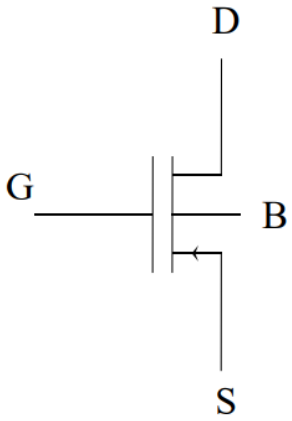


n-channel MOS
Transistor





p-channel MOS
Transistor



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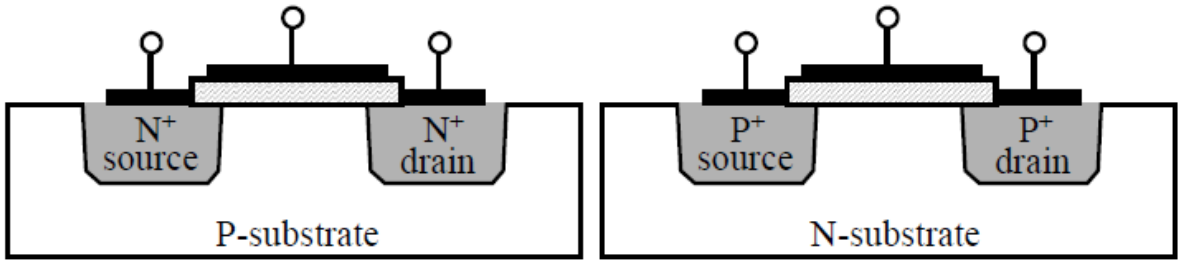
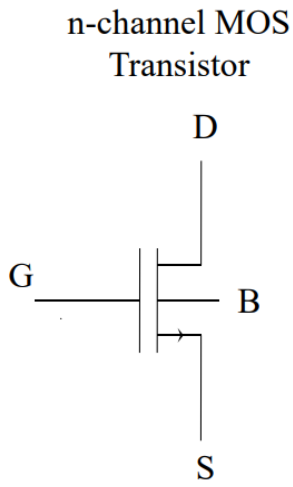
Review of MOSFETs

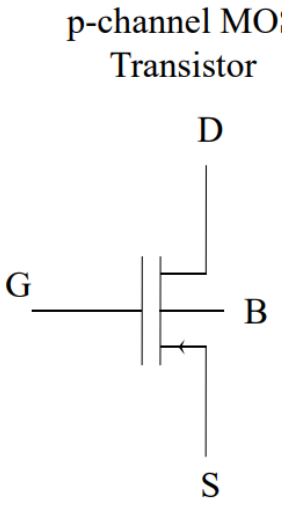
MOS Transistor

- Add "source" and "drain" terminals to MOS capacitor
- Transistor types
  - NMOS: p-type substrate, n^+ source/drain
  - PMOS: n-type substrate, p^+ source/drain



NMOS PMOS





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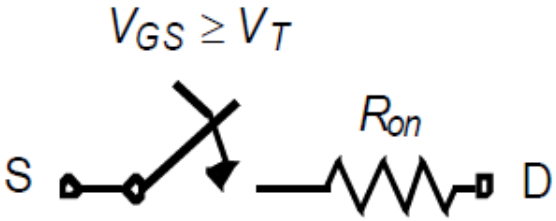
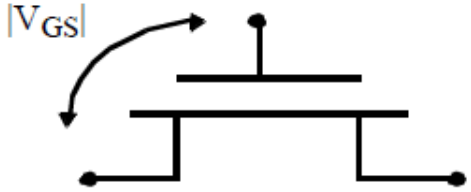
Review of MOSFETs

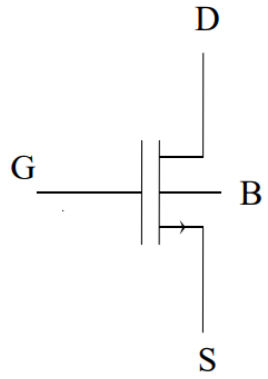
What is a Transistor?

A Switch! ⟷ An MOS Transistor

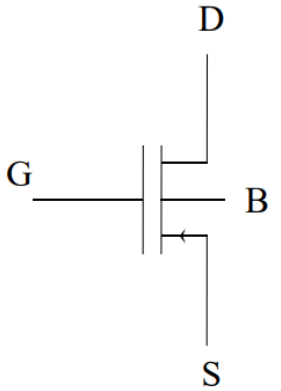




n-channel MOS Transistor



p-channel MOS Transistor



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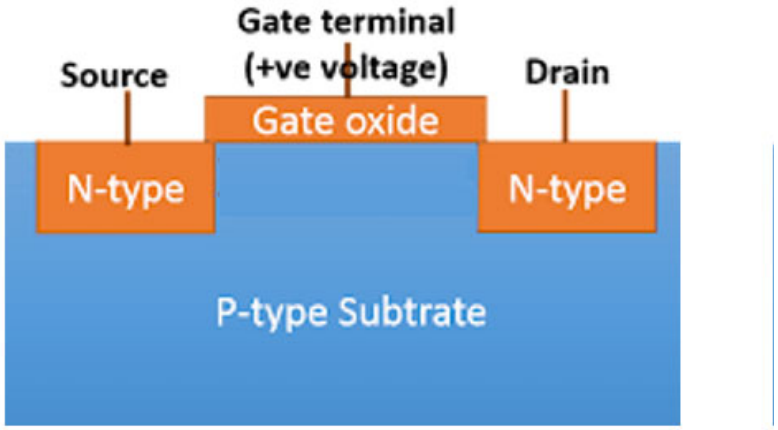
Review of MOSFETs



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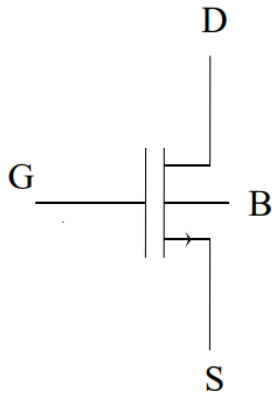
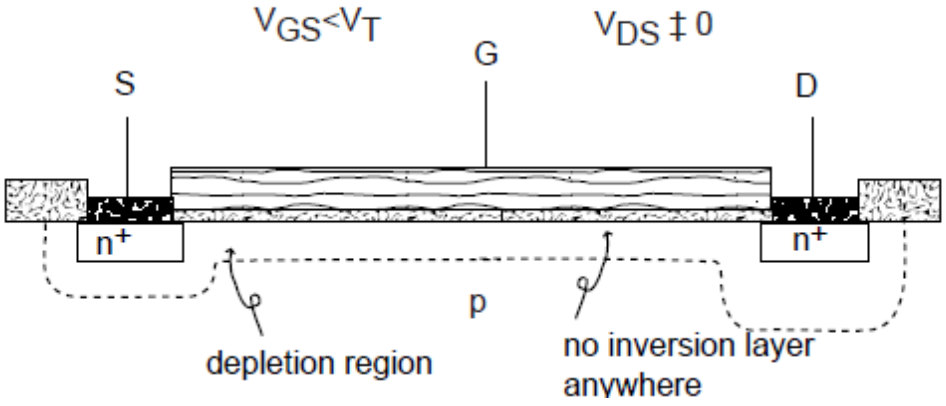


Cut-off Regime

- MOSFET:
  - $V_{GS} < V_T$, with $V_{DS} \geq 0$
- Inversion Charge = 0
- V_{DS} drops across drain depletion region
- $I_D = 0$



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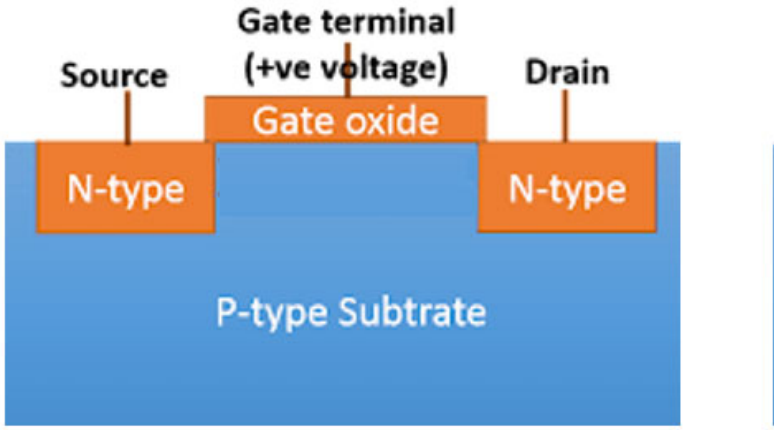
Review of MOSFETs



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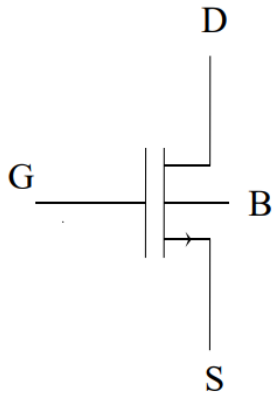
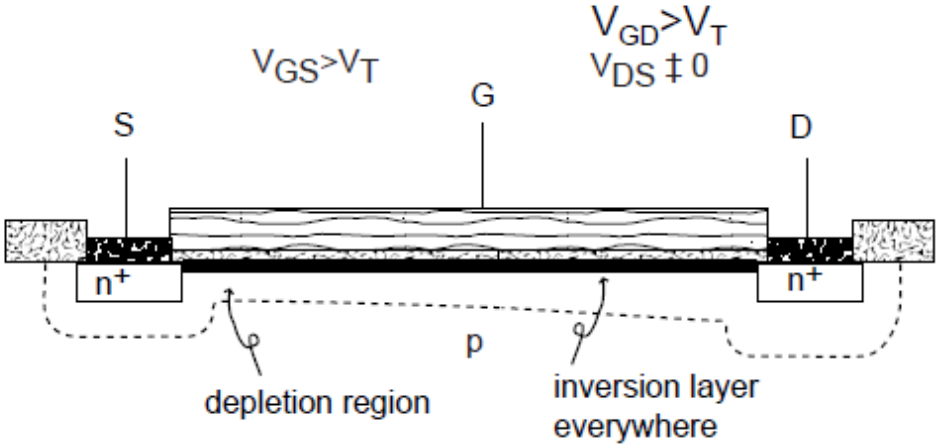


Linear or Triode Regime



$$V_{GD} = V_{GS} - V_{DS}$$

Electrons drift from source to drain ⇒ **electrical current**

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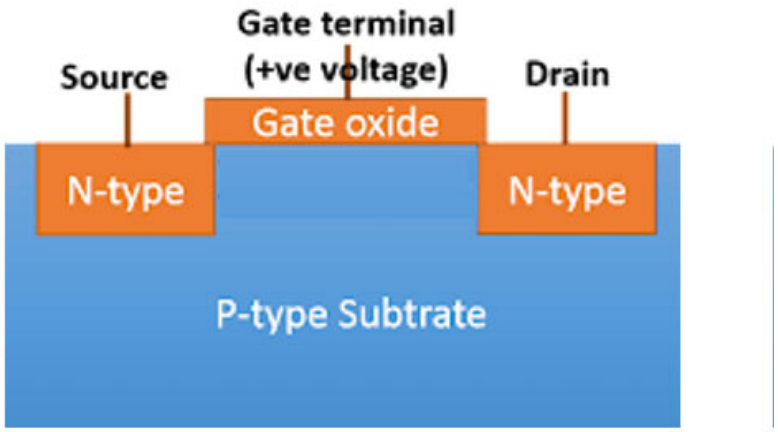
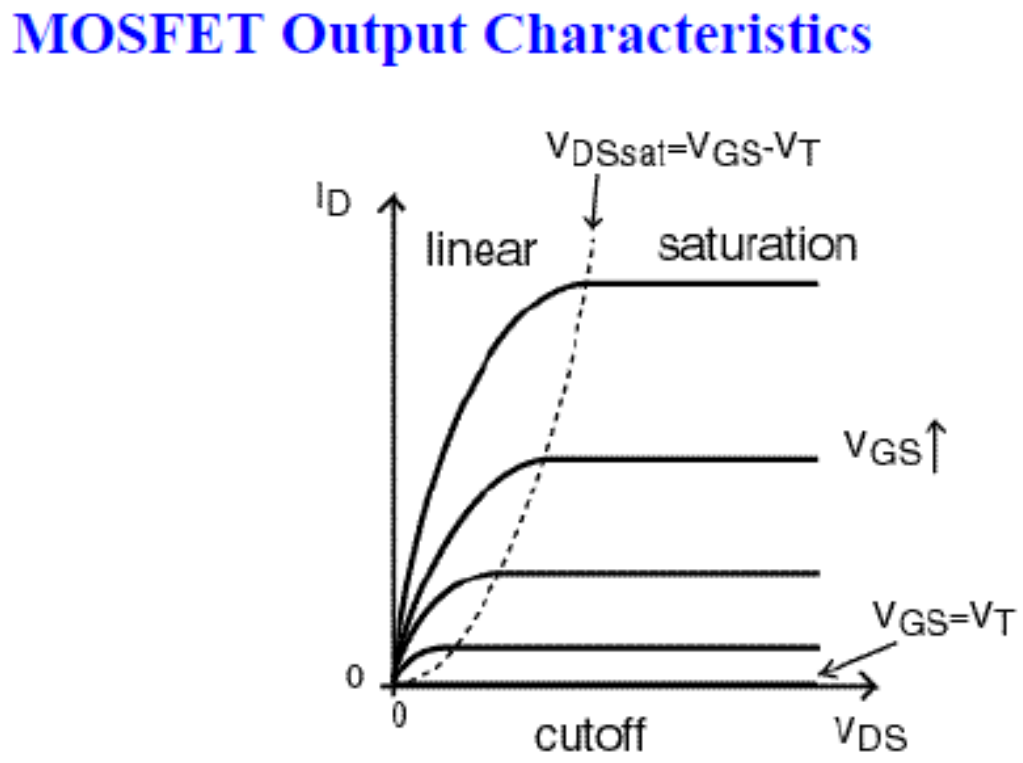
Review of MOSFETs





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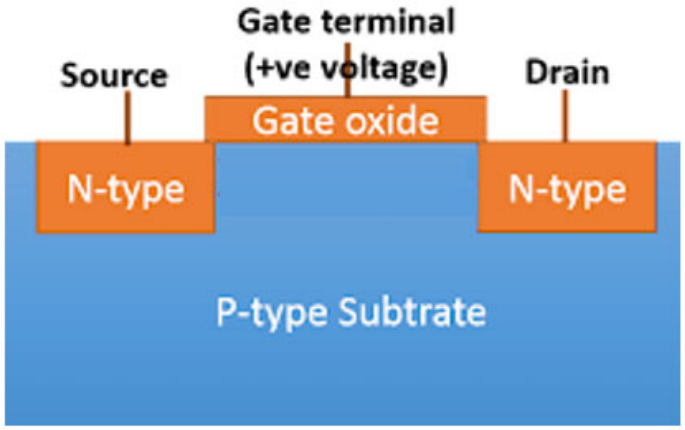
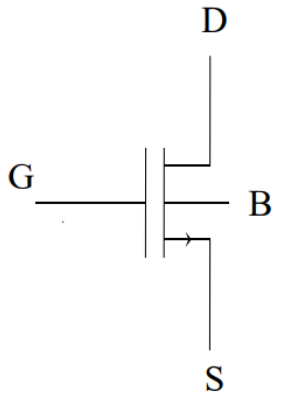
Review of MOSFETs



$$\beta = \mu C_{ox} \frac{W}{L}$$

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

n-channel MOS Transistor



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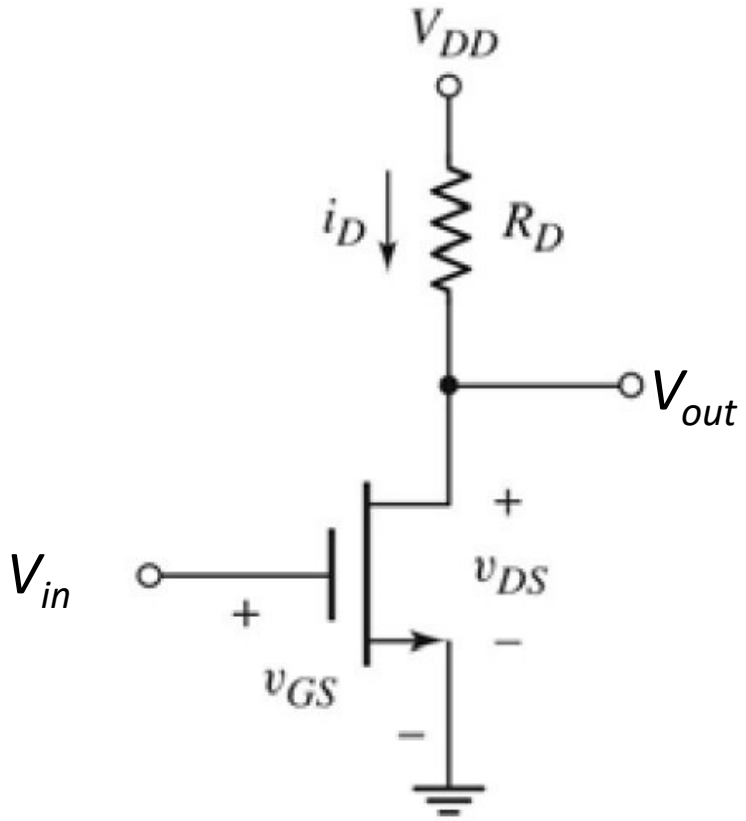
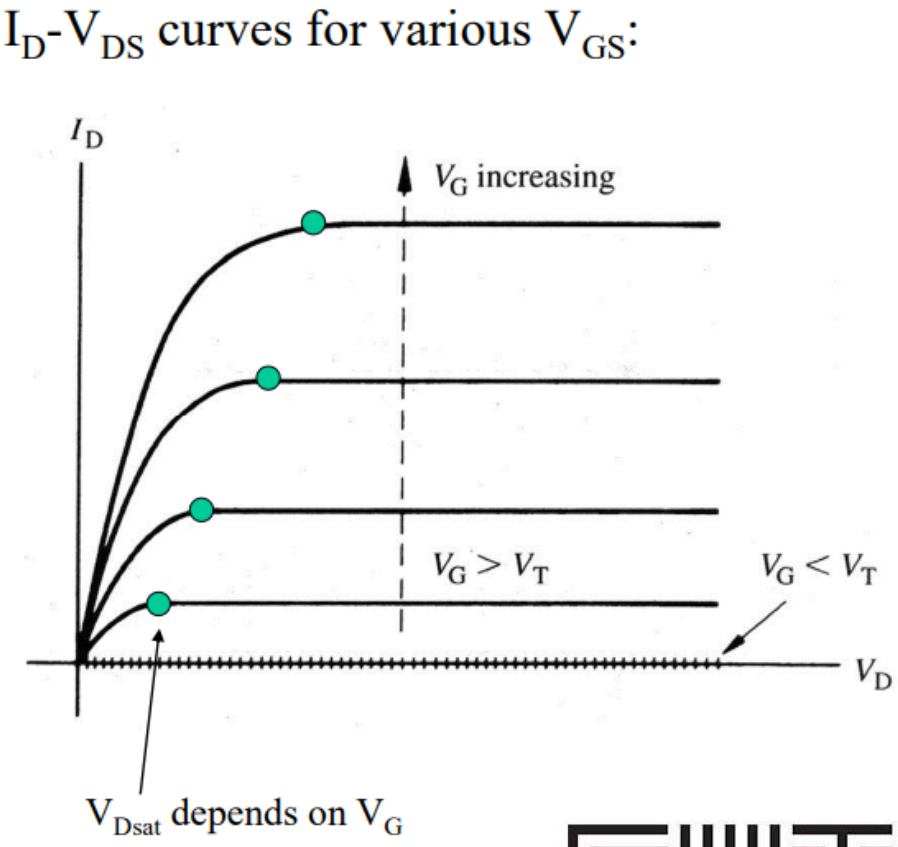
Review of MOSFETs: DC load line of n-MOSFET





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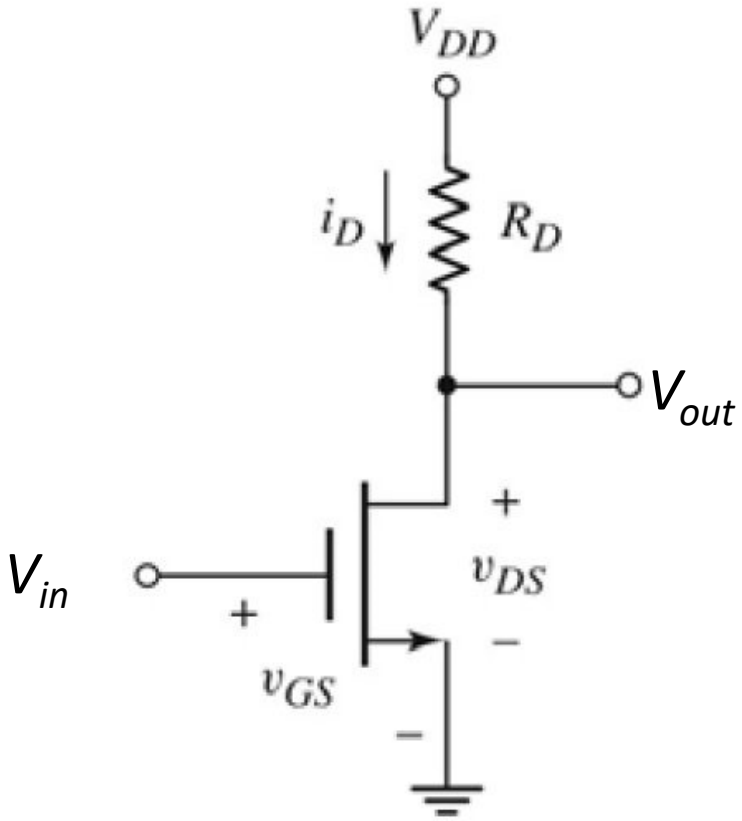

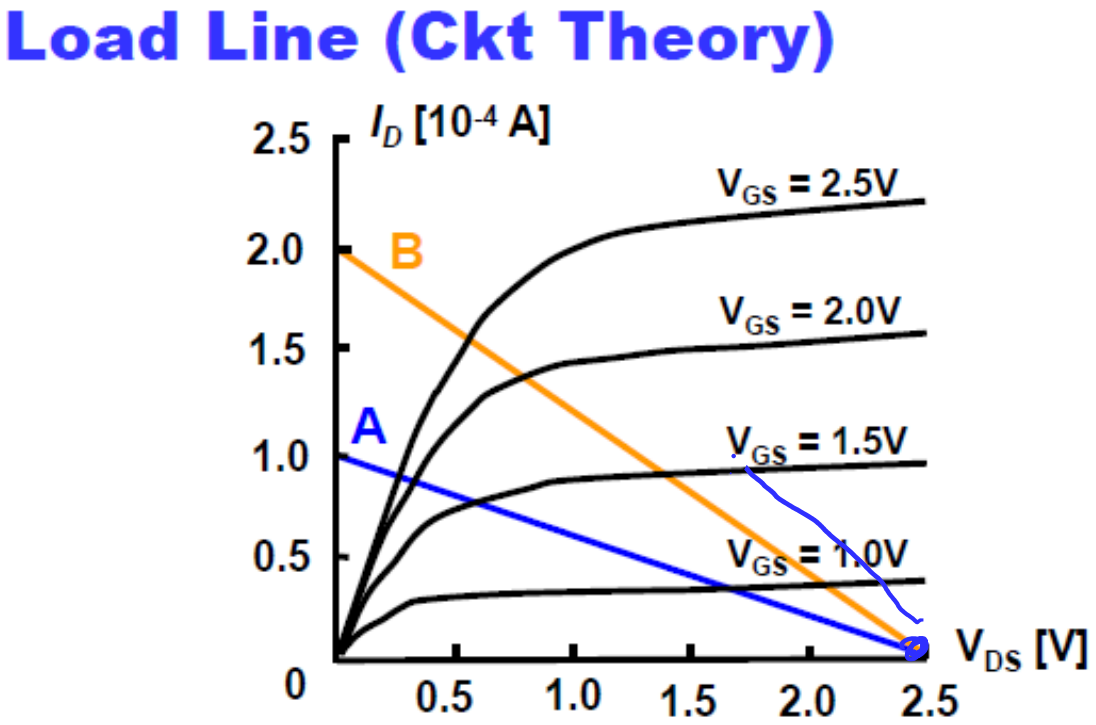

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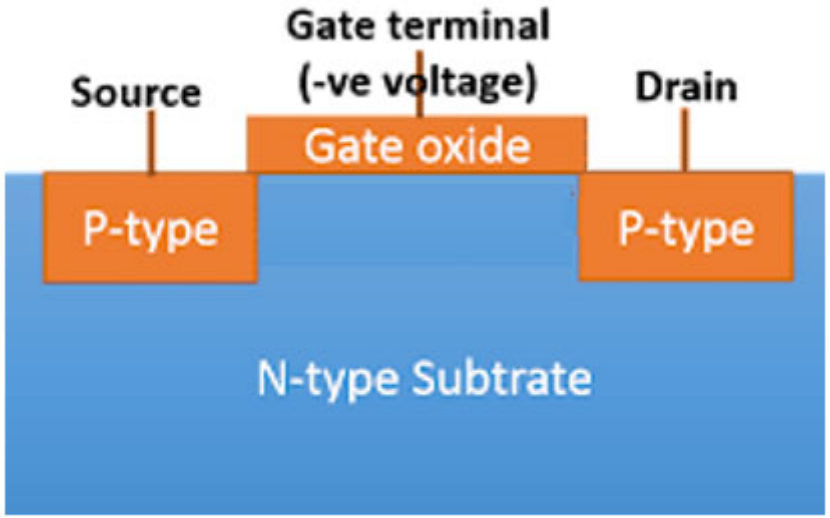
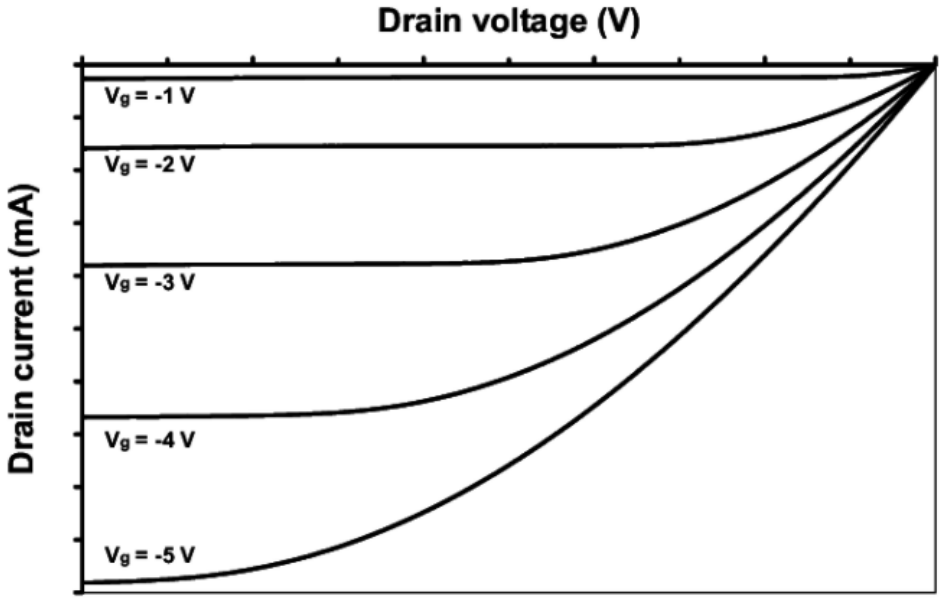
Review of MOSFETs

p-MOSFET





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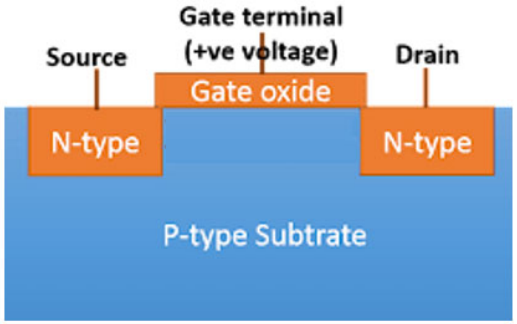
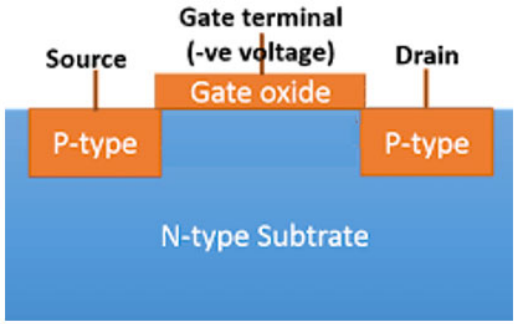
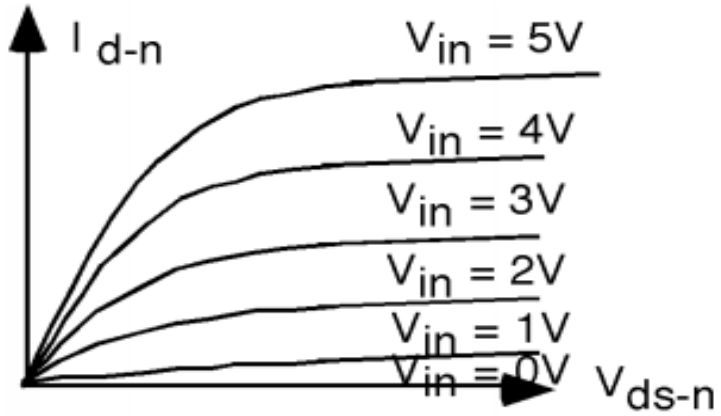
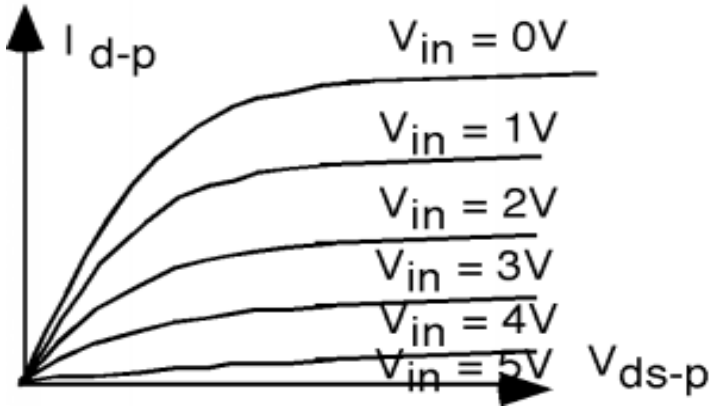
Review of MOSFETs









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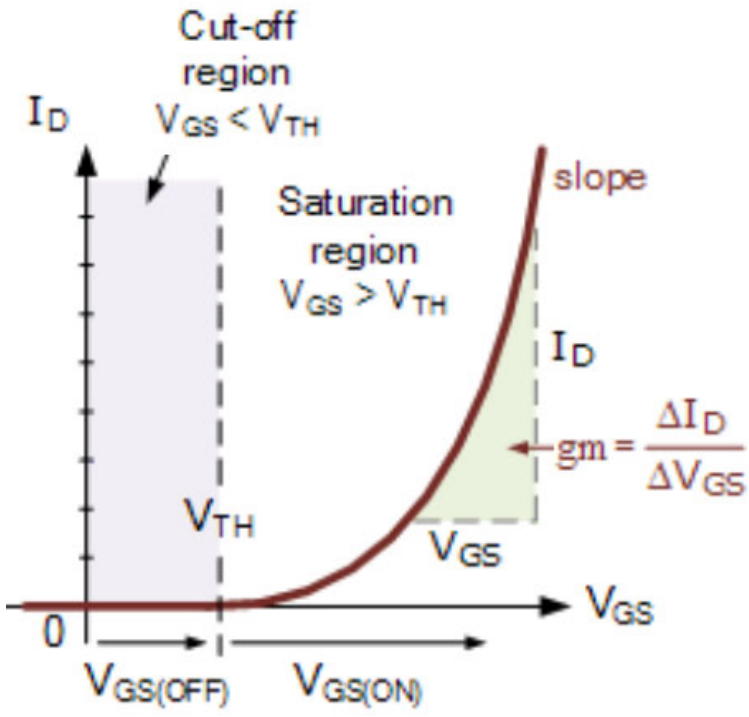
MOSFET: Threshold Voltage (V_{th})

- The voltage needed on the Gate terminal of the MOSFET to form a thin channel beneath the gate electrode (between Source & Drain terminals).
- The current can flow between S and D terminals through the channel.
- So threshold voltage is the voltage needed to turn on the device.
- As the MOSFET is voltage controlled current source, the output current will depend on the gate voltage applied.



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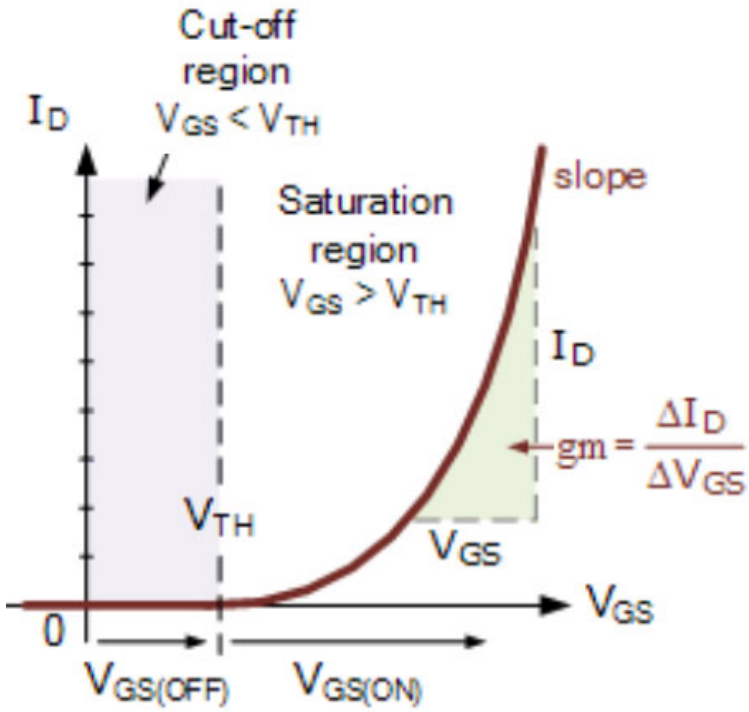
MOSFET: Threshold Voltage (V_{th})

- Lower Vth:
  - Faster in timing
  - Higher subthreshold current
- Higher Vth:
  - Less leakage
  - Higher delay
- V_{th} scales with MOSFET scaling



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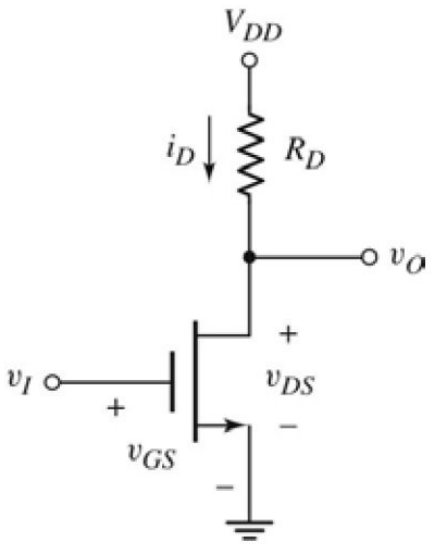
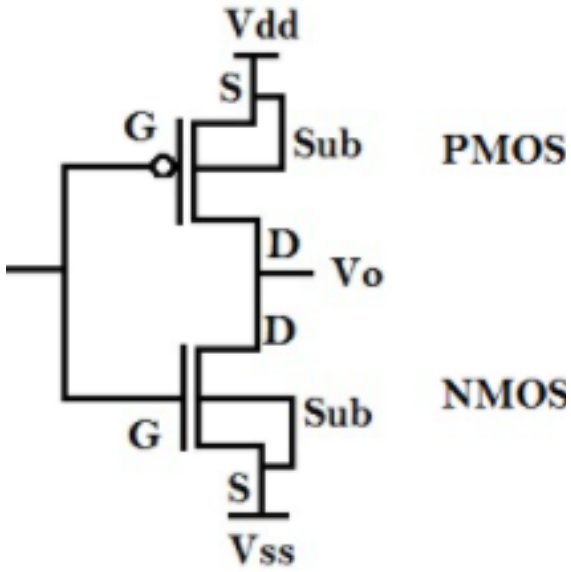
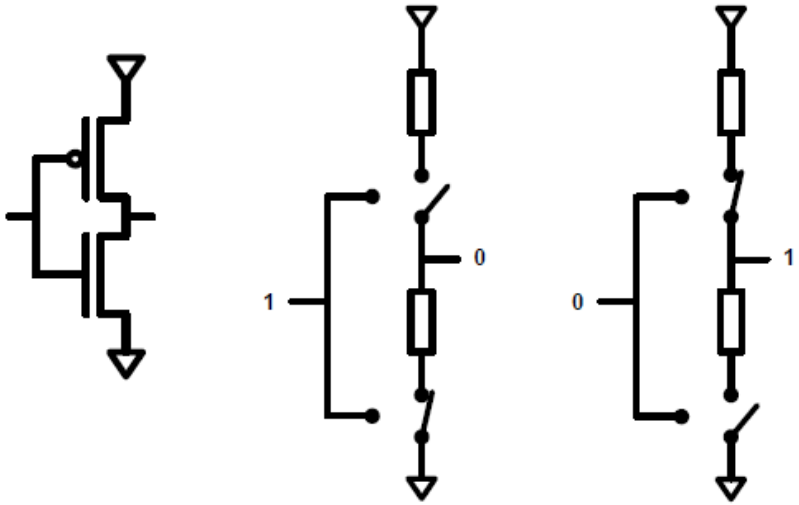
CMOS circuit





CMOS Inverter Operation Principle



G = Gate Terminal
S = Source Terminal
D = Drain Terminal
Sub = Substrate Terminal

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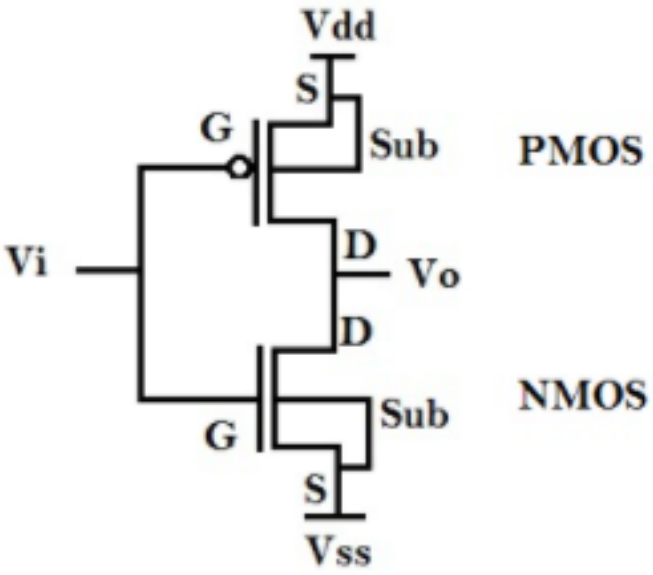
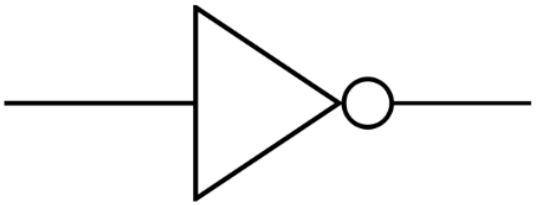
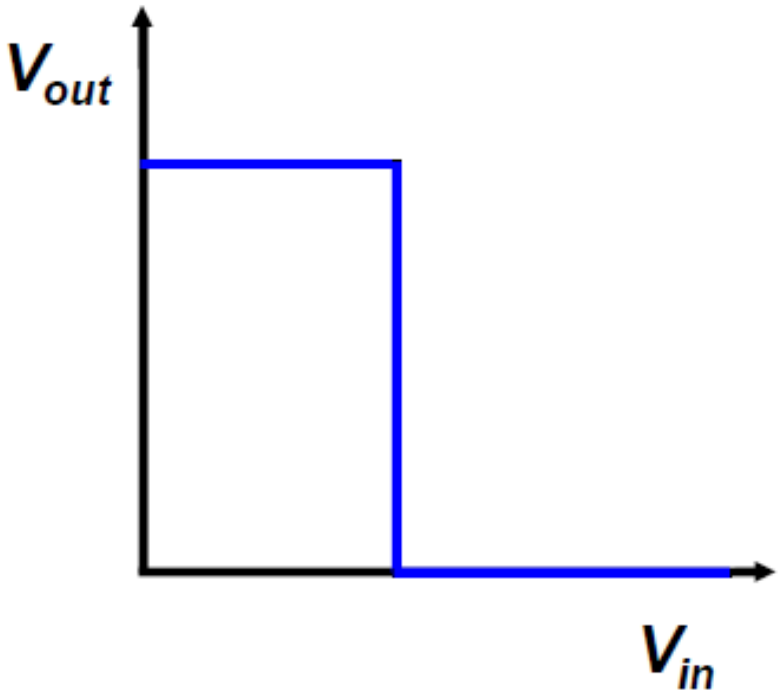
CMOS circuit







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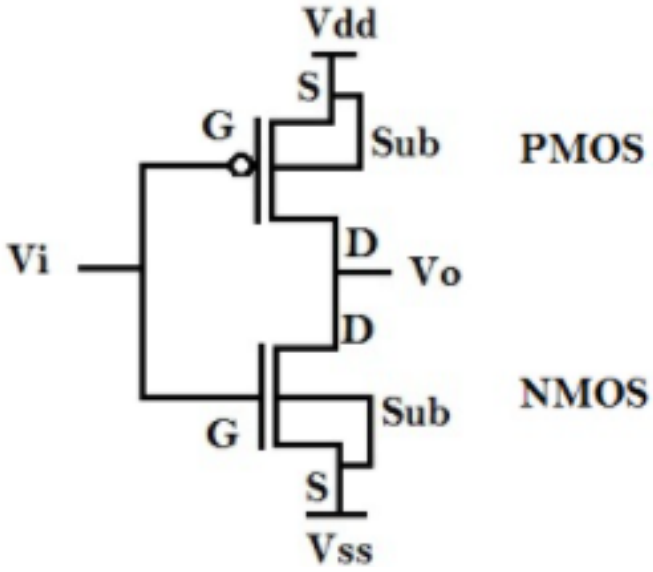

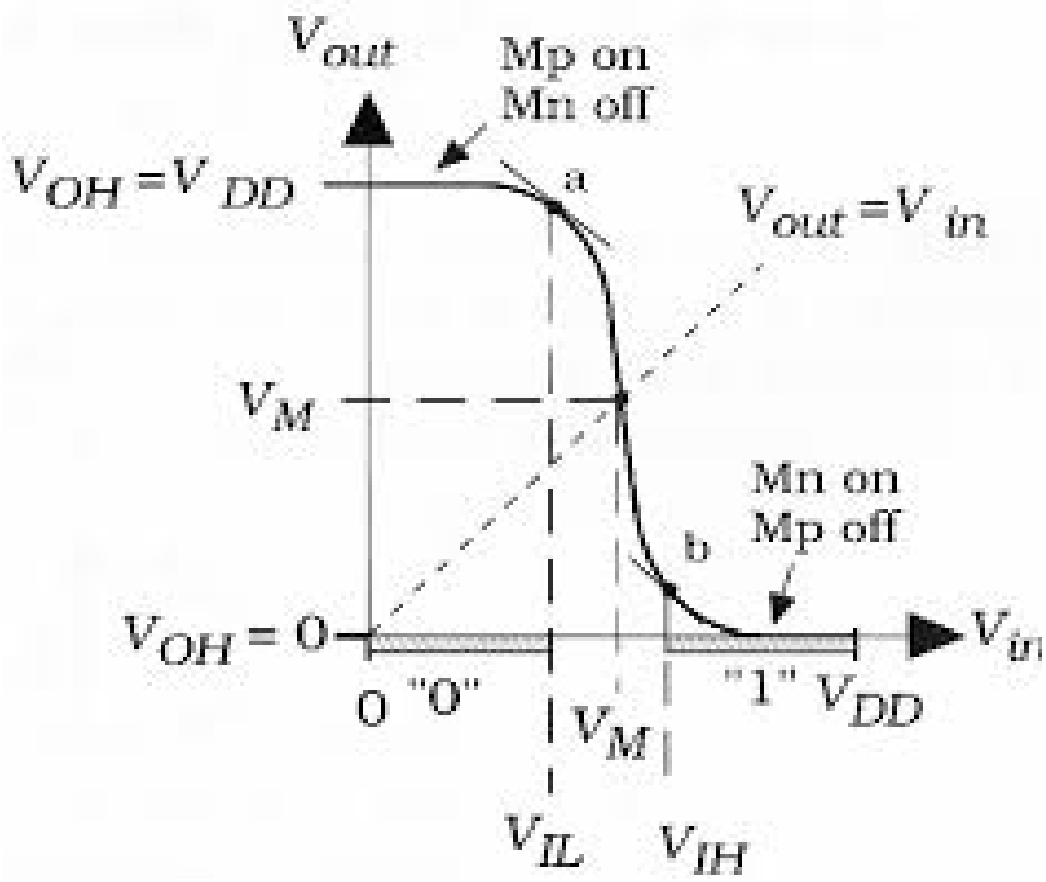

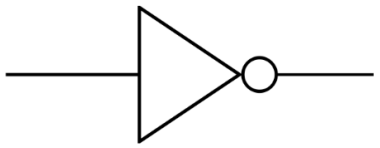

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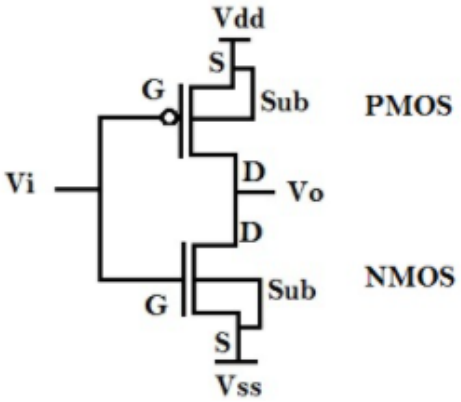

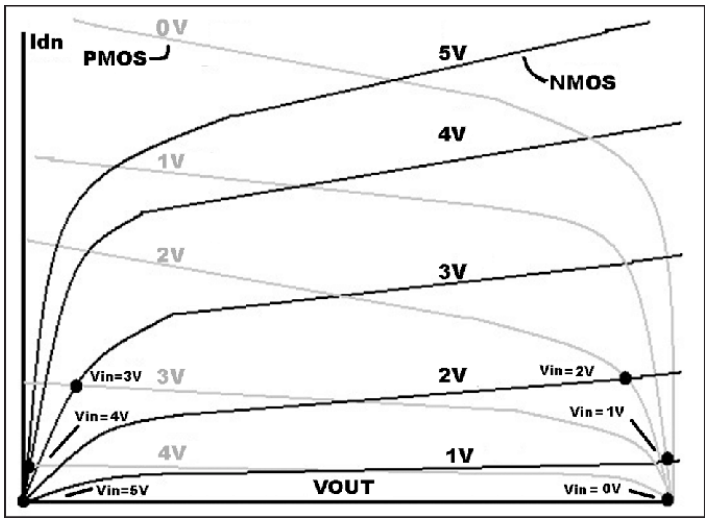

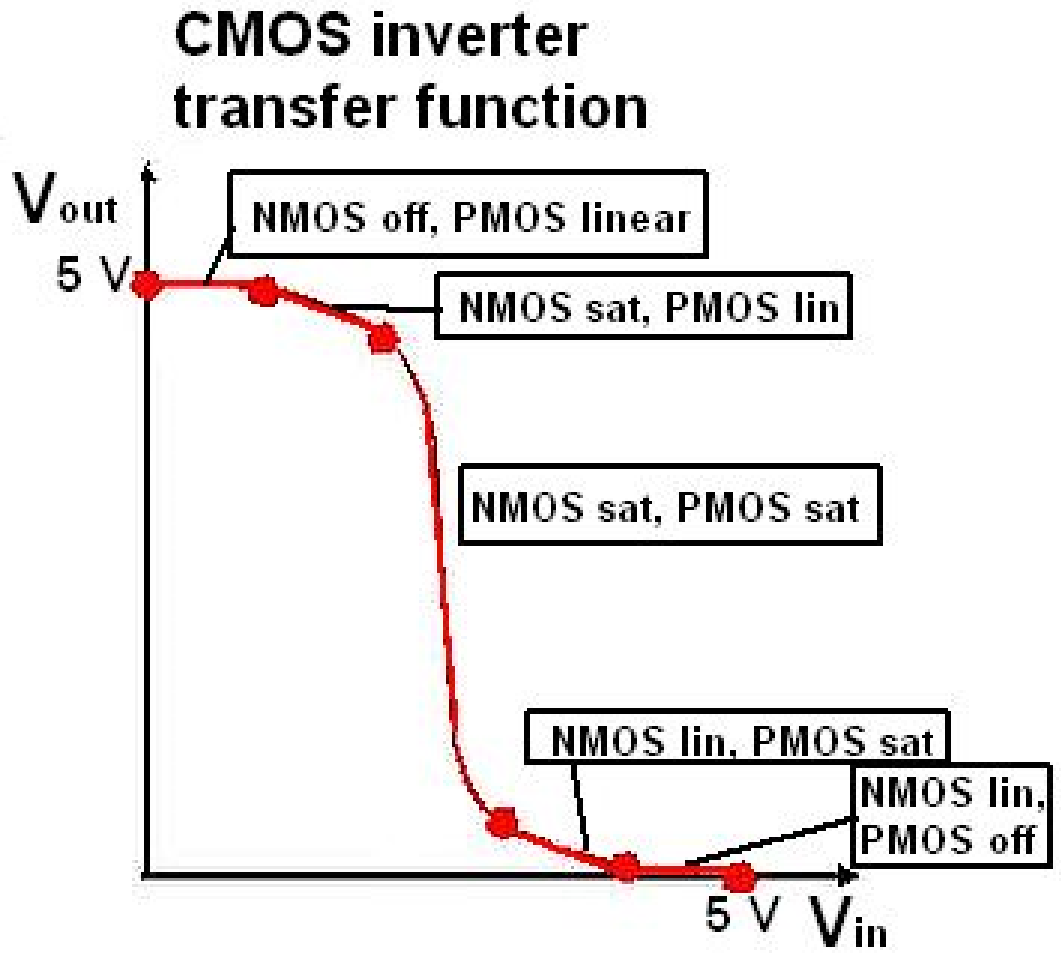

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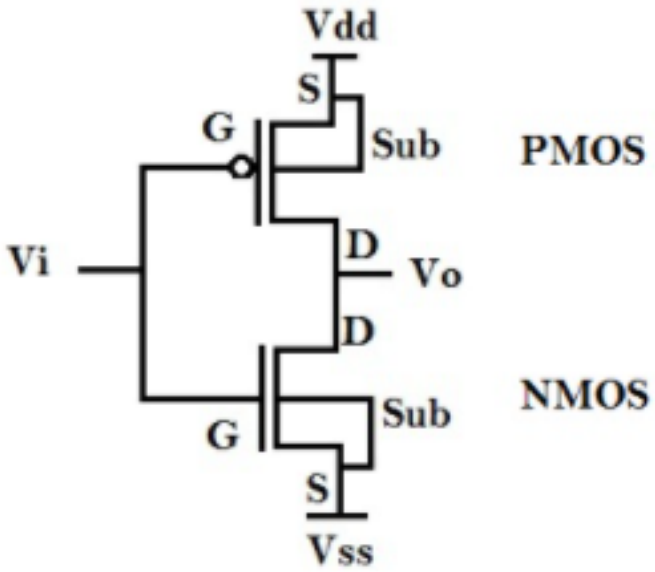
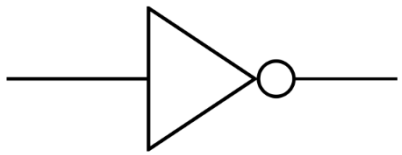
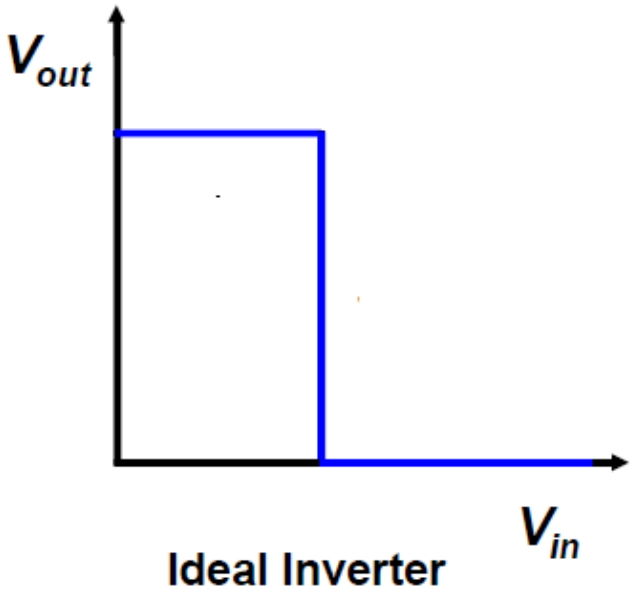
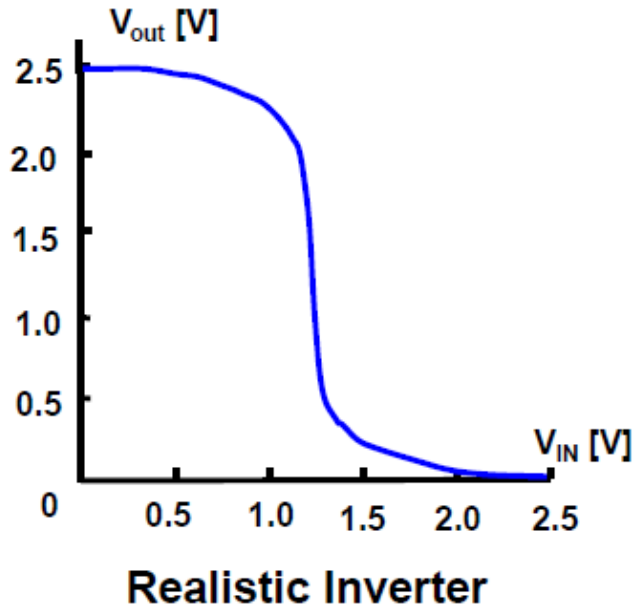
CMOS circuit





The Realistic Inverter





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CMOS circuit: Noise Margin

- Noise margin is the ratio by which the signal exceeds the minimum acceptable amount.
- It explains up to what extent IC allows noise in the transmission of logic ‘0’ and logic ‘1’.
- Logic ‘0’ and ‘1’ – represent the range of input values
- Hence, for error free digital signal transmission noise margin is required

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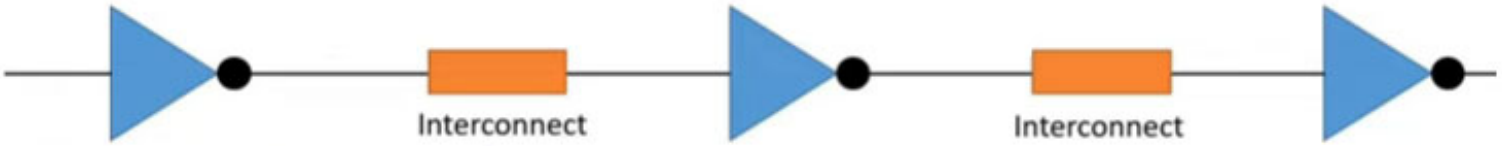

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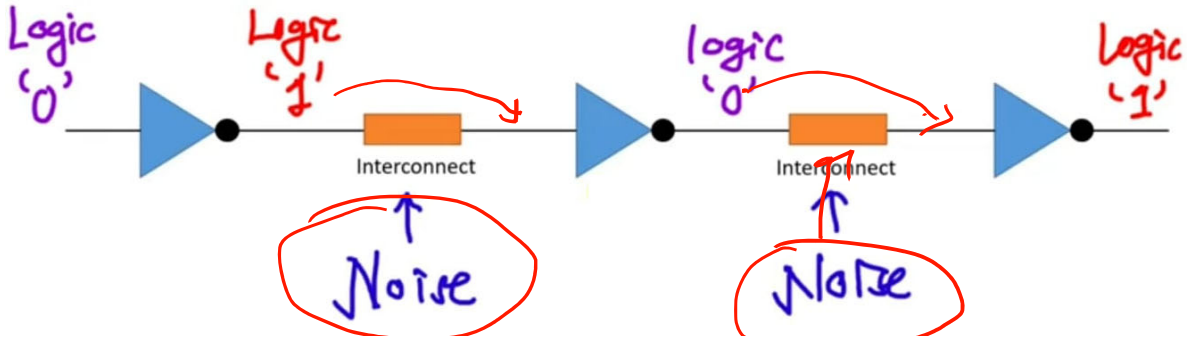
CMOS circuit: Noise Margin

- Noise margin is the ratio by which the signal exceeds the minimum acceptable amount.
- It explains up to what extent IC allows noise in the transmission of logic ‘0’ and logic ‘1’.
- Logic ‘0’ and ‘1’ – represent the range of input values
- Hence, for error free digital signal transmission noise margin is required



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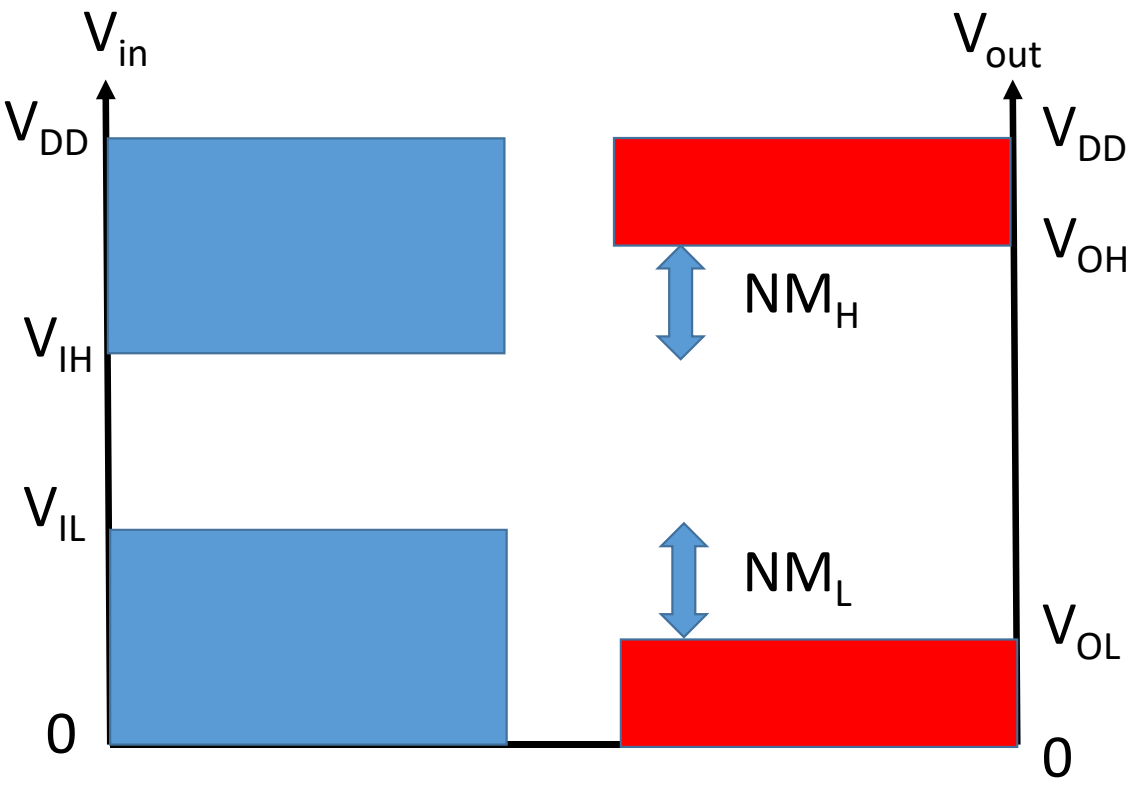
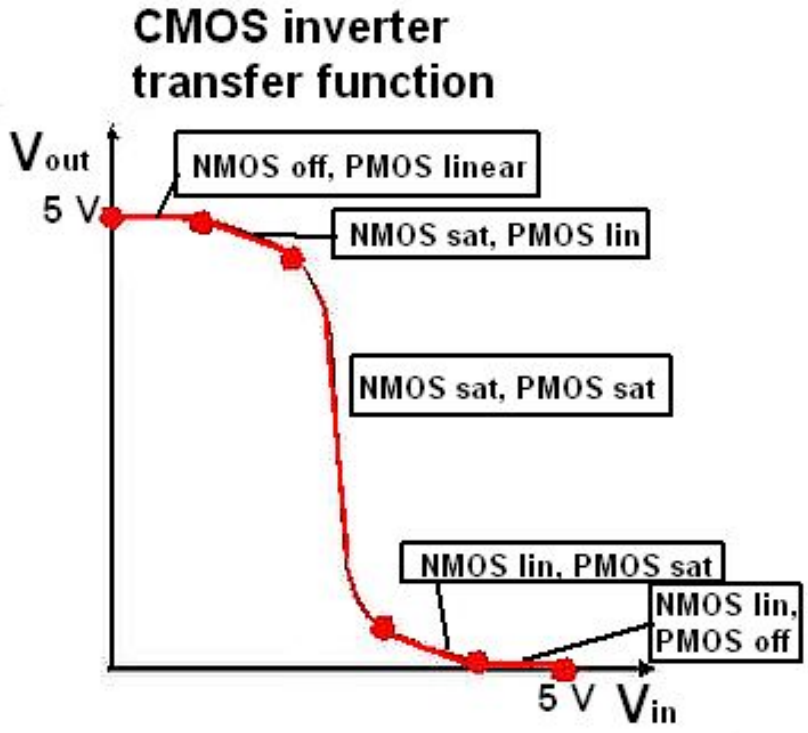
CMOS circuit: Noise Margin





$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

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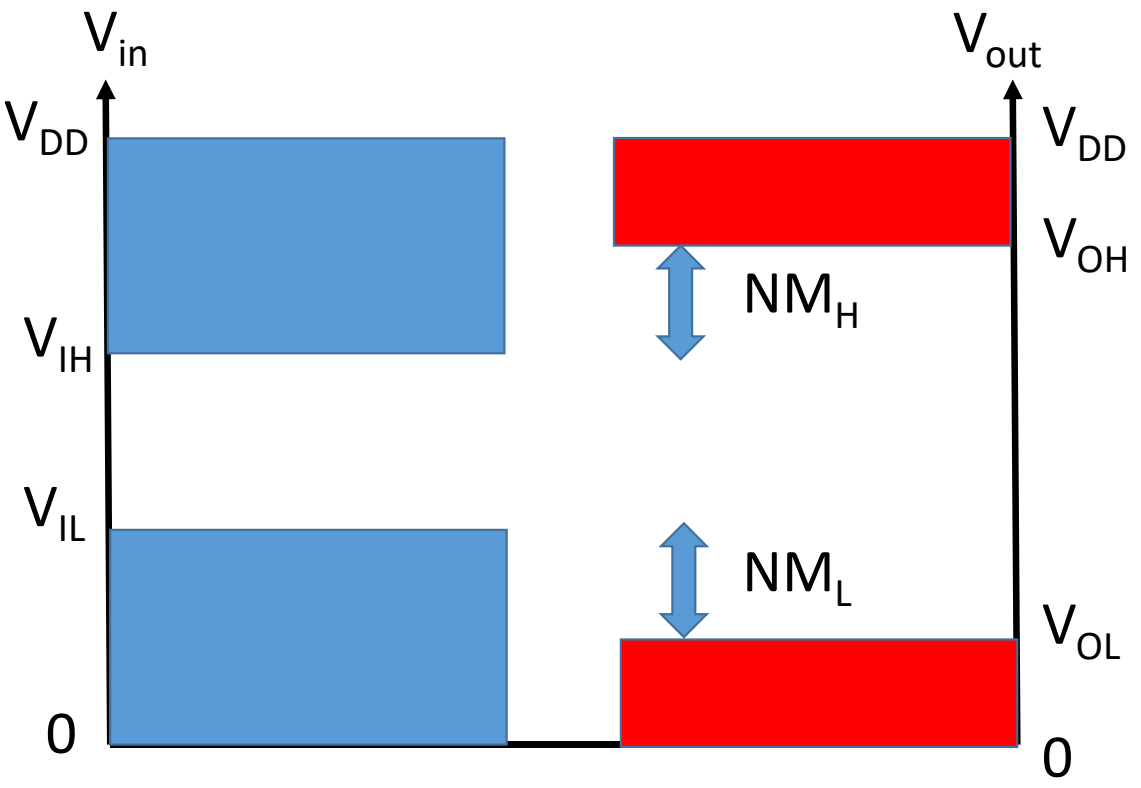
CMOS circuit: Noise Margin



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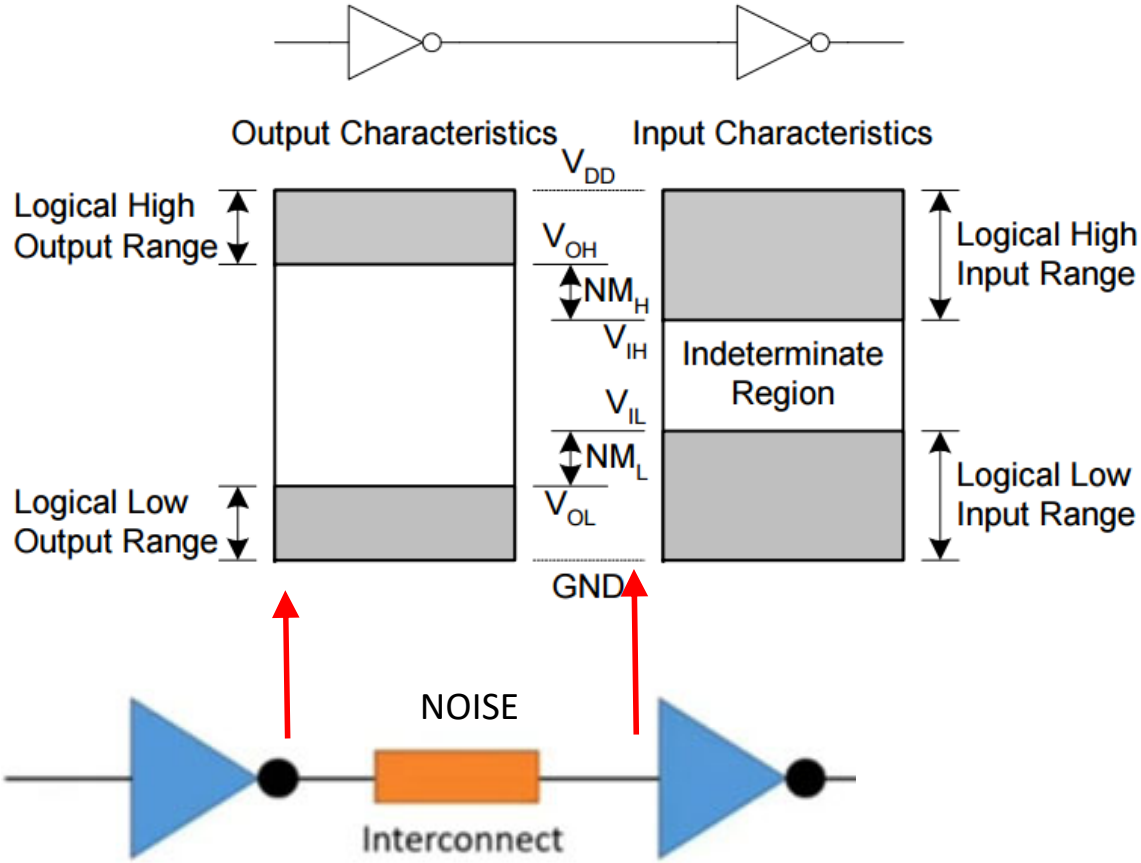
CMOS circuit: Noise Margin



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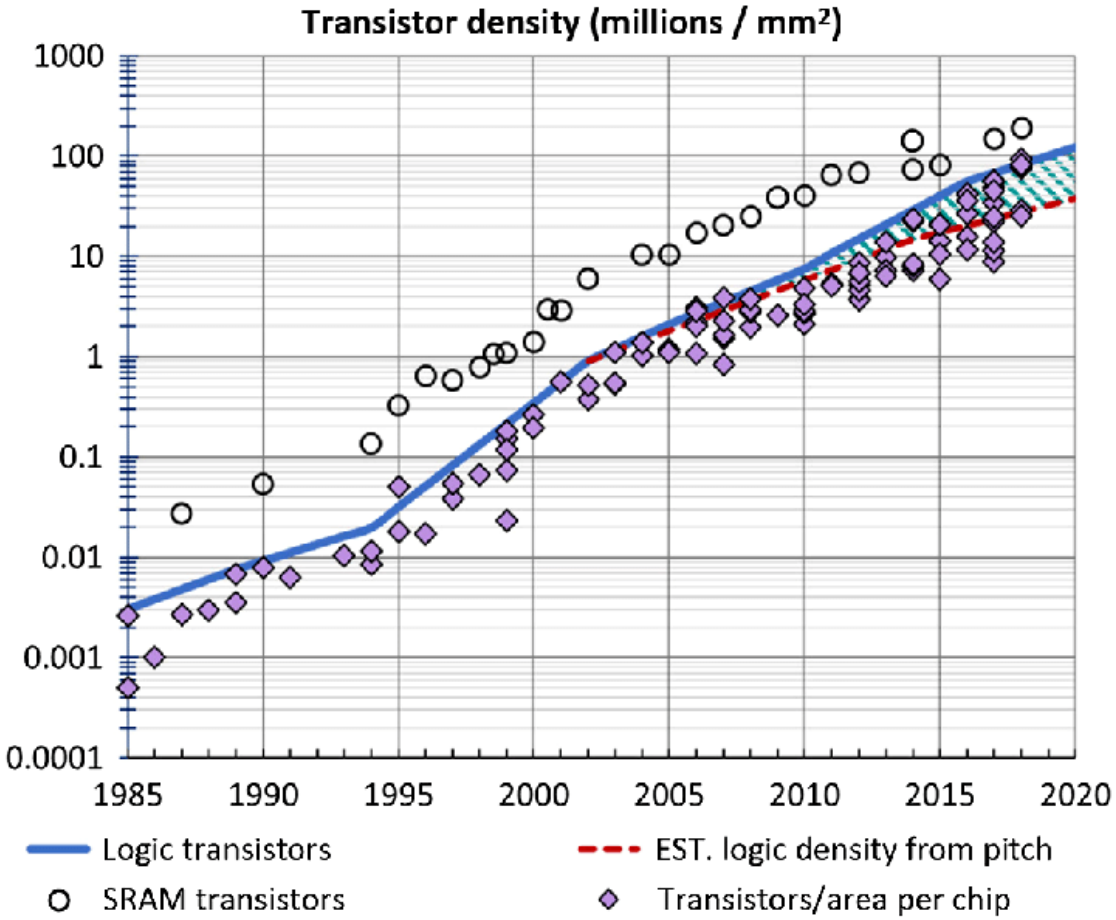
CMOS scaling: Moore's Law

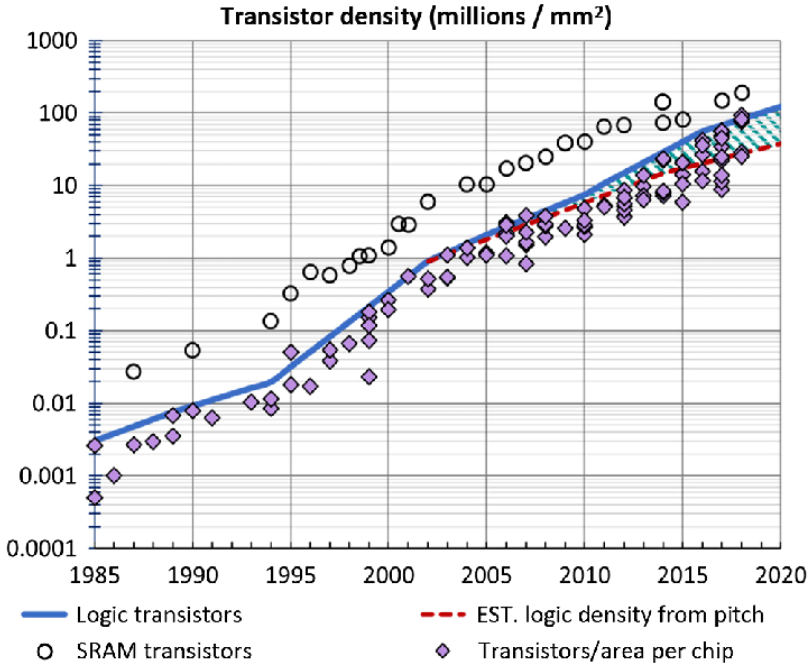


Moore's law says that the number of transistors doubles approximately every two years.

- CMOS scaling
  - Speed
  - High density
  - Less power
  - Reduced cost/transistor

Ref: M. L. Rieger, " Retrospective on VLSI value scaling and lithography" Journal of Micro/Nanolithography-2019

CMOS scaling: Dennard's scaling

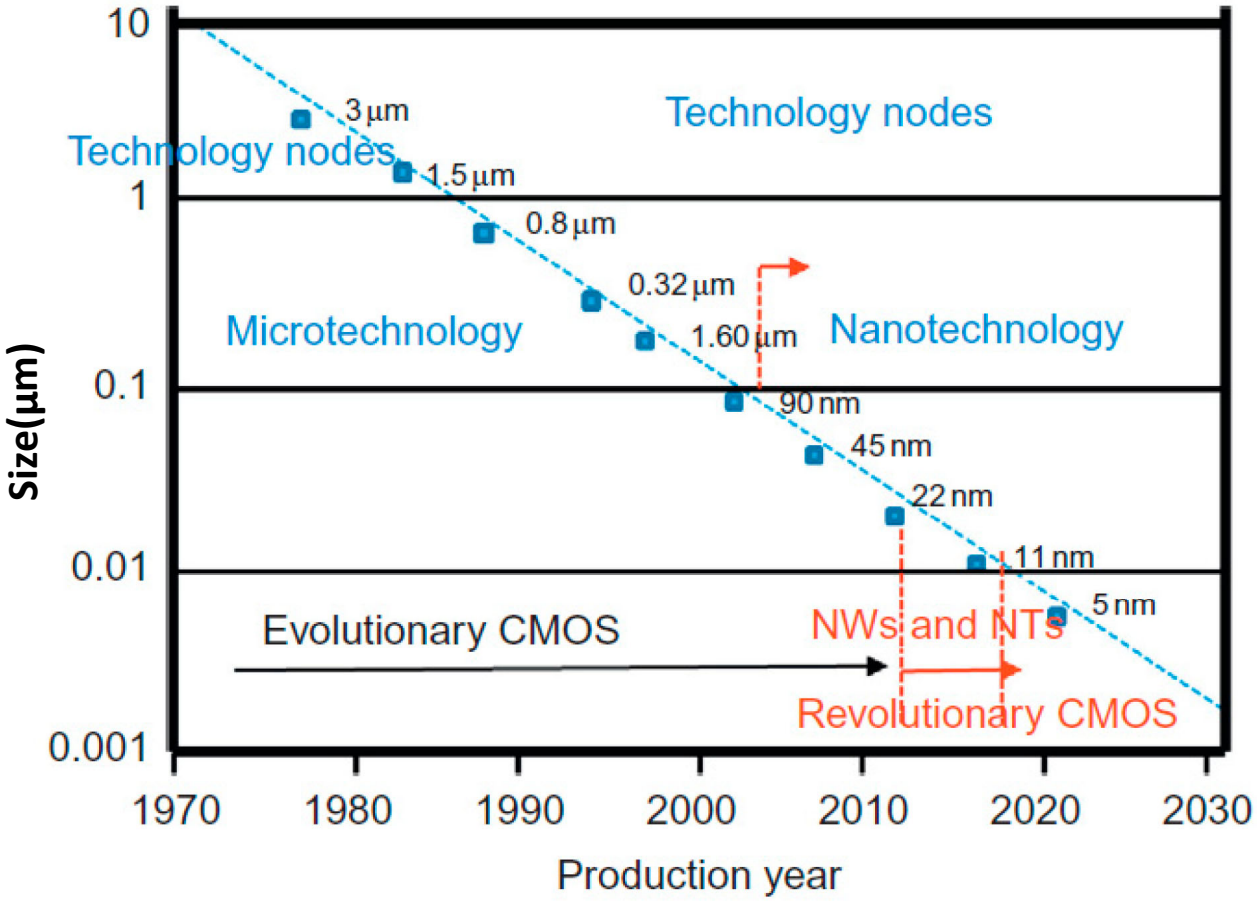


Dennard scaling, also known as MOSFET scaling, is a scaling law which states roughly that, as transistors get smaller, their power density stays constant, so that the power use stays in proportion with area; both voltage and current scale (downward) with length.

With feature sizes below 65nm, these rules could no longer be sustained, because of the exponential growth of the leakage current."

Ref: M. L. Rieger, " Retrospective on VLSI value scaling and lithography" Journal of Micro/Nanolithography-2019

CMOS scaling: Moore's Law



Ref: H. H. Radamson, et al., " Miniaturization of CMOS" Micromachines 10(5) 293-2019