

**Graduate Elective course (Term 7)**

**99.503: Nanoelectronics and Technology**

**Instructor: Shubhakar Kalya**

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**Class Timings**

- Tuesday- 3.30PM-6PM
- Thursday-3.30PM-6PM

**Class Venue**

- TT-1.408 (Building 1 Level 4)

**Grading and assessment:**

- Homework - 10%
- Mid-term Exam-30%
- Final Exam-30%
- Course project- 20%
- Seminar presentation- 5%
- Class participation and attendance-5%

### Weekly teaching contents

<u>Week No.</u>	<u>Topic</u>	<u>Description</u>
Week 1	Introduction to Nanoelectronics and nano-CMOS scaling	ITRS Roadmap for CMOS scaling for advanced technology nodes towards 5nm/3nm technology node and challenges for further scaling. Need for new concepts in nanoelectronic materials and devices. Importance of high-k gate dielectric and metal electrodes in nanoscale MOSFETs.
Week 2	Nanoscale MOSFET, FinFET and other emerging devices	Working principle, physics and electrical characterization of nanoscale MOSFETs. Theory and working principle of FinFET. Fabrication and characterization of nanoscale MOSFETs, FinFETs and scaling trend towards 5nm/3nm technology node.
Week 3	Thin film deposition techniques and cleanroom experiment 1	Review of physical vapour deposition (PVD), chemical vapour deposition (CVD). Atomic layer deposition (ALD) and electron –beam evaporation method. Cleanroom experiment 1 (2 <sup>nd</sup> class)-Growth of gate dielectric on silicon substrate.
Week 4	Nanofabrication techniques/methods	Extreme UV lithography, electron-beam lithography and nanopatterning, Self-aligned multiple patterning (SAMP) process solution for advanced CMOS technology nodes. Self-aligned double patterning (SADP) and self-aligned quadruple patterning (SAQP) processes.
Week 5	Reliability and failure analysis of nanoelectronic materials and devices	Study of key reliability and failure issues in nanoelectronic devices: process-induced defects, self-heating, carrier scattering, hot-carrier transport, dielectric degradation and breakdown.
Week 6	Interconnect technology	Interconnect technology, impact of scaling of CMOS devices on interconnects, reliability and failure mechanism in interconnects. Emerging interconnect technologies. Cleanroom experiment 2 (2 <sup>nd</sup> class)- electron beam lithography and nanopatterning.

### Week 7: RECESS

<u>Week No.</u>	<u>Topic</u>	<u>Description</u>
Week 8	Three dimensional integrated circuit (3D-IC) systems and technology	3D integration circuit technology, heterogeneous 3D IC systems and design challenges. Electrical probing experiment 3 (2 <sup>nd</sup> class)- electrical characterization of nanoscale devices.
Week 9	Understanding of Quantum mechanics : Carrier transport and application of quantum mechanics in nanoscale electronic devices	Electronic bond structure, electron transport, carrier scattering, coulomb blockade and quantum confinement in low-dimensional structures and nanoscale electronic devices
Week 10	Nanoscale characterization using scanning probe microscopy (SPM) techniques	Working principle of scanning tunneling microscopy (STM), atomic force microscopy (AFM) and its applications for analysing properties of nanoscale materials and devices.
Week 11	Nanoscale analysis using electron microscopy techniques	Scanning electron microscopy (SEM) and transmission electron microscopy (TEM) analysis of nanoscale materials and devices. Study of SEM-STM nanoprobe and in-situ TEM characterization.
Week 12	Non-volatile memory (NVM) technology	Review of memory technologies. NAND-flash NVM technology and its scaling. Vertical (3D) NAND flash technology and emerging NVM devices such as resistive random-access memory (RRAM) and magnetic RAM (MRAM).
Week 13	Applications of nanomaterials and nanoelectronic devices	Applications of nanomaterials and nanoelectronic devices in different fields of nanoelectronics and nanotechnology. (a) Oxide and 2D-hexagonal boron nitride based RRAM devices for neuromorphic computing (b) 2D-graphene based logic devices (c) Energy technology (d) High-power and automobile application
Week 14	Review session – class 1	Review session – class 1