



Term 7- Sept 2025

Nanoelectronics and Technology (01.119/99.503)-Week 3 Class 1

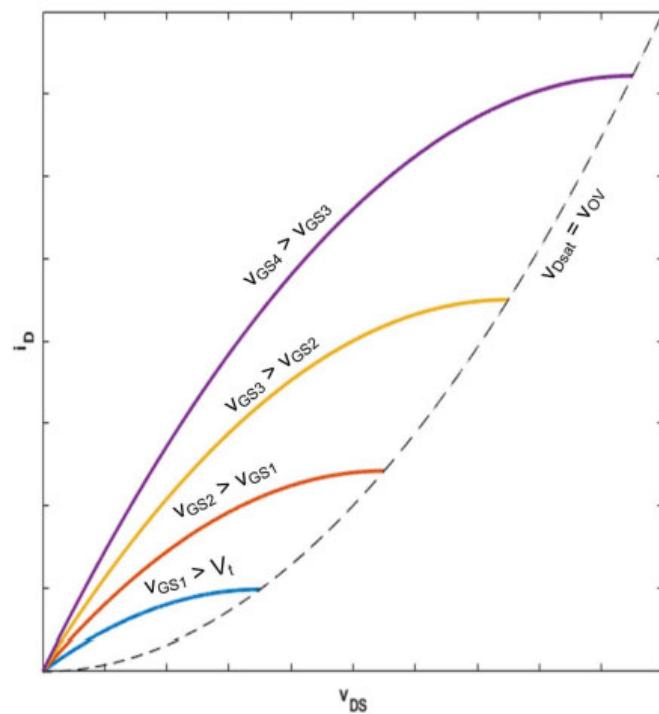
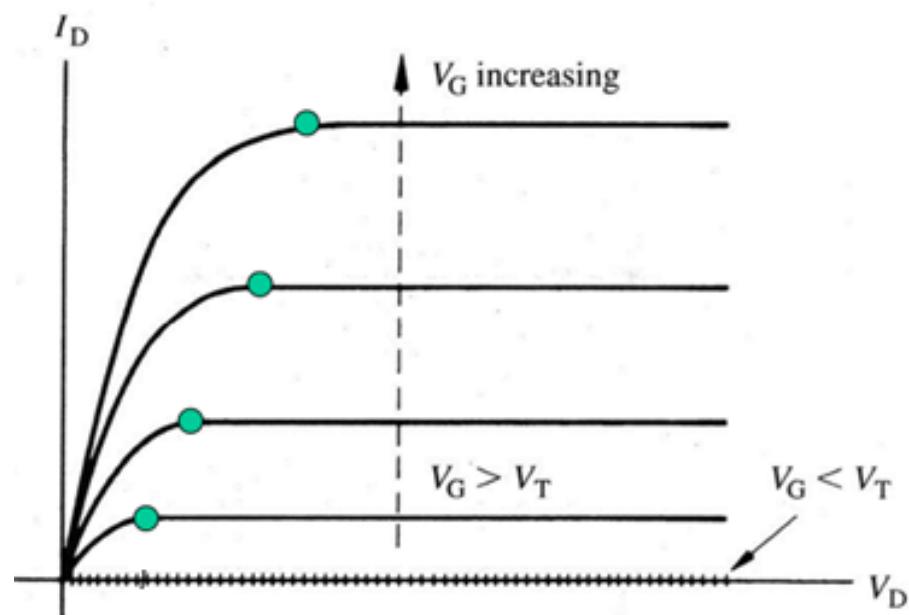
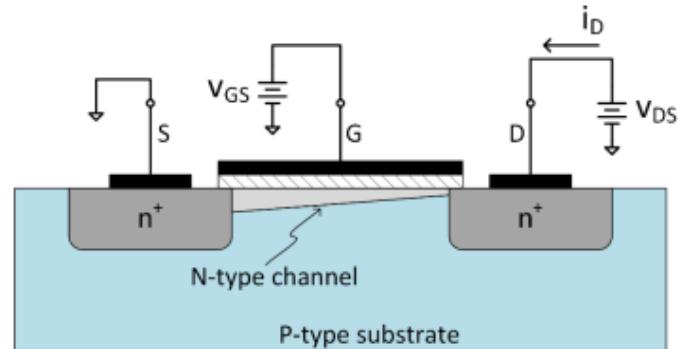
Shubhakar K
30-Sept- 2025

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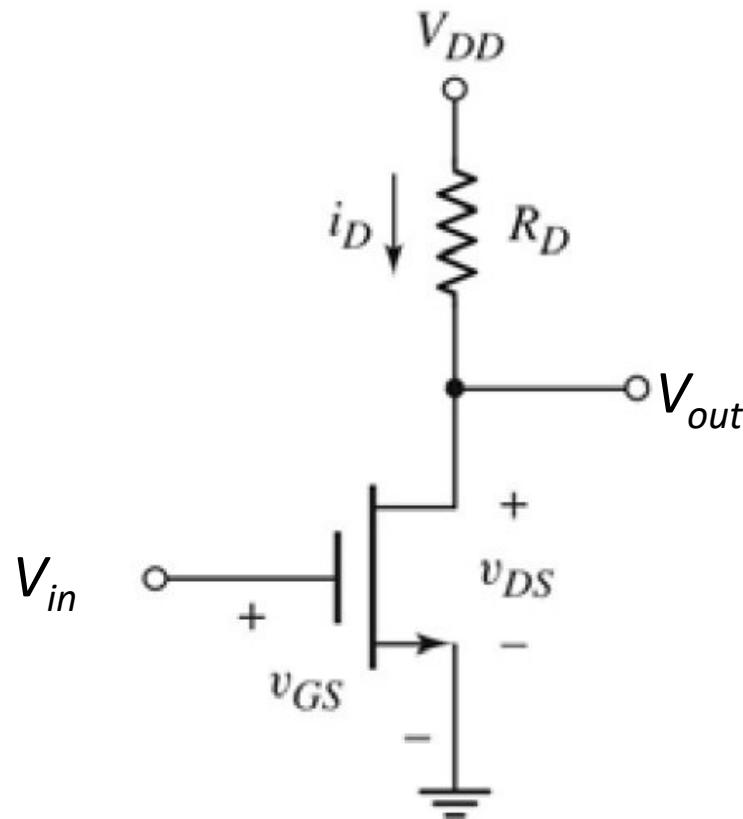
Outline

- CMOS Inverter
- Noise Margin
- CMOS scaling
- Impact of Scaling on different CMOS parameters
- Scaling Challenges

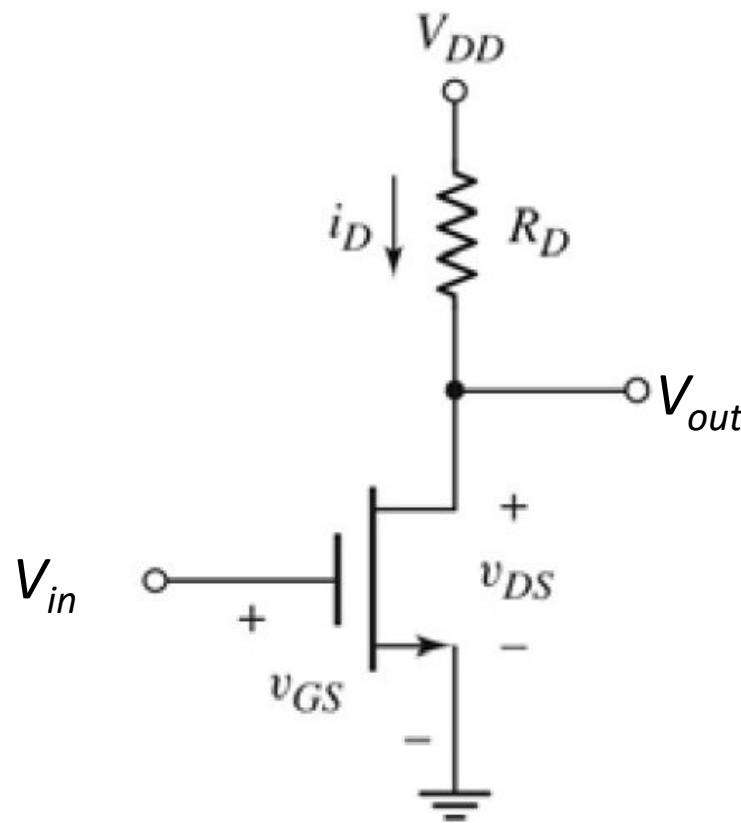
Review of MOSFETs- Linear Region



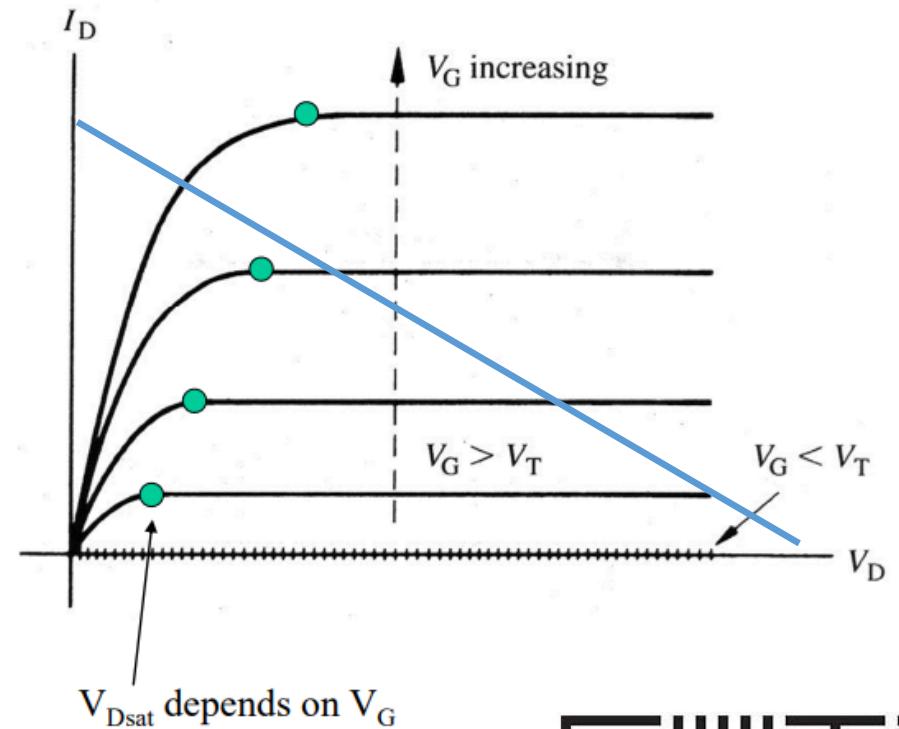
Review of MOSFETs: DC load line of n-MOSFET



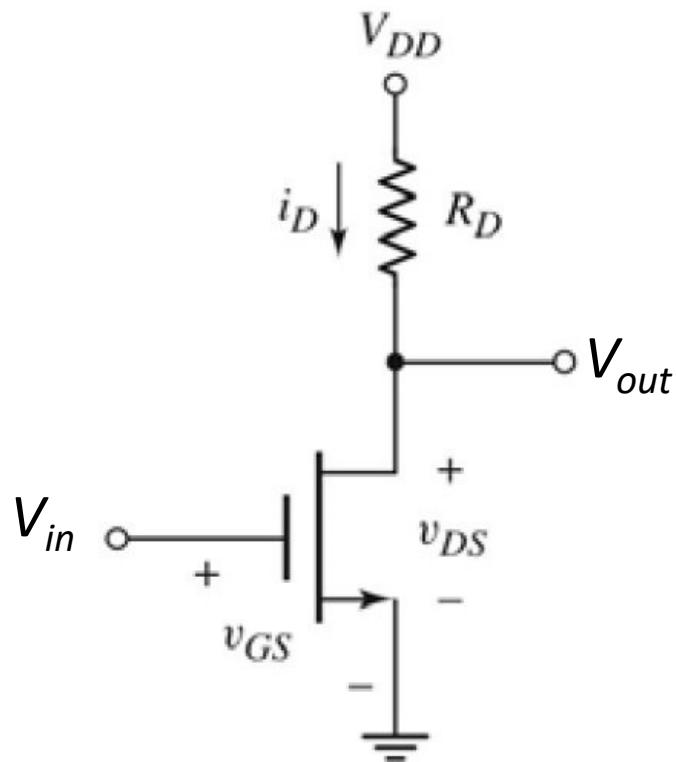
Review of MOSFETs: DC load line of n-MOSFET



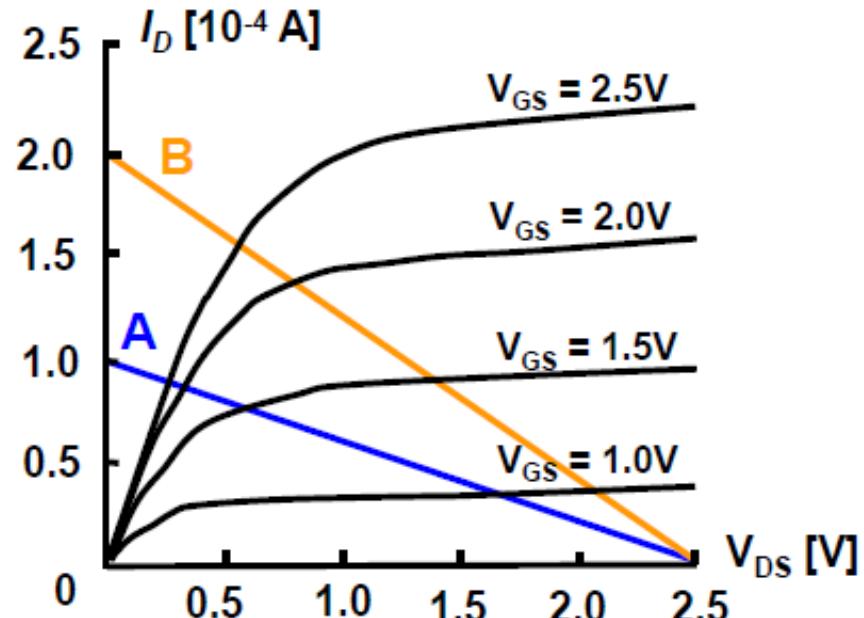
I_D - V_{DS} curves for various V_{GS} :



Review of MOSFETs: DC load line of n-MOSFET

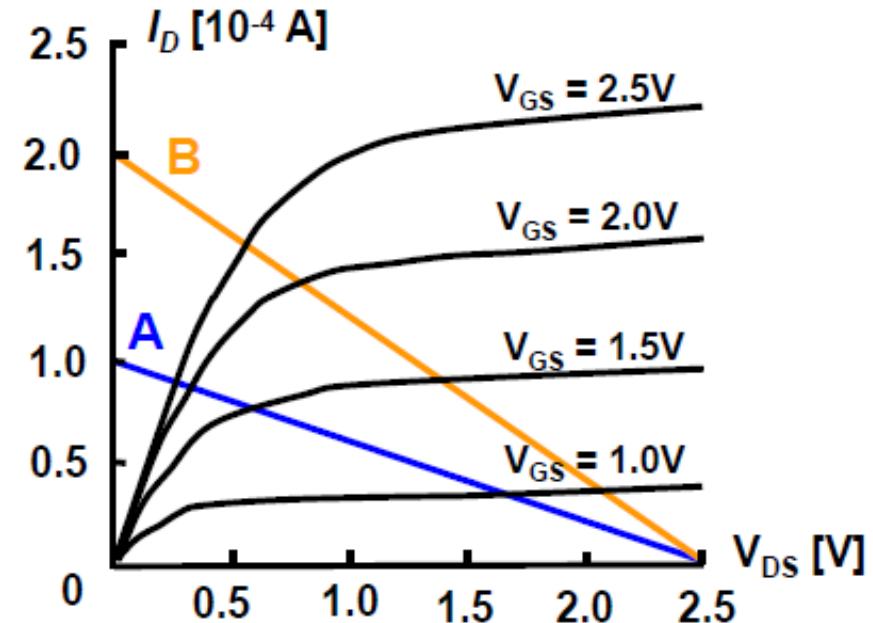
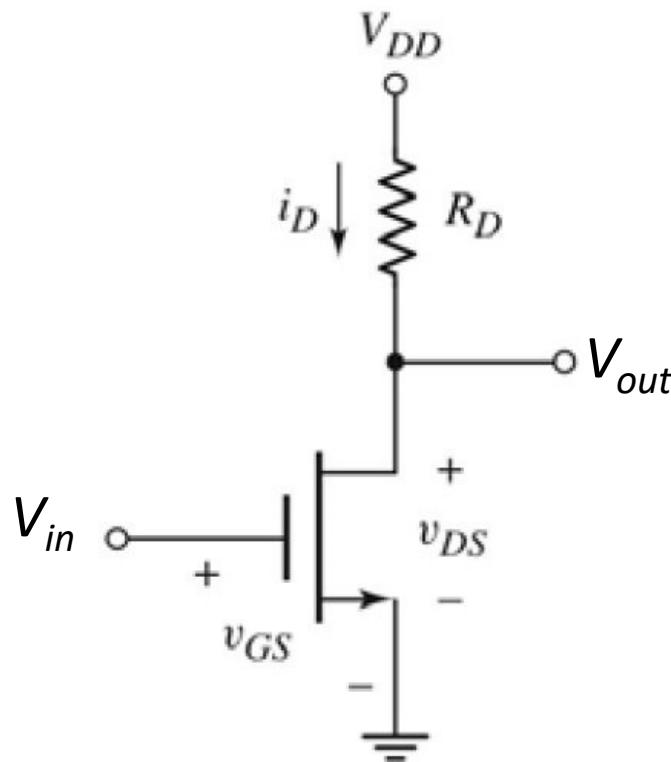


Load Line (Ckt Theory)



Review of MOSFETs: DC load line of n-MOSFET

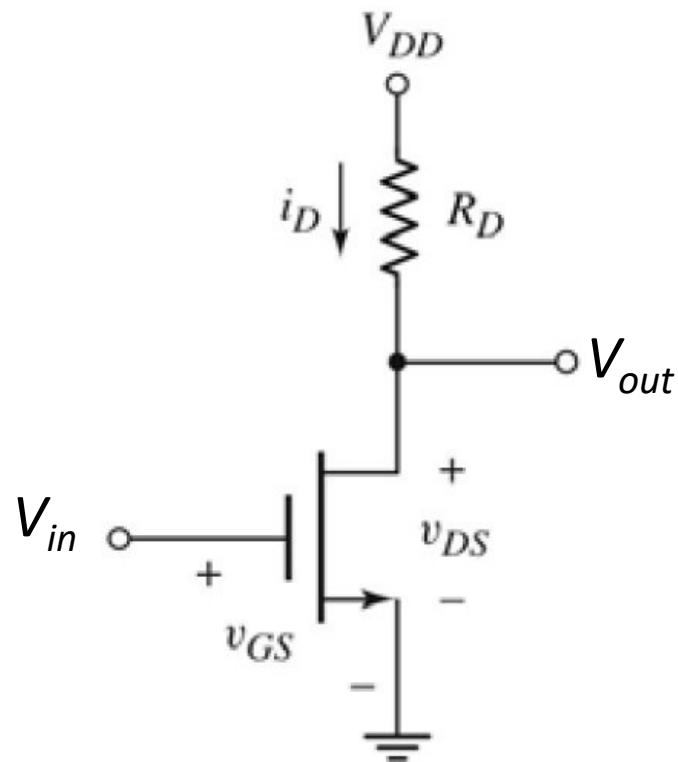
Load Line (Ckt Theory)



As R_D increases the DC Load line Shifts from B to A

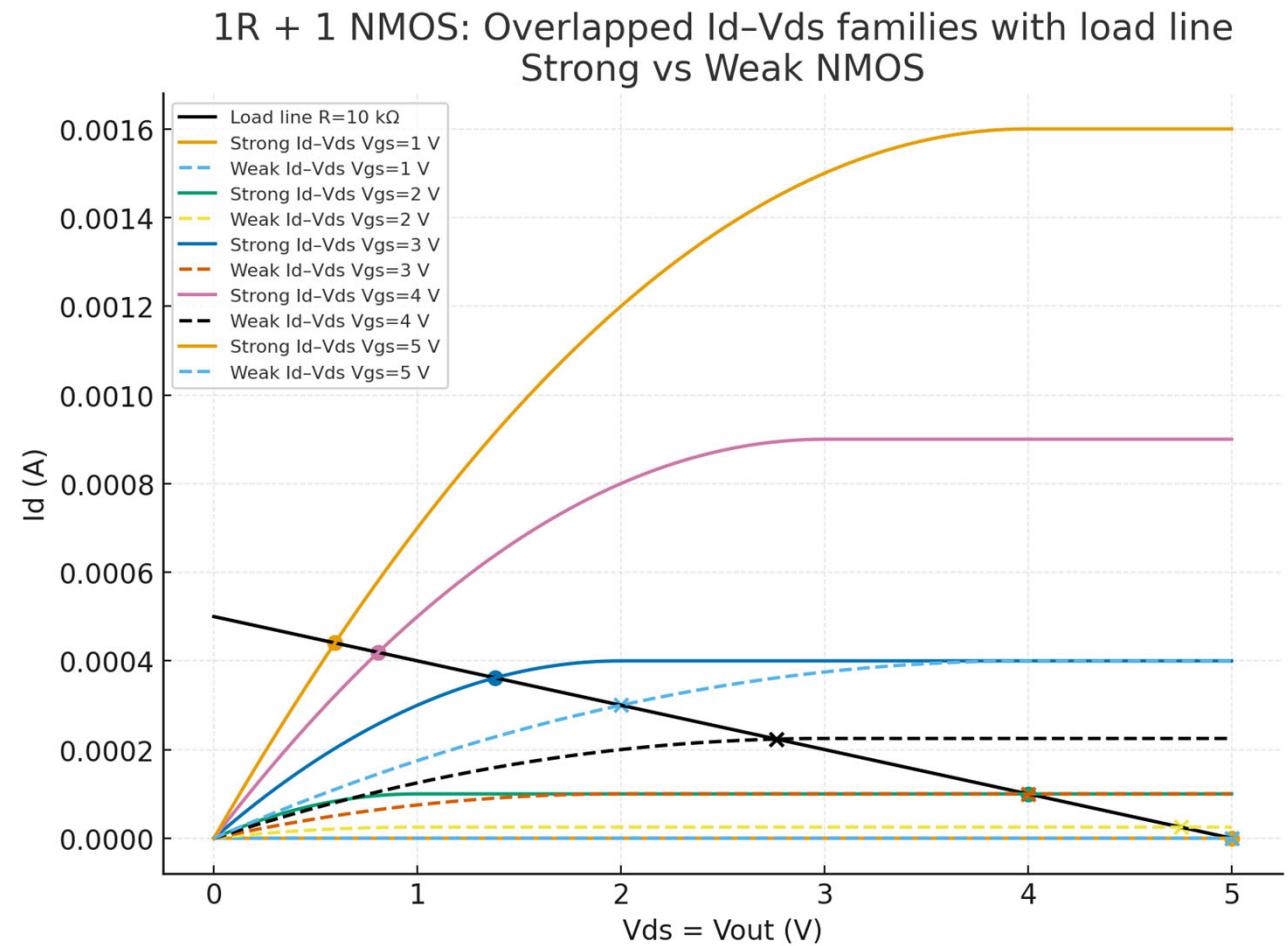
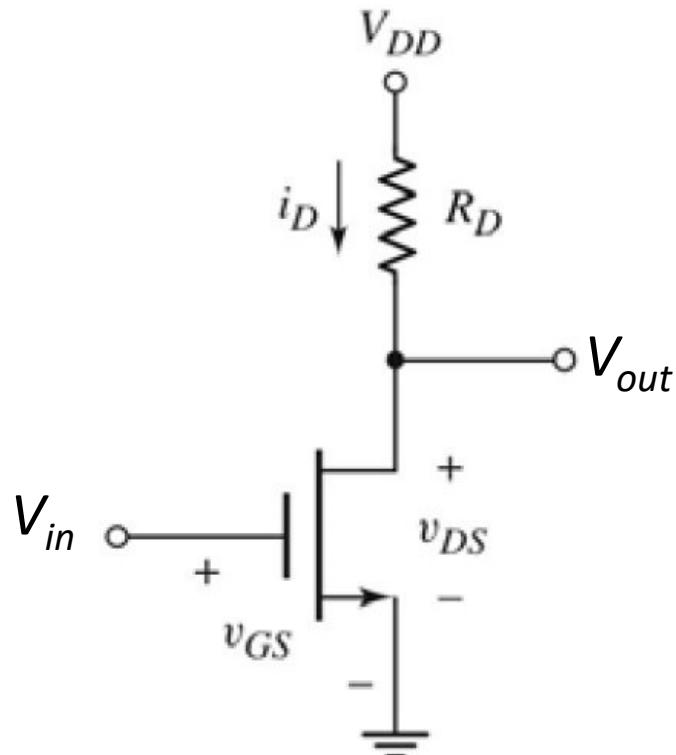
MOSFETs: DC load line of n-MOSFET

(Strong NMOS and Weak NMOS)



MOSFETs: DC load line of n-MOSFET

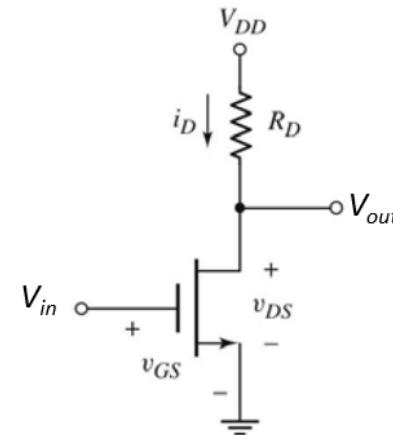
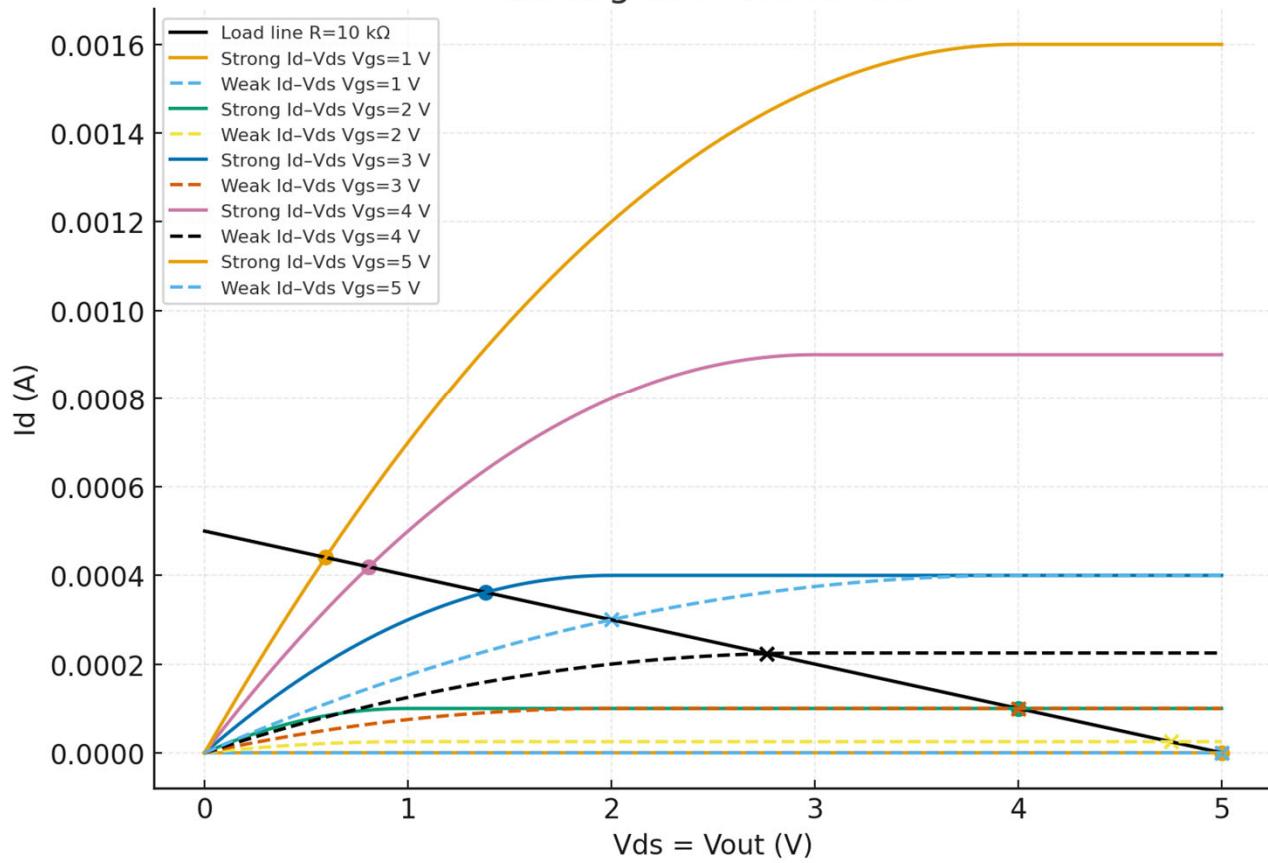
(Strong NMOS and Weak NMOS)



MOSFETs: DC load line of n-MOSFET

(Strong NMOS and Weak NMOS)

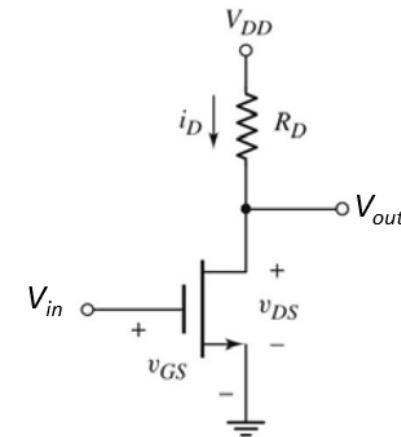
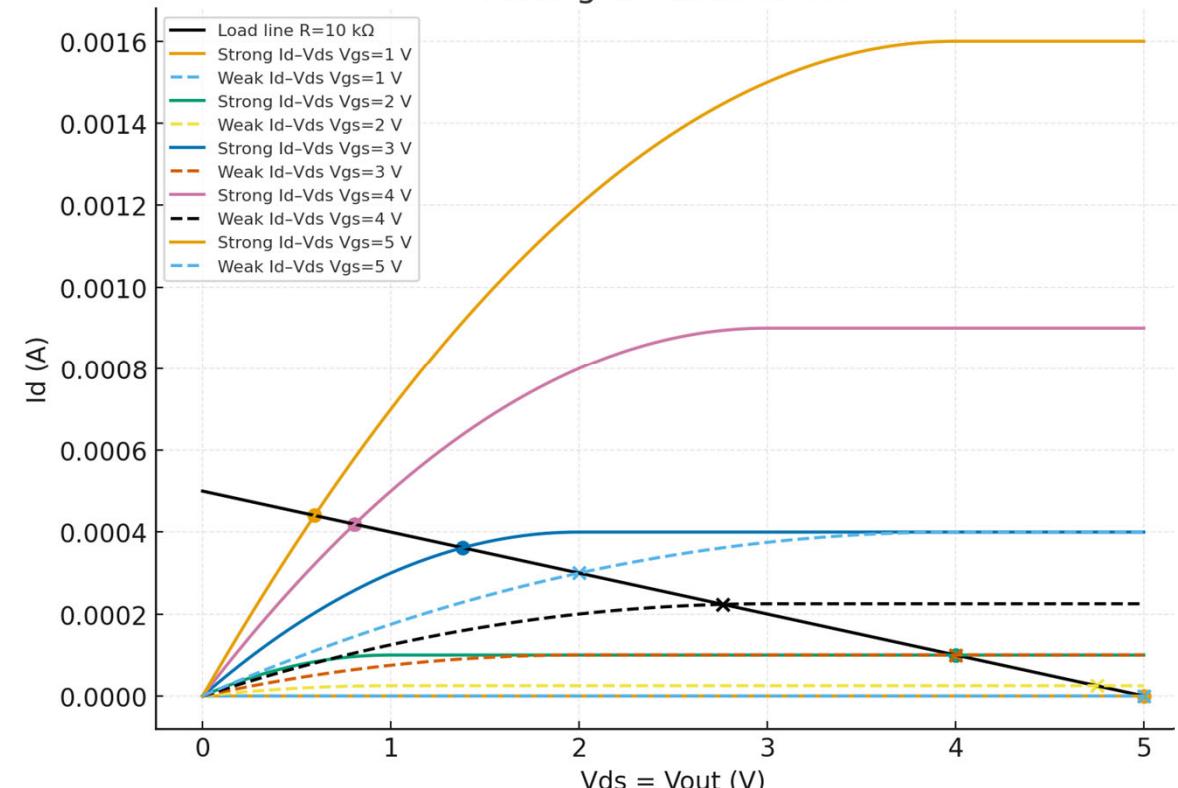
1R + 1 NMOS: Overlapped Id-Vds families with load line
Strong vs Weak NMOS



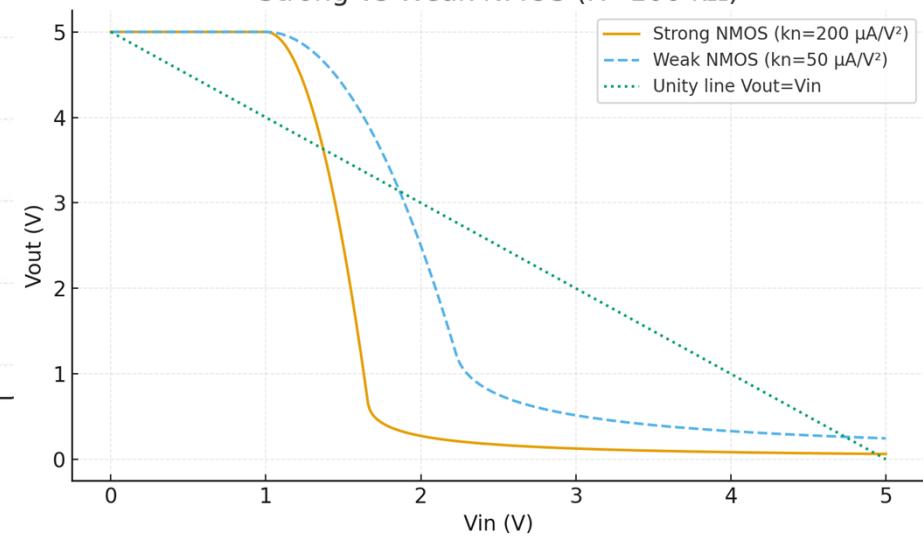
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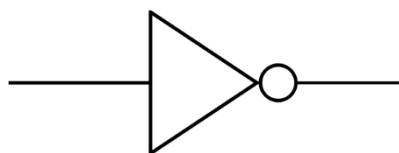
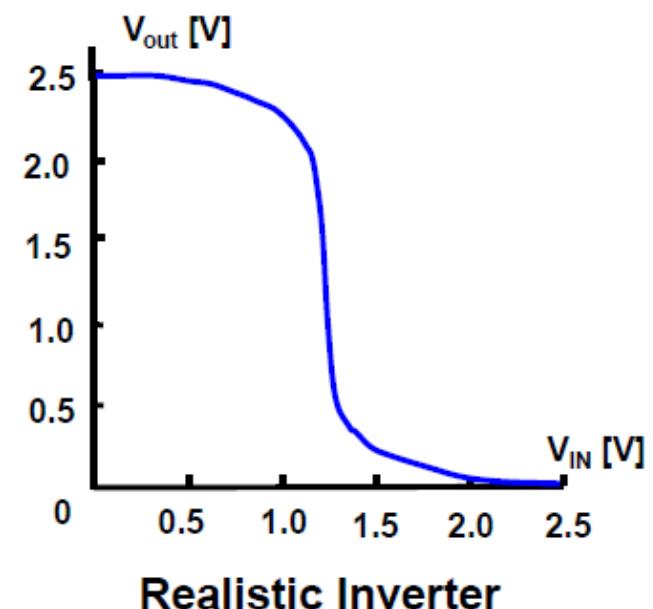
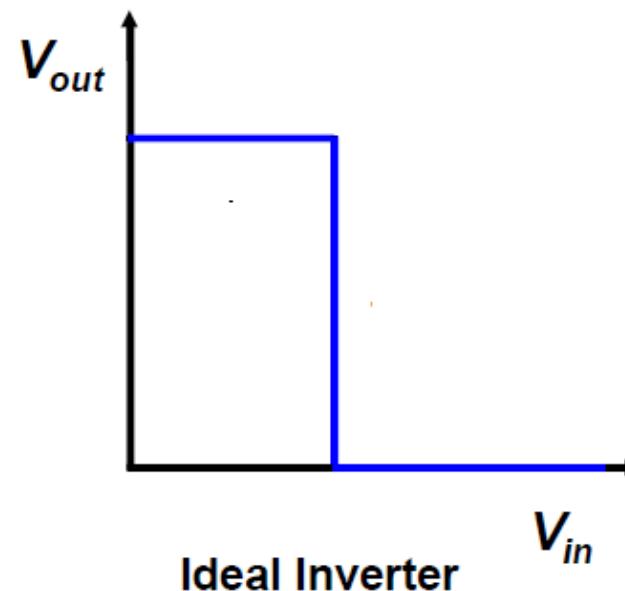
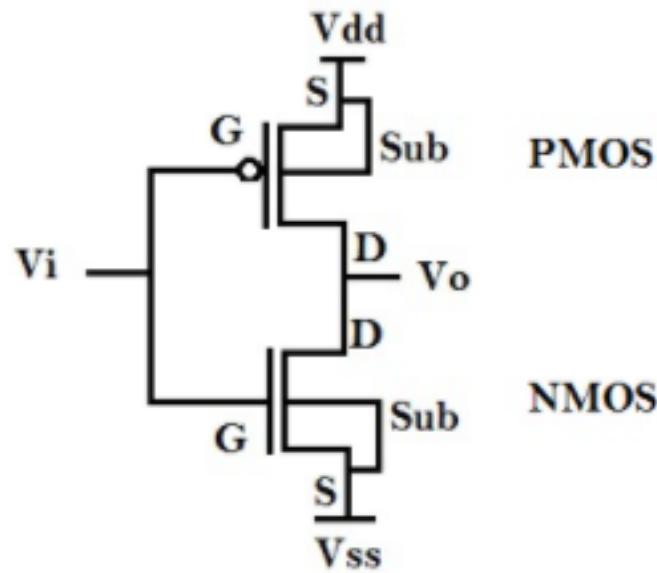


1R + 1 NMOS Inverter Transfer Characteristics
Strong vs Weak NMOS ($R=100 \text{ k}\Omega$)

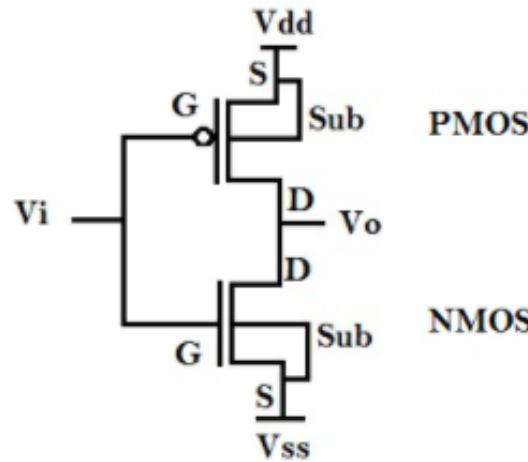


CMOS circuit

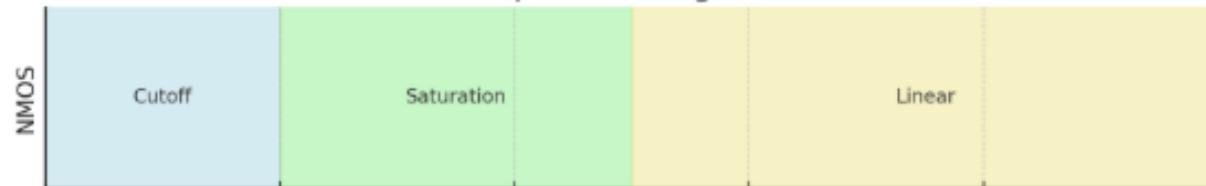
The Realistic Inverter



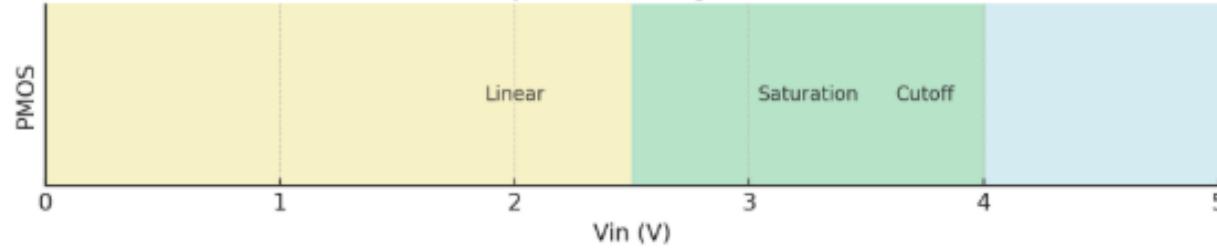
CMOS circuit



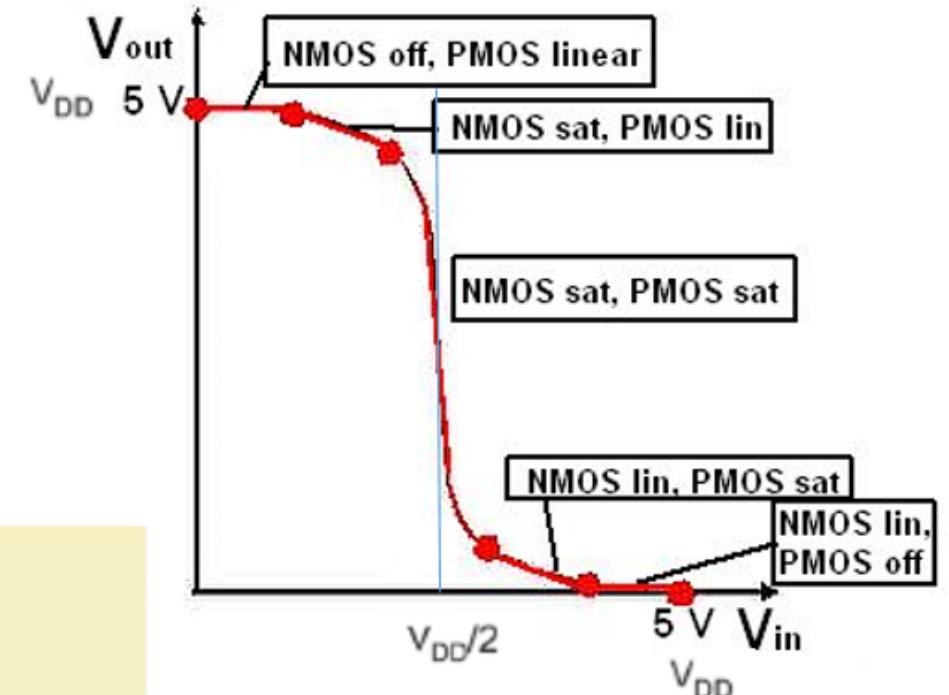
NMOS Operation Regions vs V_{in}



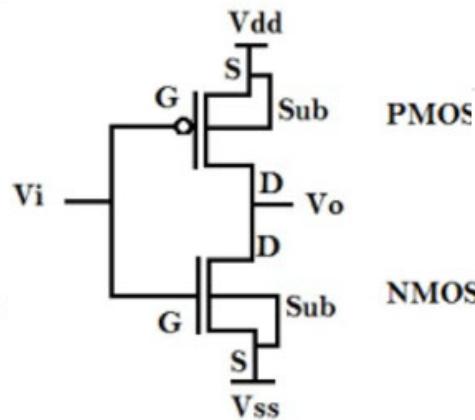
PMOS Operation Regions vs V_{in}



CMOS inverter transfer function

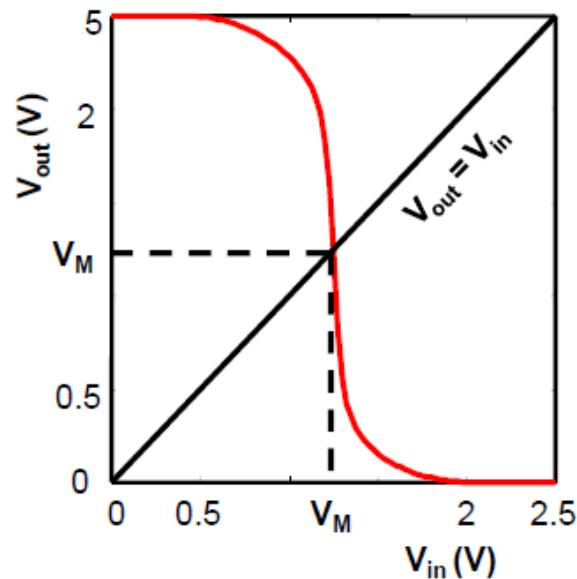


CMOS circuit



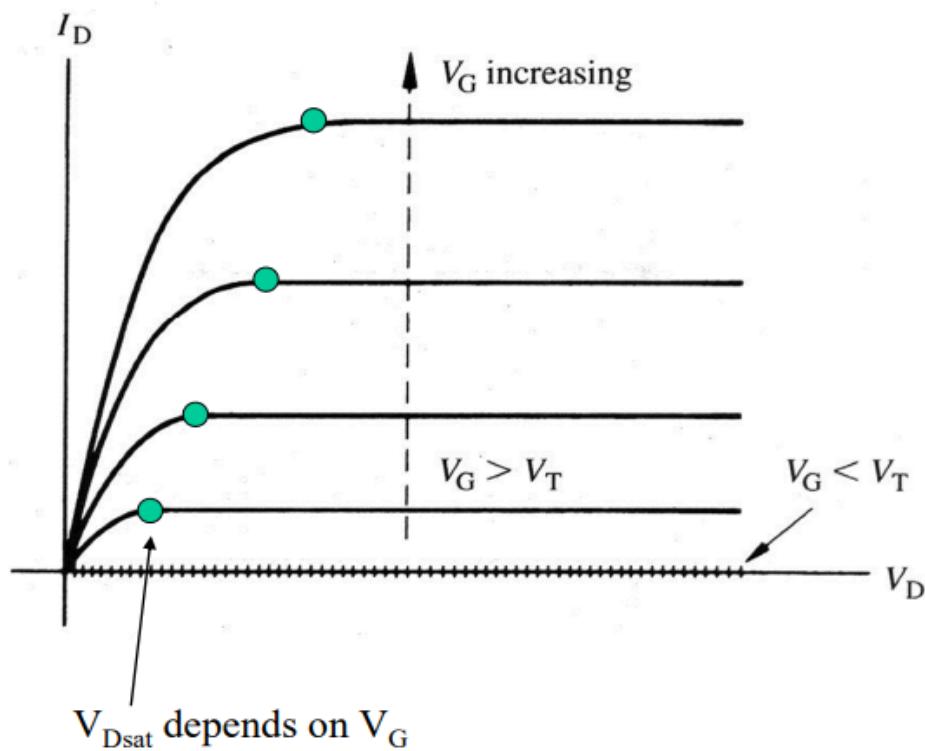
$$V_m = \frac{\sqrt{\beta_p} (V_{DD} - |V_{tp}|) + \sqrt{\beta_n} V_{tn}}{\sqrt{\beta_n} + \sqrt{\beta_p}}$$

- If $\beta_n = \beta_p$, the inverter is "balanced" and $V_m \approx \frac{V_{DD} + V_{tn} - |V_{tp}|}{2}$.
- Skewing transistor sizing (W/L) shifts V_m left or right.



Review of MOSFETs

I_D - V_{DS} curves for various V_{GS} :

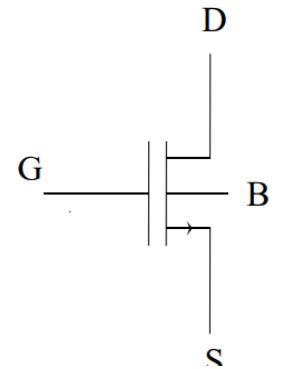


$$\beta = \mu C_{ox} \frac{W}{L}$$

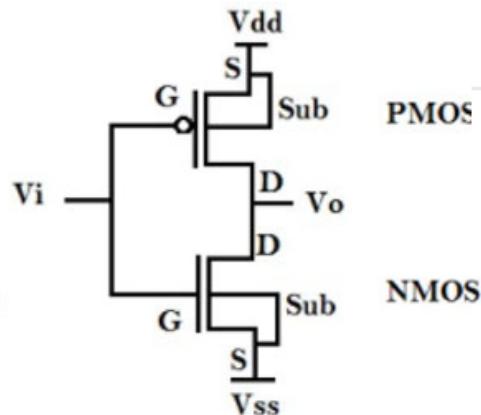
$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \end{cases}$$

cutoff linear saturation

n-channel MOS
Transistor

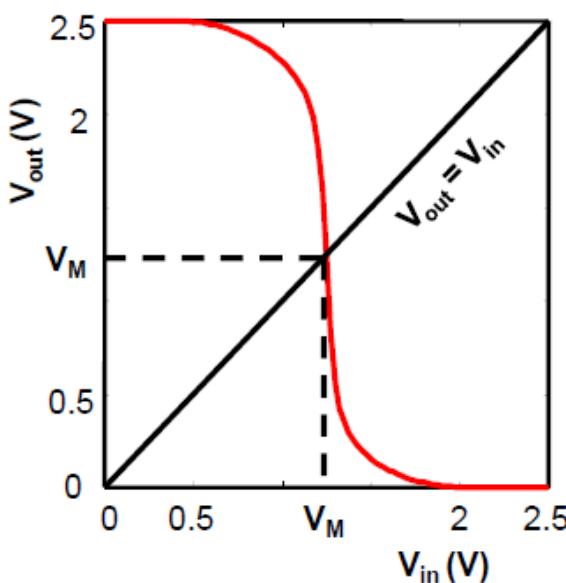


CMOS circuit



$$V_m = \frac{\sqrt{\beta_p} (V_{DD} - |V_{tp}|) + \sqrt{\beta_n} V_{tn}}{\sqrt{\beta_n} + \sqrt{\beta_p}}$$

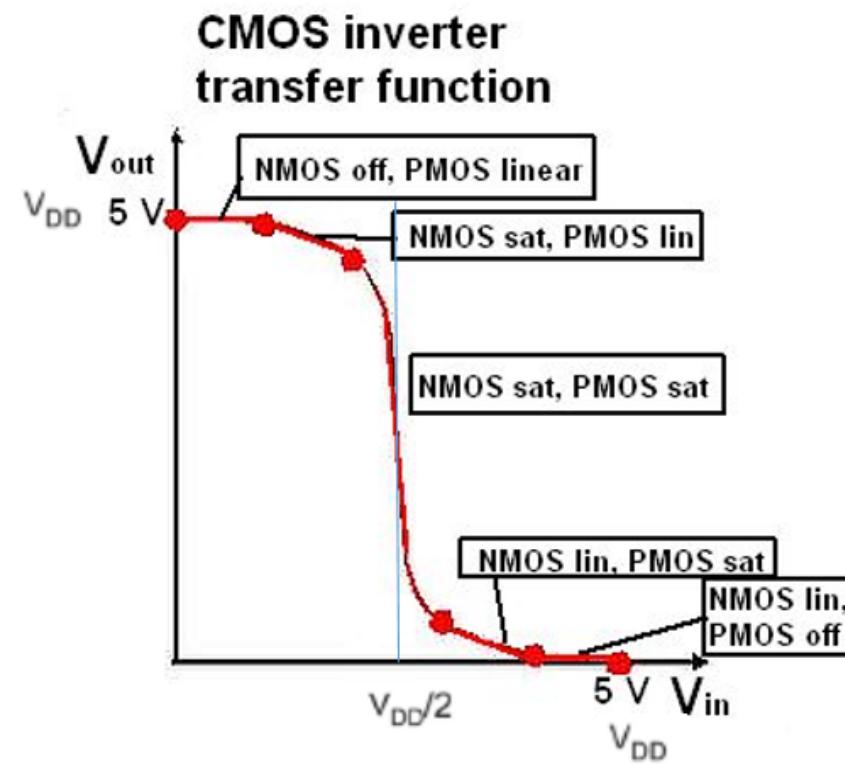
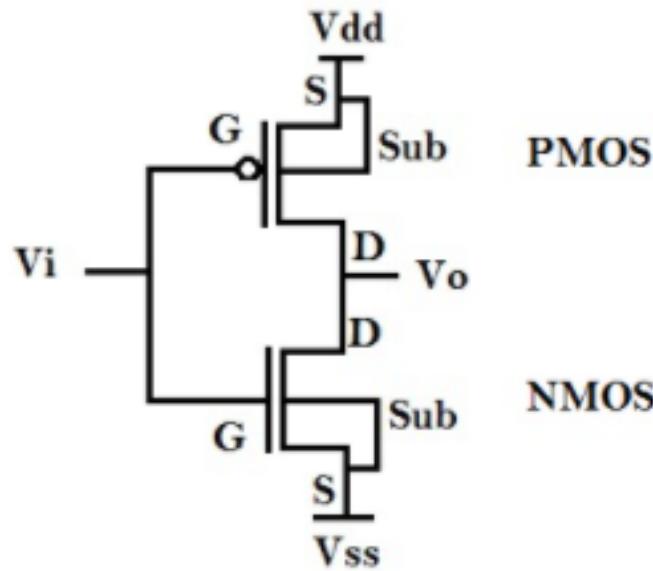
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- Skewing transistor sizing (W/L) shifts V_m left or right.



With equal lengths and typical mobility ratio $\mu_n / \mu_p \approx 2 - 3$,
you often choose $W_p \approx 2 - 3 W_n$ to center V_m

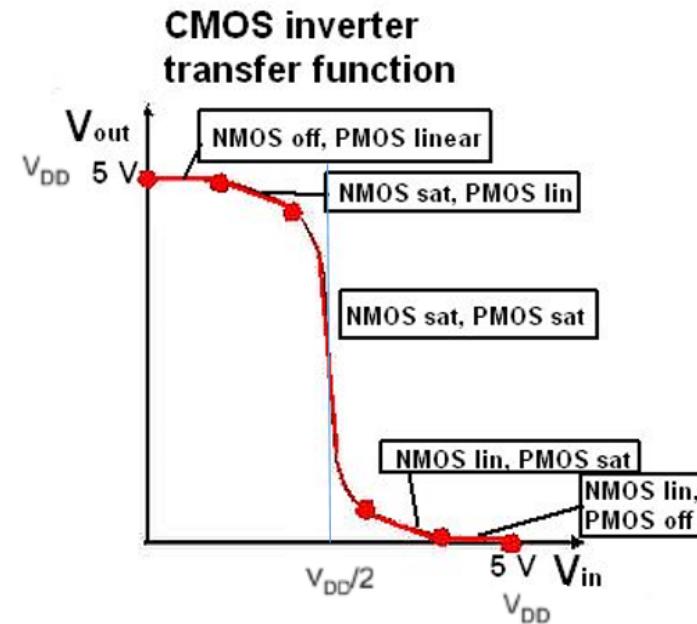
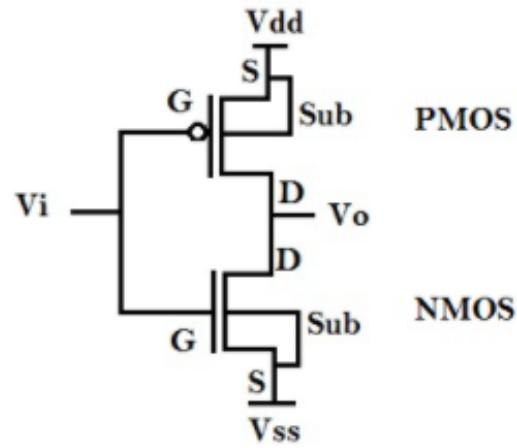
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CMOS circuit



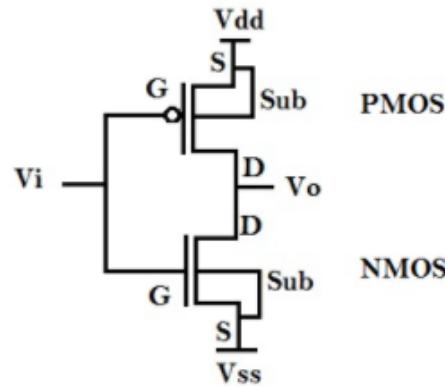
Impact of Strong NMOS and Weak NMOS on Transfer function?

CMOS circuit

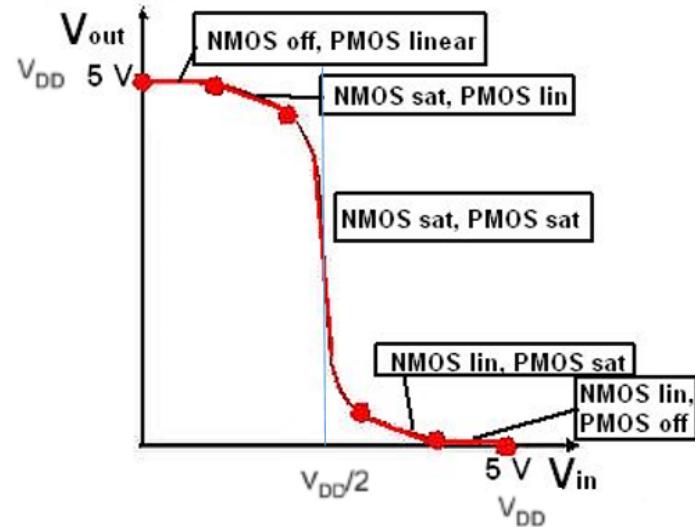


Impact of Strong NMOS and Weak NMOS on Transfer function?

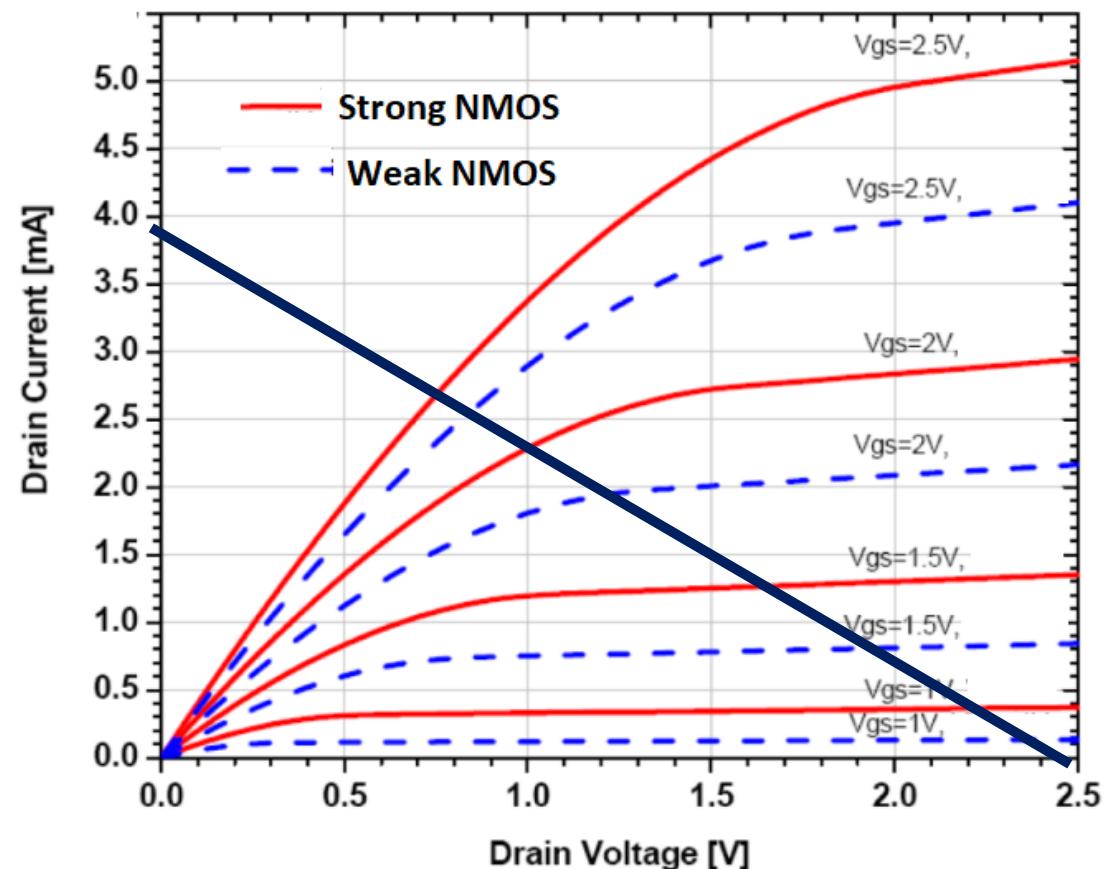
CMOS circuit



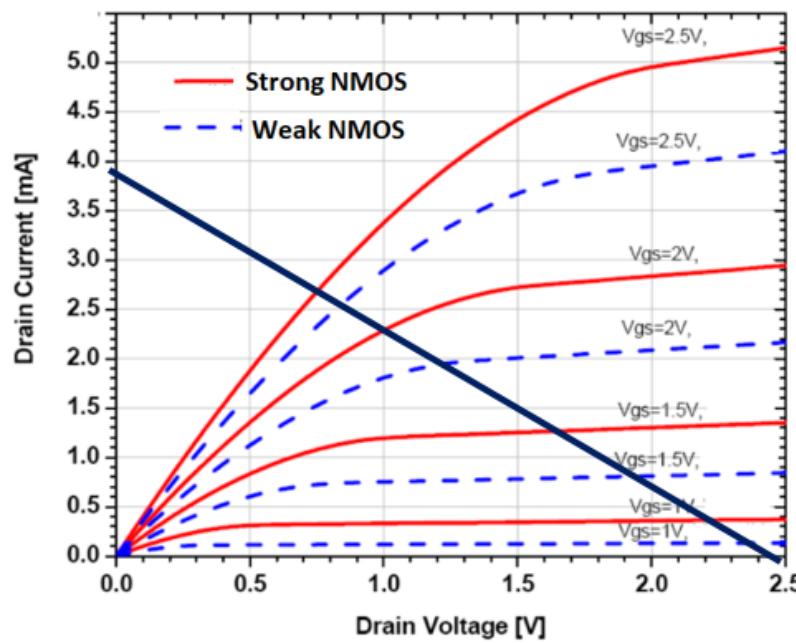
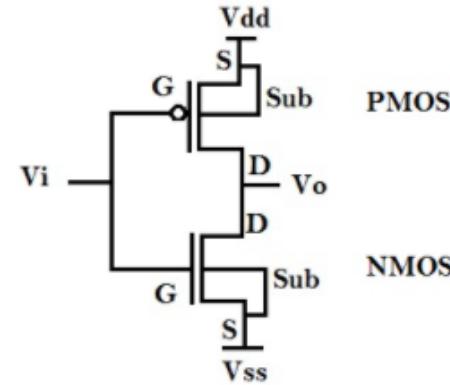
CMOS inverter transfer function



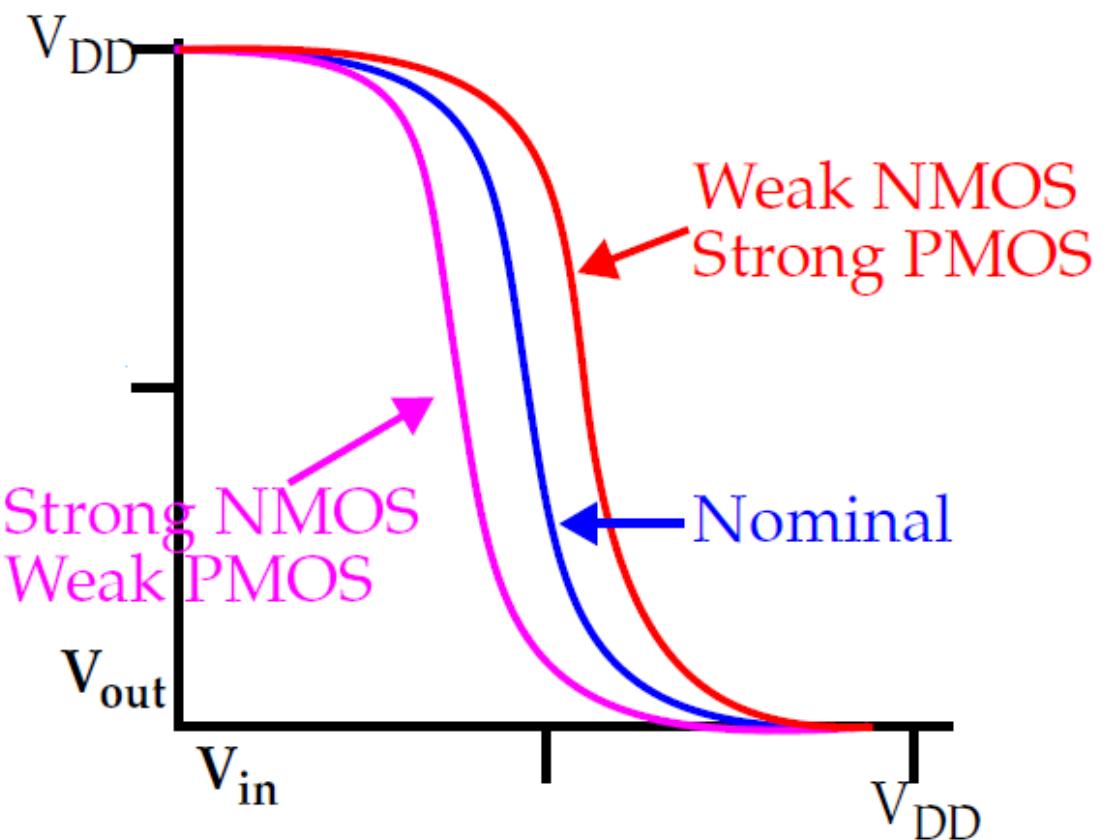
Strong NMOS and Weak NMOS



CMOS circuit

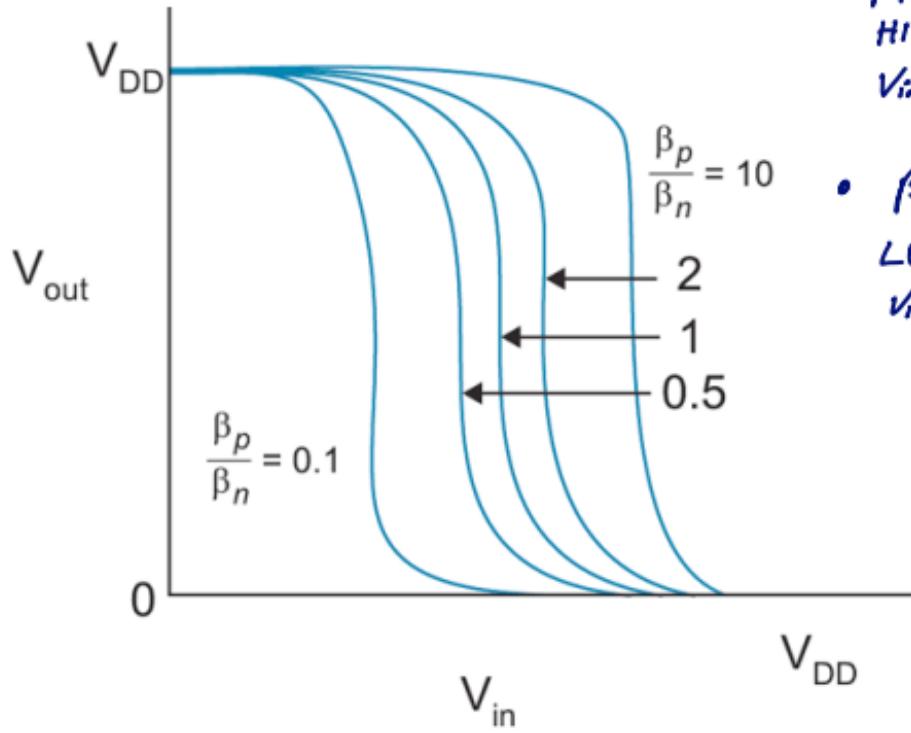


NMOS and PMOS- variation

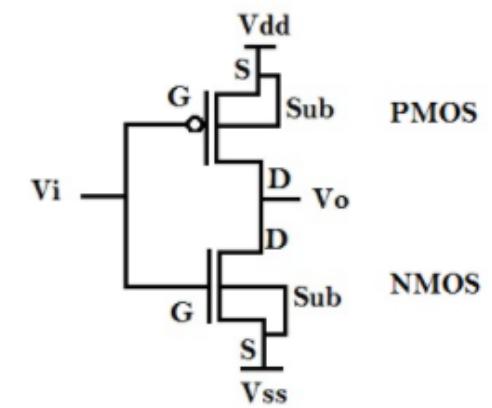


CMOS circuit

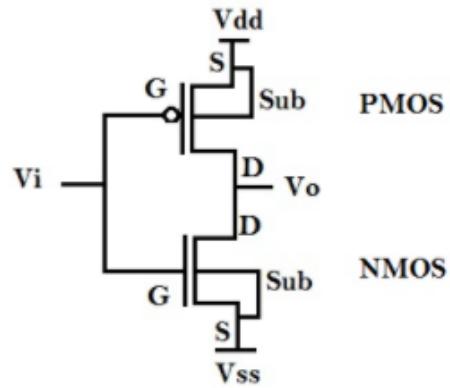
If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$



- $\beta_p > \beta_n$
HIGH SKEWED inverter
 $V_{in} = \frac{V_{DD}}{2} \rightarrow V_{out} > \frac{V_{DD}}{2}$
- $\beta_p < \beta_n$
LOW SKEWED inverter
 $V_{in} = \frac{V_{DD}}{2} \rightarrow V_{out} < \frac{V_{DD}}{2}$

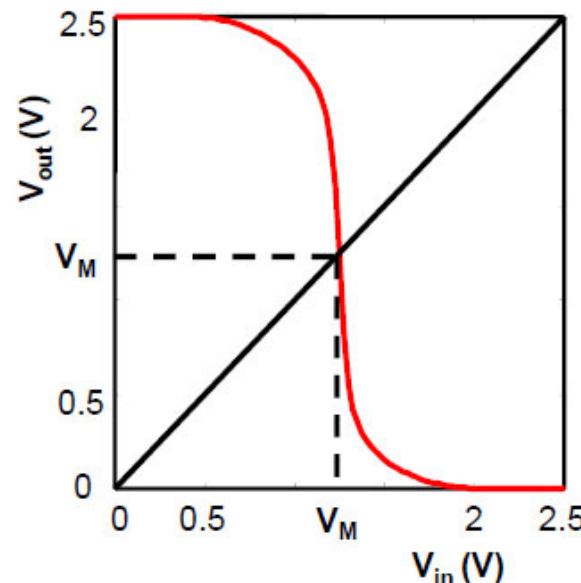


CMOS circuit

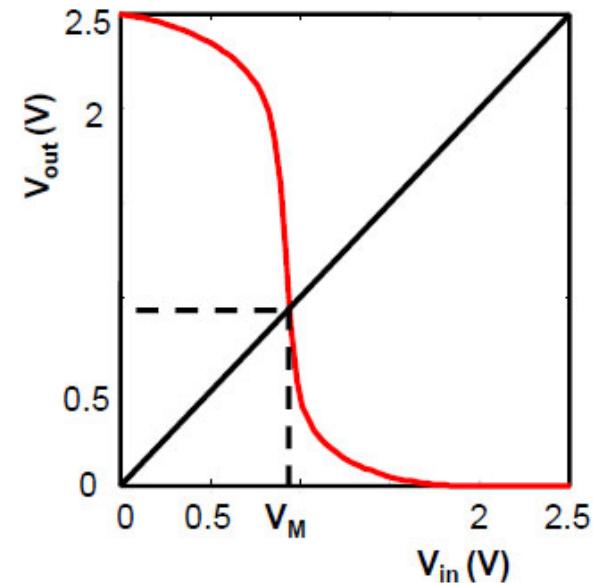


$$V_m = \frac{\sqrt{\beta_p} (V_{DD} - |V_{tp}|) + \sqrt{\beta_n} V_{tn}}{\sqrt{\beta_n} + \sqrt{\beta_p}}$$

Stronger NMOS



Balanced NMOS and PMOS sizes



Strong NMOS, Weak PMOS

CMOS circuit: Noise Margin

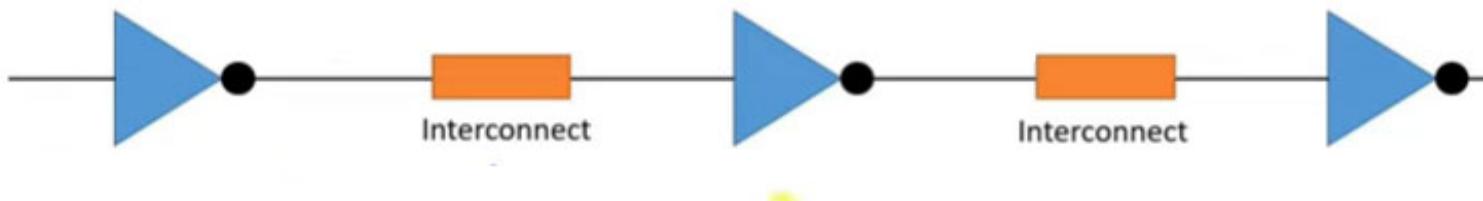
- Noise margin is the ratio by which the signal exceeds the minimum acceptable amount.
- It explains up to what extent IC allows noise in the transmission of logic '0' and logic '1'.
- Logic '0' and '1' – represent the range of input values
- Hence, for error free digital signal transmission noise margin is required

CMOS circuit: Noise Margin

- **Noise margin** refers to how much unwanted noise (disturbance in voltage levels) a circuit can tolerate without misinterpreting logic levels. It essentially defines the safety “buffer” between valid logic-0 and logic-1 signals.
- Noise margin is critical in digital IC design because it ensures reliable operation in the presence of crosstalk, supply fluctuations, or electromagnetic interference.
- Higher VDD gives bigger absolute noise margins, but modern technology scales VDD down, so circuit design must ensure sufficient margins.

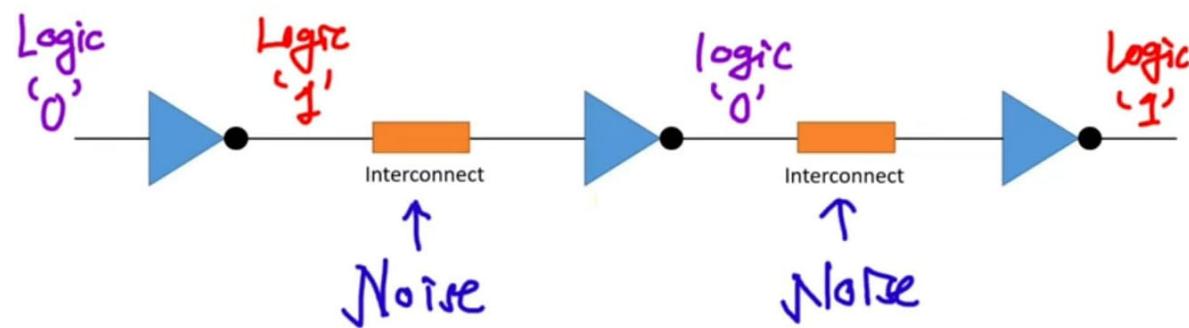
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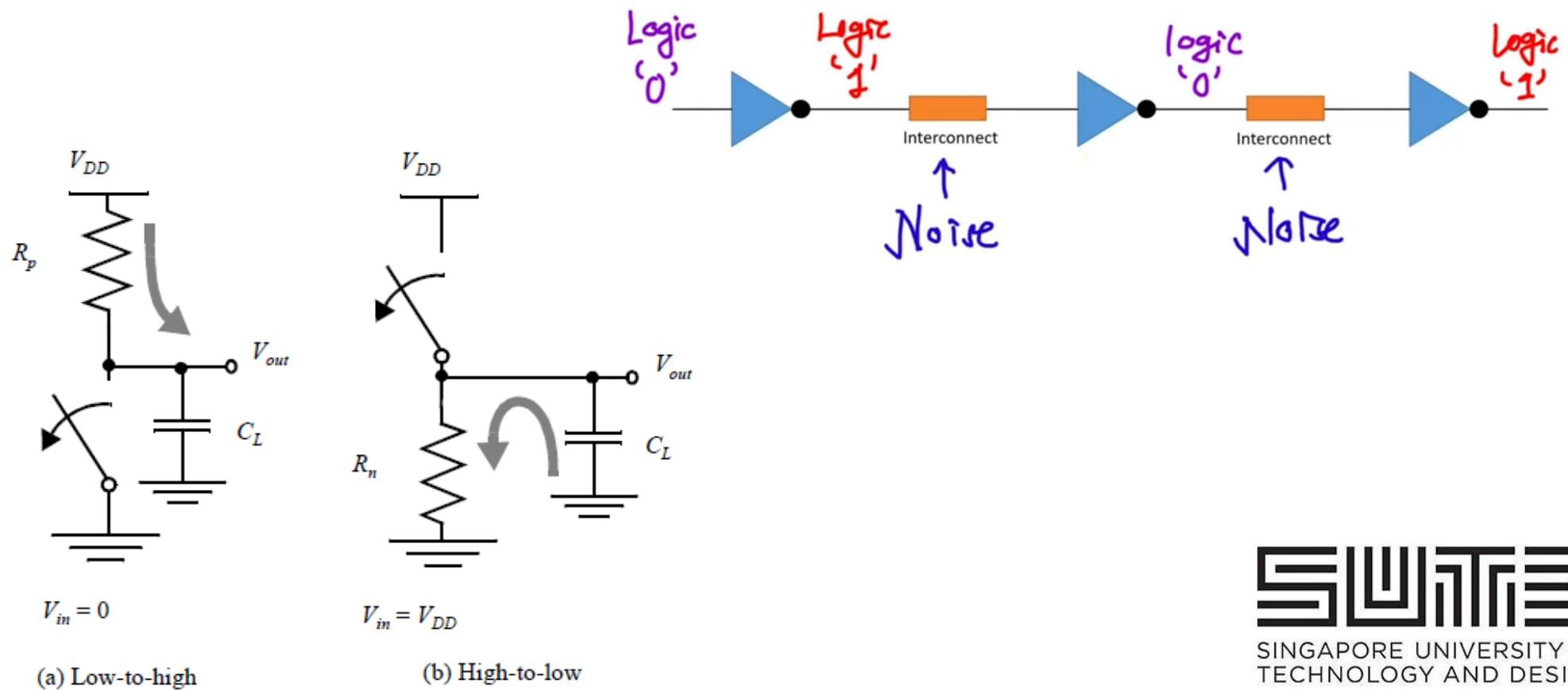
CMOS circuit: Noise Margin

- Hence, for error free digital signal transmission noise margin is required

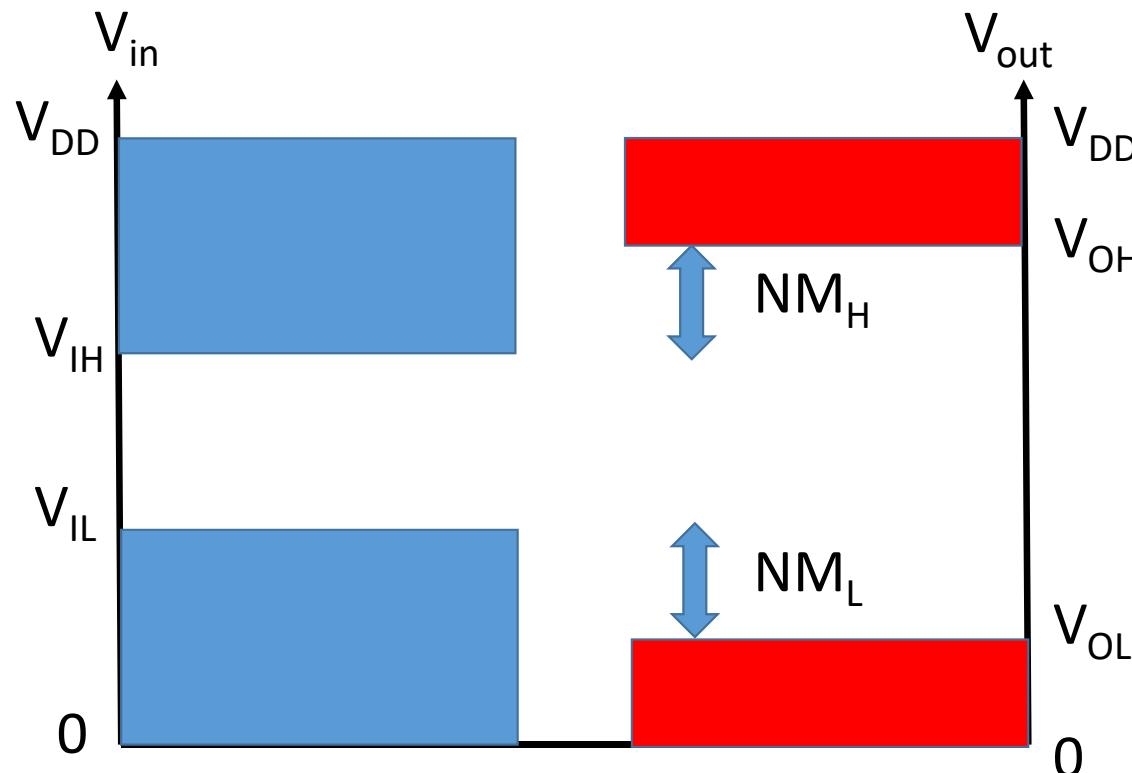


CMOS circuit: Noise Margin

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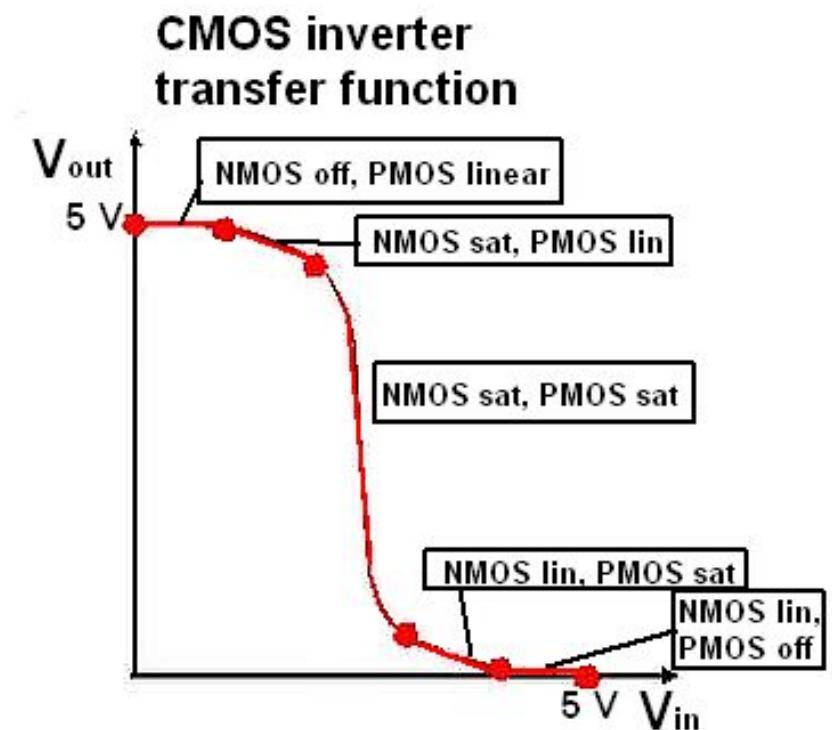


CMOS circuit: Noise Margin

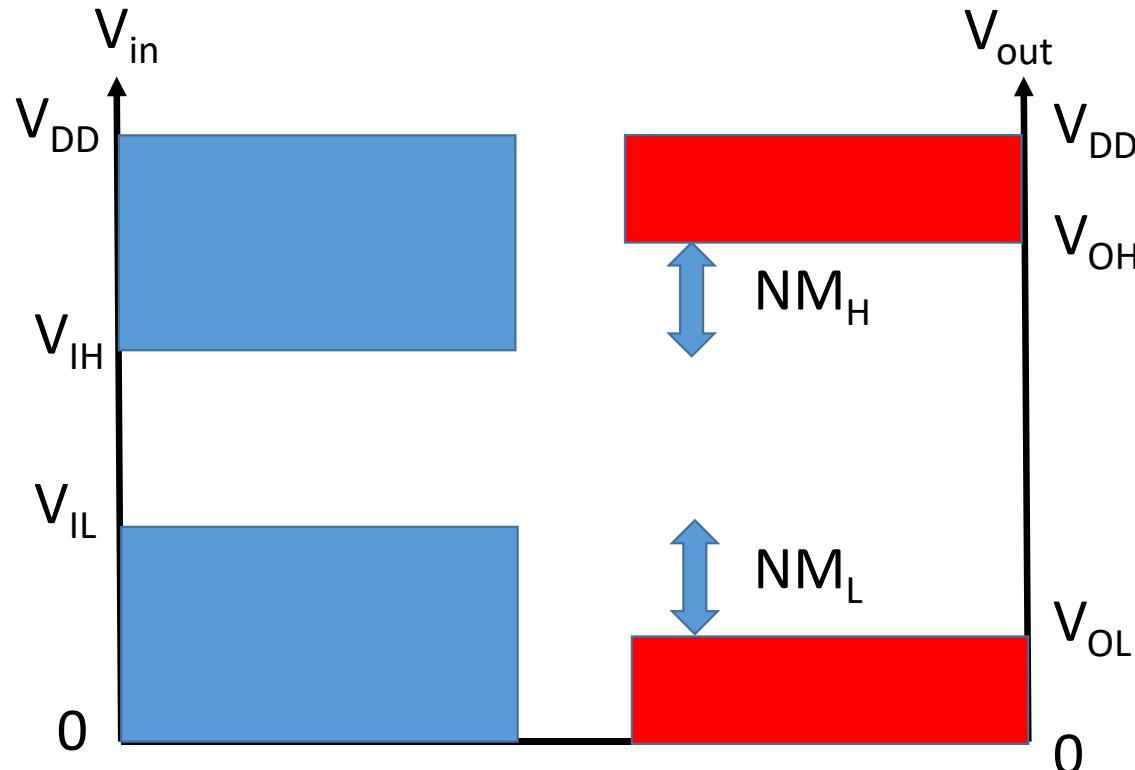


$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$



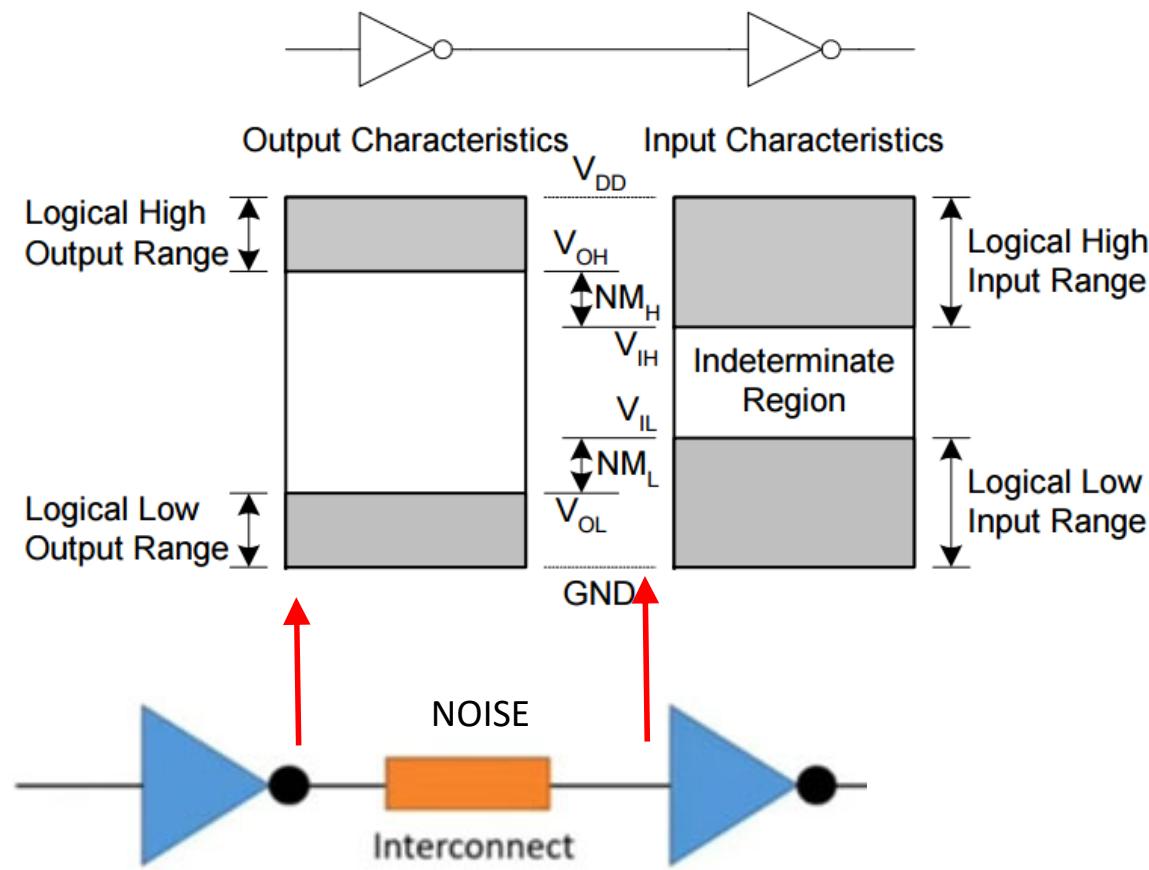
CMOS circuit: Noise Margin



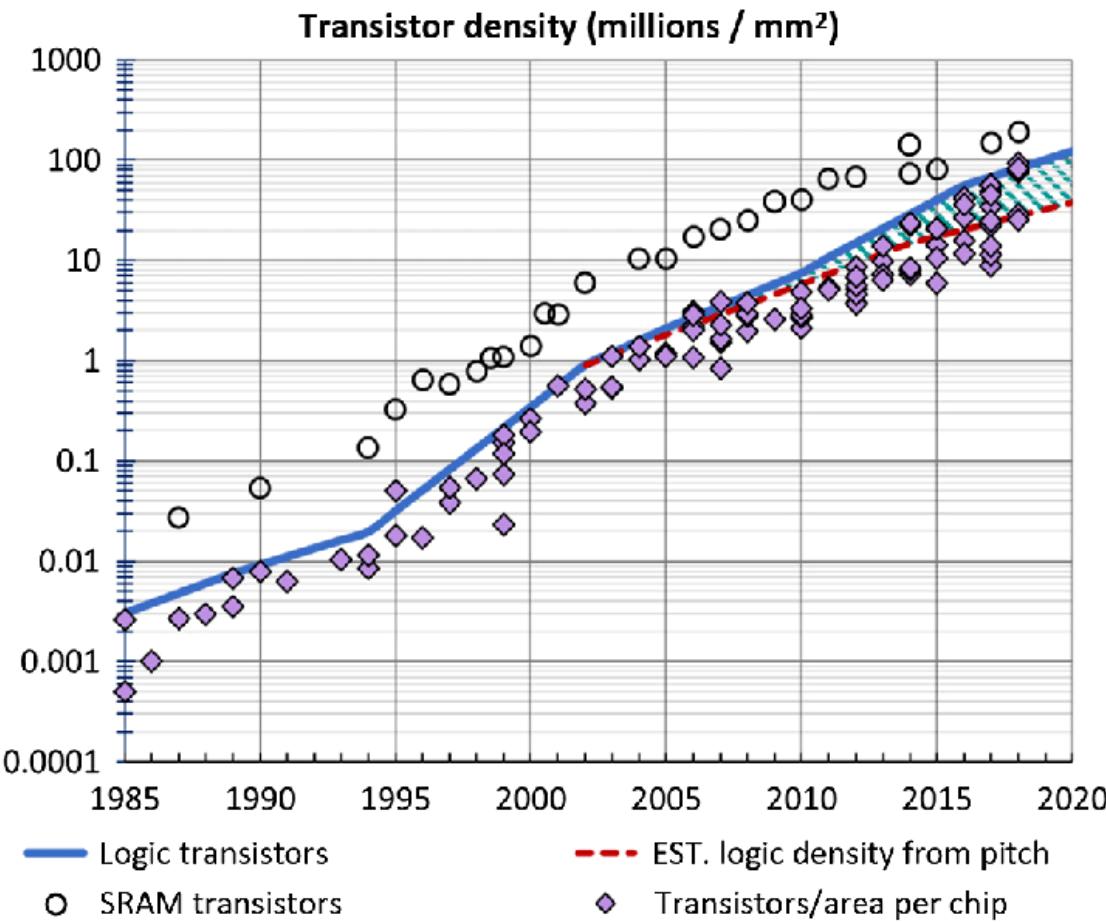
$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

CMOS circuit: Noise Margin



CMOS scaling: Moore's Law

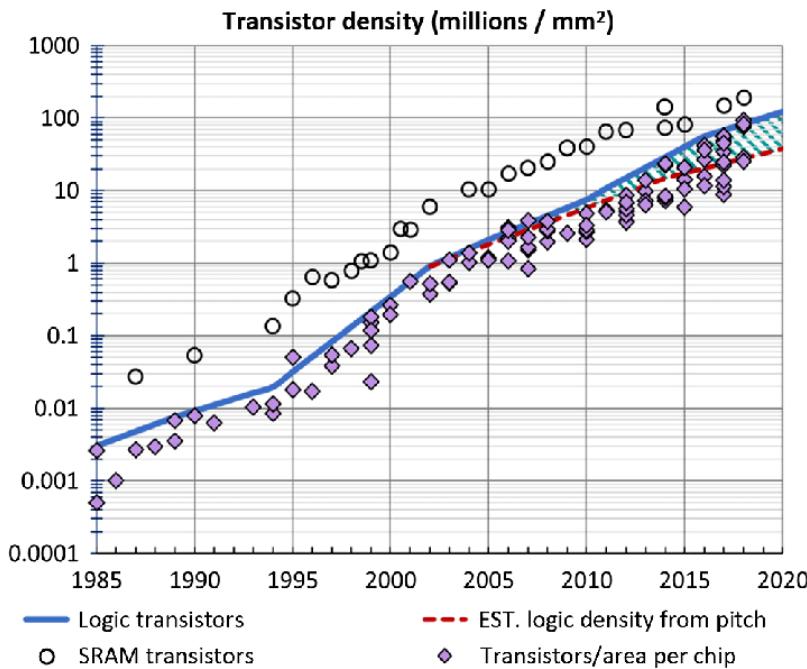


Moore's law says that the number of transistors doubles approximately every two years.

- CMOS scaling
 - Speed
 - High density
 - Less power
 - Reduced cost/transistor

Ref: M. L. Rieger, "Retrospective on VLSI value scaling and lithography" Journal of Micro/Nanolithography-2019

CMOS scaling: Dennard's scaling

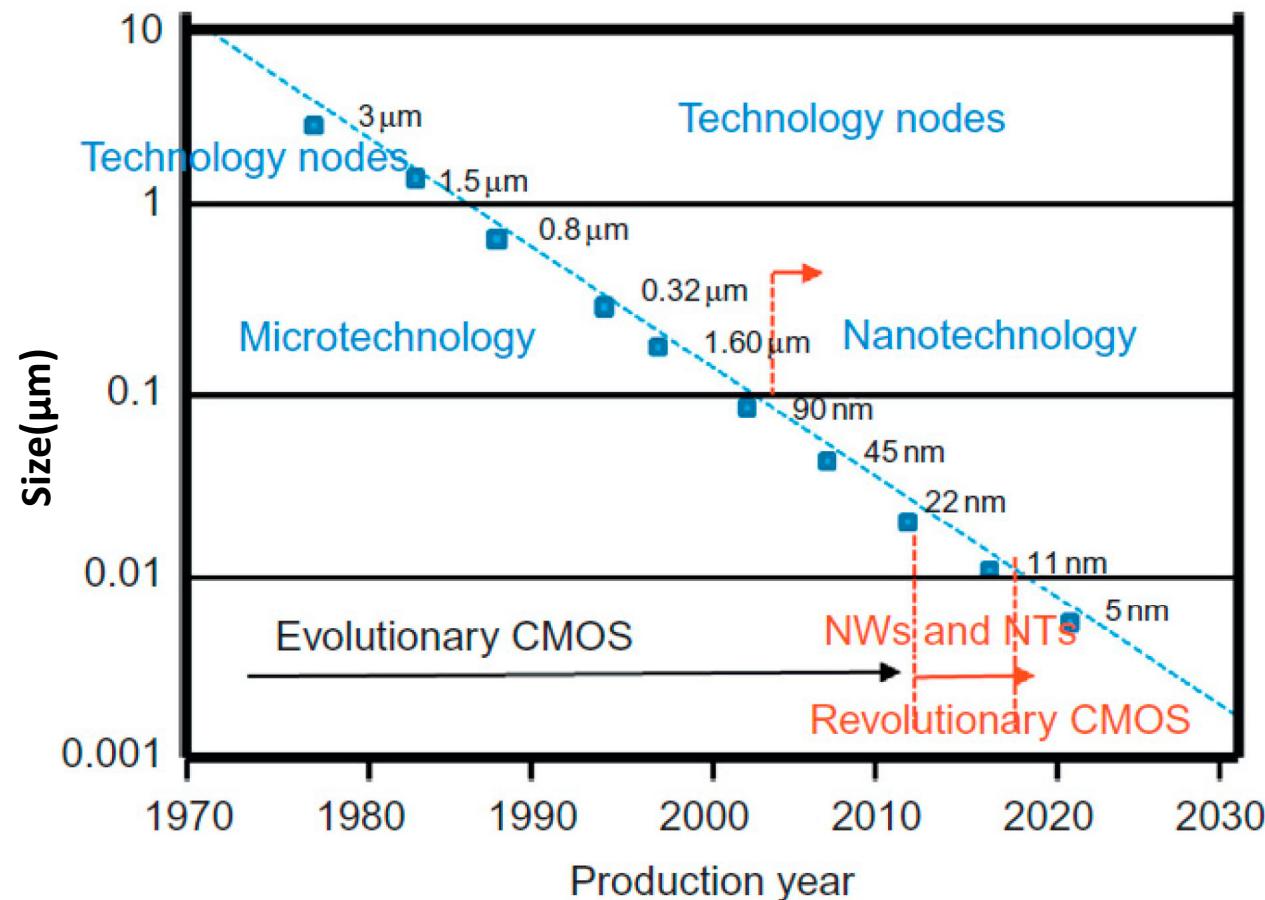


Dennard scaling, also known as MOSFET scaling, is a scaling law which states roughly that, as transistors get smaller, their power density stays constant, so that the power use stays in proportion with area; both voltage and current scale (downward) with length.

With feature sizes below 65nm, these rules could no longer be sustained, because of the exponential growth of the leakage current.”

Ref: M. L. Rieger, “ Retrospective on VLSI value scaling and lithography” Journal of Micro/Nanolithography-2019

CMOS scaling: Moore's Law



Ref: H. H. Radamson, et al., " Miniaturization of CMOS" Micromachines 10(5) 293-2019

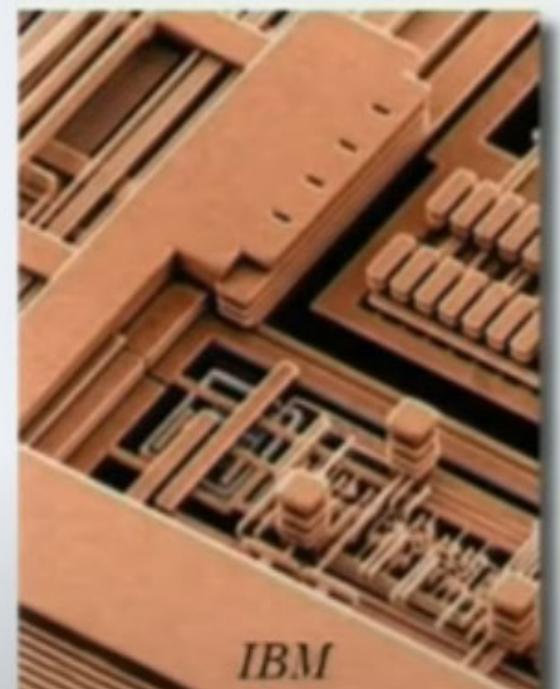
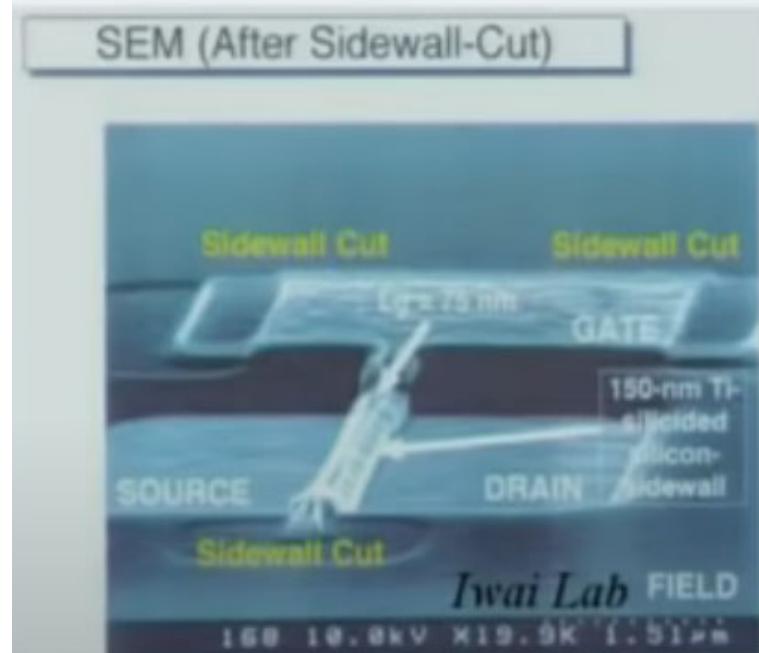
CMOS scaling: ITRS Roadmap

ITRS Projections			
Year of Production	2007	2010	2013
Technology Node (nm)	65	45	32
Transistor Gate Length in Microprocessors circuits (nm)	25	18	13
Wafer diameter (inch)	12	12	18
Number of masks required for fabrication of Microprocessor	33	35	37
Number of Transistors in Microprocessor (billion)	1.1	2.2	4.4
Number of interconnect wiring levels in the Microprocessor	15	16	17

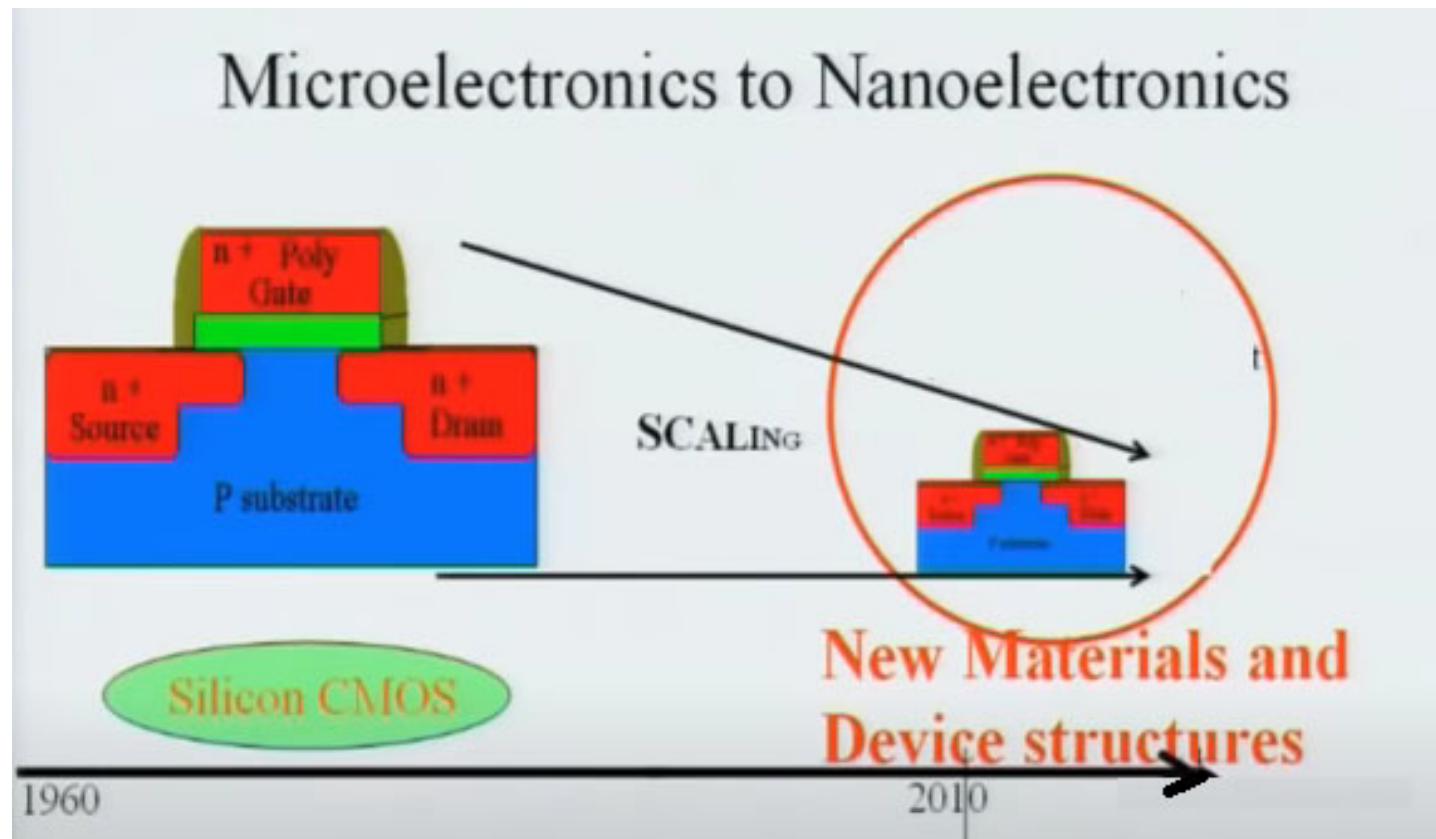
<http://www.itrs2.net/>

CMOS chip

A large ensemble of **transistors** connected “appropriately” through multilevel **metal interconnection** lines...



CMOS scaling



Ref: N. Bhat, CeNSE, IISc Bangalore- Nanoelectronic Device Technology

CMOS scaling:

Micro-MOSFET

Nano-MOSFET

Periodic Table of the Elements

1 IA	H	Hydrogen	1.008	Symbol
2 IA	Li	Lithium	6.94	Atomic Weight
3 IA	Be	Boron	10.81	Electrons per shell
4 IA	Na	Magnesium	24.31	State of matter (color of name)
5 IA	K	Ca	39.10	GAS LIQUID SOLID (colorless)
6 IA	Rb	Sc	85.47	
7 IA	Fr	Ti	45.90	
8 IB	Ca	V	50.94	
9 IB	Sr	Cr	52.00	
10 IB	La	Mn	54.94	
11 IB	Ce	Fe	55.85	
12 IB	Pr	Co	58.93	
13 IIIA	Nd	Ni	58.7	
14 IVB	Pm	Cu	63.55	
15 VB	Sm	Zn	65.41	
16 VIB	Eu	Ga	69.72	
17 VIIA	Gd	Ge	72.63	
18 VIIIA	Tb	As	74.98	
19	Dy	Se	78.30	
20	Ho	Br	79.90	
21	Fm	Kr	83.80	
22	Lu	Xe	84.78	
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1 IA	H	Hydrogen	1.008	Symbol
2 IA	Li	Lithium	6.94	Atomic Weight
3 IA	Be	Boron	10.81	Electrons per shell
4 IA	Na	Magnesium	24.31	State of matter (color of name)
5 IA	K	Ca	39.10	GAS LIQUID SOLID (colorless)
6 IA	Rb	Sc	85.47	
7 IA	Fr	Ti	45.90	
8 IB	Ca	V	50.94	
9 IB	Sr	Cr	52.00	
10 IB	La	Mn	54.94	
11 IB	Ce	Fe	55.85	
12 IB	Pr	Co	58.93	
13 IIIA	Nd	Ni	58.7	
14 IVB	Pm	Cu	63.55	
15 VB	Sm	Zn	65.41	
16 VIB	Eu	Ga	69.72	
17 VIIA	Gd	Ge	72.63	
18 VIIIA	Tb	As	74.98	
19	Dy	Se	78.30	
20	Ho	Br	79.90	
21	Fm	Kr	83.80	
22	Lu	Xe	84.78	
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CMOS scaling

Technology scaling

Parameter	Constant Field	
Supply voltage (V_{dd})	$1/\alpha$	
Length (L)	$1/\alpha$	
Width (W)	$1/\alpha$	
Gate-oxide thickness (t_{ox})	$1/\alpha$	
Junction depth (X_j)	$1/\alpha$	
Substrate doping (N_A)	α	
Electric field across gate oxide (E)	1	
Depletion layer thickness	$1/\alpha$	
Gate area (Die area)	$1/\alpha^2$	
Gate capacitance (load) (C)	$1/\alpha$	
Drain-current (I_{dss})	$1/\alpha$	
Transconductance (g_m)	1	
Gate delay	$1/\alpha$	
Current density	α	
DC & Dynamic power dissipation	$1/\alpha^2$	
Power density	1	
Power-Delay product	$1/\alpha^3$	

Scaling Variables

Device Repercussion

Circuit Repercussion

CMOS scaling

Non Scaling Factors

Bandgap of Silicon $E_g=1.12\text{eV}$

Thermal voltage kT/q

Mobility degradation

Increasing doping and electric field

Velocity saturation

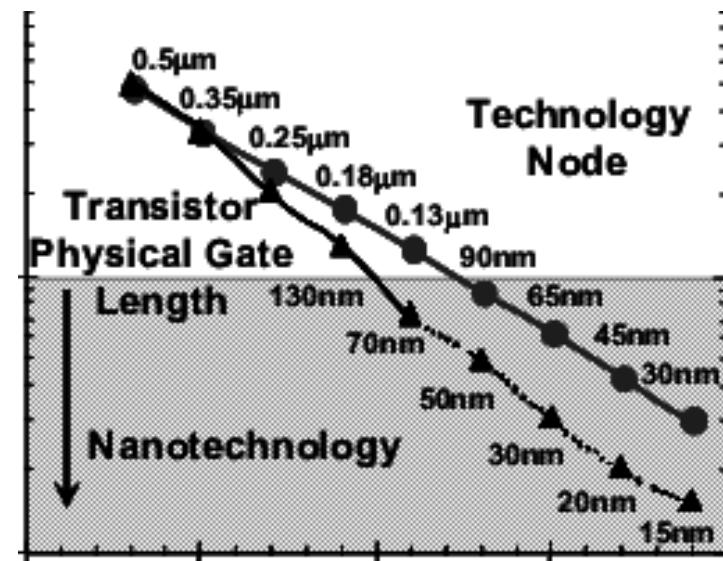
Parasitic s/d resistance



CMOS scaling

Typical Scaling Scenario

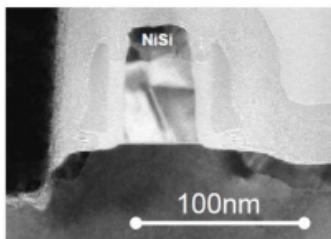
- 1974 : 5 μ m Technology, Vdd = 10V
- 1984 : 1 μ m Technology, Vdd = 5V
- 1994 : 0.35 μ m Technology, Vdd = 3.5V
- 2004 : 90nm Technology, Vdd = 1V



CMOS scaling and FINFET technology

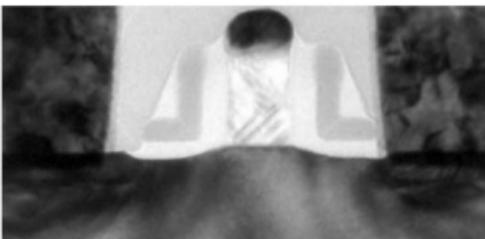
SiO_2/SiON dielectric based

90 nm node



T. Ghani *et al.*,
IEDM 2003

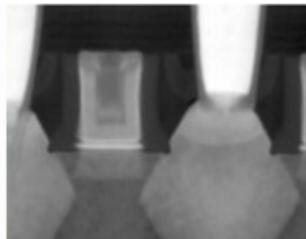
65 nm node



(after S. Tyagi *et al.*, IEDM 2005)

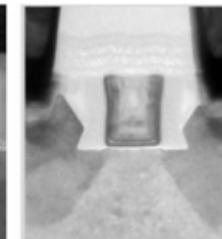
High-k/Metal gate based

45 nm node



K. Mistry *et al.*,
IEDM 2007

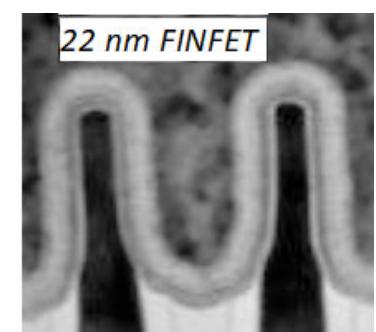
32 nm node



P. Packan *et al.*,
IEDM 2009

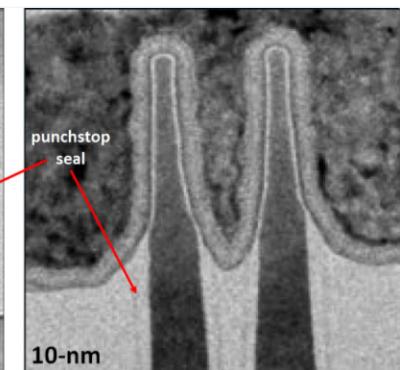
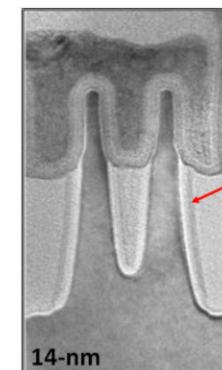
FINFET based

22nm/14nm/10nm/7nm/5nm



Gate length has not scaled proportionately with device pitch (0.7x per generation) in recent generations. – Transistor performance has been boosted by other means.

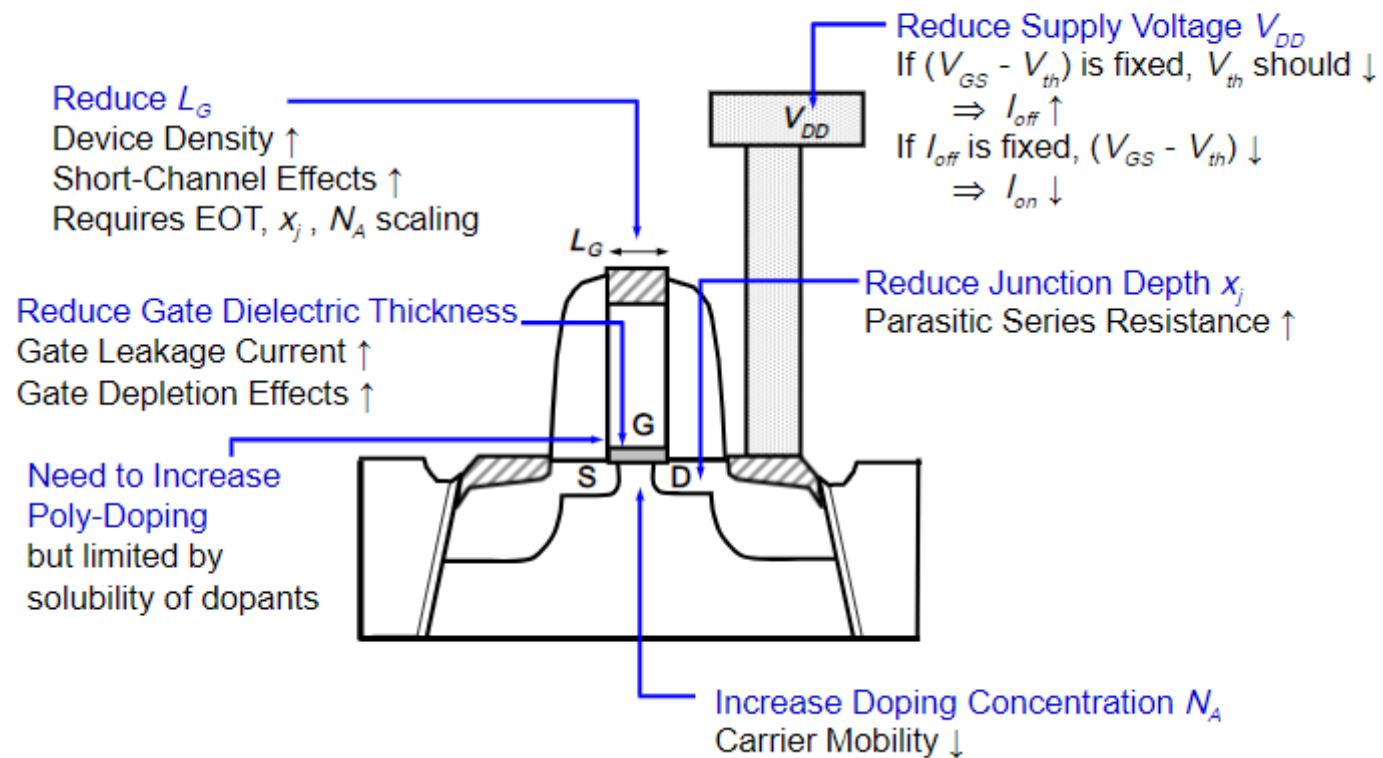
SOURCE:
Intel



CMOS scaling:

- Gate length scaling
- Supply voltage scaling
- Gate oxide scaling
- Scaling of Doping
- Shallow S/D

Overview of Scaling Limitations



CMOS scaling Issues:

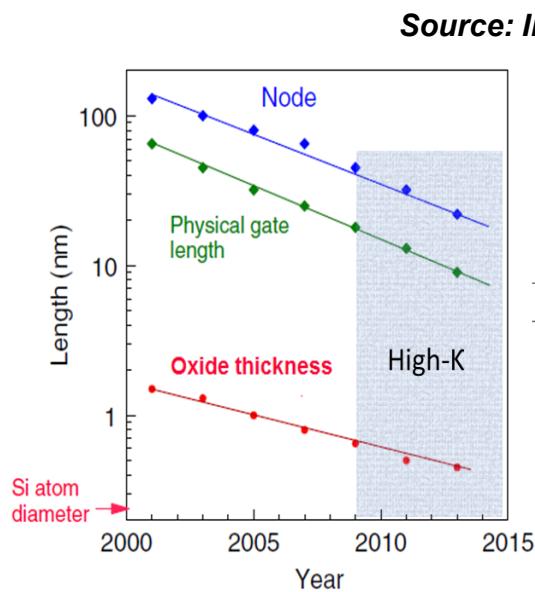
- Short channel effects
- Threshold voltage variation
- DIBL (Drain Induced Barrier Lowering)
- Gate leakage current
- GIDL (Gate Induced Drain Leakage)
- Shallow S/D – Parasitic resistance
- Mobility issues/Velocity saturation/Hot carrier effect

CMOS scaling: Gate dielectric Scaling

- SiO₂/SiON based dielectric till 65 nm CMOS Technology Node
- Best properties with silicon substrate
- Conventional SiON < 12 Å loses its intrinsic insulative property.
- SiON < 12 Å -Increased leakage current and poses reliability issues
- To reduce leakage, **high-κ dielectrics** with equivalent C_{ox} introduced.

SiO₂/SiON Dielectric based

1st Production	1997	1999	2001	2003	2005	2007	2009
Process Generation	0.25 μm	0.18 μm	0.13 μm	90 nm	65 nm	45 nm	32 nm
Gate dielectric	SiO ₂	High-k	High-k				
Gate electrode	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Metal	Metal



$$EOT = \left(\frac{\kappa_{ox}}{\kappa_{hi-k}} \right) t_{hi-k}$$

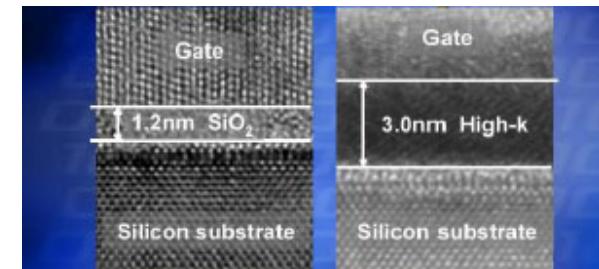
Robertson, Rep. Prog. Phys. 69 (2006) 327-396

CMOS scaling: HK-MG technology

- HK-MG technology: 45 nm and 32 CMOS Technology Node
- k value - high enough and scalable
- Thermal stability
- Compatible with Si CMOS tech.
- Good interface with Si
- Lower defects in the bulk
- Not used after 32nm CMOS technology

HK-MG technology							
1st Production	1997	1999	2001	2003	2005	2007	2009
Process Generation	0.25 μ m	0.18 μ m	0.13 μ m	90 nm	65 nm	45 nm	32 nm
Gate dielectric	SiO ₂	High-k	High-k				
Gate electrode	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Metal	Metal

Source: Intel



Benefits compared to current process technologies

Source: Intel

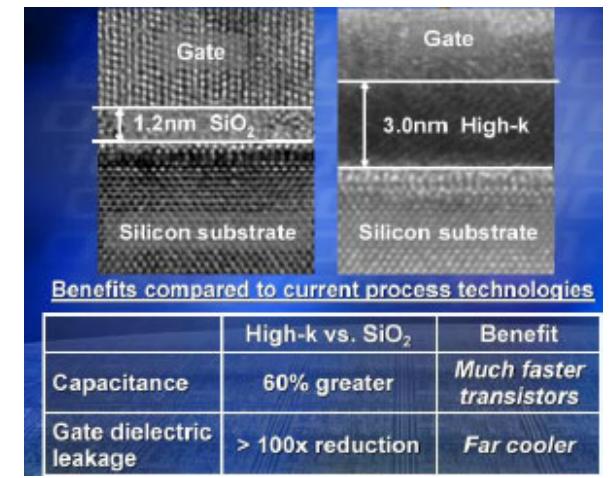
	High-k vs. SiO ₂	Benefit
Capacitance	60% greater	<i>Much faster transistors</i>
Gate dielectric leakage	> 100x reduction	<i>Far cooler</i>

Same C_{ox}, $\uparrow t_{HK}$

Robertson, Rep. Prog. Phys. 69 (2006) 327-396

CMOS scaling: HK-MG technology

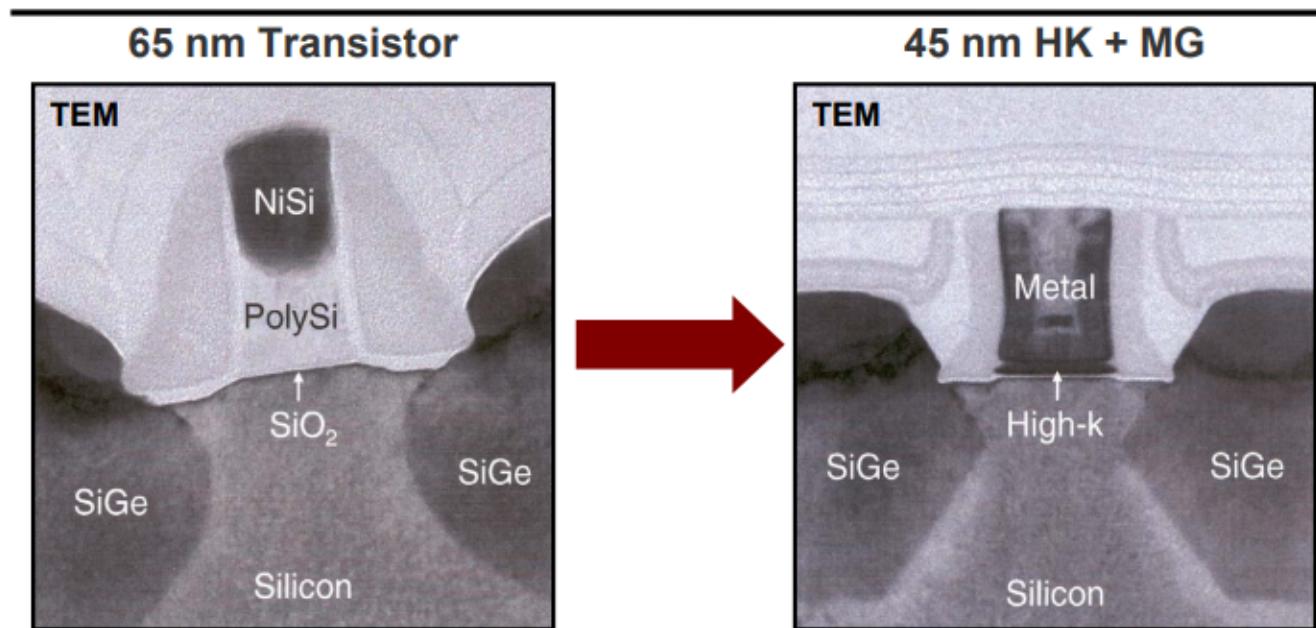
- Challenges:
 - High density of defects
 - Interaction with the polysilicon gate
 - Interaction with the substrate
 - Polycrystallization structure
 - Increased trap-assisted tunneling
 - Increased leakage current
 - Reliability and failure of high-k dielectric



Source: Intel

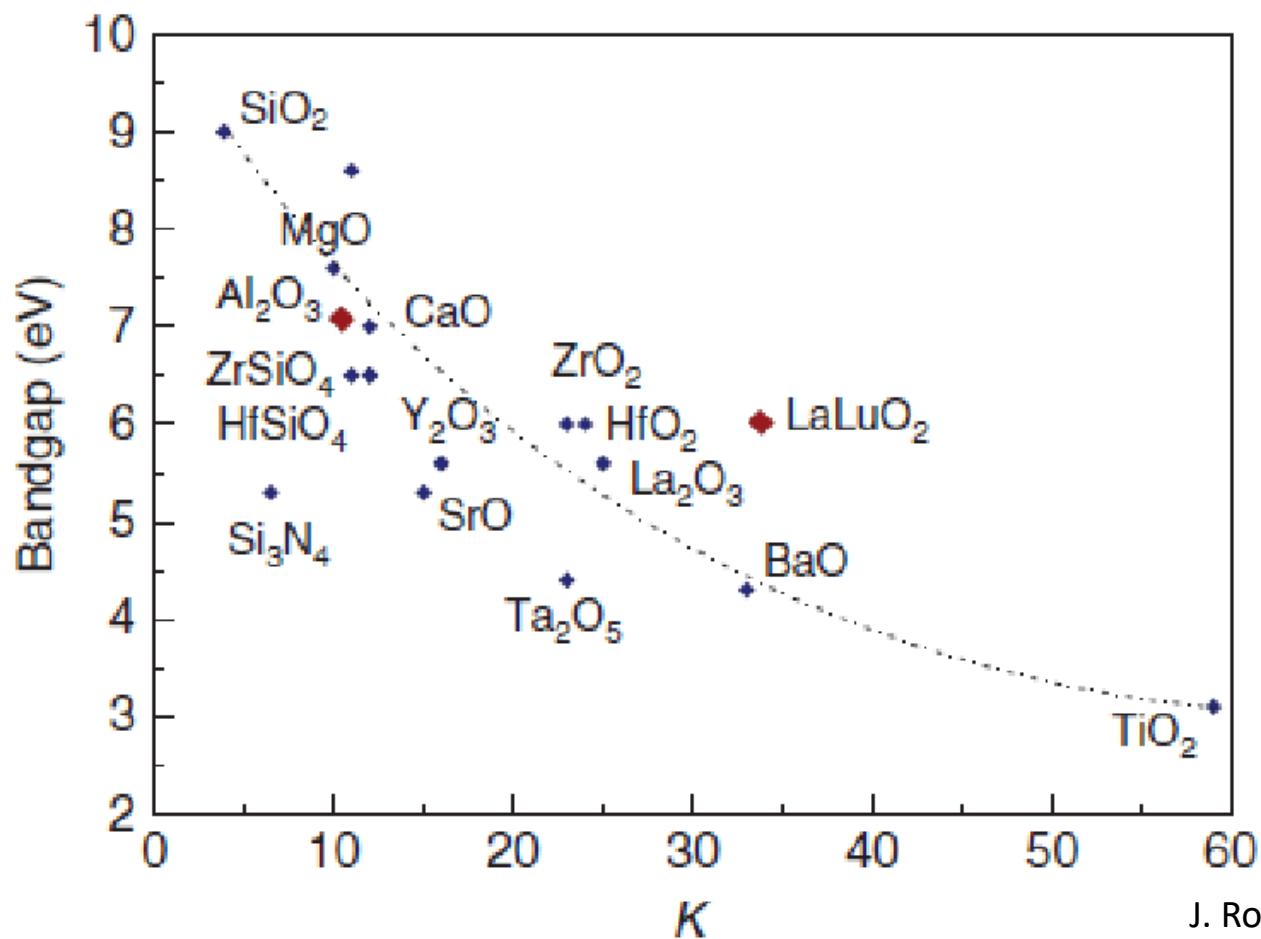
CMOS scaling: HK-MG technology

45nm High-k + Metal Gate Transistors



Source: Intel

CMOS scaling: HK-MG technology



$$\text{EOT} = \left(\frac{\kappa_{\text{ox}}}{\kappa_{\text{hi-}k}} \right) t_{\text{hi-}k}$$

J. Robertson, J. Vac. Sci. Technol. B 18, 1785 (2000)

CMOS scaling:

Micro-MOSFET

Periodic Table of the Elements

H	18 VIIIA																	
Li	2 IIA																	
Be	3 Boron Period 2 Group 13																	
Na	4 Boron Period 3 Group 13																	
Mg	5 Boron Period 4 Group 13																	
K	6 Boron Period 5 Group 13																	
Ca	7 Boron Period 6 Group 13																	
Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr			
Rb	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Cd	In	Sn	Tl	Pb	Bi	At				
Cs	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Cd	In	Sn	Tl	Pb	Bi	At	Fr	Og
Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	At				
Ra	Ac	Rf	Db	Sg	Hs	Mt	Ds	Rg	Cm	Bk	Fm	Md	Lr					
Fr	La	Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Ts			
Og	Ac	Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr			

Nano-MOSFET

Periodic Table of the Elements

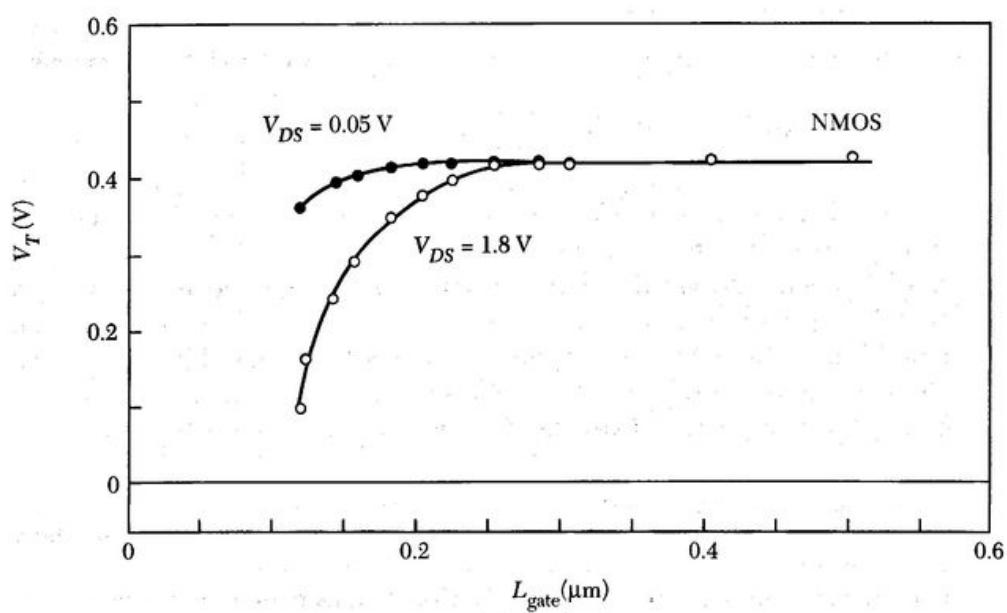
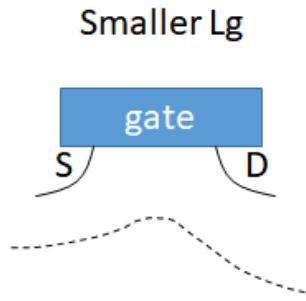
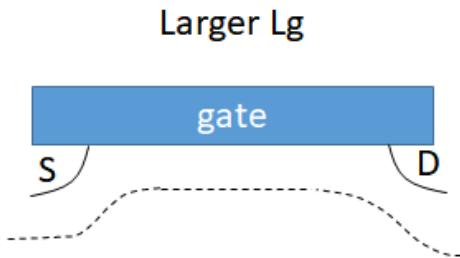
CMOS scaling:

- Gate length scaling

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

$$\beta = \mu C_{ox} \frac{W}{L}$$

Threshold Voltage: (V_{th}) Variation



CMOS scaling:

- Gate length scaling

Channel Length Modulation

- It occurs when transistor is in *Saturation region*.

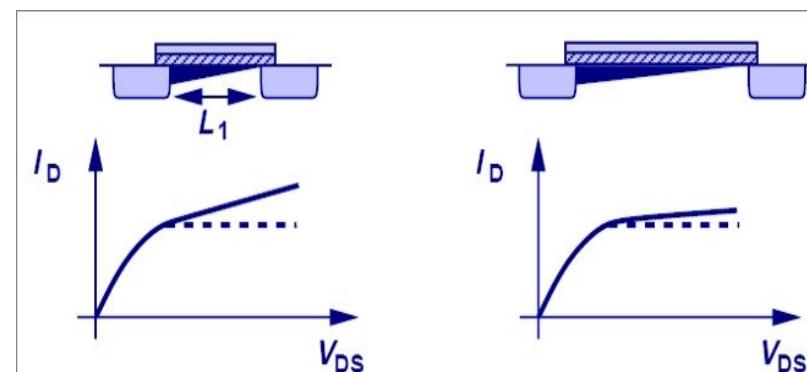
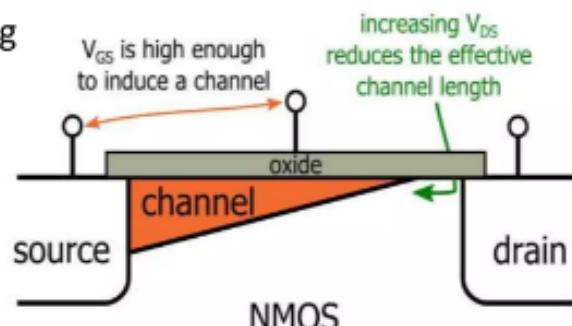
i.e. **Saturation region**,

$$V_{GS} > V_{th} \text{ and } V_{DS} > V_{GS} - V_{th}$$

I_D increases slightly with increasing V_{DS} .

- The pinch-off point moves toward the source as V_{DS} increases.

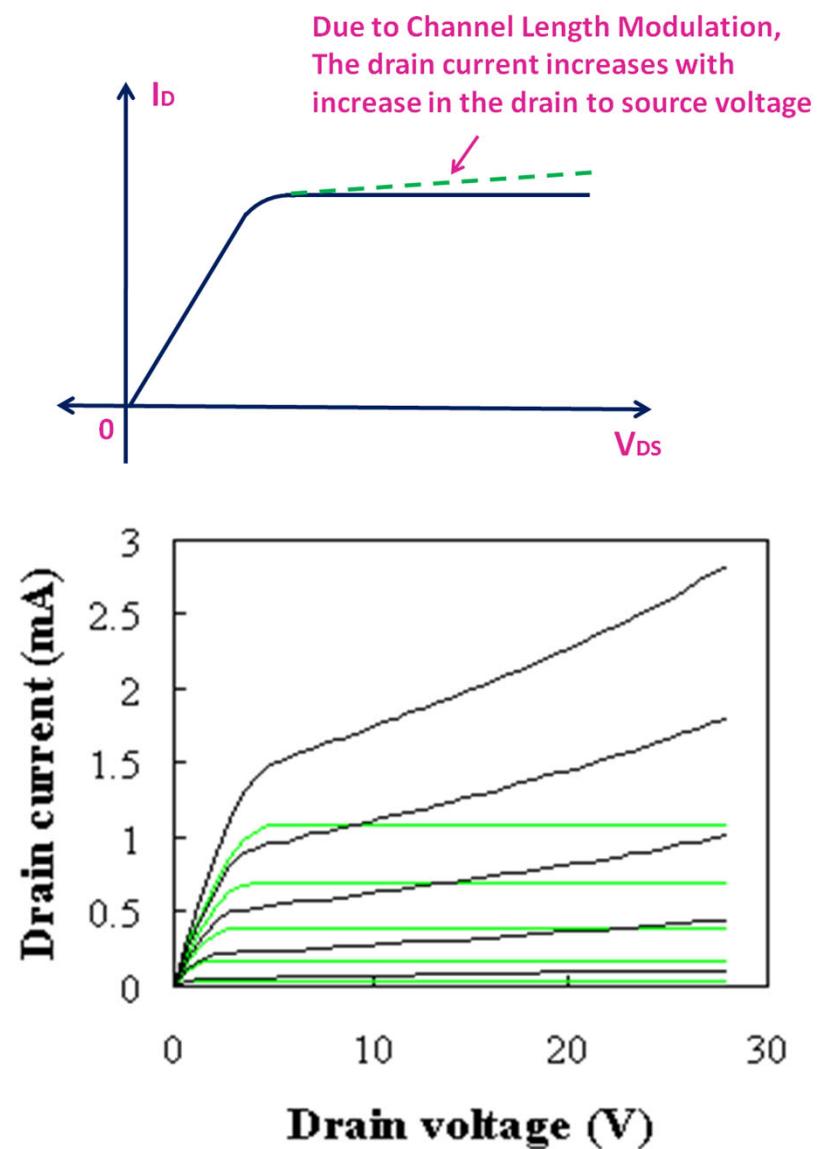
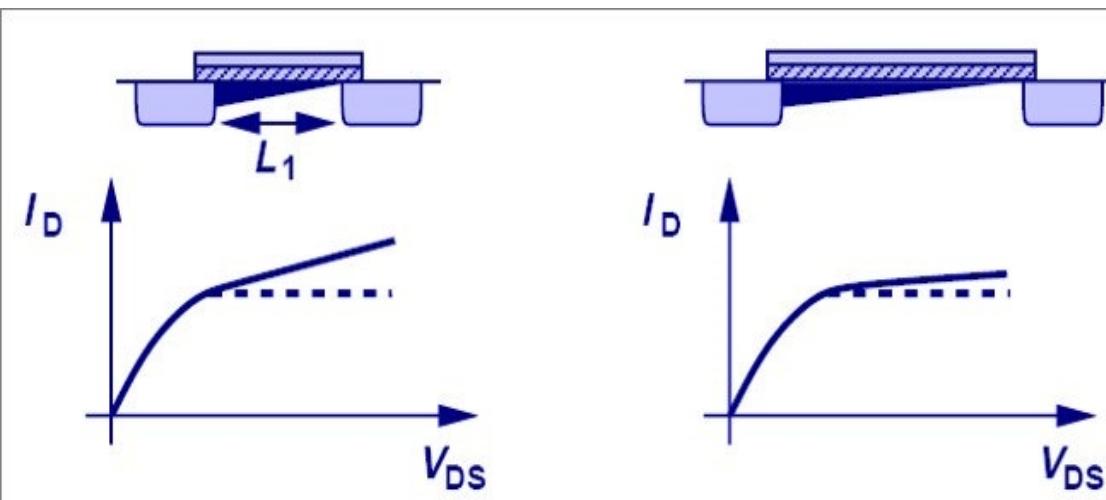
- The length of the channel becomes shorter with increasing V_{DS} .



CMOS scaling:

- Gate length scaling

Channel length Modulation



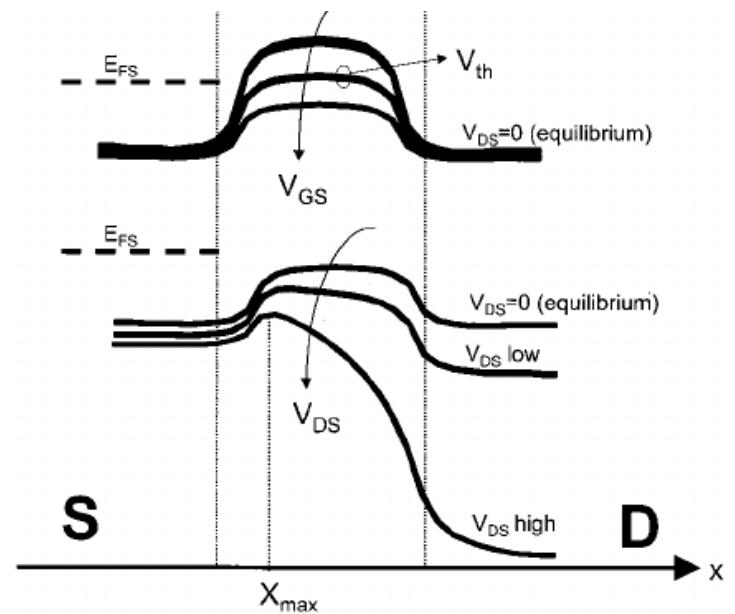
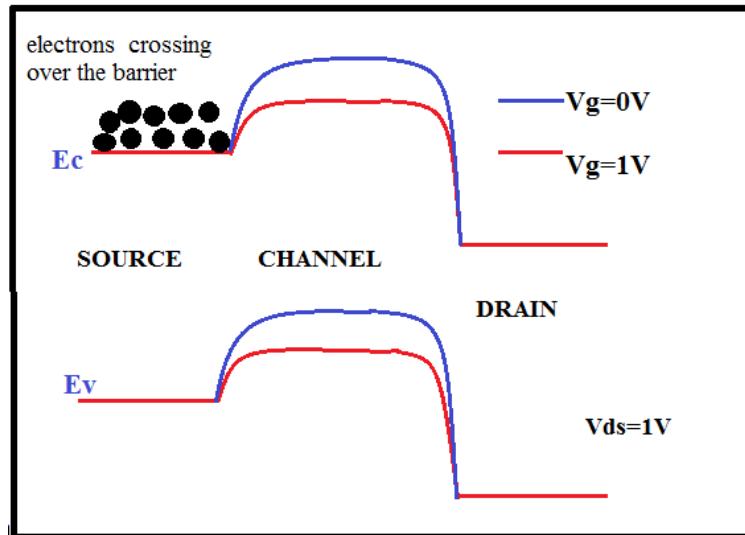
CMOS scaling:

- Gate length scaling

Drain Induced Barrier Lowering (DIBL)

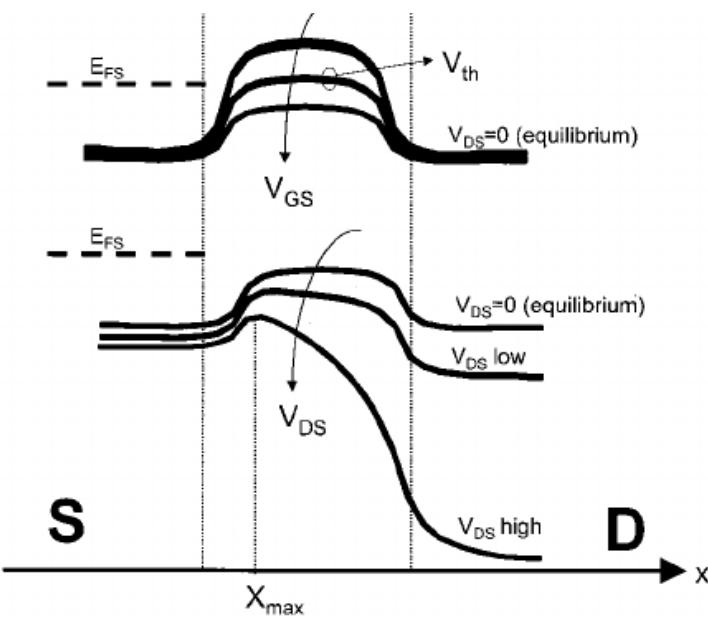
As the source and drain get closer, they become electrostatically coupled, so that the drain bias can affect the potential barrier to carrier diffusion at the source junction

→ V_T decreases (*i.e.* OFF state leakage current increases)

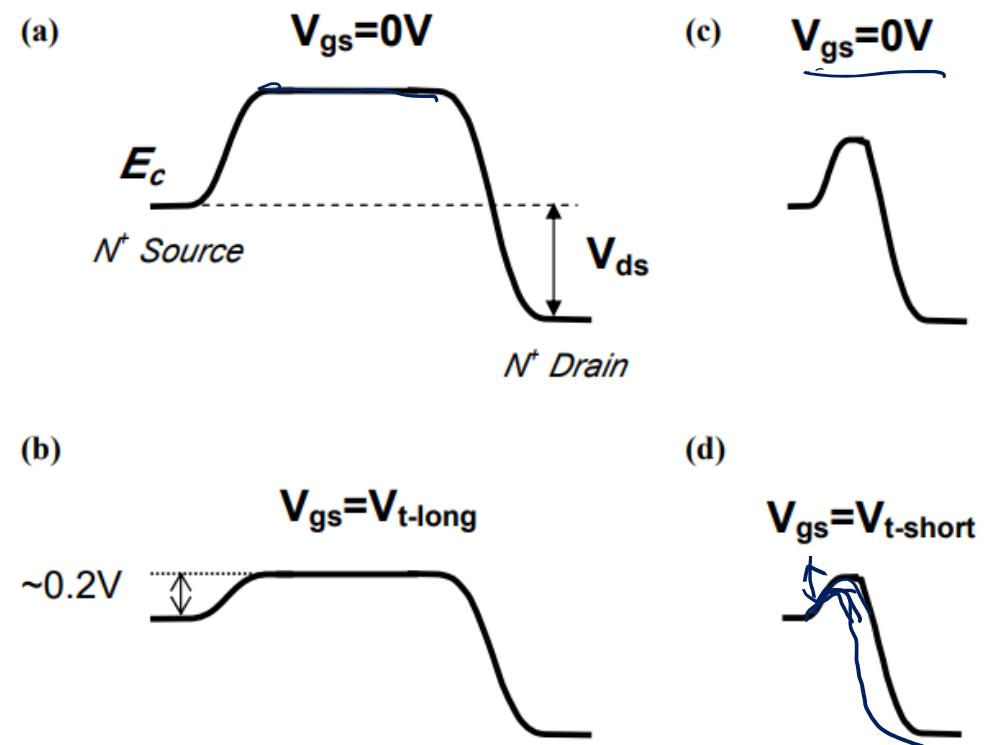


CMOS scaling:

- Gate length scaling



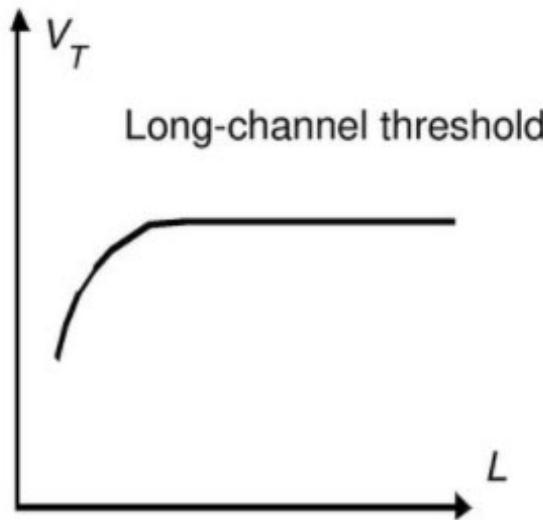
Drain Induced Barrier Lowering (DIBL)



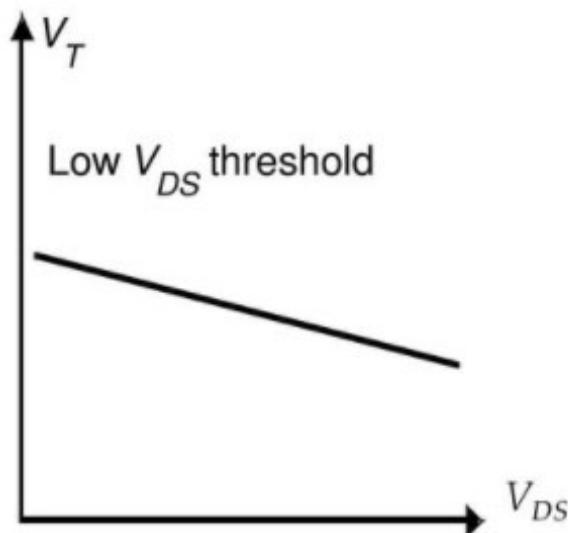
(a)-(d): Energy-band diagram from source to drain when $V_{gs}=0V$ and $V_{gs}=V_t$

Gate length scaling

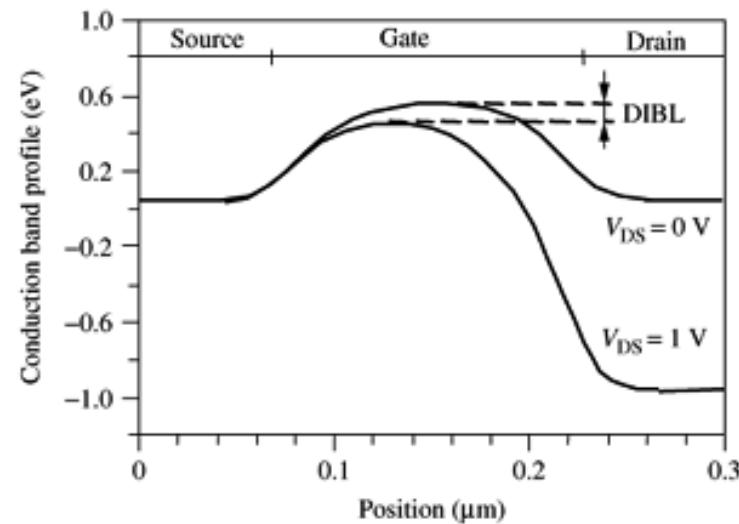
Threshold Voltage: (V_{th}) and DIBL



Threshold as a function of the length (for low V_{DS})



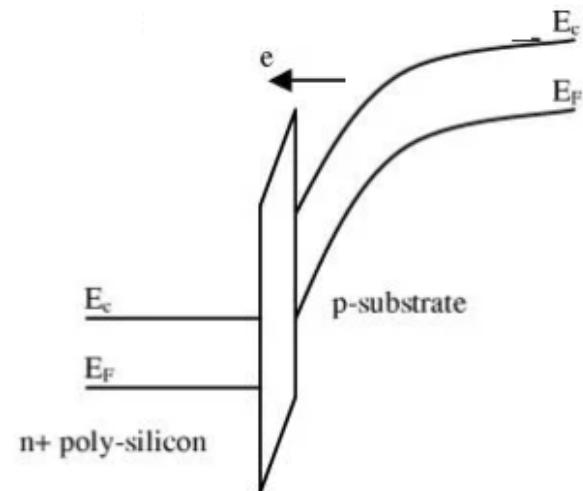
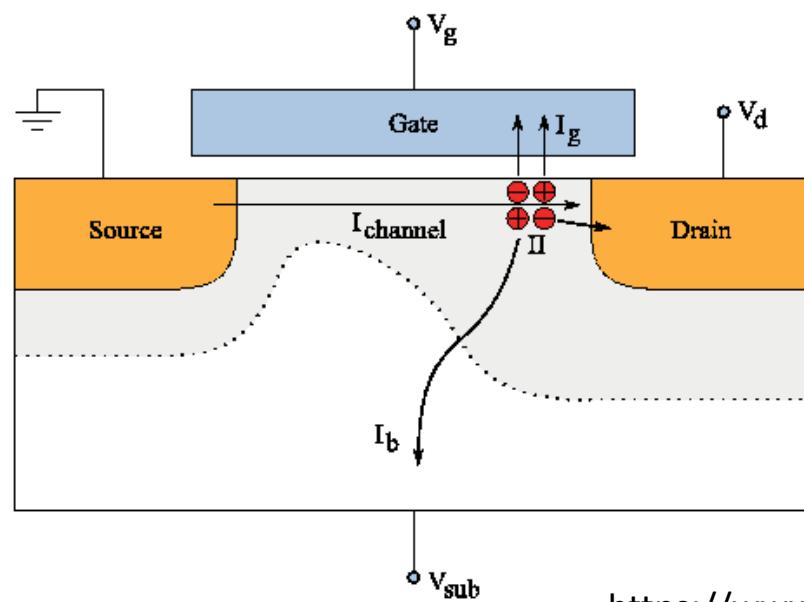
Drain-induced barrier lowering (for low L) ... (DIBL)



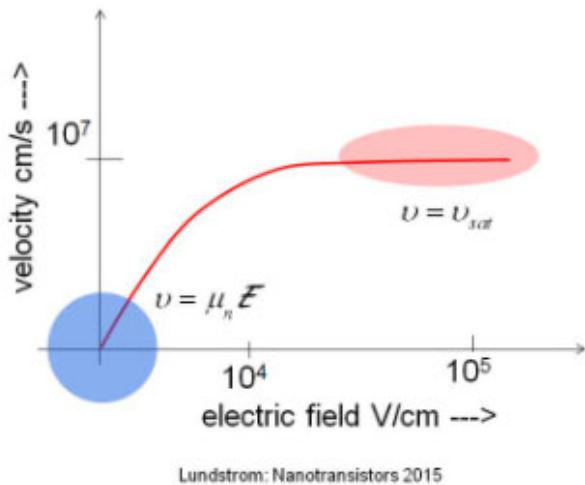
J. Ho, "Introduction and Short Channel Effects", 2014, Semiconductors

Hot carrier injection

High electric field near the substrate-oxide interface energizes the electrons or holes and they cross the substrate-oxide interface to enter the oxide layer. This phenomenon is known as hot carrier injection.



Velocity saturation

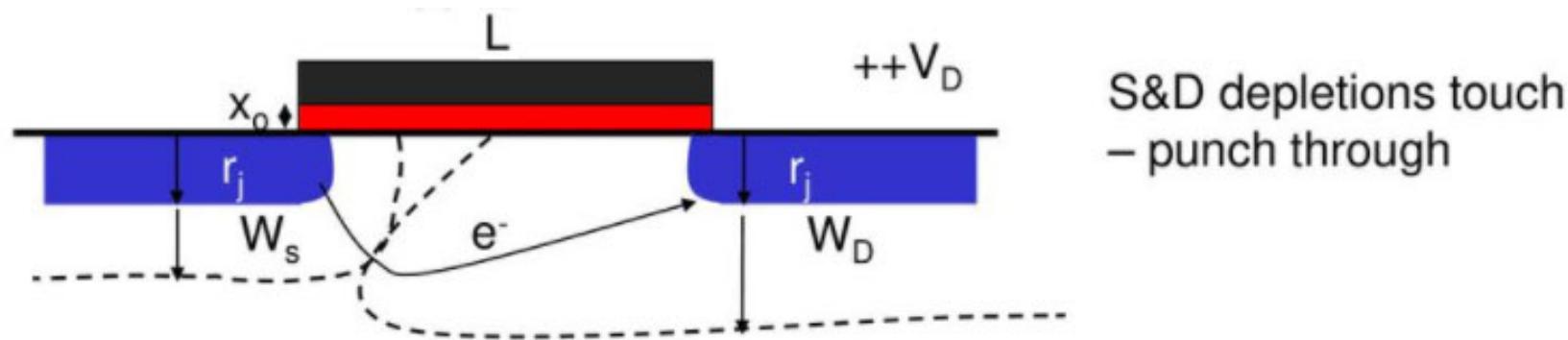


$$V=\mu E$$

- Velocity of charge carriers is linearly proportional to the electric field and the proportionality constant is called as mobility of carrier.
- But when we increase the electric field beyond certain velocity called as the thermal velocity or saturated velocity the velocity of the charge carrier does not change with electric field
- The electric field at which the velocity of carrier saturates is called as the critical electric field. The loss of energy is because of the collisions of carriers called as scattering effect.

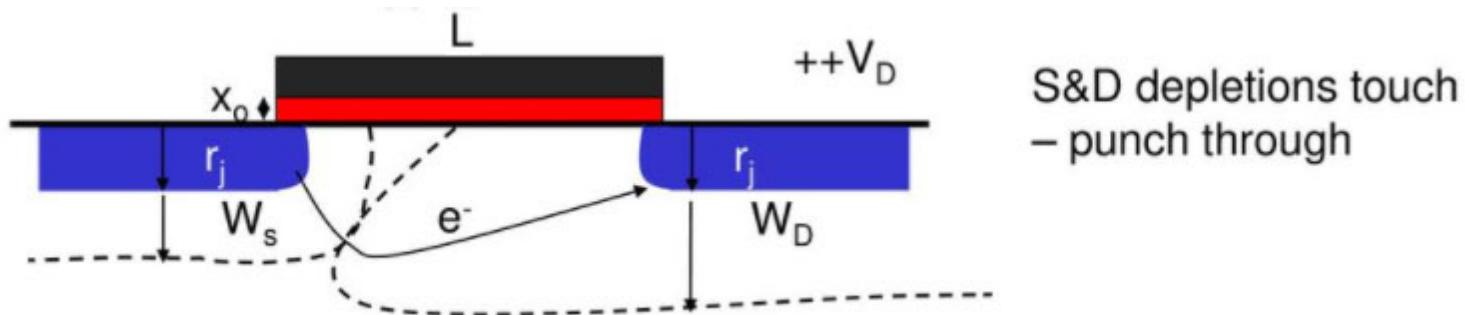
Punch through effect

- In short channel devices, due to the proximity of drain and source terminals, the depletion region of both the terminals come together and eventually merge. In such a condition, "punch-through" is said to have taken place.



J. Ho, "Introduction and Short Channel Effects", 2014,
Semiconductors

Punch through effect



- Drain current no longer controlled by gate voltage
- Drain current does not saturate
- High subthreshold current

J. Ho, "Introduction and Short Channel Effects",
2014, Semiconductors