SINGAPORE UNIVERSITY OF TECHNOLOGY AND DESIGN

Term 7- Sept 2024

Nanoelectronics and Technology (01.119/99.503)

Shubhakar K

Email: shubhakar@sutd.edu.sg

Office location: 1.602-26

17-Sept- 2024

Outline

- Course information
- Course background
- Introduction to Nanotechnology and Nanoelectronics
- Latest news on Nanoelectronics and Semiconductor industries
- Micro- to Nanoelectronics-CMOS
- Review of semiconductors-MOS capacitors, MOSFETs

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Course information

- (01.119/99.503)-UG and PG course combined

- Venue: Think Tank 26 (2.514)

- Timings: Tuesday 3.30PM – 6.00PM
  Thursday 3.30PM – 6.00PM

Course information

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Homework

Weekly homework questions will be uploaded on edimension on Friday from Week 2

Submission: Next week Thursday (5PM)

UG

Grading and assessment:

- Homework - 10%
- Mid-term Exam-30%
- Final Exam-30%
- Course project- 20%
- Seminar attendance- 5%
- Class participation-5%

PG

Grading and assessment:

- Homework - 10%
- Mid-term Exam-30%
- Final Exam-30%
- Course project- 20%
- Seminar presentation- 5%
- Class participation and attendance-5%

Course information

Mid-Term Exam

Week 6, 2 hours in-class

Final Exam

17 December, Tuesday
5.00PM - 7.00PM (Week 14)

Course project

Week 6: Briefing

Week 13: Submission of report and presentation

Seminar Presentation by graduate students

Week 12

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Course information

Policies:

- Students are expected to attend all classes and lab sessions.
- Attendances for mid-term and final exams are compulsory.
- Assignments must be submitted on time. Late submission will not be accepted and graded.
- Active participation and interaction in the class and course project.

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Course information: Semiconductor Physics and MOSFETs

Reference Books

Device Physics

- "Fundamentals of Modern VLSI Devices" by Taur and Ning, Cambridge University Press
- "Solid State Electronic Devices" by Streetman and Banerjee
- "Fundamentals of Electronic Devices" by Achutan and Bhat, McGraw Hill
- "MOS (Metal Oxide Semiconductor) Physics and Technology" by E.H. Nicollian and J.R.Brews, Wiley Publishers.

Process Technology and Materials Characterization

- "Silicon VLSI Technology" by Plummer, Deal, and Griffin
- "ULSI Technology" by S. M. Sze, McGraw Hill

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Weekly teaching contents

Week No.	Topic	Description
Week 1	Introduction to Nanoelectronics and nano-CMOS scaling	ITRS Roadmap for CMOS scaling for advanced technology nodes towards 5nm/3nm technology node and challenges for further scaling. Need for new concepts in nanoelectronic materials and devices. Importance of high-k gate dielectric and metal electrodes in nanoscale MOSFETs.
Week 2	Nanoscale MOSFET, FinFET and other emerging devices	Working principle, physics and electrical characterization of nanoscale MOSFETs. Theory and working principle of FinFET. Fabrication and characterization of nanoscale MOSFETs, FinFETs and scaling trend towards 5nm/3nm technology node.
Week 3	Thin film deposition techniques and cleanroom experiment 1	Review of physical vapour deposition (PVD), chemical vapour deposition (CVD). Atomic layer deposition (ALD) and electron –beam evaporation method. Cleanroom experiment 1 (2nd class)-Growth of gate dielectric on silicon substrate.

Week 4	**Nanofabrication techniques/methods**	**Extreme UV lithography, electron-beam lithography and nanopatterning, Self-aligned multiple patterning (SAMP) process solution for advanced CMOS technology nodes. Self-aligned double patterning (SADP) and self-aligned quadruple patterning (SAQP) processes.**
Week 5	**Reliability and failure analysis of nanoelectronic materials and devices**	**Study of key reliability and failure issues in nanoelectronic devices: process-induced defects, self-heating, carrier scattering, hot-carrier transport, dielectric degradation and breakdown.**
Week 6	**Interconnect technology**	**Interconnect technology, impact of scaling of CMOS devices on interconnects, reliability and failure mechanism in interconnects. Emerging interconnect technologies.** **Cleanroom experiment 2 (2nd class)- electron beam lithography and nanopatterning.**

Week No.	Topic	Description
Week 8	Three dimensional integrated circuit (3D-IC) systems and technology	3D integration circuit technology, heterogeneous 3D IC systems and design challenges. Electrical probing experiment 3 (2nd class)- electrical characterization of nanoscale devices.
Week 9	Understanding of Quantum mechanics : Carrier transport and application of quantum mechanics in nanoscale electronic devices	Electronic bond structure, electron transport, carrier scattering, coulomb blockade and quantum confinement in low-dimensional structures and nanoscale electronic devices
Week 10	Nanoscale characterization using scanning probe microscopy (SPM) techniques	Working principle of scanning tunneling microscopy (STM), atomic force microscopy (AFM) and its applications for analysing properties of nanoscale materials and devices.

Week 11	Nanoscale analysis using electron microscopy techniques	Scanning electron microscopy (SEM) and transmission electron microscopy (TEM analysis of nanoscale materials and devices. Study of SEM-STM nanoprobing and in-situ TEM characterization.
Week 12	Non-volatile memory (NVM) technology	Review of memory technologies. NAND-flash NVM technology and its scaling. Vertical (3D) NAND flash technology and emerging NVM devices such as resistive random-access memory (RRAM) and magnetic RAM (MRAM).
Week 13	Applications of nanomaterials and nanoelectronic devices	Applications of nanomaterials and nanoelectronic devices in different fields of nanoelectronics and nanotechnology. (a) Oxide and 2D-hexagonal boron nitride based RRAM devices for neuromorphic computing (b) 2D-graphene based logic devices (c) Energy technology (d) High-power and automobile application
Week 14	Review session – class 1	Review session – class 1

Course Project Term 7

(Sept)-2024

01.119/99.503: Nanoelectronics and Technology

1. Fabrication of MOS capacitor

- Select highly doped Silicon substrate
- Deposition of Silicon dioxide (SiO_2) and HK dielectric (10 nm)
- Deposition of Al (aluminium) metal electrode
- MOSCAP structures with different sizes using given mask.
- If required backside metal deposition for better Si substrate contact

2. Electrical characterizatio of MOS capacitor

- I_g-V_g , initial I_g –time characteristics
- Analyse leakage current
- Find the Breakdown voltage of SiO_2
- I_g –time characteristics for soft breakdown and hard breakdown
- Analyse any other characteristics of the MOS capacitor

3. Simulation study of MOS capacitor

- C-V characteristics
- Correlation to experimental results

MOS cap tool: https://nanohub.org/resources/moscap

Nanotechnology

- Nanotechnology- Products created with building blocks at length scale <100nm
  - There is a tremendous activities going on in the field of Nanotechnology
  - Nanoelectronics is one of the most mature of the nanotechnologies
  - Nanoelectronics growth in the future relies on innovations in the new materials and device structures

Ref: N. Bhat, CeNSE, IISc Bangalore- Nanoelectronic Device Technology

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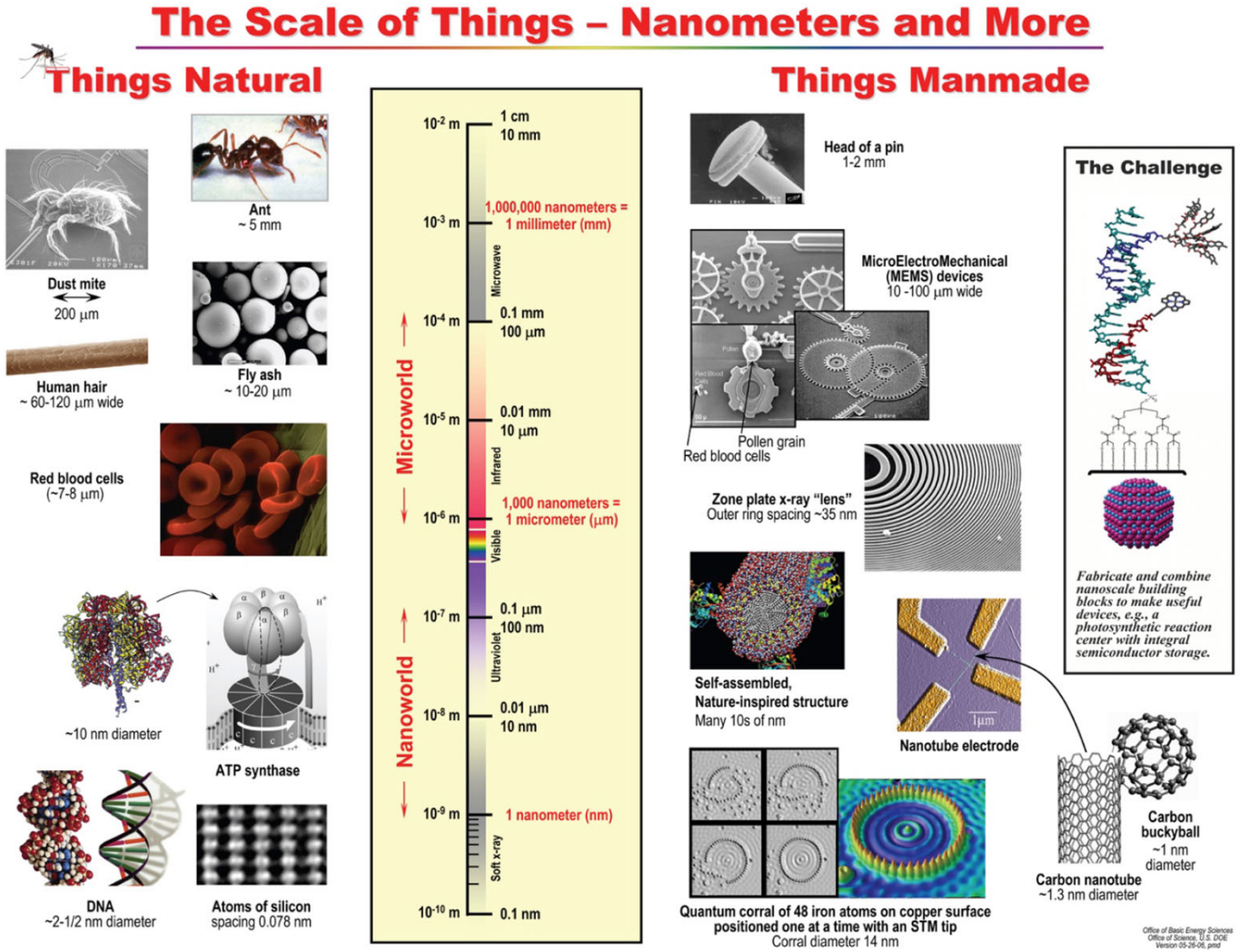
Nanotechnology: Size and scale



Ref: A Compar ison of Scale: Macro, Micr o, Nano-*Office of Basic Energy Sciences, U.S. DOE*
National Nanotechnological Initiative

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Nanotechnology Areas

- Nano-medicine and Bio- engineering
- Nano-robots
- Nano-MEMS
- Nanotechnology for energy applications
- Military applications
- Nanoelectronics and etc

Ref: NANOTECHNOLOGY AND IT'S APPLICATIONS-Chinmoy Paul

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Nanoelectronics

- One of the major and successful technologies of Nanotechnology
- It involves very small scale (nanoscale) devices
- Highly scalable devices (Moore's Law)
- Nanoelectronic devices consume less power and operates at low voltage
- Interface and Integration on a single chip
- Semiconductor Industry is driven by Nanoelectronic semconductor devices

Ref: https://www.slideshare.net/AakankshaR/nanoelectronics-63718699

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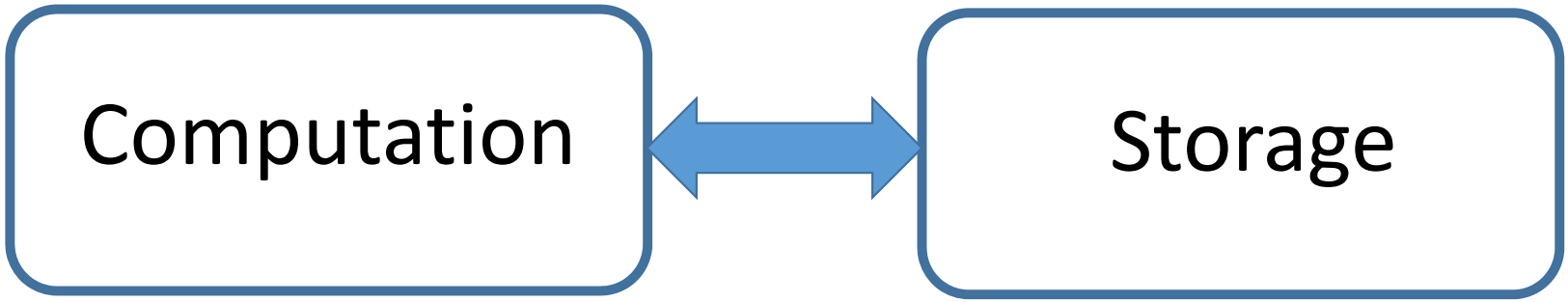
Electronics: Big Picture



Microprocessors
Microcontrollers
DSP
Other processors

SRAM
DRAM
FLASH

Ref: N. Bhat, CeNSE, IISc Bangalore- Nanoelectronic Device Technology

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Nanoelectronics

- From Sand to Silicon: the Making of a Chip | Intel

https://www.youtube.com/watch?v=Q5paWn7bFg4

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Discussion on latest news and updates on Nanoelectronics and Nanotechnology from Industries and research centers

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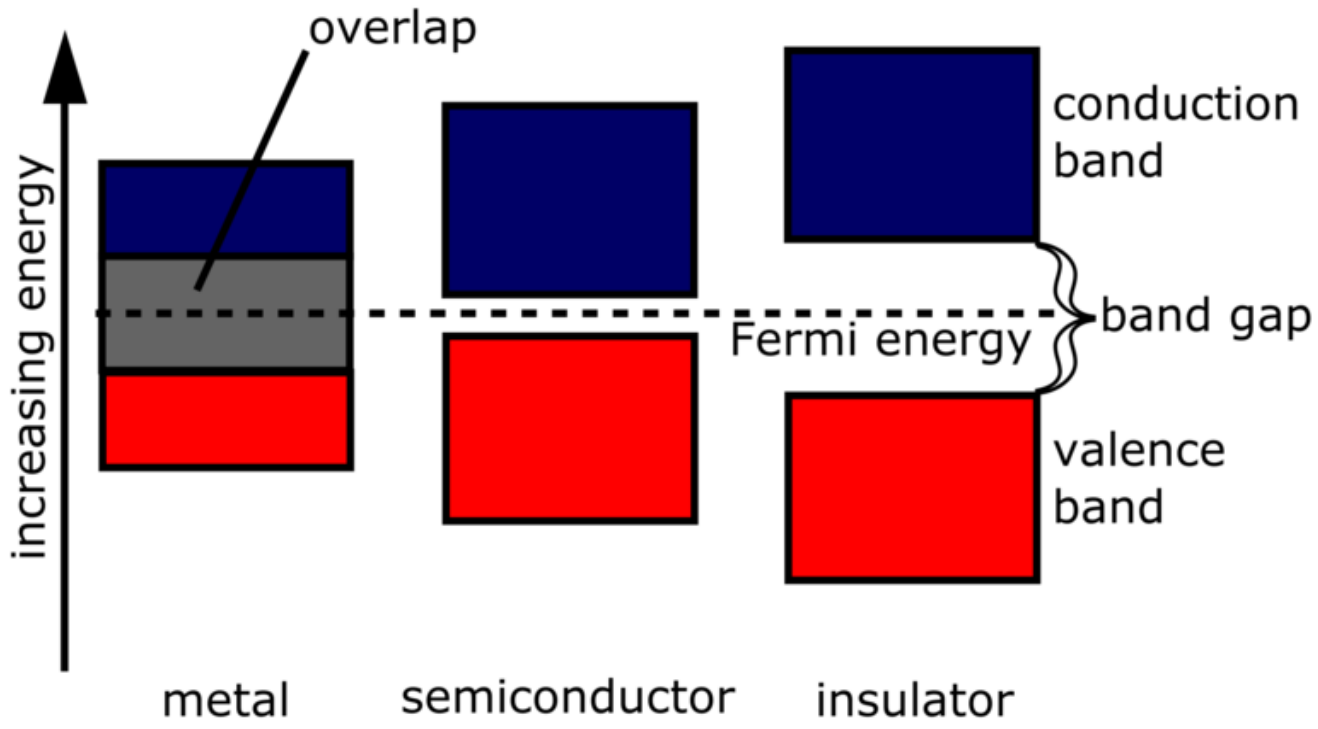
Review of Semiconductors



Ref: https://energyeducation.ca/encyclopedia/Band_gap#cite_note-3

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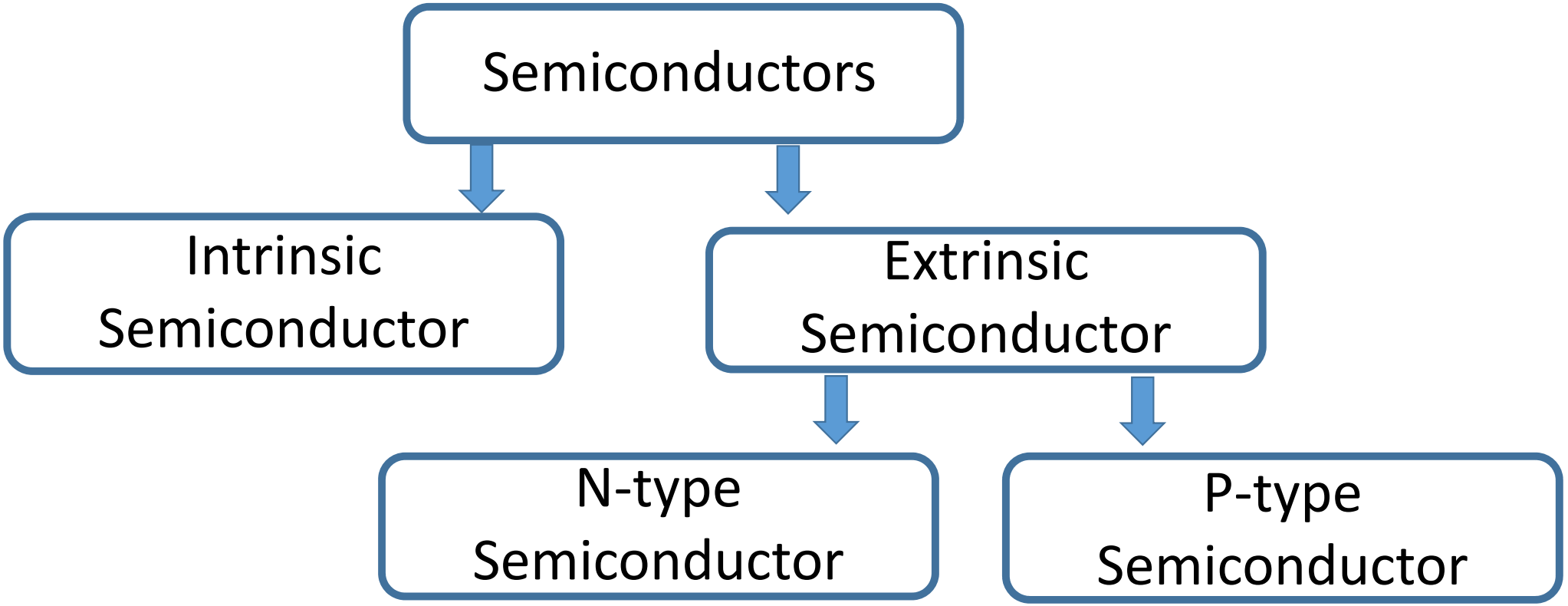
Review of Semiconductors



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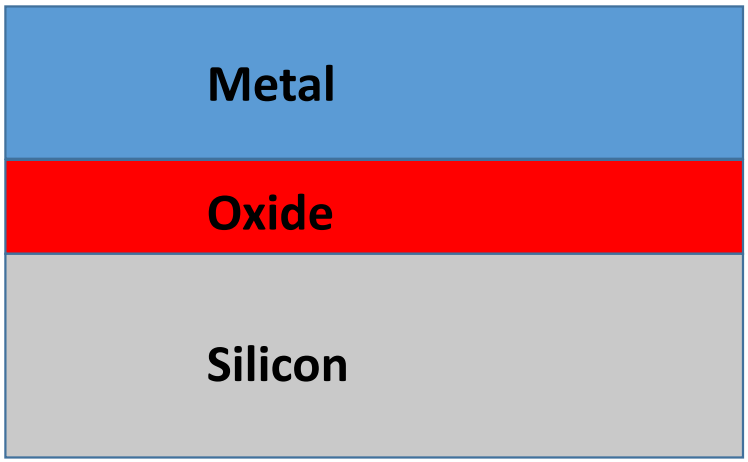
Review of MOS structures



- Accumulation mode
- Depletion mode
- Inversion mode

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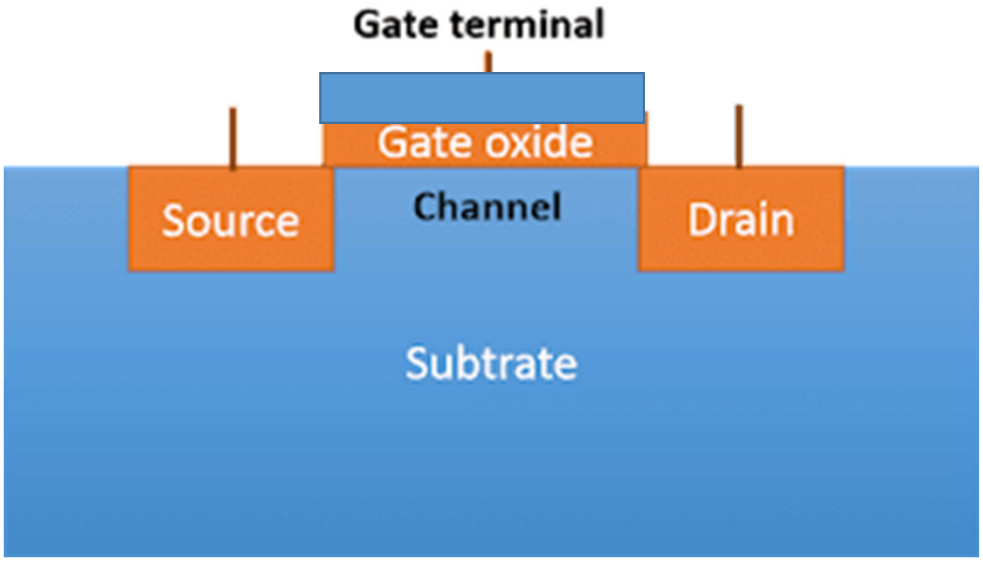
Review of MOSFETs



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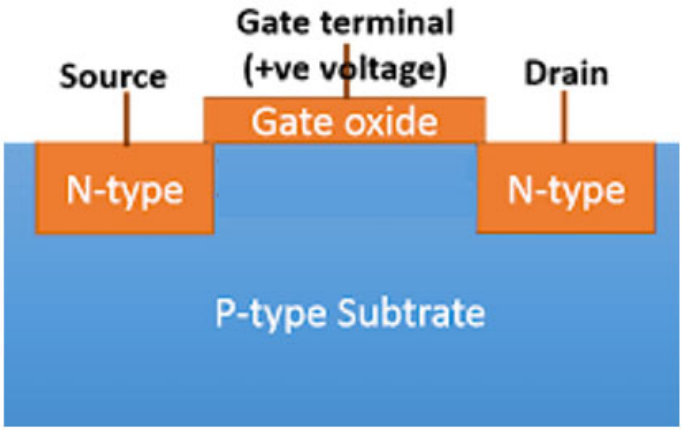
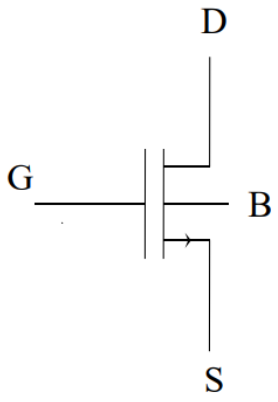
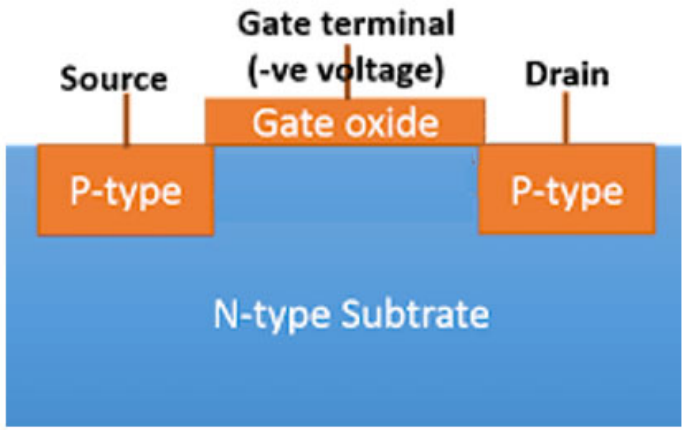
Review of MOSFETs

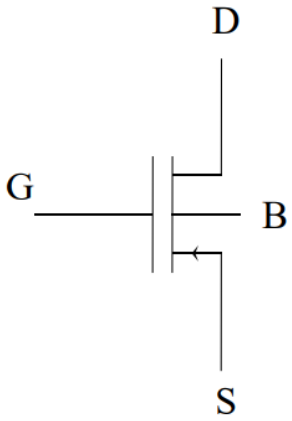


n-channel MOS
Transistor





p-channel MOS
Transistor



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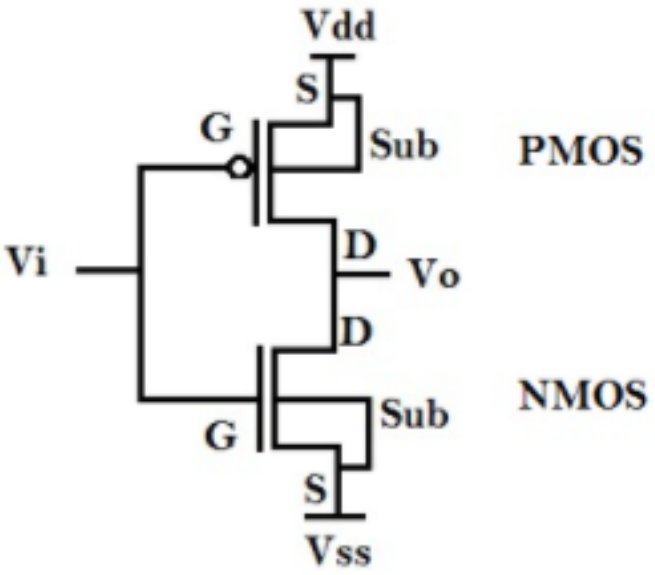
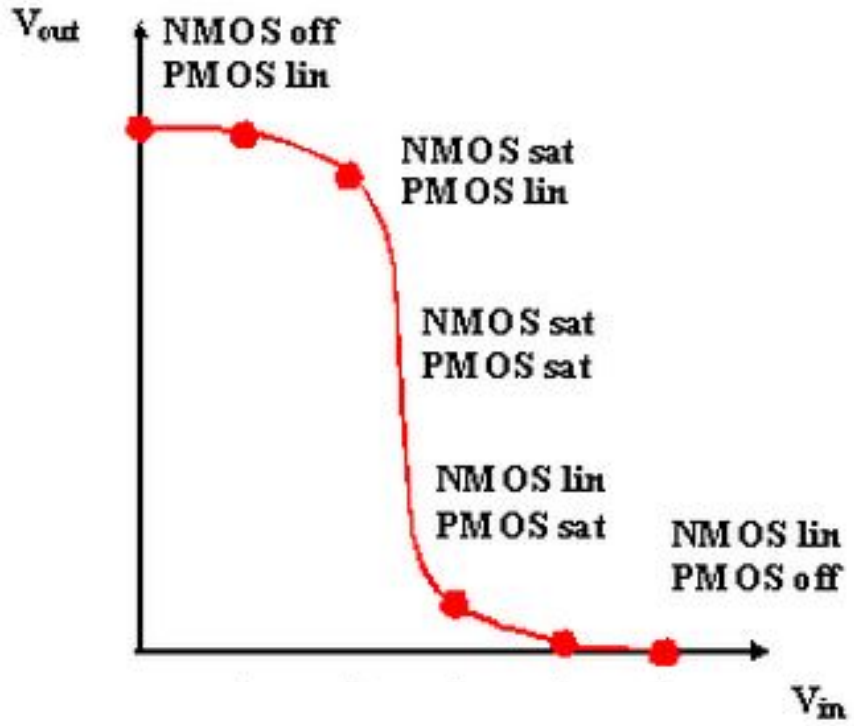
CMOS circuit



G = Gate Terminal
S = Source Terminal
D = Drain Terminal
Sub = Substrate Terminal



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