MOS Transistor

MOSFET

- Metal oxide semiconductor field transistors can be considered as switch which operates with proper biasing.
- MOSFET is three terminal device source , drain and gate.
- Biasing means application of appropriate voltage at three terminal of MOSET so that it can be moved from on to off state or vice versa.

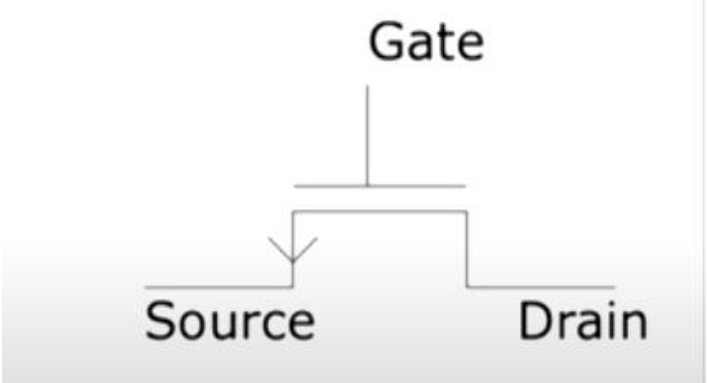


Figure : MOS device Schematic

MOSFET

- Metal-Oxide-Semiconductor (MOS) structure is created by superimposing several layers of conducting and insulating materials to form a sandwich- like structure.
- These structures are manufactured using a series of chemical processing steps involving oxidation of the silicon, selective introduction of dopants, and deposition and etching of metal wires and contacts.
- Transistor operation is controlled by electric fields so the devices are also called Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)
- Types of MOSFET

✓ Based on material properties

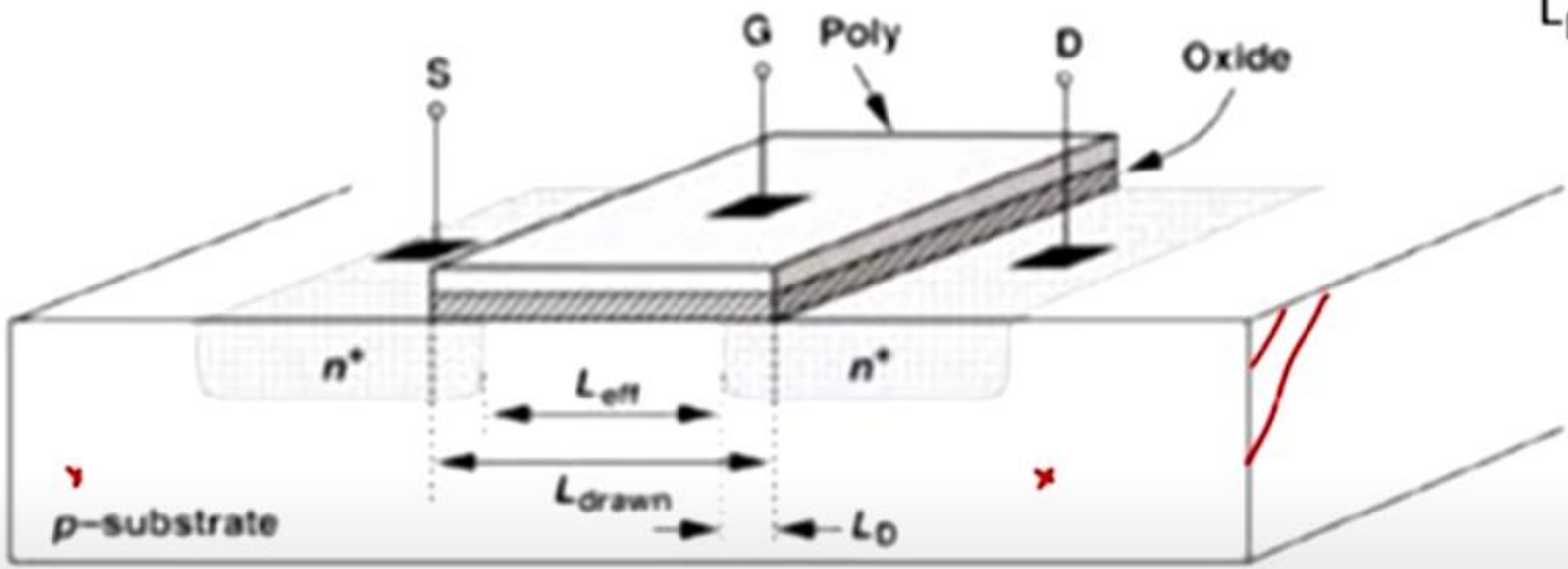
- N Mos- where electrons are charge carriers
- P Mos- where holes are charge carriers

MOSFET

✓Based on electrical properties

- Enhancement mode MOSFET
- Depletion mode MOSFET
- So technically four types of MOSFET
  - N channel Enhancement mode MOSFET
  - P channel Enhancement mode MOSFET
  - P channel Depletion mode MOSFET
  - N channel Depletion mode MOSFET

MOSFET Structure



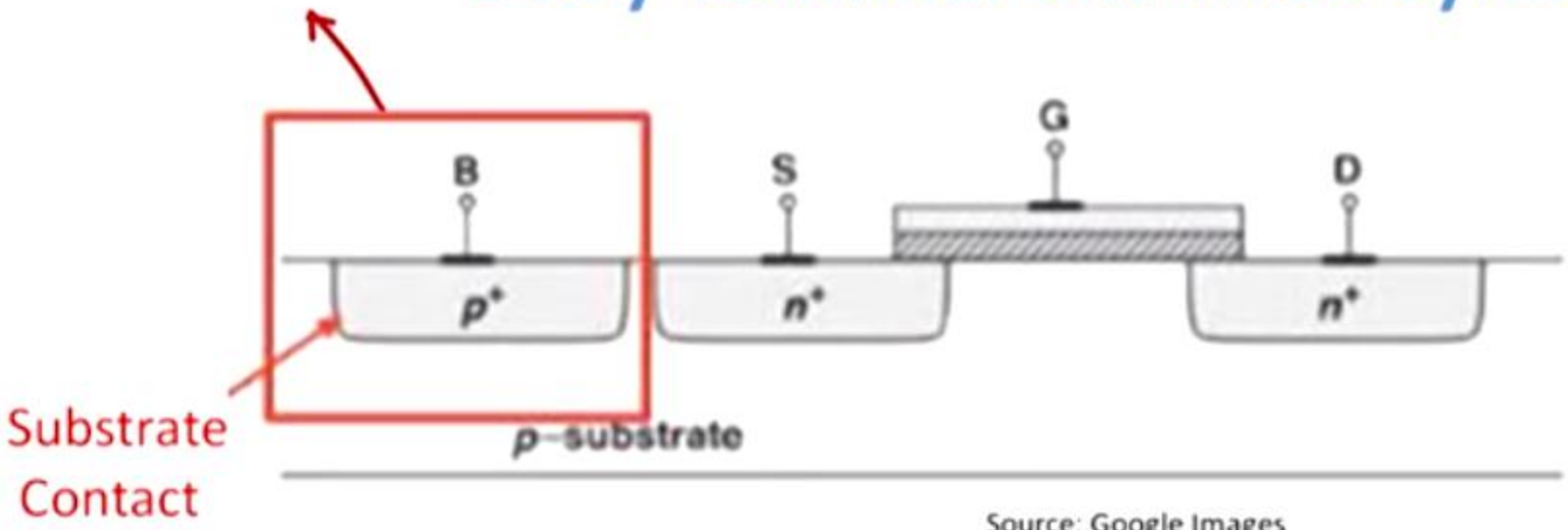
L_D: Side Diffusion Length

$L_{eff} = L_{drawn} - 2L_D$

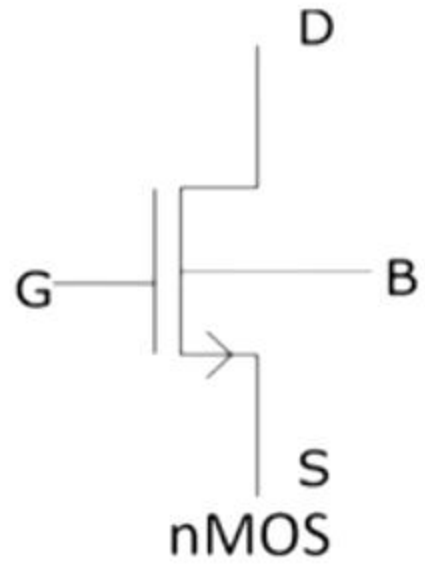
Introduction

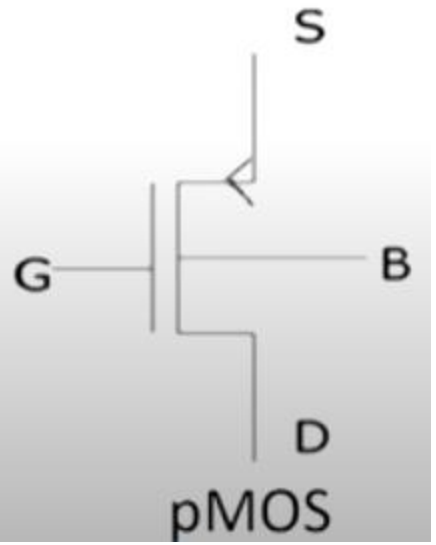
- Each transistor consists of a stack of the conducting gate, an insulating layer of silicon dioxide (SiO2), and the silicon wafer, also called the substrate, or body, or bulk.
- An nMOS transistor is built with a p-type body and has regions of n-type
  - semiconductor adjacent to the gate called the source and drain
- A pMOS consists of p-type source and drain regions with an n-type body.

Body Terminal and MOS symbols



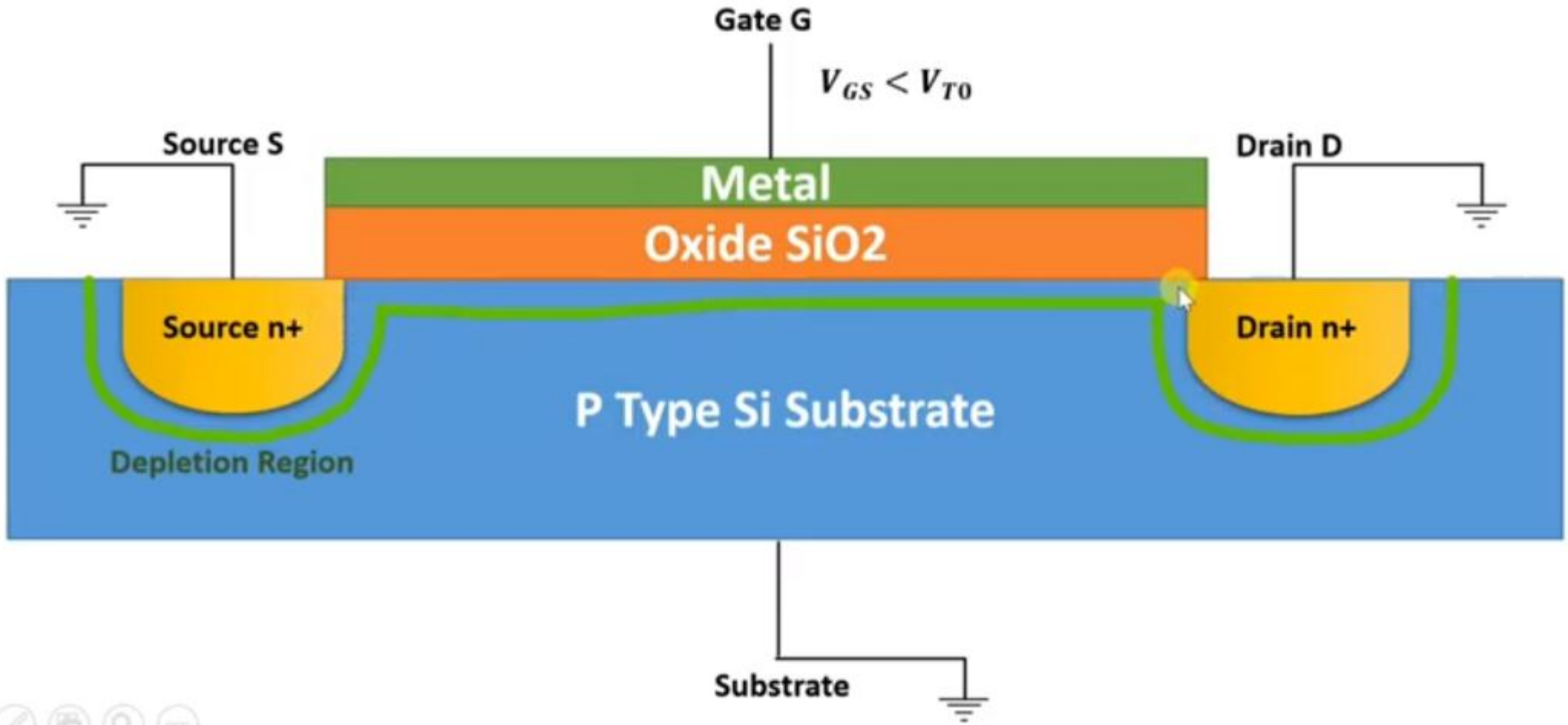
Source: Google Images





- The substrate bias should be connected with the negative most supply of the system.
- nMOS and pMOS are in general made in same wafer, in which one device can placed in local substrate called as well.

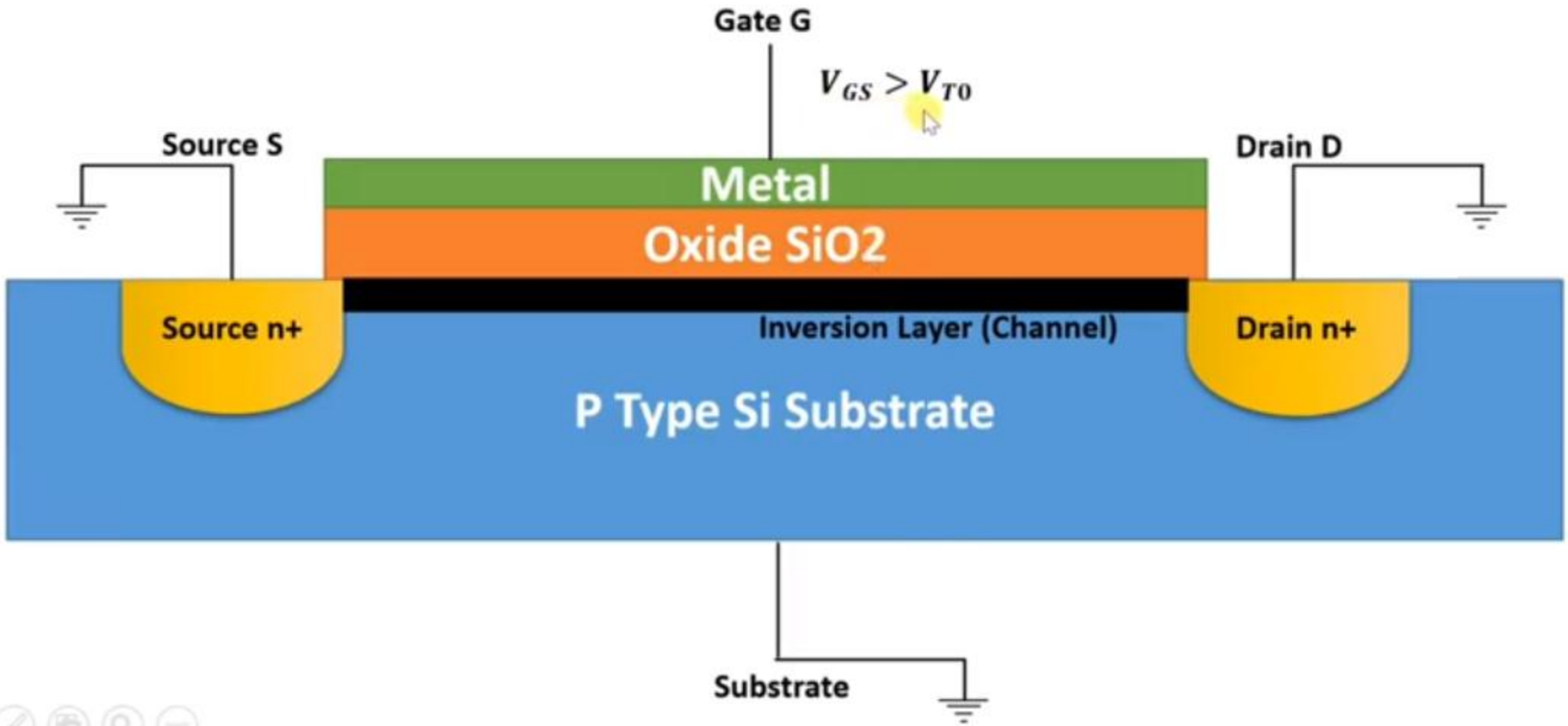
Working of n Channel MOSFET in cut off region



MOSFET :Cutoff Region mode

- When $V_{GS} < V_T$, there is no channel formed between the Drain and Source and hence I_{DS}=0 A
- This region is called the *Cutoff Region*
- *T*his region of operation is when the Transistor is OFF

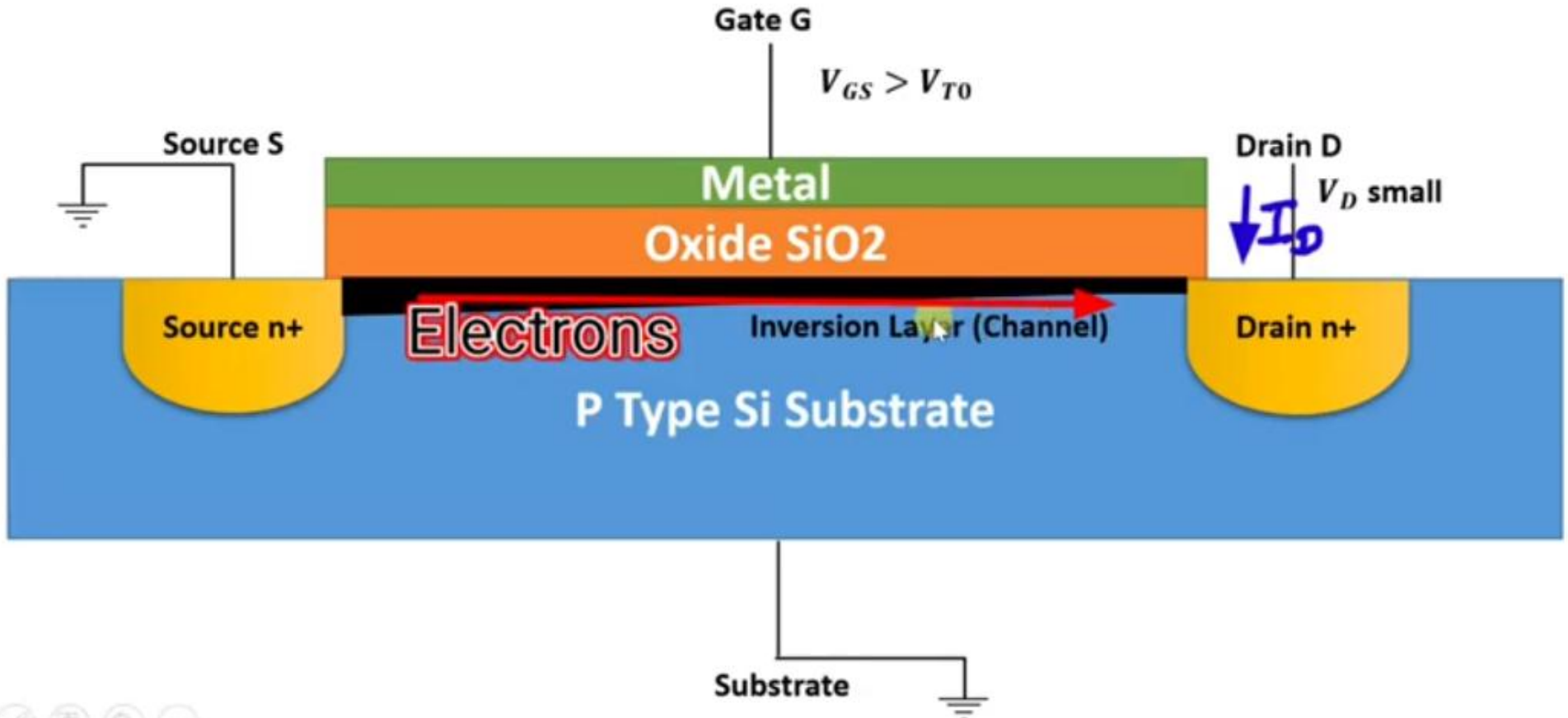
Working of n Channel MOSFET cut off region



MOSFET : Cutoff Region mode

- When VGS > VT, a channel is formed. IDS is dependent on the VDS voltage
- When VDS = 0v, no current flows.

Working of n Channel MOSFET in Linear region



MOSFET: Linear Region mode

• If VGS > VT and VDS > 0, then a current will flow from the Drain to Source (IDS).The MOSFET operates like a voltage controlled resistor which yields a *linear* relationship between the applied voltage (VDS) and the resulting current (IDS)

• For this reason, this mode of operation is called the *Linear Region. T*his region is also sometimes called the *triode region* (we'll use the term "linear")

• VDS can increase up to a point where the current ceases to increase linearly (saturation)

• We denote the highest voltage that VDS can reach and still yield a linear increase in current as the *saturation voltage* or VDSAT

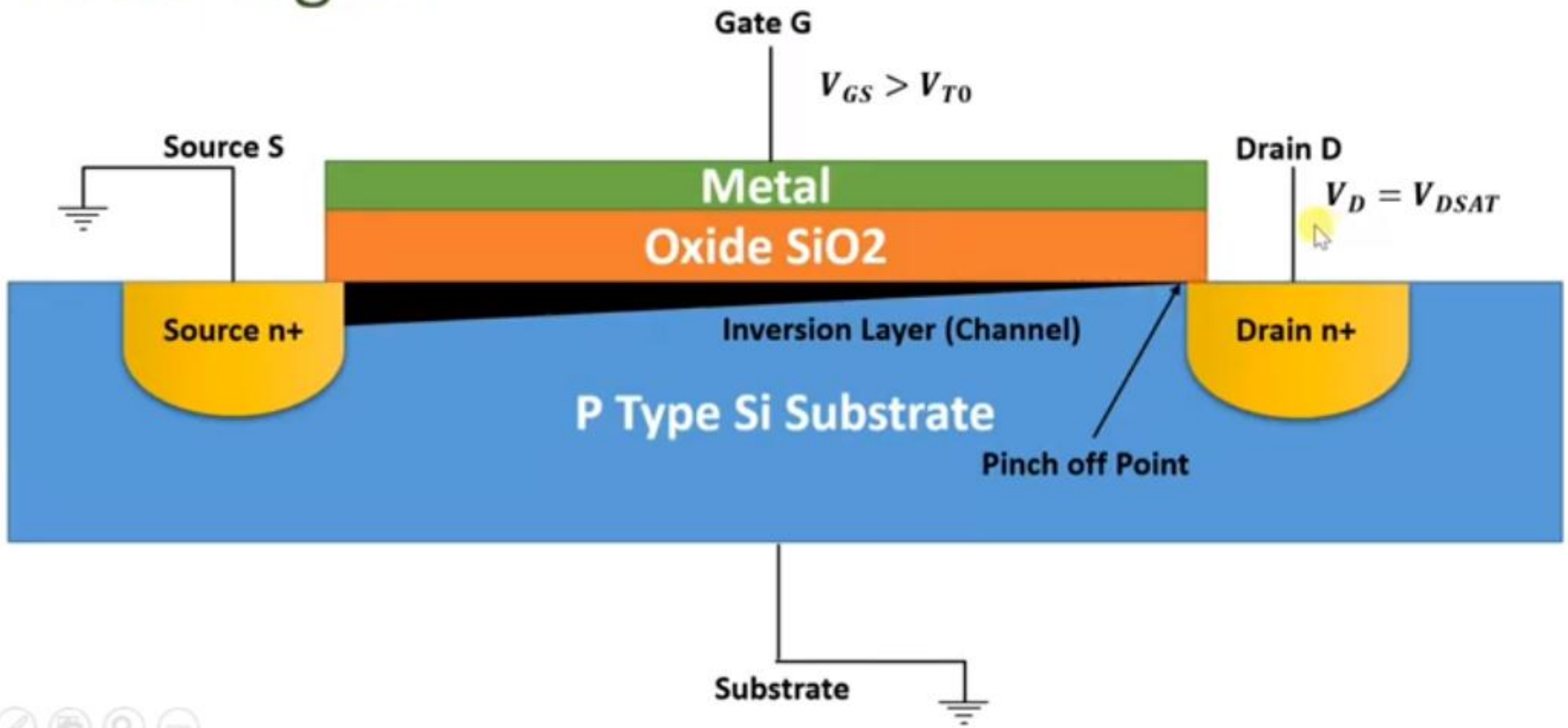
when a voltage is applied at VD, its positive charge pushes the majority charge carriers (holes) that exist at the edge of the depletion region further from the Drain.

- As the depletion region increases, it becomes more difficult for the Gate voltage to induce an inversion layer. This results in the inversion layer depth decreasing near the drain.
- As VD increases further, it eventually causes the inversion layer to be *pinched-off* and prevents the current flow to increase any further.
- This point is defined as the *saturation voltage* (VDSAT)
- From this, we can define the *linear region* as:

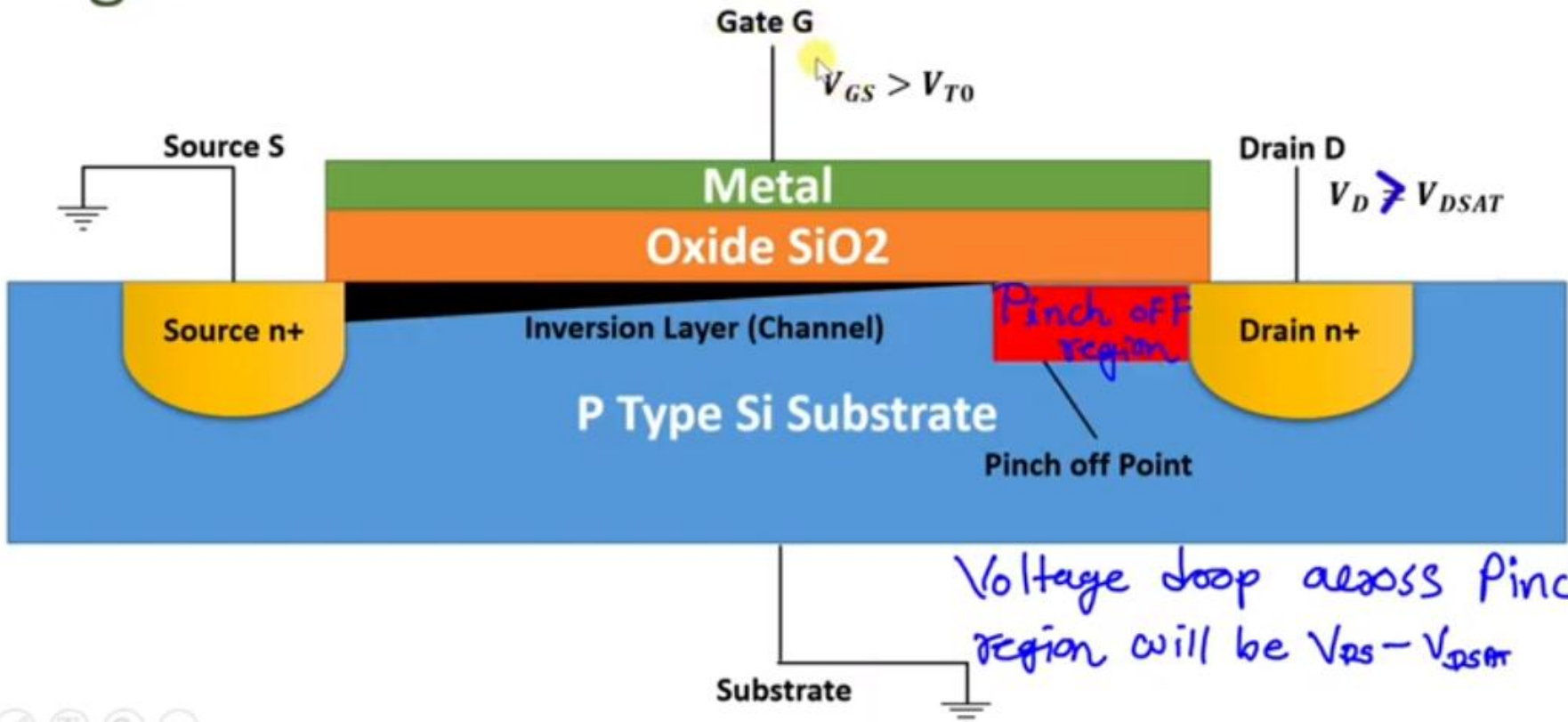
$$VGS > VT$$

$$0 < VDS < VDSAT$$

Working of n Channel MOSFET threshold of linear region



Working of n Channel MOSFET in saturation region



Voltage drop across Pinch off region will be $V_{DS} - V_{DSAT}$

MOSFET : Saturation Region mode

- MOSFET is defined as being in saturation when: Saturation Region :

$$VGS > VT \text{ and } VDS > (VGS-VT)$$

- An increase in VDS does not increase IDS because the channel is *pinched-off*
- However, an increase in VGS DOES increase IDS by increasing the channel depth and hence the amount of current that can be conducted.

MOSFET Regions of Operation

- Cut-Off Region
  When VGS < VT, no conductive channel is present and IDS = 0, the cutoff region.
- Ohmic or Linear Region

  Ohmic or linear region is a region where in the current I_{DS} increases with an increase in the value of V_{DS}. When MOSFETs are made to operate in this region, they can be used as amplifiers.
- Saturation Region

  In saturation region, the MOSFETs have their I_{DS} constant inspite of an increase in V_{DS} and occurs once V_{DS} exceeds the value of pinch-off voltage V_P. Under this condition, the device will act like a closed switch through which a saturated value of I_{DS} flows. As a result, this operating region is chosen whenever MOSFETs are required to perform switching operations.

MOSFET

- For the **n-channel MOS transistor** a drain current will only flow when a gate voltage (VGS) is applied to the gate terminal greater than the threshold voltage (VTH) level in which conductance takes place making it a transconductance device.
- The application of a positive (+ve) gate voltage to a n-type eMOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing (hence its name) the thickness of the channel allowing more current to flow. This is why this kind of transistor is called an enhancement mode device as the application of a gate voltage enhances the channel.
- Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current, ID through the channel. In other words, for an n-channel enhancement mode MOSFET: +VGS turns the transistor “ON”, while a zero or -VGS turns the transistor “OFF”. Thus the enhancement-mode MOSFET is equivalent to a “normally-open” switch.

MOSFET

- The reverse is true for the p-channel enhancement MOS transistor. When VGS = 0 the device is “OFF” and the channel is open. The application of a negative (-ve) gate voltage to the p-type eMOSFET enhances the channels conductivity turning it “ON”. Then for an p-channel enhancement mode MOSFET: +VGS turns the transistor “OFF”, while -VGS turns the transistor “ON”.

n-channel MOSFET

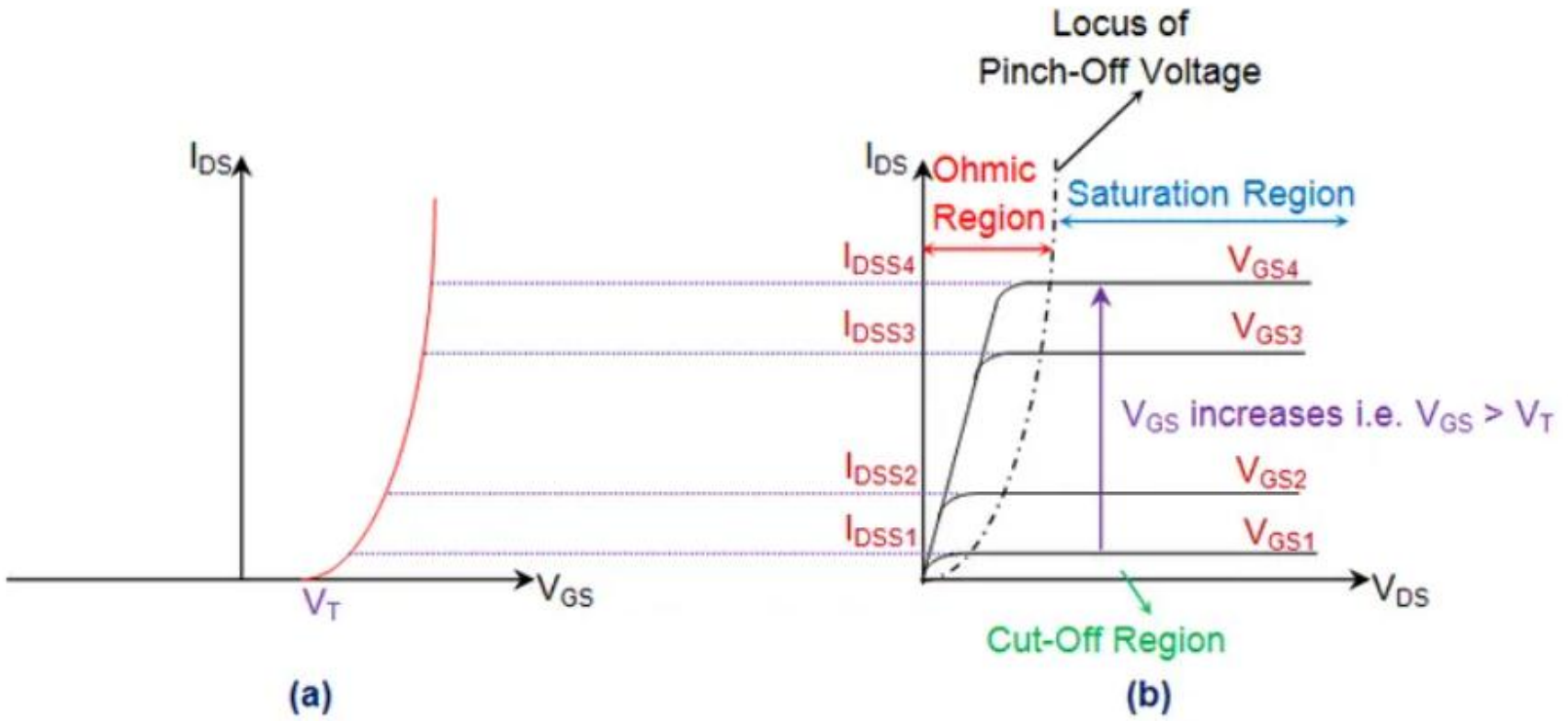
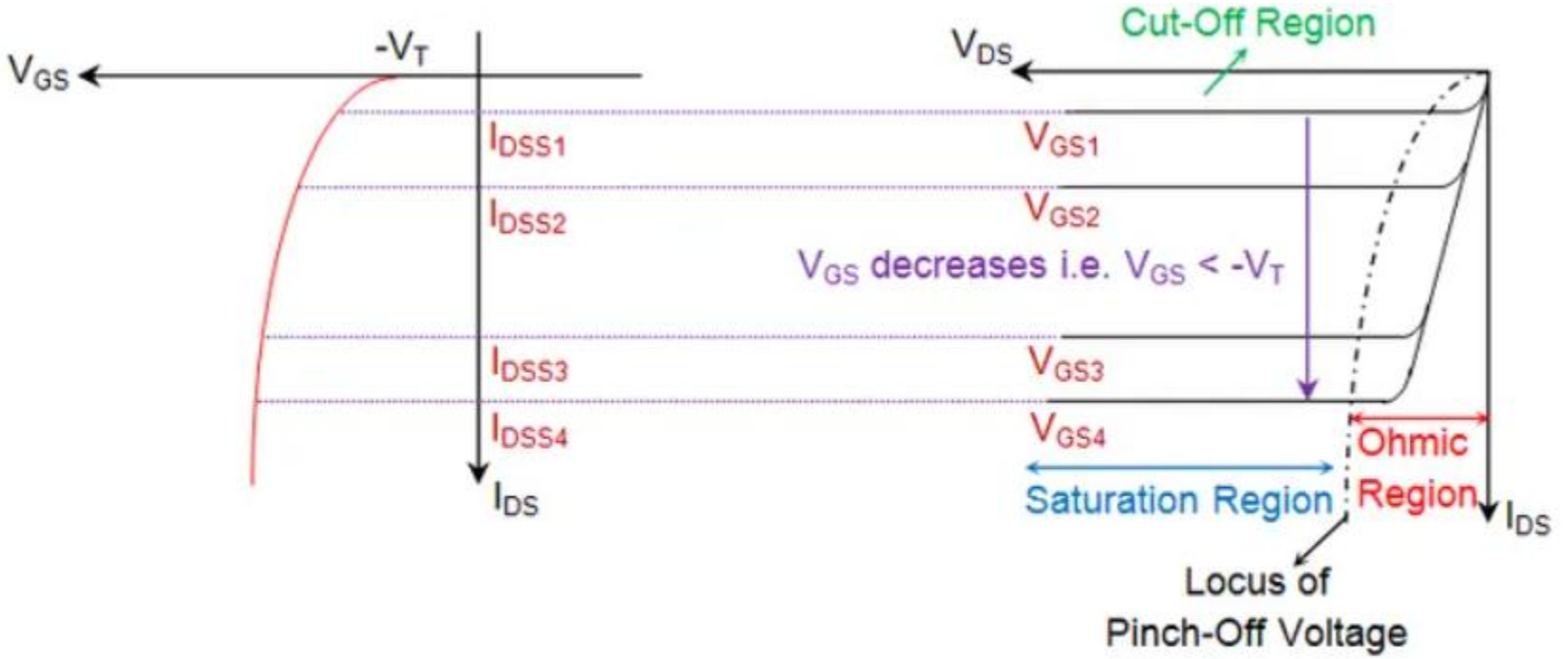


Figure 1 *n*-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics

Transfer characteristics

- The transfer characteristics (drain-to-source current I_{DS} versus gate-to-source voltage V_{GS}) of **n-channel Enhancement-type MOSFETs**. From this, it is evident that the current through the device will be zero until the V_{GS} exceeds the value of threshold voltage V_T. This is because under this state, the device will be void of channel which will be connecting the drain and the source terminals. Under this condition, even an increase in V_{DS} will result in no current flow as indicated by the corresponding output characteristics (I_{DS} versus V_{DS}) shown by Figure 1b. As a result this state represents nothing but the cut-off region of MOSFET's operation.
- Next, once V_{GS} crosses V_T, the current through the device increases with an increase in I_{DS} initially (Ohmic region) and then saturates to a value as determined by the V_{GS} (saturation region of operation) i.e. as V_{GS} increases, even the saturation current flowing through the device also increases. This is evident by Figure 1b where I_{DSS2} is greater than I_{DSS1} as $V_{GS2} > V_{GS1}$, I_{DSS3} is greater than I_{DSS2} as $V_{GS3} > V_{GS2}$, so on and so forth. Further, Figure 1b also shows the locus of pinch-off voltage (black discontinuous curve), from which V_P is seen to increase with an increase in $V_{GS.}$

p-channel MOSFET

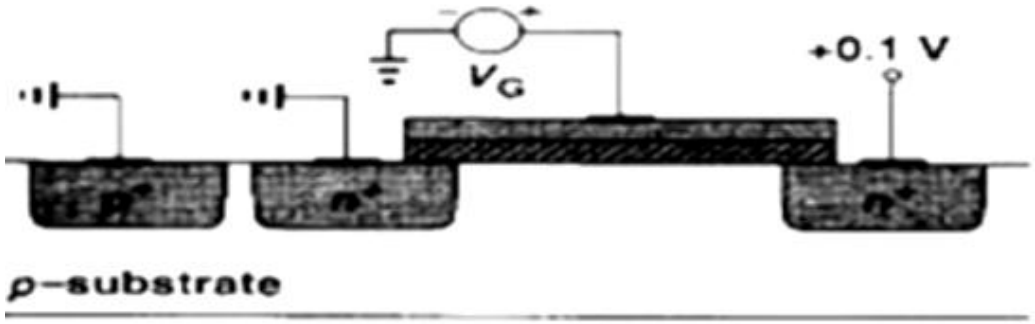


(a) (b)

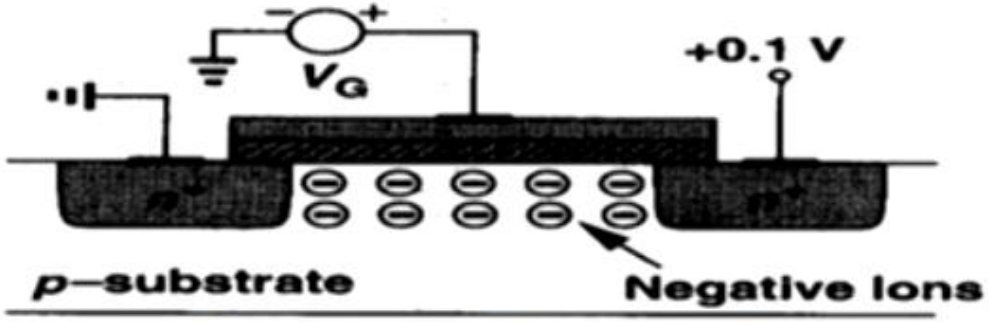
Figure 2 ***p*-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics**

Threshold Voltage of MOSFET

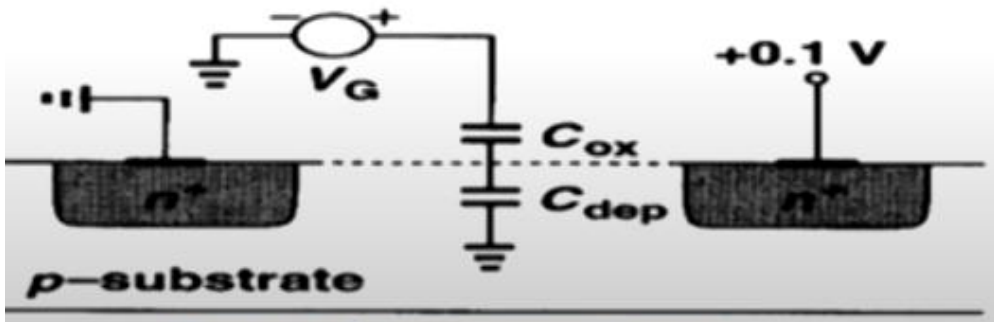
- With keeping constant drain bias, we'll analyze the different modes



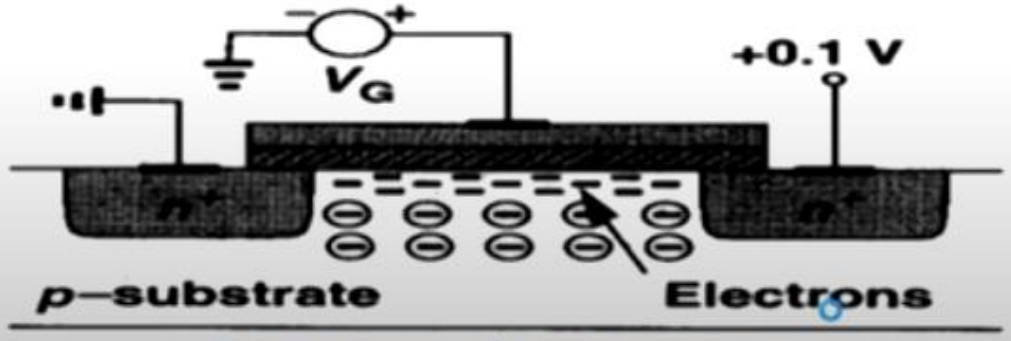
Device under consideration



Formation of Depletion Region



Onset of Inversion Layer



Formation of Inversion Layer

- As the gate and substrate forms a capacitor, the applied V_G images a opposite charge on the substrate.
- The increase in V_G increases the drop across gate-oxide and also the width of depletion region. Therefore, depletion capacitance (C_{dep}) and oxide capacitance (C_{ox}) are in series.
- Now, what would be the threshold value?

➢ The value of minimum gate voltage which inverts the surface, and hence an effective channels gets formed.

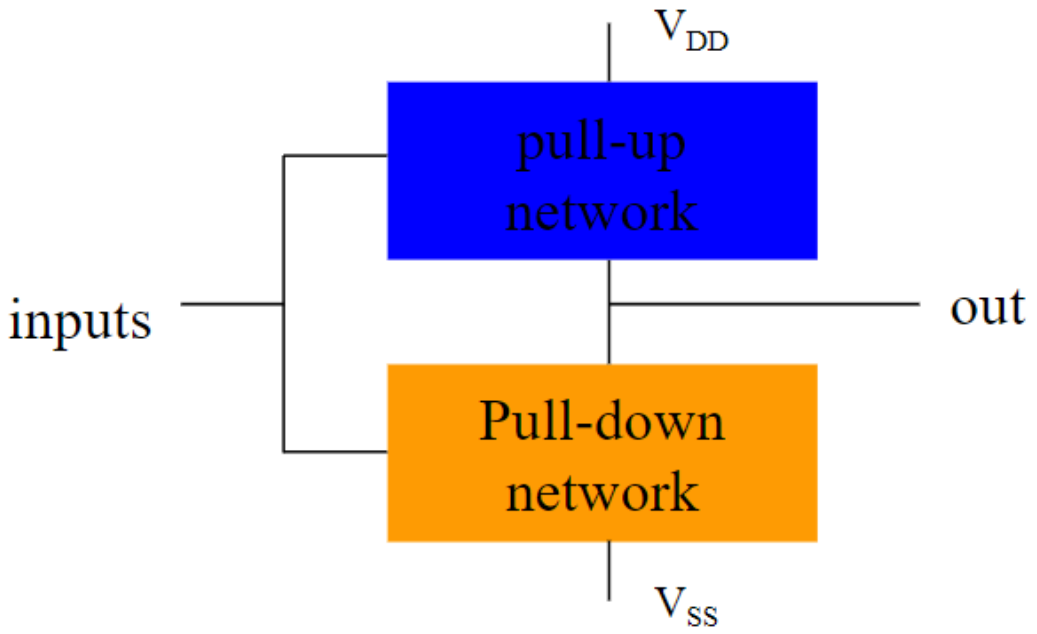
$$V_{TH}=\Phi_{MS}+2\Phi_F+\frac{Q_{dep}}{C_{ox}}$$

where $\Phi_{MS}=\Phi_M-\Phi_S$ is difference between metal and semiconductor work-functions

CMOS structure

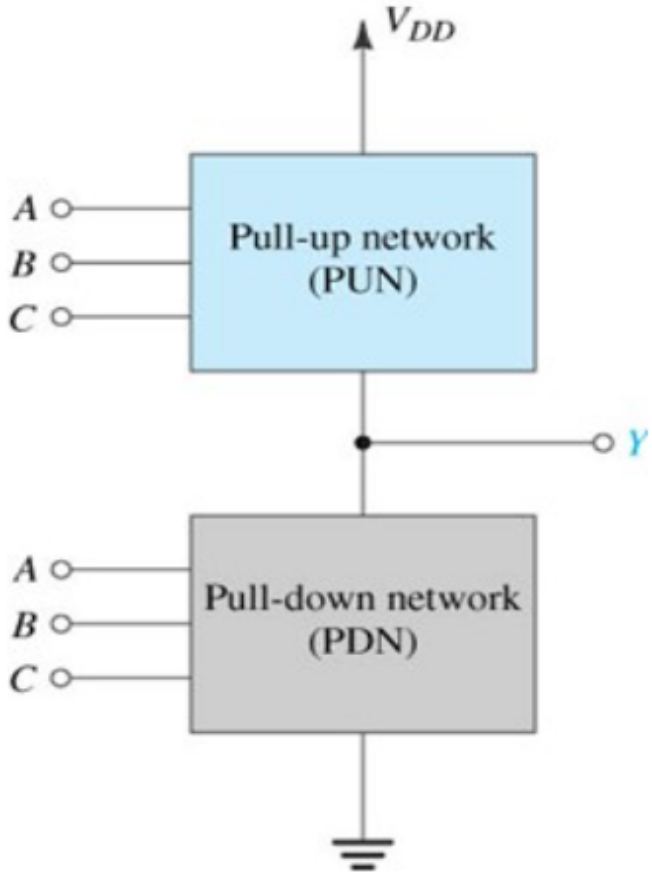
- Complementary CMOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*
  - a.k.a. static CMOS

Pull-up and pull-down networks



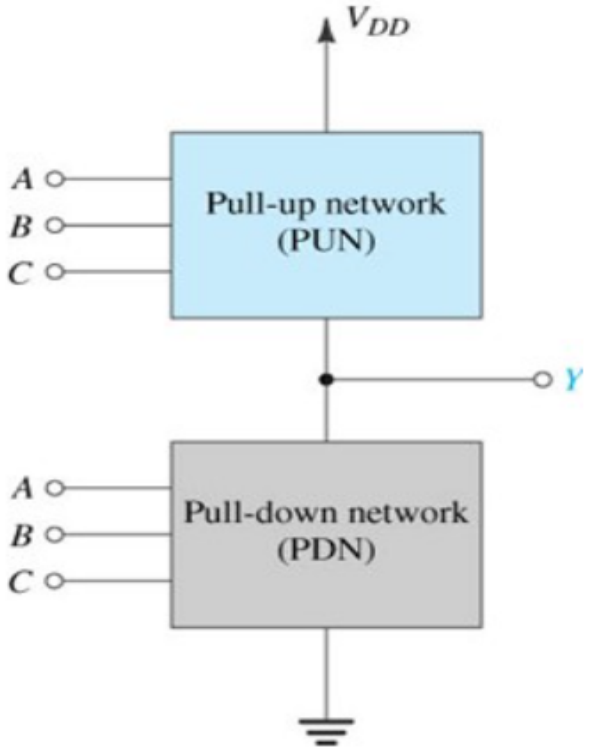
Basic structure

- When All Three input combinations are High **PDN** will conduct and will Pull the output node down to Ground making Output Low (Y=0) (Voltage Zero)
- Simultaneously, PUN will be OFF and no path will Exists between V_{DD} and Ground



Basic structure

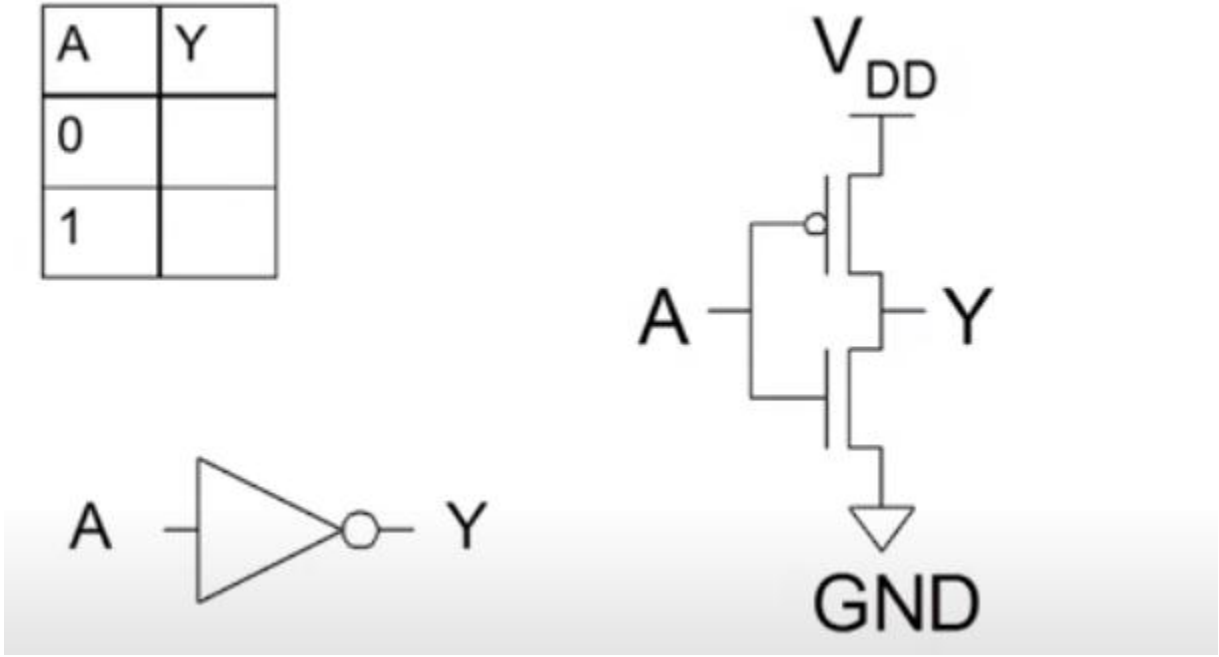
- When All Three input combinations are Low **PUN** will conduct and will Pull the output node Up to V_{DD} making Output High (Y=1) (Voltage = V_{DD})
- Simultaneously, PDN will be OFF and no path will Exists between V_{DD} and Ground



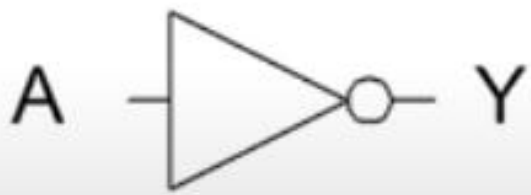
CMOS Inverter

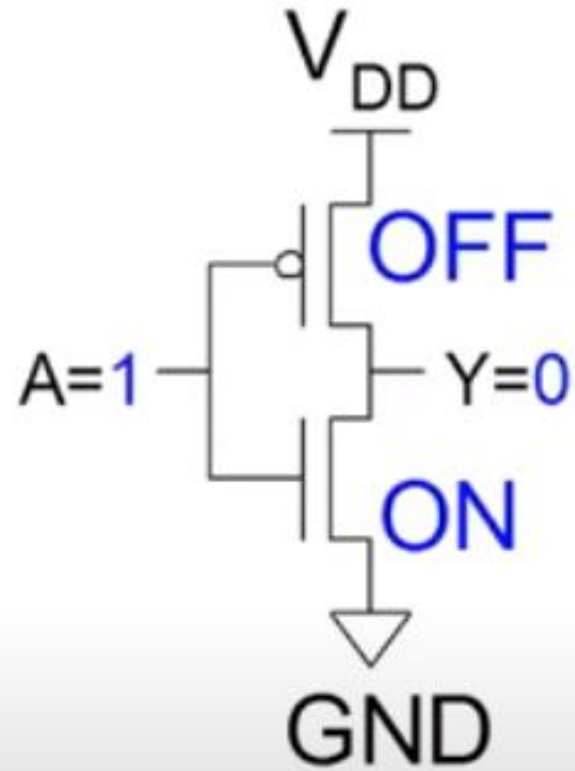
-

A	Y
0	
1	

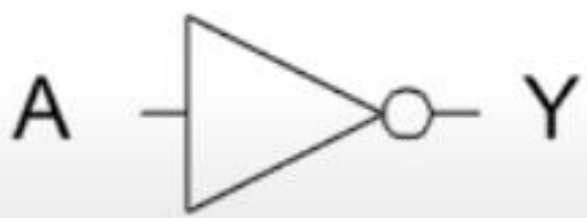


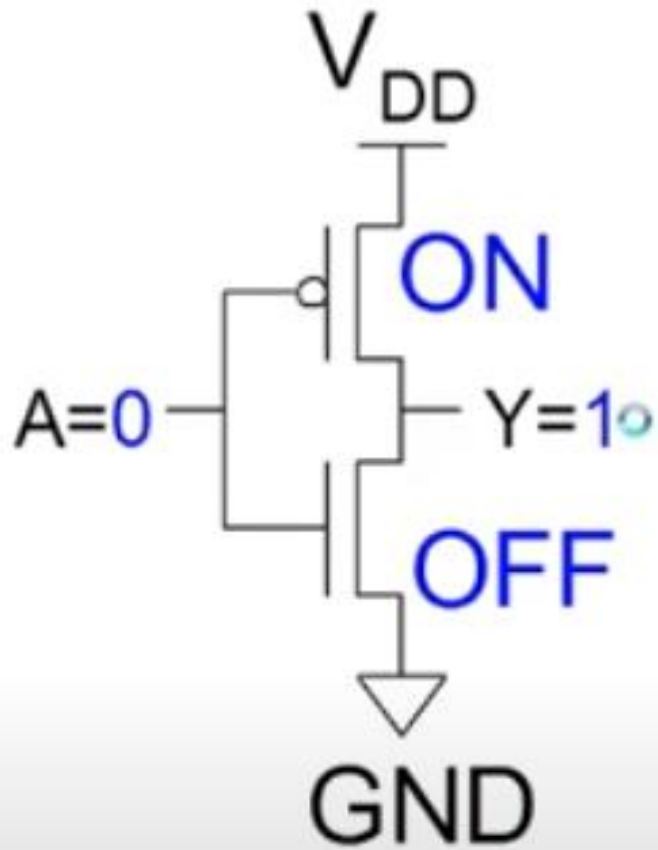
A	Y
0	
1	**0**





A	Y
0	1
1	0

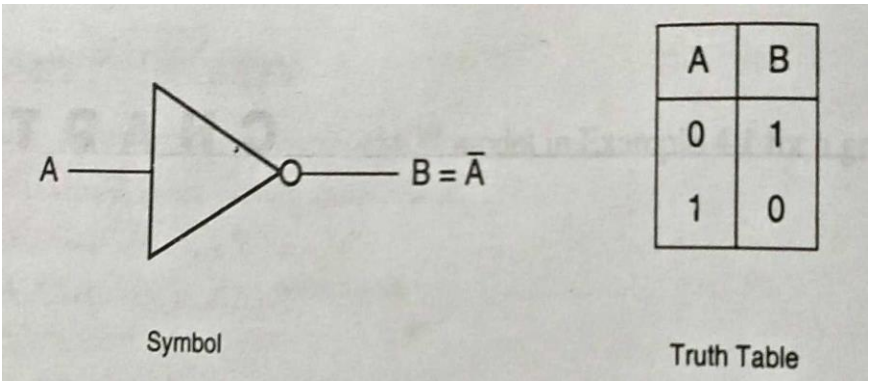




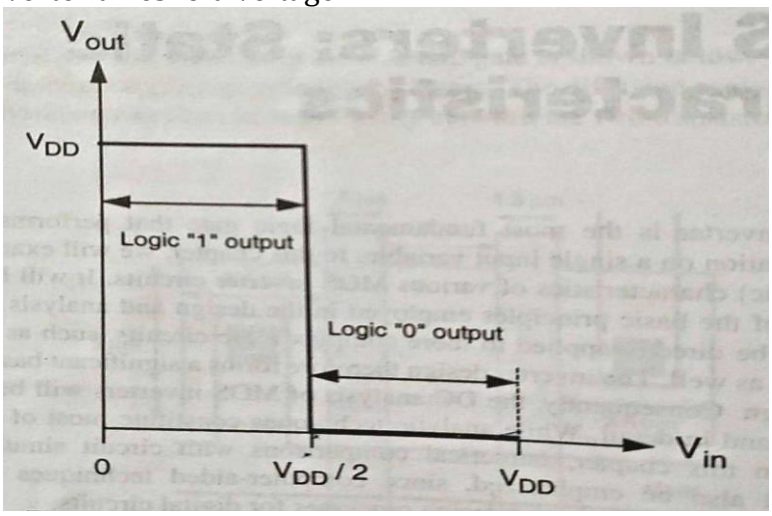
MOS INVERTER

BASIC NMOS INVERTER-

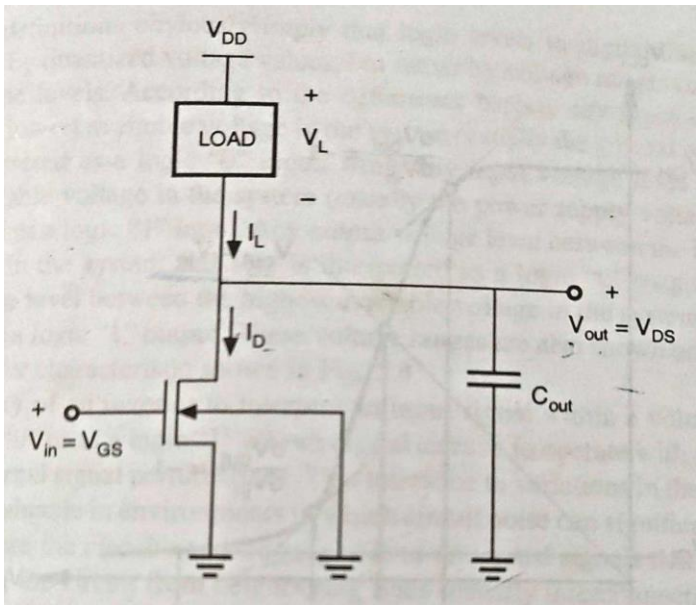
- In ideal inverter circuits, both the input variable A and the output variable B are represented by node voltages.



- Here the Boolean value of '1' means logic 1 can be represented by a high voltage of V_{DD} and the Boolean value of '0' means logic '0' can be represented by a low voltage of '0'. The voltage V_{th} is called the inverter threshold voltage.

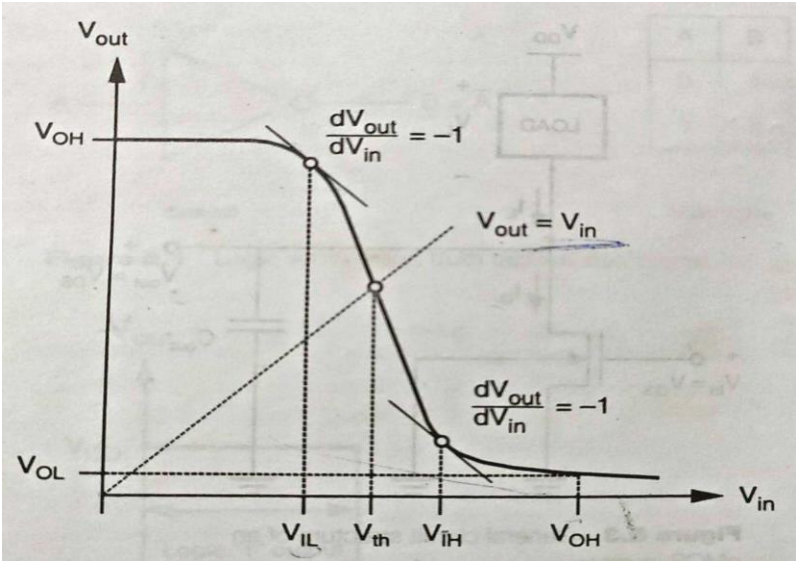


- For any input voltage between 0 to V_{th} the output voltage is equal to V_{DD}. The output switches from V_{DD} to 0 when the input is equal to V_{th}.
- For any input voltage between V_{th} andV_{DD}, the output voltage is equal to '0'. Thus an input voltage $0 \leq V_{in} < V_{th}$ is interpreted by this ideal inverter as a logic '0'.While an input voltage $V_{th} < V_{in} \leq V_{DD}$ is interpreted as a logic '1'.



- The input voltage of the inverter circuit is the gate to source voltage of the NMOS transistor. While the output voltage of the circuit is equal to the drain to source voltage.
- The source and the substrate terminals of the NMOS transistor are connected to ground potential. Hence $V_{SB} = 0$. The NMOS transistor is used as a driver transistor.
- The drain of NMOS is connected to the output terminal. The load device is represented as a two terminal circuit element with terminal currentI_L *and terminal voltage* V_L.
- One terminal of the load device is connected to the drain of the NMOS, while the other terminal is connected to V_{DD}.

VTC Curve-



- VTC curve, which is a plot of input vs output voltage. The VTC indicates that for low input voltage the circuit output is high and for high input, the output decreases towards 0 volt.
- Applying Kirchhoff's current law, the load current is always equal to the NMOS drain current.

$$I_D = I_L$$

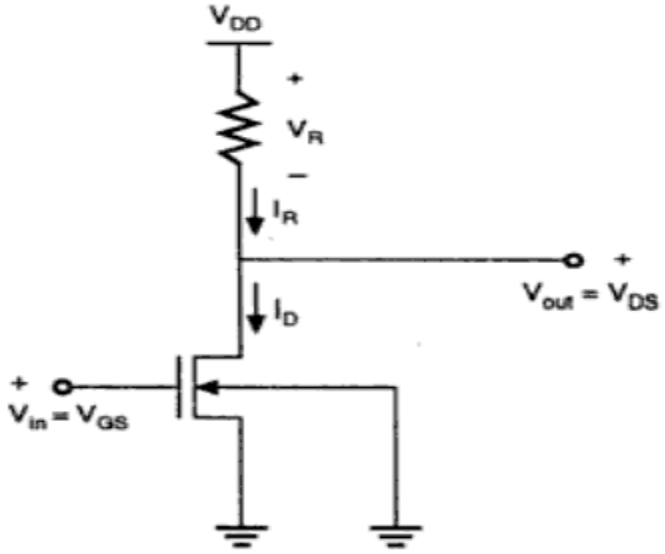
- For very low input voltage levels the output voltage V_{out} is equal to the high value of V_{OH}. The driver NMOS transistor is in cut off and hence does not conduct any current. The voltage drop across the load device is very small in magnitude and the output voltage is high.
- As the input voltage V_{in} increases, the driver transistor starts conducting a drain current and the output voltage starts to decrease. This drop in the output voltage level does not occur abruptly but in an ideal inverter it occur abruptly.
- In this curve two critical voltage points are present, where the slope becomes equal to -1.

$$\frac{dV_{out}}{dV_{in}} = -1$$

- The smaller input voltage at which first slope occur is called the input low voltage 'V_{IL}' and the larger input voltage at which second slope occur is called the input high voltage 'V_{IH}'.
- As the input voltage is further increased, the output voltage continues to drop and reaches a value of 'V_{OL}', when the input voltage is equal to 'V_{OH}'. The inverter threshold voltage V_{th} which is considered as the transition voltage is defined as the point where $V_{OUT} = V_{in}$.

RESISTIVE LOAD INVERTER-

Here, enhancement type nMOS acts as the driver transistor. The load consists of a simple linear resistor R_L. The power supply of the circuit is V_{DD} and the drain current I_D is equal to the load current I_R.



Circuit Operation

- When the input of the driver transistor is less than threshold voltage, driver transistor is in cut off region and does not conduct any current. So, the voltage drop across the load resistor is zero and output voltage is equal to the V_{DD}.
- Here $I_R = I_D$.
- So, output voltage V_{out} is

$$V_{out} = V_{DD} - I_R R$$

$$V_{out} = V_{DD} - I_D R$$

- So, Drain current equation will be

$$I_D = \frac{V_{DD} - V_{out}}{R}$$

- When the input voltage increases further, driver transistor will start conducting the non-zero current and NMOS goes in saturation region.
- if MOSFET is there in saturation region then

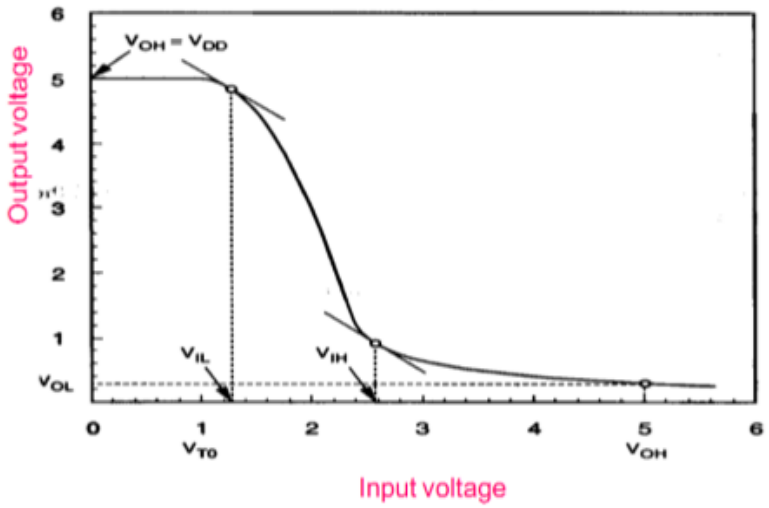
$$V_{in} - V_{To} < V_{out} \text{ and } I_D = \frac{K}{2}(V_{GS} - V_{TO})^2$$

- If MOSFET is there in linear region then

$$V_{in} - V_{To} > V_{out} \text{ and } I_D = \frac{K}{2}[2(V_{GS} - V_{TO})V_{DS} - V_{DS}^2]$$

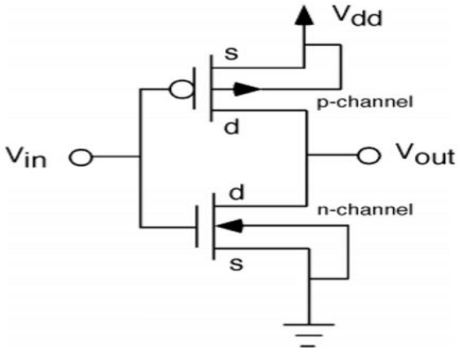
VTC curve-

- Initially when input is at lower voltage, the NMOS is at cut off region, the V_{out} is equal to V_{DD} until the NMOS is not turned ON.
- Once the NMOS turned ON, slow decrease in output voltage starts.



CMOS INVERTER-

In CMOS inverter NMOS work as driver and PMOS transistors work as load and always one transistor is ON, other is OFF.



This configuration is called **complementary MOS (CMOS)**. The input is connected to the gate terminal of both the transistors such that both can be driven directly with input voltages. Substrate of the NMOS is connected to the ground and substrate of the PMOS is connected to the power supply, V_{DD}.

So $V_{SB} = 0$ for both the transistors.

$$V_{GS,n} = V_{in}$$

$$V_{DS,n} = V_{OUT}$$

And,

$$V_{GS,n} = V_{in} - V_{DD}$$

$$V_{DS,n} = V_{out} - V_{DD}$$

When the input of nMOS is smaller than the threshold voltage ($V_{in} < V_{TO,n}$), the nMOS is cut – off and pMOS is in linear region. So, the drain current of both the transistors is zero.

$$I_{D,n} = I_{D,p} = 0$$

Therefore, the output voltage V_{OH} is equal to the supply voltage.

$$V_{out} = V_{OH} = V_{DD}$$

When the input voltage is greater than the $V_{DD} + V_{TO,p}$, the pMOS transistor is in the cutoff region and the nMOS is in the linear region, so the drain current of both the transistors is zero.

$$I_{D,n} = I_{D,p} = 0$$

Therefore, the output voltage V_{OL} is equal to zero.

$$V_{out} = V_{OL} = 0$$

The nMOS operates in the saturation region if $V_{in} > V_{TO}$ and if following conditions are satisfied.

$$V_{DS,n} \geq V_{GS,n} - V_{TO,n}$$

$$V_{out} \geq V_{in} - V_{TO,n}$$

The pMOS operates in the saturation region if $V_{in} < V_{DD} + V_{TO,p}$ and if following conditions are satisfied.

$$V_{DS,P} \leq V_{GS,P} - V_{TO,P}$$

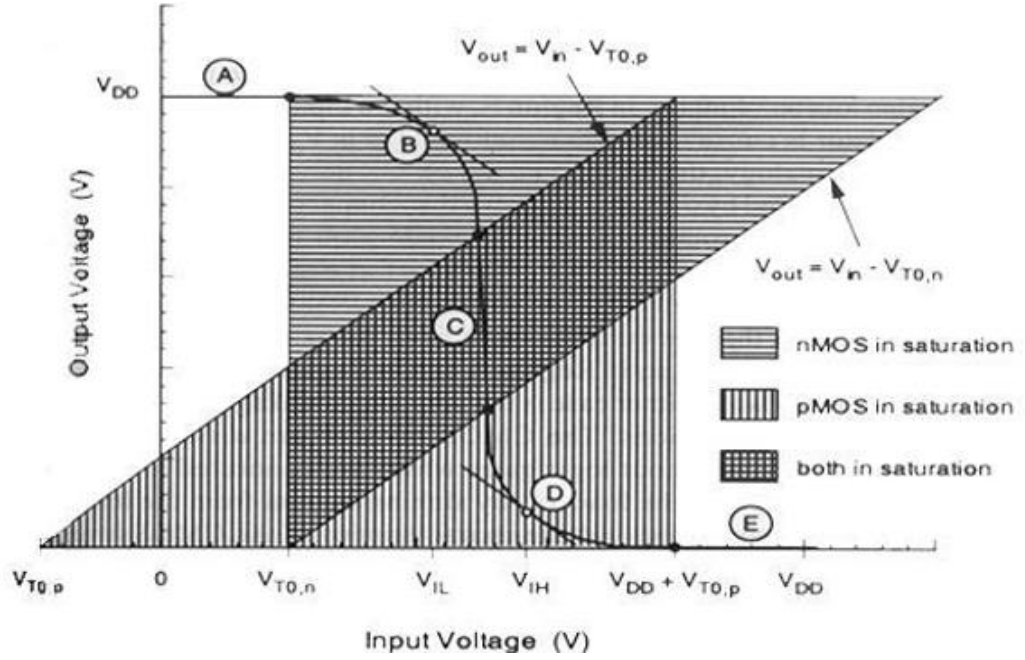
$$V_{out} \geq V_{in} - V_{TO,P}$$

For different value of input voltages, the operating regions are listed below for both transistors.

Region	**V_{in}**	**V_{out}**	**nMOS**	**pMOS**
A	$< V_{TO,n}$	V_{OH}	Cut – off	Linear
B	V_{IL}	High ≈ V_{OH}	Saturation	Linear
C	V_{th}	V_{th}	Saturation	Saturation

D	V_{IH}	Low ≈ V_{OL}	Linear	Saturation
E	> (V_{DD} + $V_{TO,p}$)	V_{OL}	Linear	Cut – off

The VTC of CMOS is shown in the figure below –



INTERCONNECT EFFECTS-

DELAY TIME DEFINATION-

The propagation delay times τ_{PHL} and τ_{PLH} determine the input to output signal delay during the high to low and low to high transitions of the output, respectively.

Definition-

τ_{PHL} is the time delay between the $V_{50\%}$ transition of the rising input voltage and the $V_{50\%}$transition of the falling output voltage.

τ_{PLH} is the time delay between the $V_{50\%}$ transition of the falling input voltage and the $V_{50\%}$transition of the rising output voltage.

τ_{PHL} becomes the time required for the output voltage to fall from V_{OH} to the $V_{50\%}$ level and

τ_{PLH} becomes the time required for the output voltage to rise from V_{OL} to the $V_{50\%}$ level.

$$V_{50\%} = V_{OL} + \frac{1}{2}(V_{OH} - V_{OL})$$