SINGAPORE UNIVERSITY OF TECHNOLOGY AND DESIGN

Term 7- Sept 2025

Nanoelectronics and Technology (01.119/99.503)-Week 2 Class 1

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23-Sept- 2025

Outline

- Schottky Diodes
- Ohmic contact
- Introduction to MOS structure
- MOSFET structure

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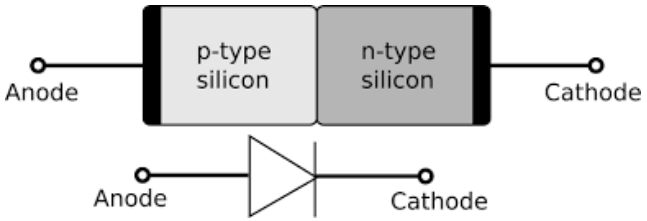
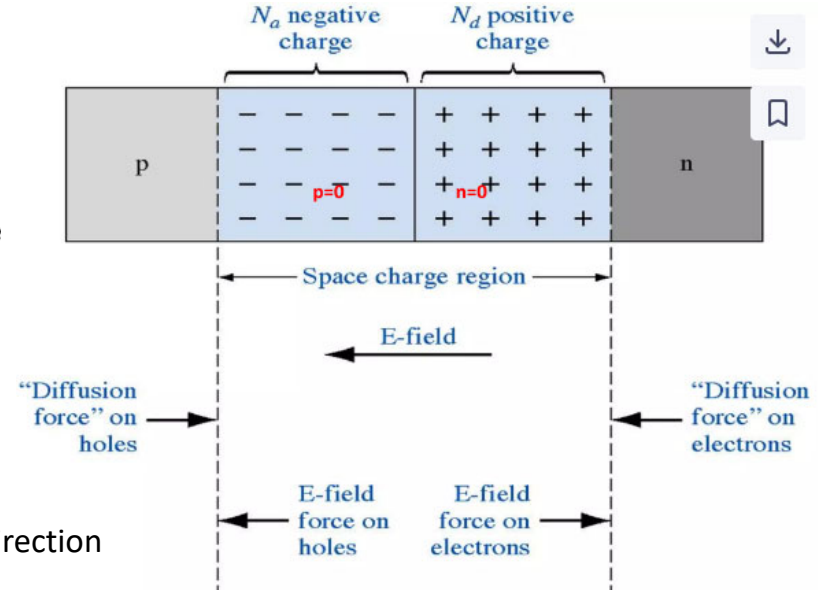
P-N Junction (Diode)

A p-n junction diode is a basic semiconductor device that controls the flow of electric current in a circuit. It has a positive (p) side and a negative (n) side created by adding impurities to each side of a silicon semiconductor.





- Current only flows in forward bias
- **Diodes** allow for current to flow in one direction and rectify (change AC to DC)

https://www.slideshare.net/slideshow/p-n-junctioneema/68227503

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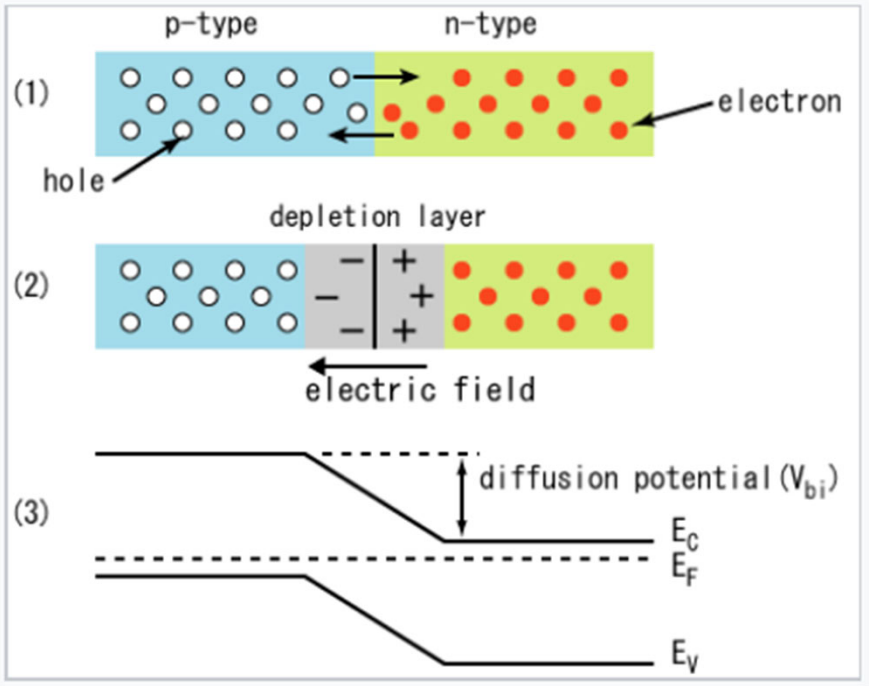
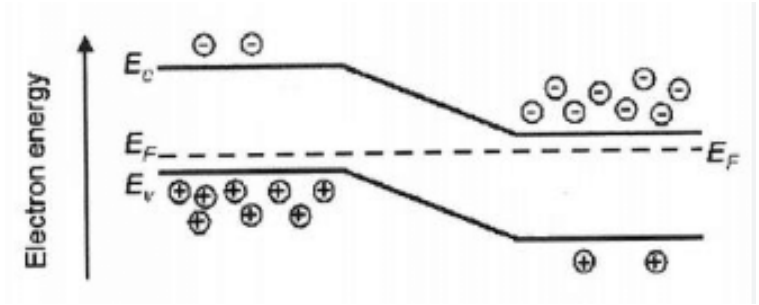
P-N Junction (Diode)-Built in potential



The built-in potential of a P-N junction is the potential difference that develops at the intersection of its p-type semiconductor material and n-type semiconductor material. This built-in potential develops in the depletion region.



https://study.com/academy/lesson/p-n-junction-diode-definition-properties.html

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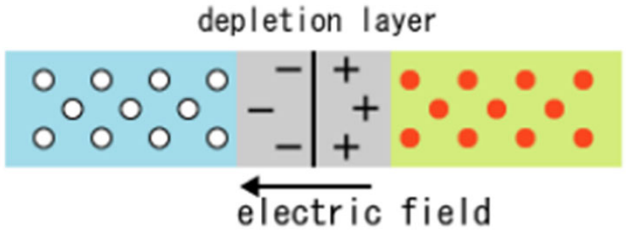
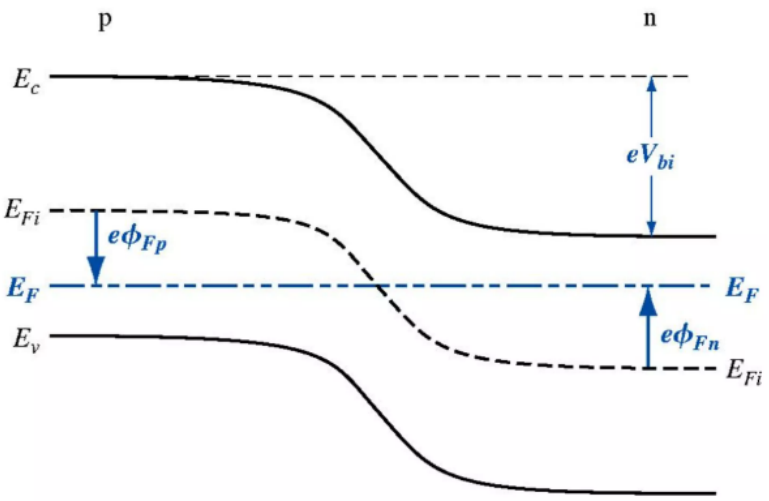
P-N Junction (Diode)-Built in potential





$$\phi_{\mathrm{bi}} = \frac{kT}{q}\ln\frac{N_{\mathrm{d}}N_{\mathrm{a}}}{n_{\mathrm{i}}^2}$$

The built-in potential of a P-N junction is the potential difference that develops at the intersection of its p-type semiconductor material and n-type semiconductor material. This built-in potential develops in the depletion region.

Formula

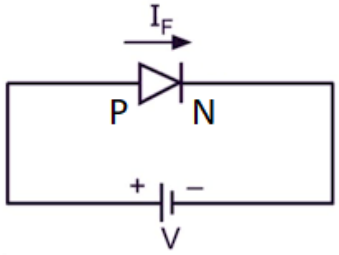
PN Junction Built-in Potential

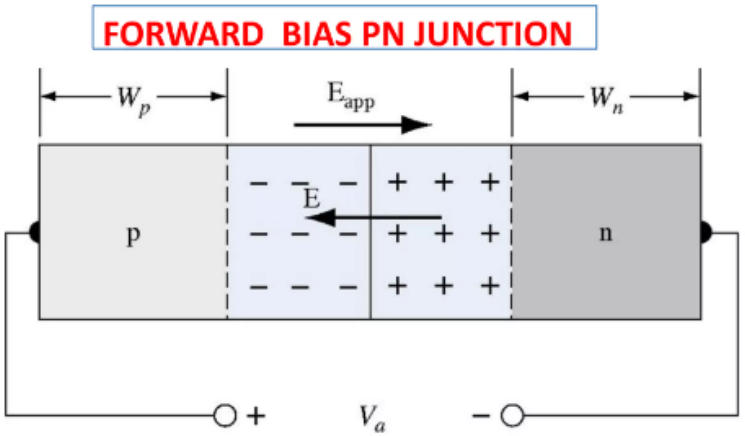
$$V_{\text{built-in}} = \frac{kT}{q}\ln\left(\frac{N_D N_A}{n_i^2}\right)$$

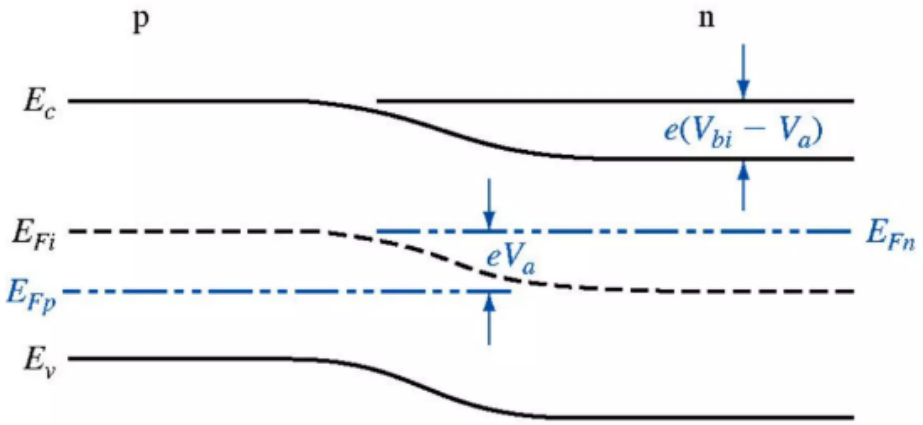
$V_{\text{built-in}}$	→	Built-in potential in volts
N_D	→	n type - donor atoms concentration
N_A	→	p type - acceptor atoms concentration
n	→	concentration of electrons
kT/q	→	thermal voltage
T	→	temperature in Kelvin
q	→	charges in coulombs

P-N Junction (Diode)-Forward Bias

When positive terminal of the source is connected to the P side and the negative terminal is connected to N side then the junction diode is said to be connected in forward bias condition.







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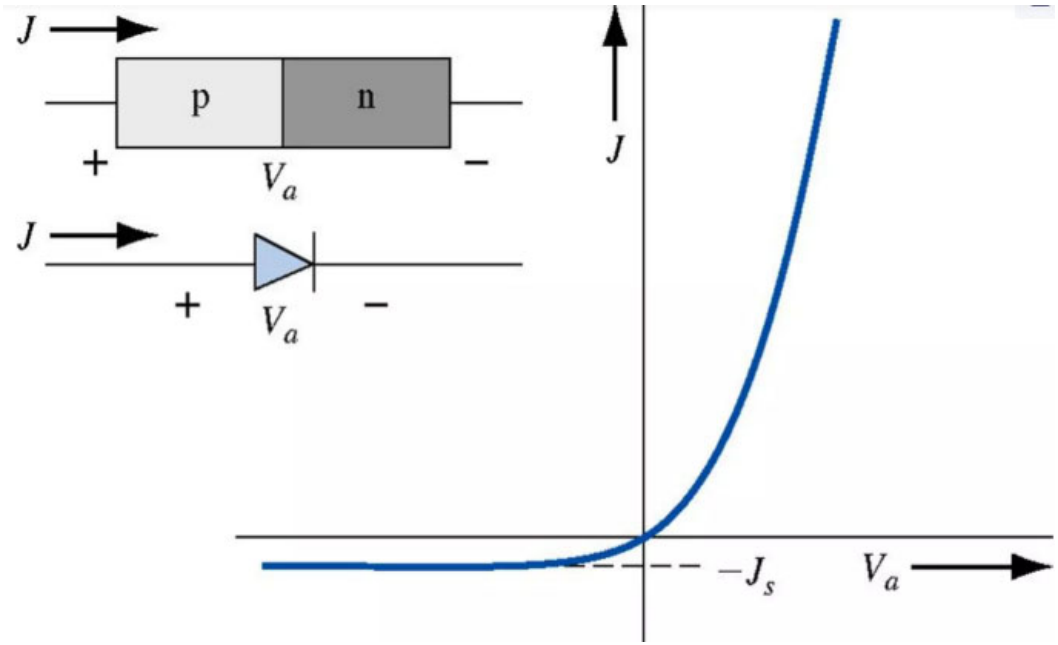
P-N Junction (Diode)-Forward Bias



$$J \simeq J_s \left[\exp\left(\frac{eV_a}{kT} \right) - 1 \right]$$

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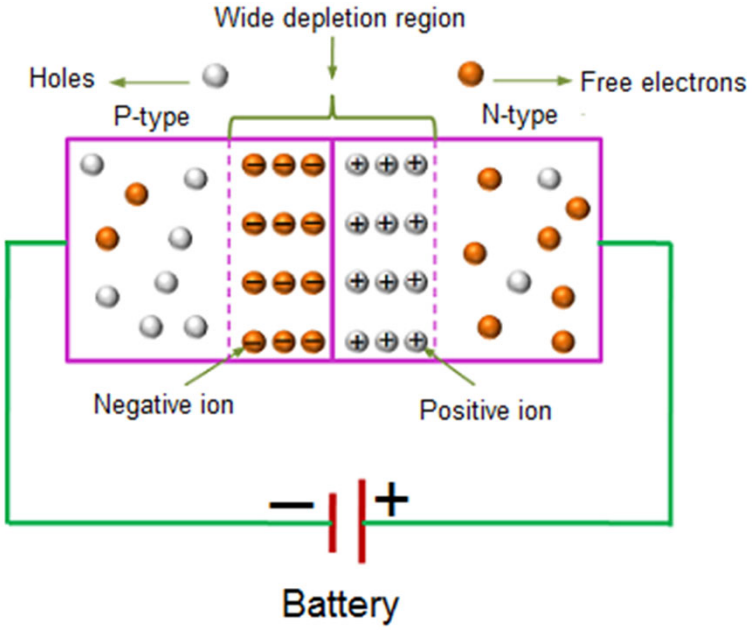
P-N Junction (Diode)-Reverse Bias



- Positive terminal attracts the electrons away from the junction in N side and negative terminal attracts the holes away from the junction in P side.
- As a result of it, the width of the potential barrier increases that impedes the flow of majority carriers in N side and P side.

https://www.physics-and-radio-electronics.com/electronic-devices-and-circuits/semiconductor-diodes/reversebiaseddiode.html

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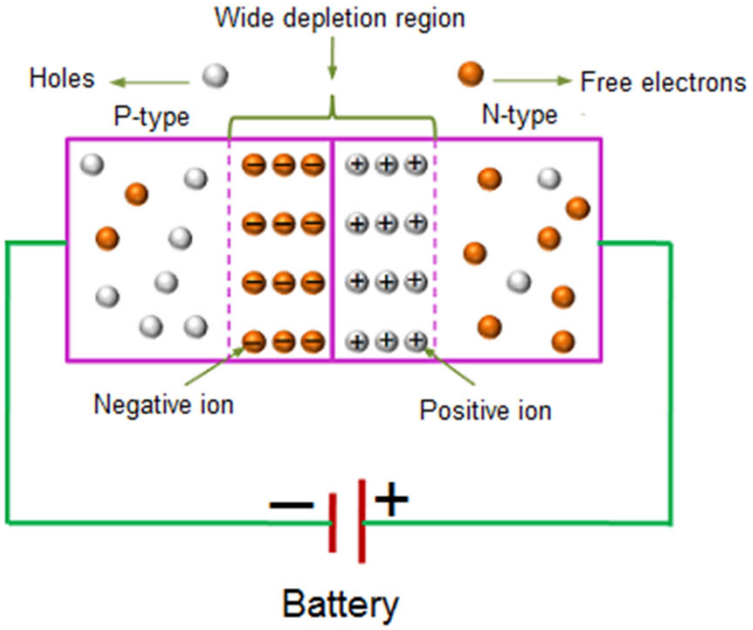
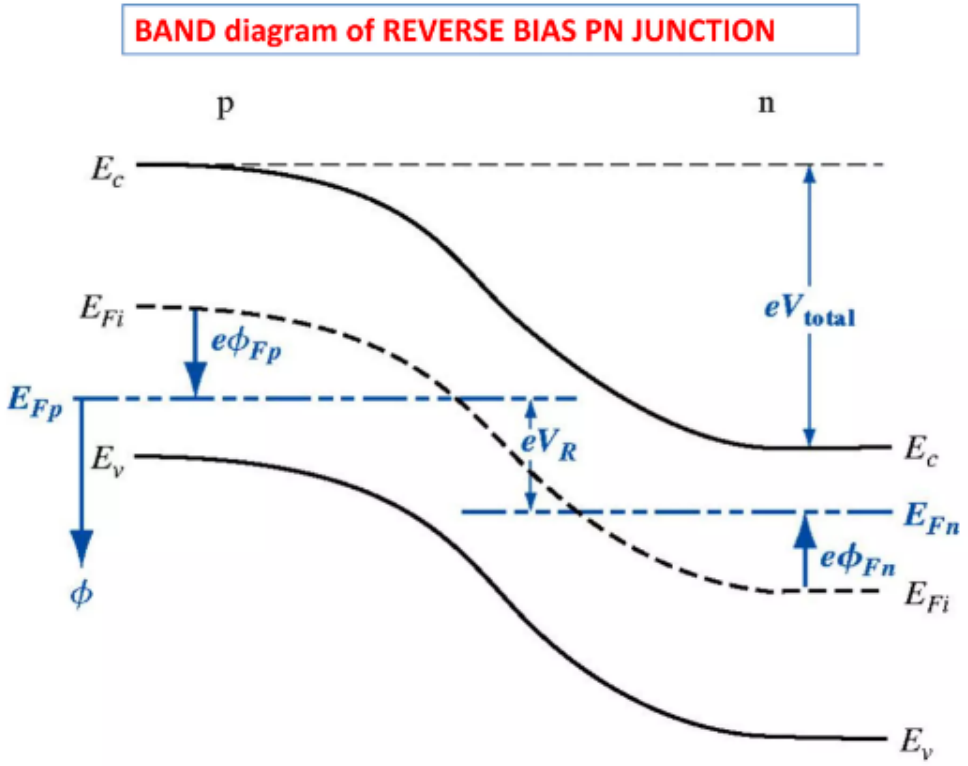
P-N Junction (Diode)-Reverse Bias





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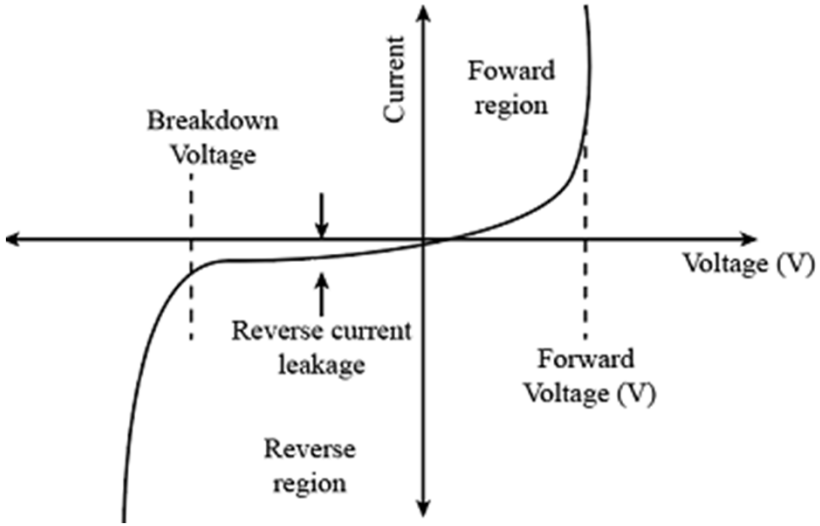
P-N Junction (Diode)-Reverse Bias



Breakdown occurs by two mechanisms.

(A) Zener Breakdown (Low Reverse Voltage, < ~5–6 V)

- Occurs in **heavily doped PN junctions** (narrow depletion region).
- Strong **electric field** develops across the narrow depletion layer.
- This field is strong enough to **break covalent bonds** and cause **quantum mechanical tunneling** of electrons from the valence band (P-side) into the conduction band (N-side).
- Result → sudden increase in current.
- Dominant in **low-voltage Zener diodes**.

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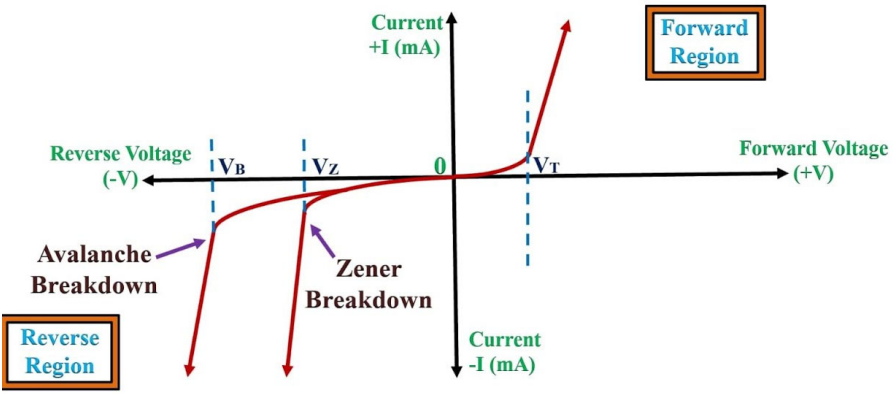
P-N Junction (Diode)-Reverse Bias

Avalanche and Zener Breakdown



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- Result → sudden increase in current.
- Dominant in **low-voltage Zener diodes**.

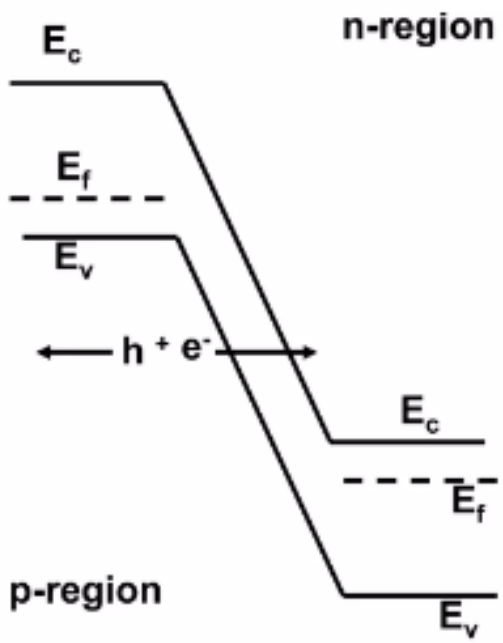
(B) Avalanche Breakdown (Higher Reverse Voltage, > ~6 V)

- Occurs in **lightly doped PN junctions** (wide depletion region).
- Minority carriers (electrons/holes) accelerated by the strong electric field gain enough energy to **ionize atoms** when they collide with the lattice.
- This generates **new electron-hole pairs**, which are again accelerated → **chain reaction (avalanche multiplication)**.
- Result → sharp rise in current.
- Dominant in **power diodes and high-voltage junctions**.

P-N Junction (Diode)-Reverse Bias

Zener Breakdown : Heavily doped junction

- the valence band edge of p-region will be at a higher potential than the conduction band edge of the n-region. Due to heavy doping depletion layer will be thin.
- Breakdown occurs due to electron tunneling between the valence band of the p-region and conduction band of the n-region. A large reverse current flows. This is known as **Zener Breakdown.**



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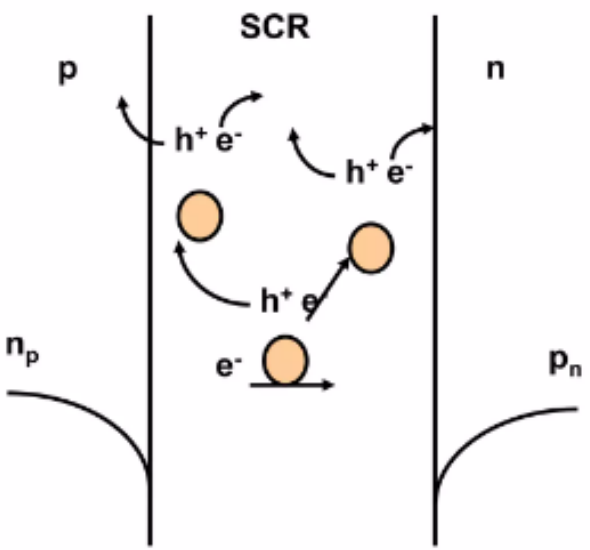
P-N Junction (Diode)-Reverse Bias

Avalanche Breakdown : in high electric field

- Electrons or holes traveling inside the SCR attain high velocity when reverse bias is high and collide with atoms dislodging an electron from the atom and causing an electron-hole pair to form, the process continues.
- This is known as **Avalanche multiplication,** resulting in a large reverse bias current leading to breakdown



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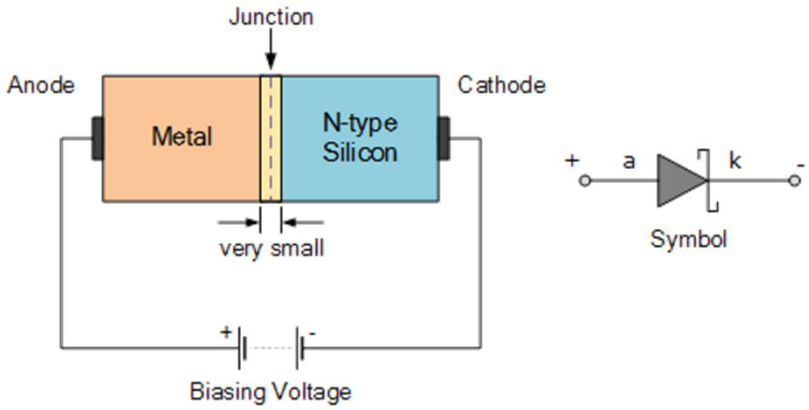
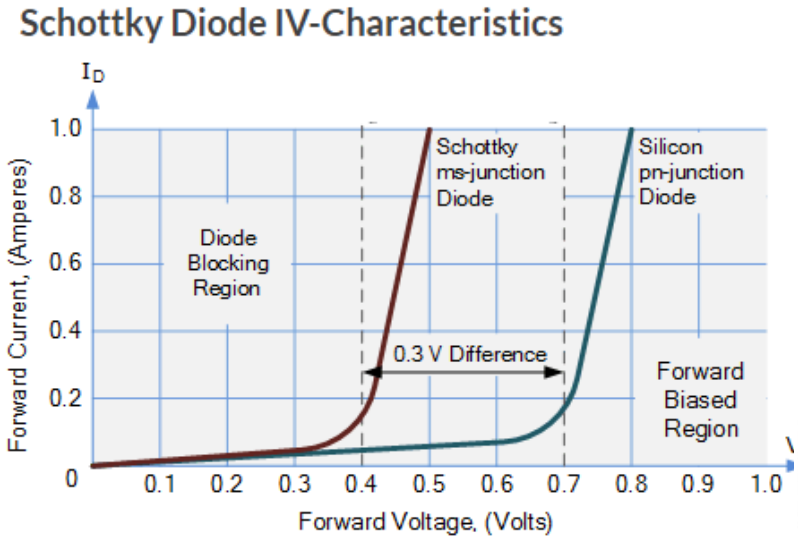
Schottky Diode: Metal-Semiconductor Junction

- The Schottky diode is a semiconductor diode formed by the junction of a semiconductor (N-type) with a metal.
- Current conduction is mainly due to **majority carriers** (usually electrons from the N-type side).
- It has a low forward voltage drop and a very fast switching action.
- The most common contact metal used for Schottky diode construction is “Silicide” which is a highly conductive silicon and metal compound.



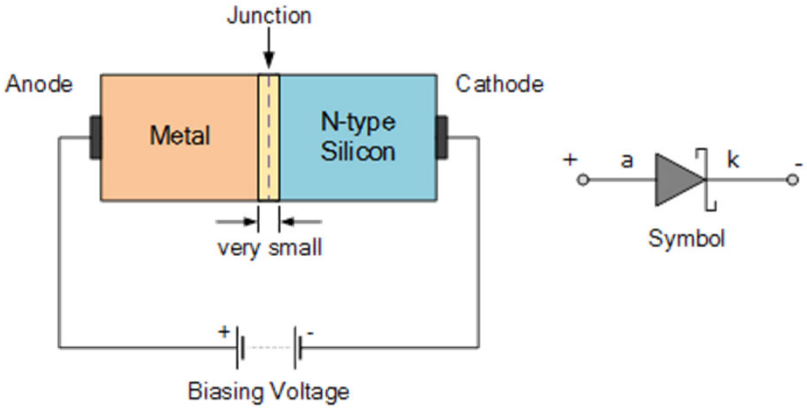


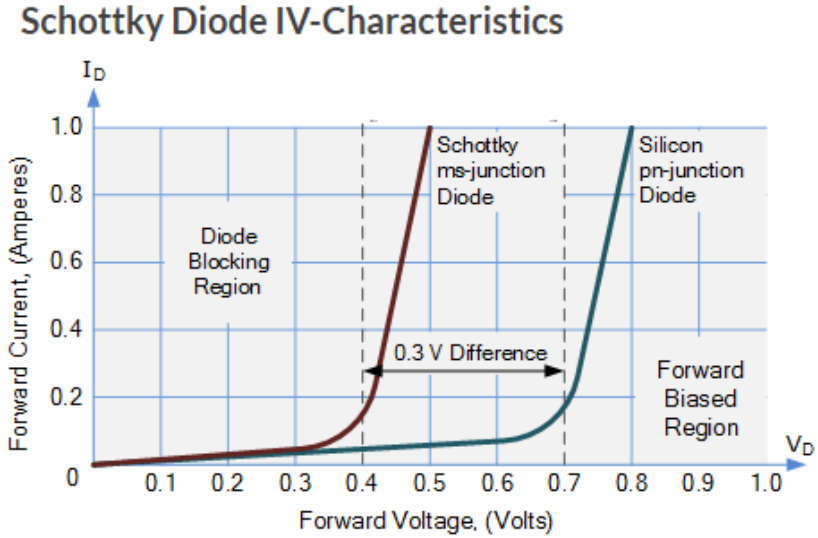
https://www.electronics-tutorials.ws/diode/schottky-diode.html

Schottky Diode: Metal-Semiconductor Junction

Barrier Potential

- **PN Diode**: Has a barrier potential of about **0.7 V (Si)**.
- **Schottky Diode**: Has a much lower barrier potential, typically **0.2–0.3 V**, because it is a metal–semiconductor junction.





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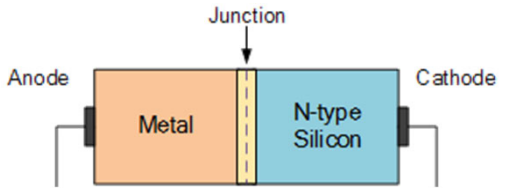
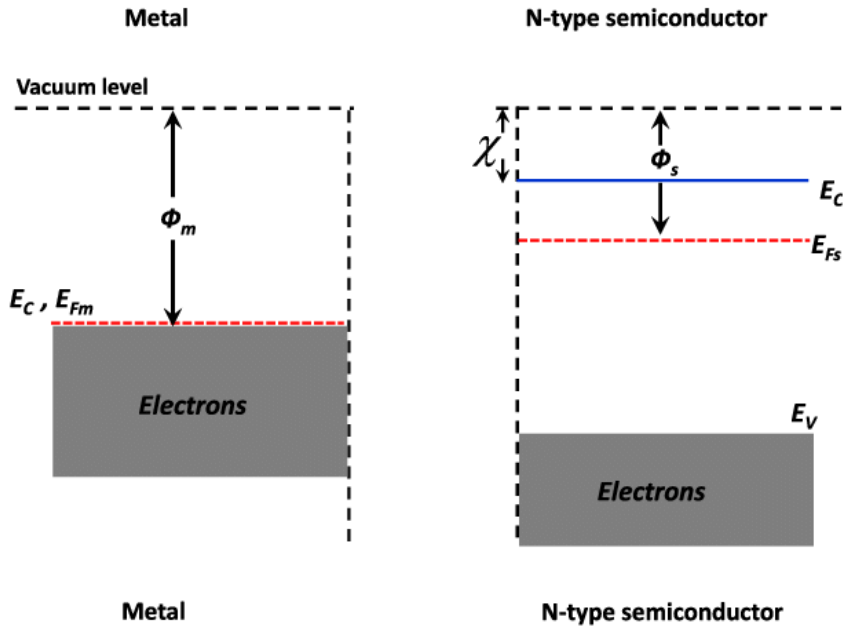
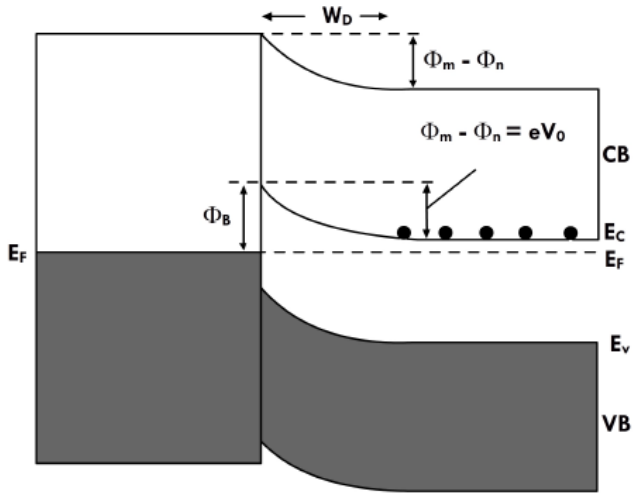
Schottky Diode: Metal-Semiconductor Junction

- **A Schottky junction is formed when the semiconductor has a lower work function than the metal.**







Equilibrium condition

https://www.icrfq.net/schottky-diode/

https://www.electronics-tutorials.ws/diode/schottky-diode.html

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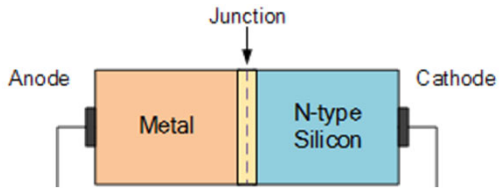
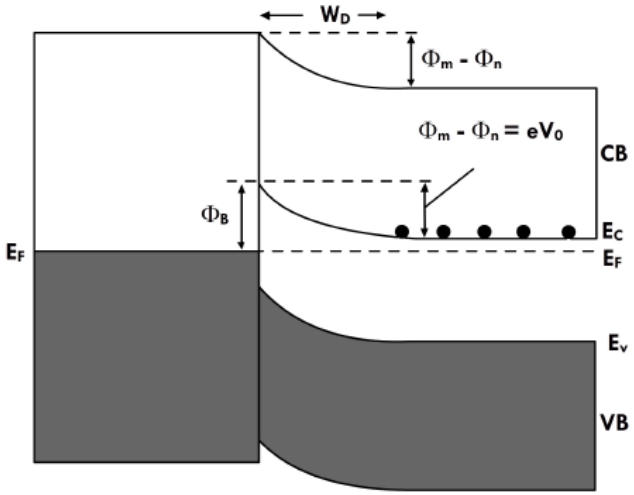
Schottky Diode: Metal-Semiconductor Junction





Equilibrium condition

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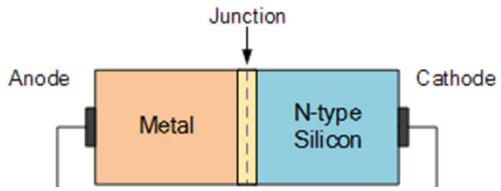
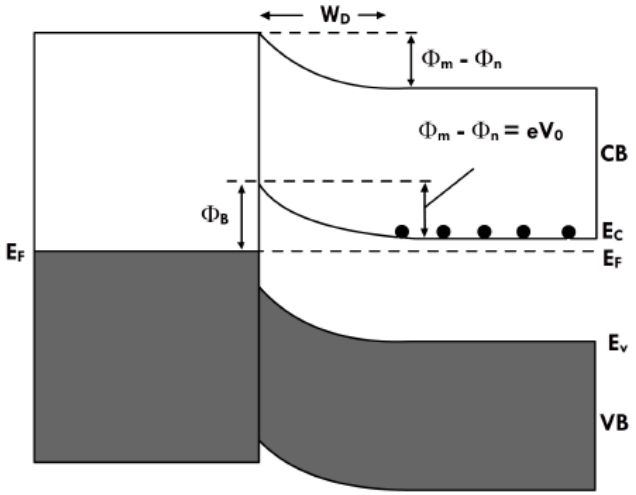
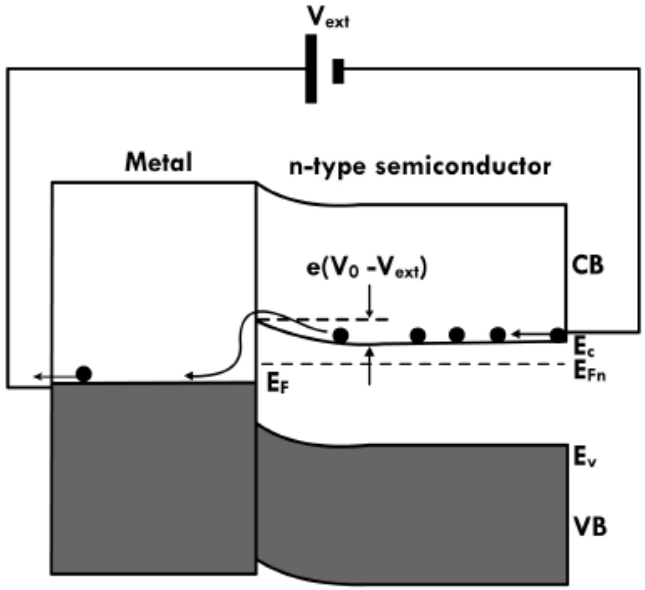
Schottky Diode: Metal-Semiconductor Junction (Forward Bias)





Equilibrium condition



Forward Bias

https://www.electronics-tutorials.ws/diode/schottky-diode.html

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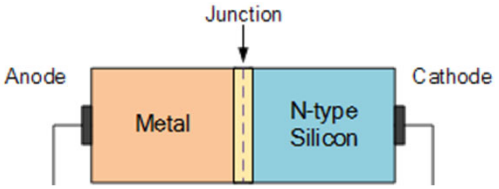
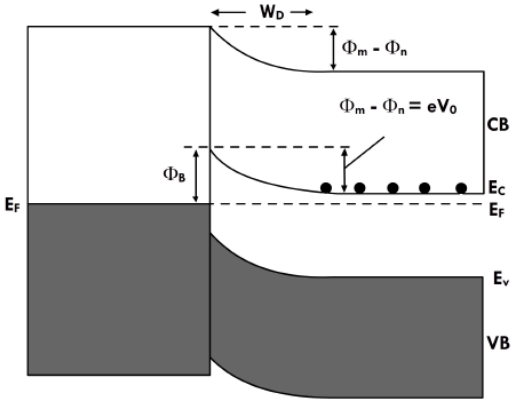
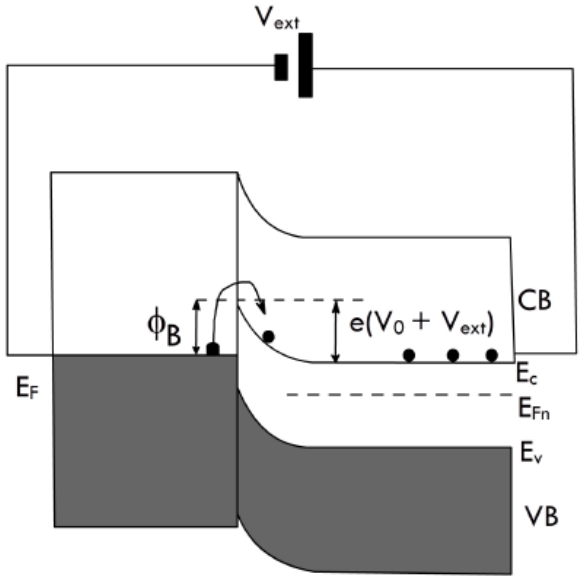
Schottky Diode: Metal-Semiconductor Junction (Reverse Bias)

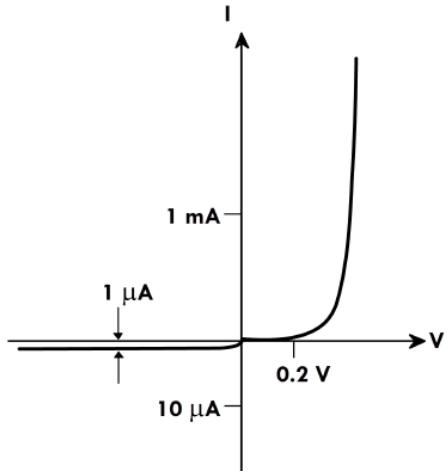




Equilibrium condition



Reverse Bias



https://www.electronics-tutorials.ws/diode/schottky-diode.html

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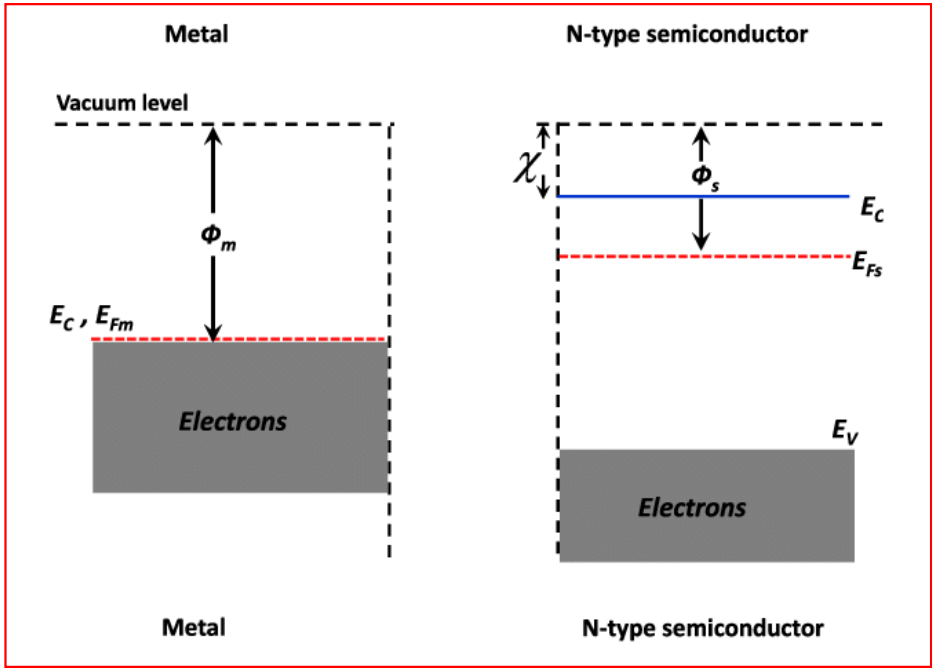
Ohmic Contact

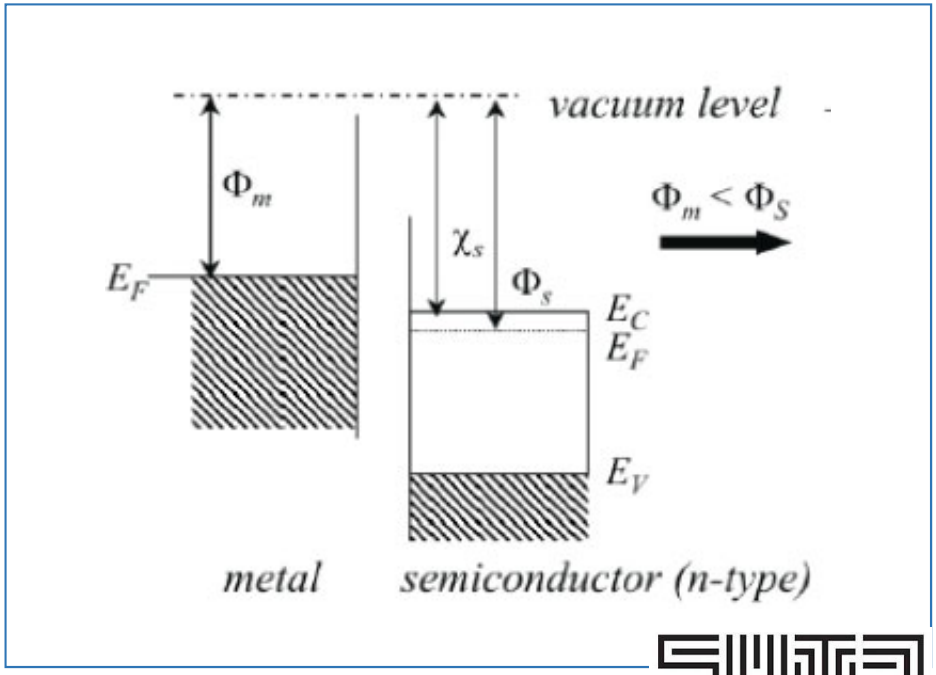
- A Schottky junction is formed when the semiconductor has a lower work function than the metal. When the semiconductor has a higher work function the junction formed is called the Ohmic junction.

Schottky junction



https://www.icrfq.net/schottky-diode/

Ohmic junction



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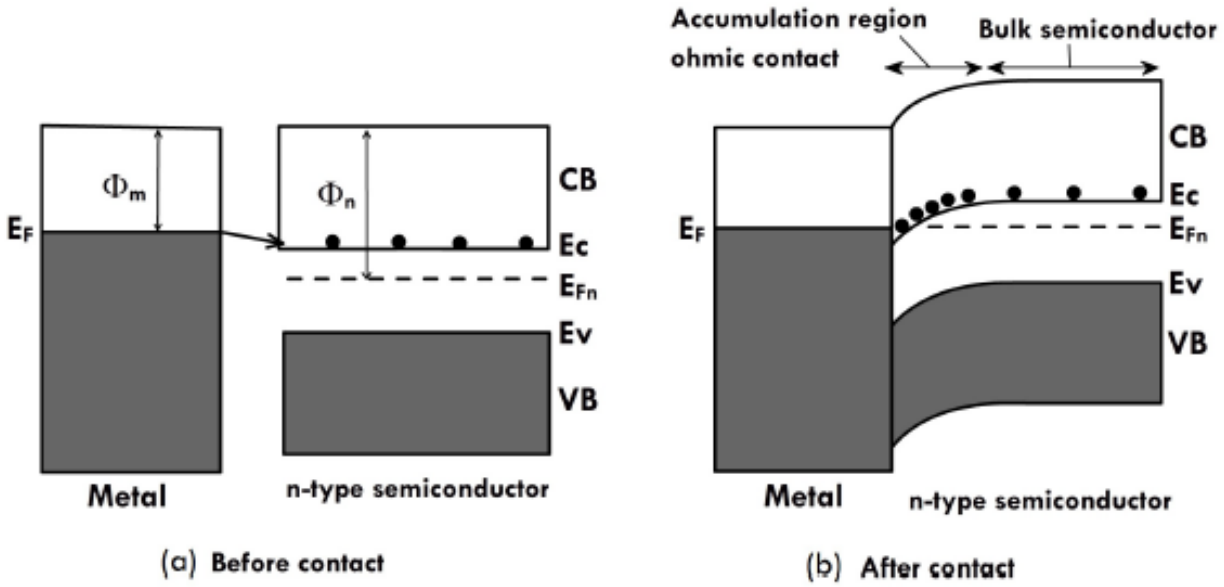
Ohmic Contact

- A Schottky junction is formed when the semiconductor has a lower work function than the metal. When the semiconductor has a higher work function the junction formed is called the Ohmic junction.

- Ohmic junction behaves as a resistor conducting in both forward and reverse bias. The resistivity is determined by the bulk resistivity of the semiconductor.



Ohmic Contact

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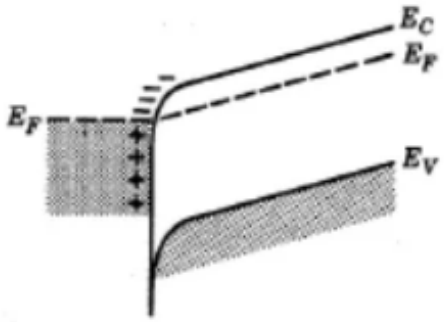
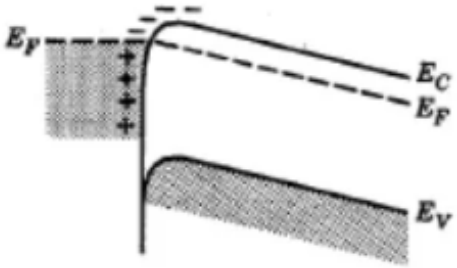
Ohmic Contact (Forward bias and Reverse Bias)

Forward Bias (V_A>0V)



- When bias is applied, practically all applied voltage drops across the higher resistance region which is the bulk neutral semiconductor.
- Current is therefore determined by the resistance of the bulk, ie. measures property of device

Reverse Bias (V_A<0V)



- no depletion region
- ***accumulation of majority carriers*** near the semiconductor surface
- low resistance to current flow
- non-rectifying ohmic

Heavy doping near the junction (degenerate semiconductor): High doping narrows the depletion region, enabling **tunneling** of carriers → ohmic behavior even if a barrier exists.

https://www.slideserve.com/ehanley/metal-semiconductor-contact-powerpoint-ppt-presentation

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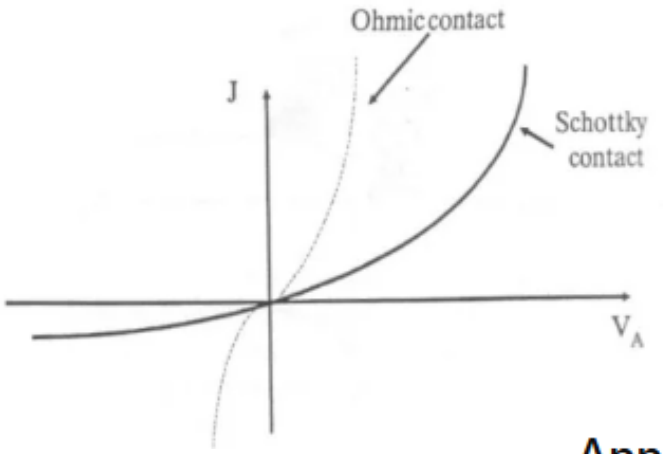
Ohmic Contact (Forward bias and Reverse Bias)

Current-Voltage Characteristics



Some discussions:

- Ohmic contacts have large current in both directions
- Typically, the resistance is very small
- Since the contact resistance is very small, the voltage will be dropped on the semiconductor

Applications

- Ohmic contacts are essential in **all semiconductor devices** (diodes, transistors, ICs).
- They provide the **electrical connection between metal electrodes and the semiconductor regions** (e.g., source, drain, emitter, collector).
- Without ohmic contacts, devices would behave like diodes at their terminals instead of allowing proper current injection.

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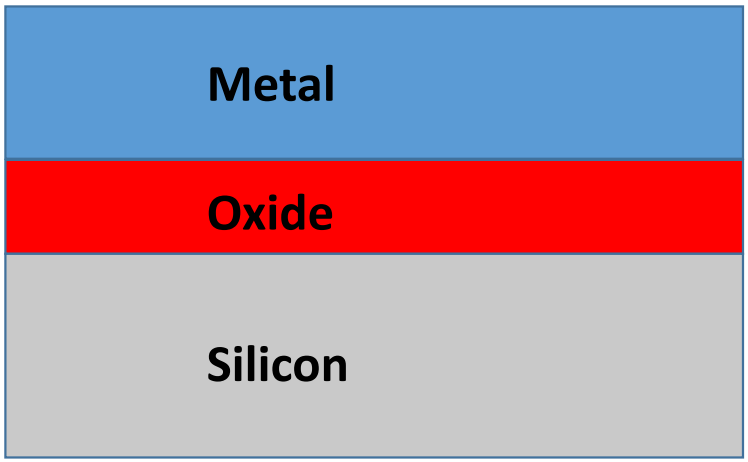
https://www.slideserve.com/ehanley/metal-semiconductor-contact-powerpoint-ppt-presentation

MOS structures



- Accumulation mode
- Depletion mode
- Inversion mode

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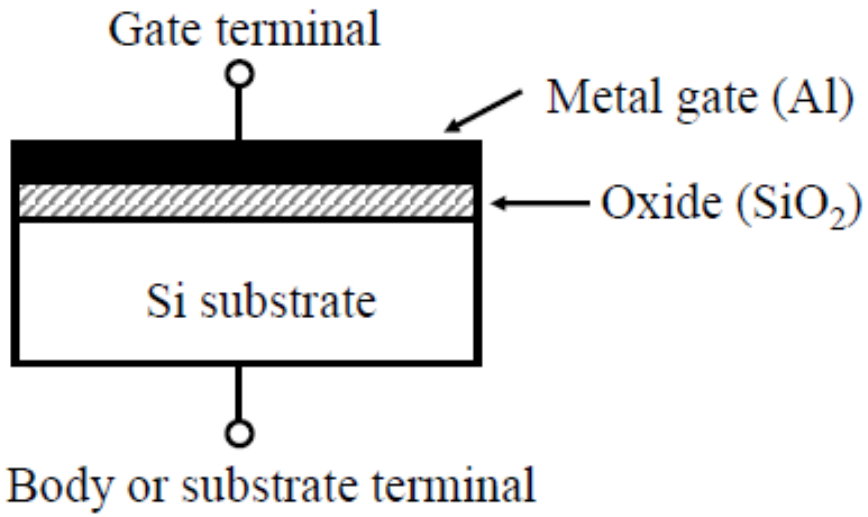
MOS Capacitor

- MOS: Metal-oxide-semiconductor
  - Gate: metal (or polysilicon)
  - Oxide: silicon dioxide, grown on substrate
- MOS capacitor: two-terminal MOS structure



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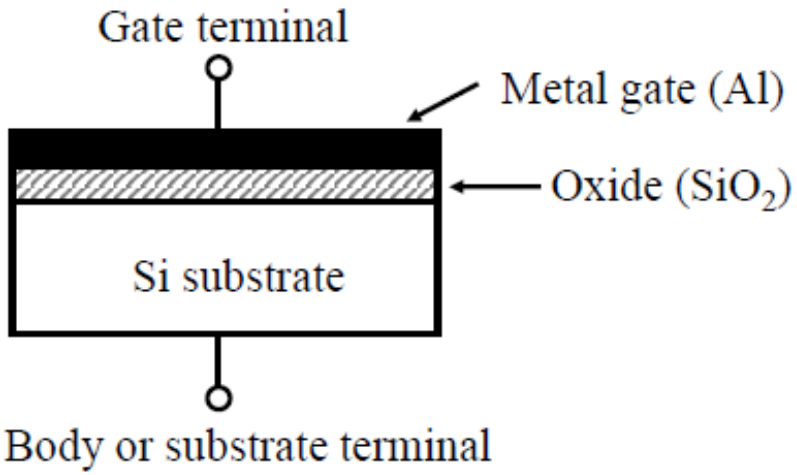
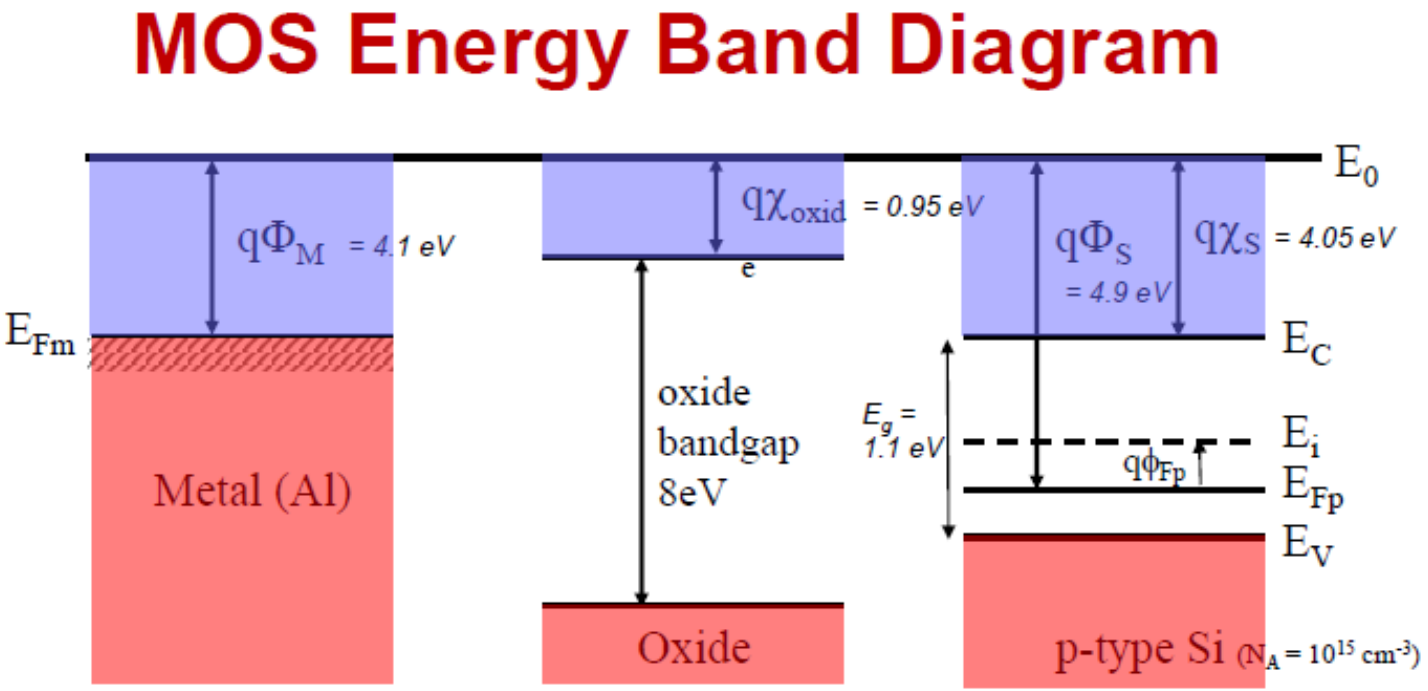


MOS Capacitors



- Work function ($q\Phi_M$, $q\Phi_S$): energy required to take electron from Fermi level to free space
- Work function difference between Al and Si = 0.8V

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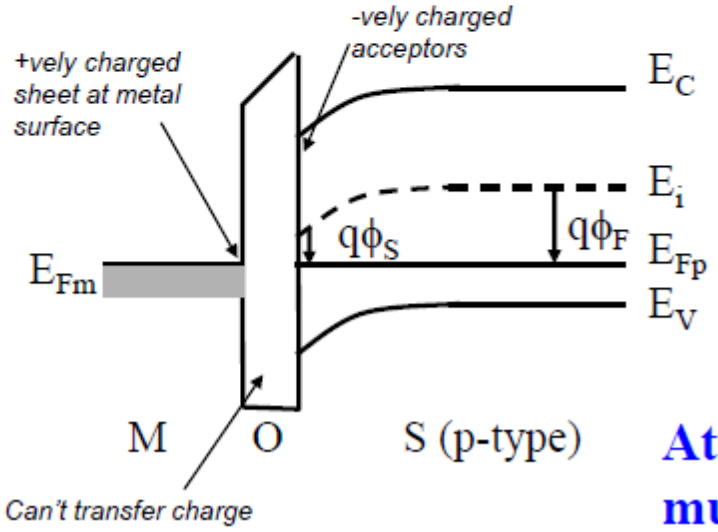
MOS Capacitors- Energy band diagram

- Bands must bend for Fermi levels to line up
- Amount of bending is equal to work function difference: $q\Phi_M - q\Phi_S$
- Fermi levels equalized by transfer of –ve charge from materials with higher E_F (smaller work functions) across interfaces to materials with lower E_F
- **Part of voltage drop occurs across oxide, rest occurs next to O-S interface**



ϕ_F = Fermi potential (difference between E_F and E_i in bulk)

ϕ_S = surface potential

At equilibrium, Fermi levels must line up!!

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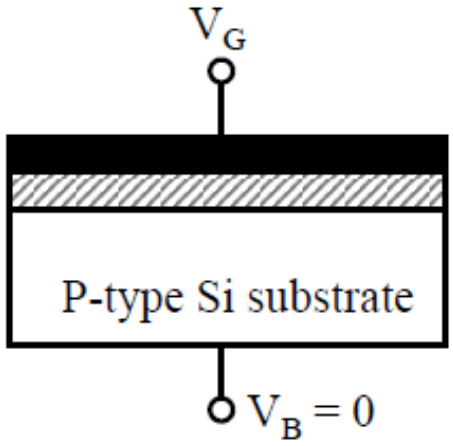
MOS Capacitors- Operation

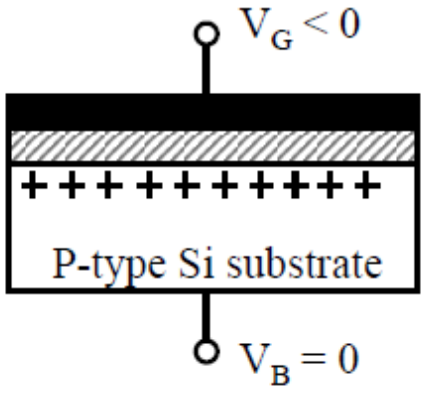
- Assume p-type substrate
- Three regions of operation
  - Accumulation ($V_G < 0$)
  - Depletion ($V_G > 0$ but small)
  - Inversion ($V_G >> 0$)

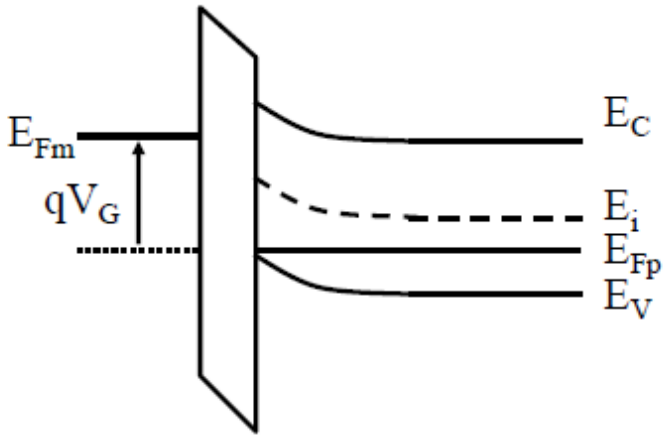


MOS Capacitors- Operation

Accumulation

- Negative voltage on gate: attracts holes in substrate towards oxide
- Holes "accumulate" on Si surface (surface is more strongly p-type)
- Electrons pushed deeper into substrate

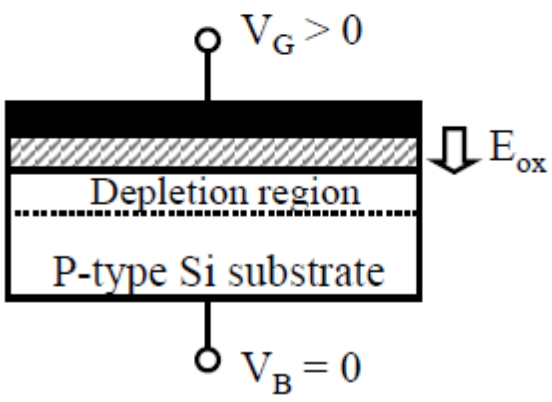


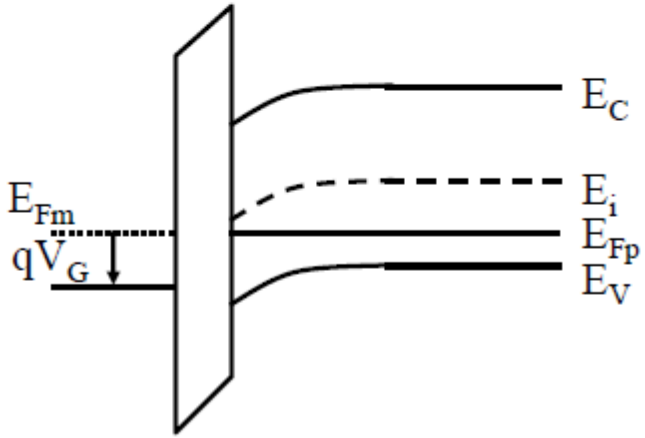


MOS Capacitors- Operation

Depletion

- Positive voltage on gate: repels holes in substrate
  - Holes leave behind negatively charged acceptor ions
- Depletion region forms: devoid of carriers
  - Electric field directed from gate to substrate
- Bands bend downwards near surface
  - Surface becomes less strongly p-type (E_F close to E_i)





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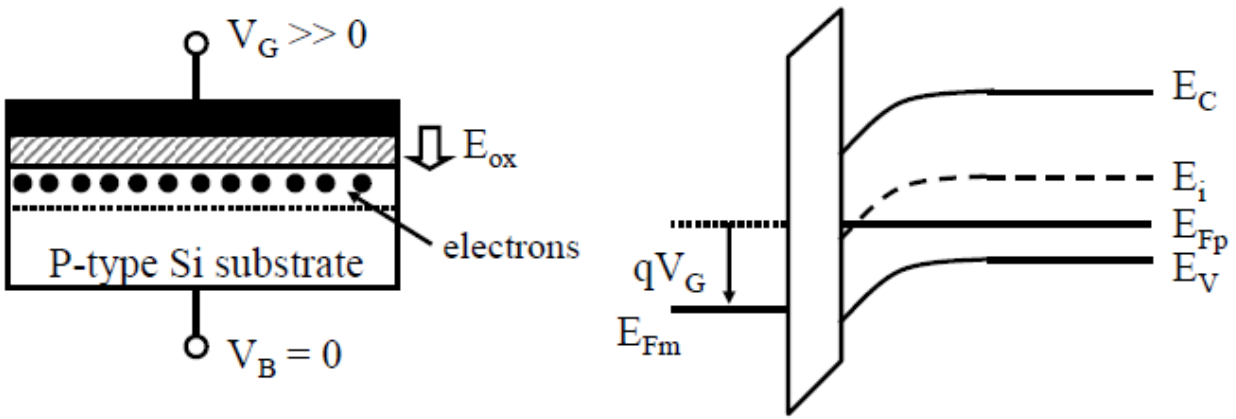
MOS Capacitors- Operation

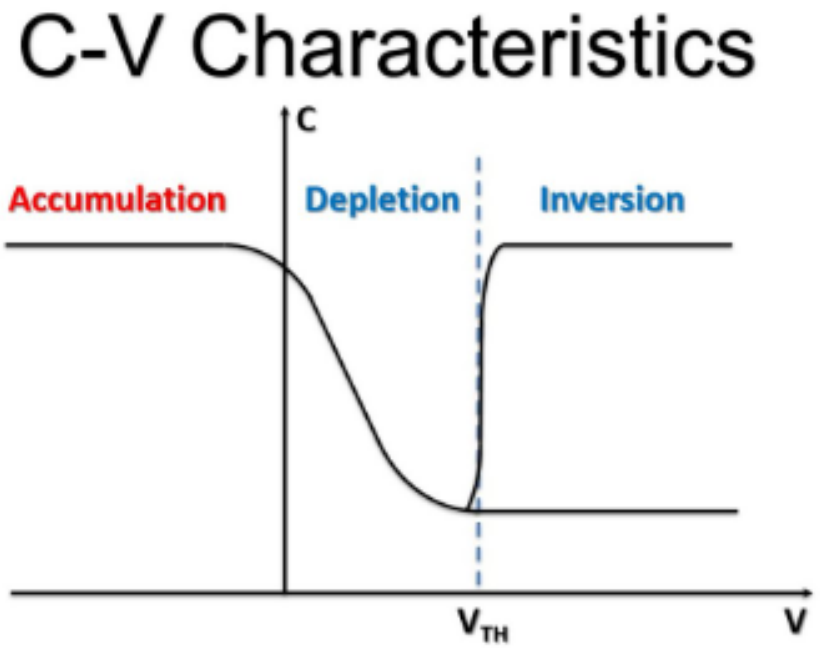
Inversion

$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}}$$

- Increase voltage on gate, bands bend more
- Additional minority carriers (electrons) attracted from substrate to surface
  - Forms "inversion layer" of electrons
- Surface becomes n-type



MOS Capacitors- C-V Characteristics



$$C_{dep} = \frac{\varepsilon_s}{W_{dep}}$$

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

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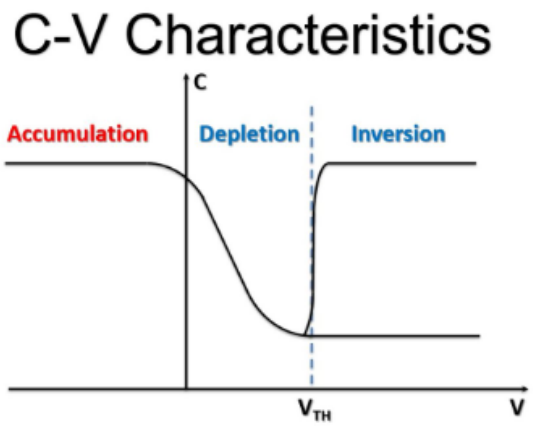
MOS Capacitors- C-V Characteristics



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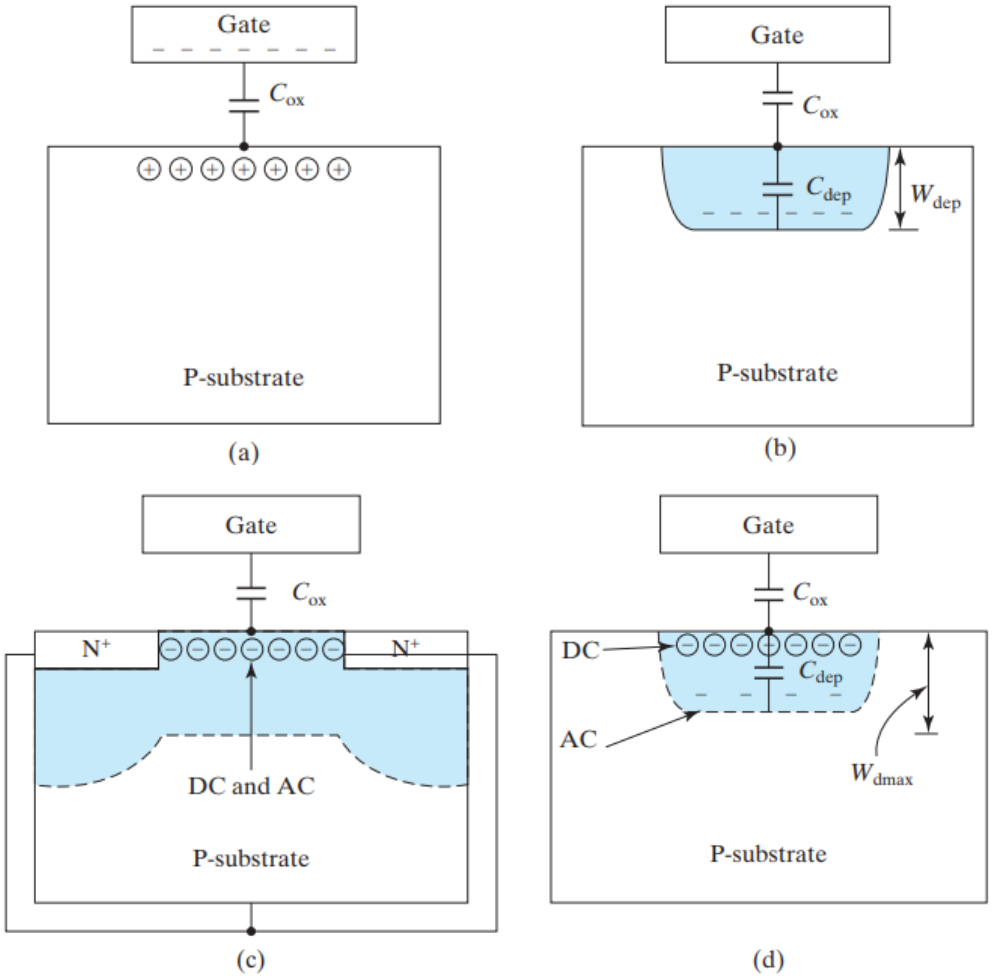

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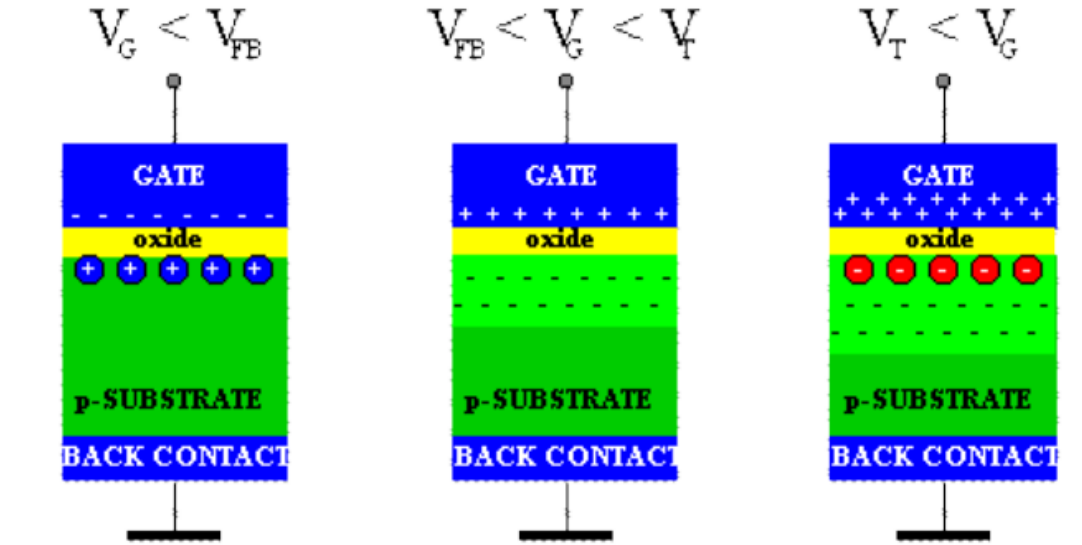

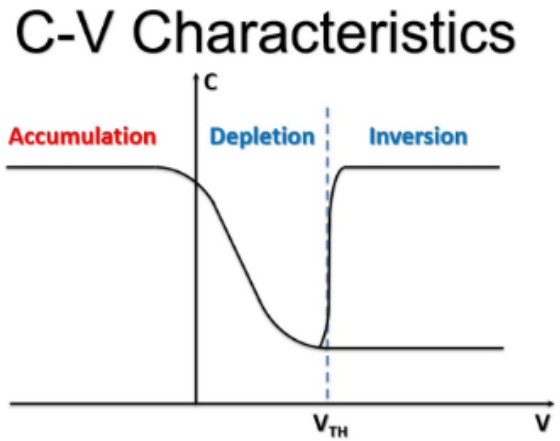

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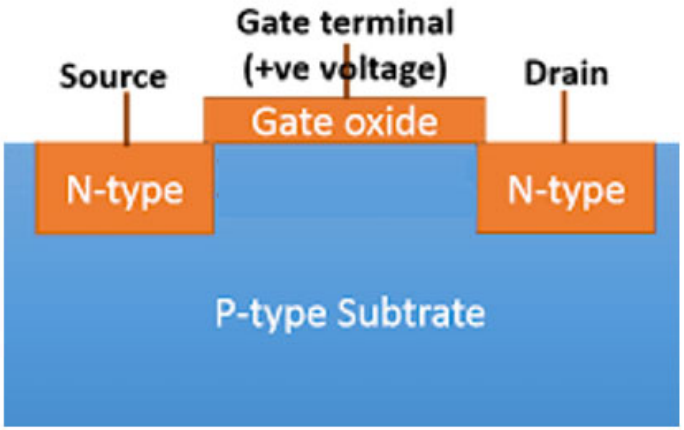
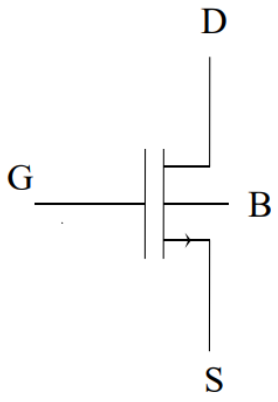
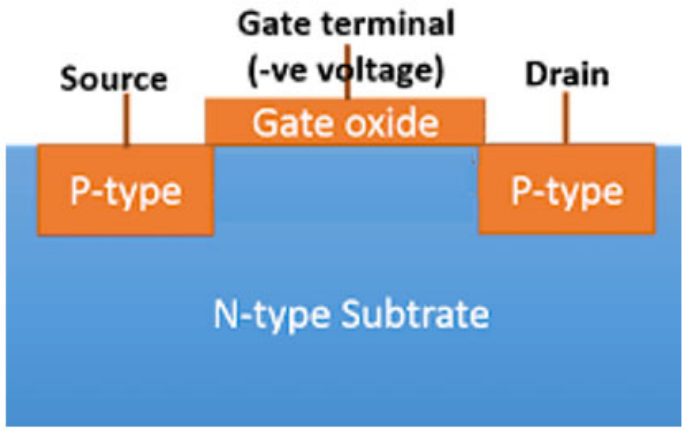
Review of MOSFETs

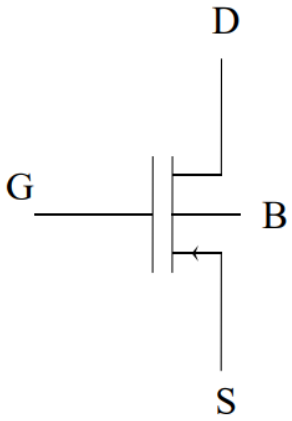


n-channel MOS
Transistor





p-channel MOS
Transistor



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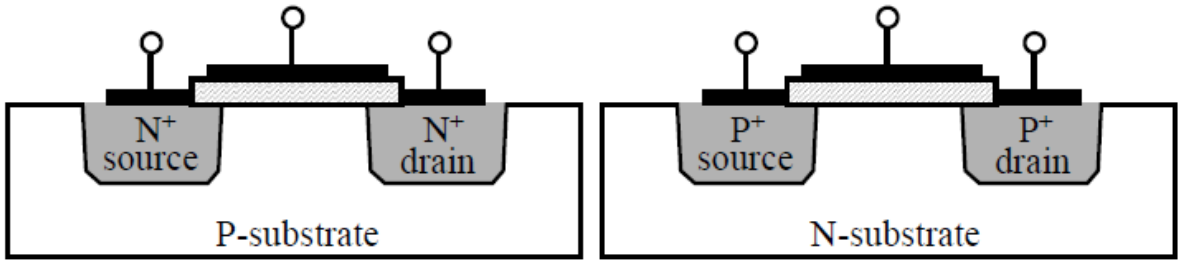
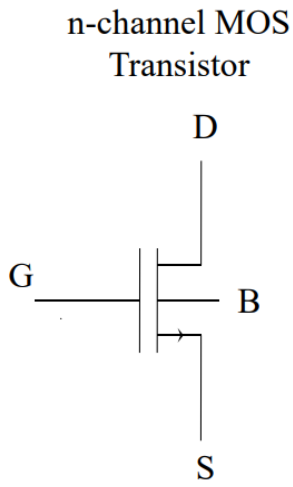
Review of MOSFETs

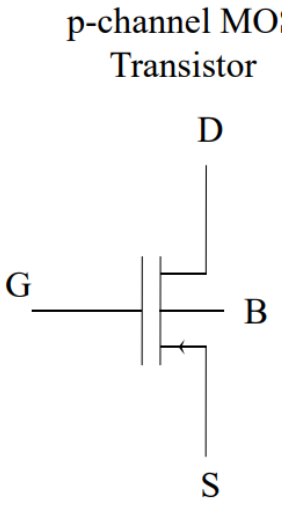
MOS Transistor

- Add "source" and "drain" terminals to MOS capacitor
- Transistor types
  - NMOS: p-type substrate, n^+ source/drain
  - PMOS: n-type substrate, p^+ source/drain



NMOS PMOS





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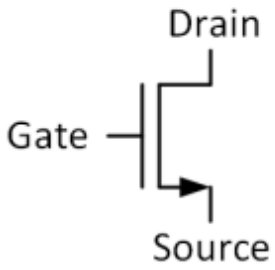
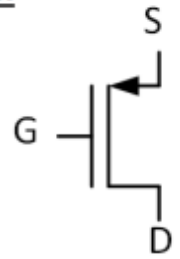
Review of MOSFETs

- We now turn our attention to another type of transistor, the **MOSFET**:
  - **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
- Many similarities to the BJT:
  - Three terminals
  - Voltage at one terminal controls current between the other two
    - A transconductance device
  - Two polarities: N-channel and P-channel MOSFETS
    - Our focus will primarily be N-channel MOSFETs (NMOS devices)

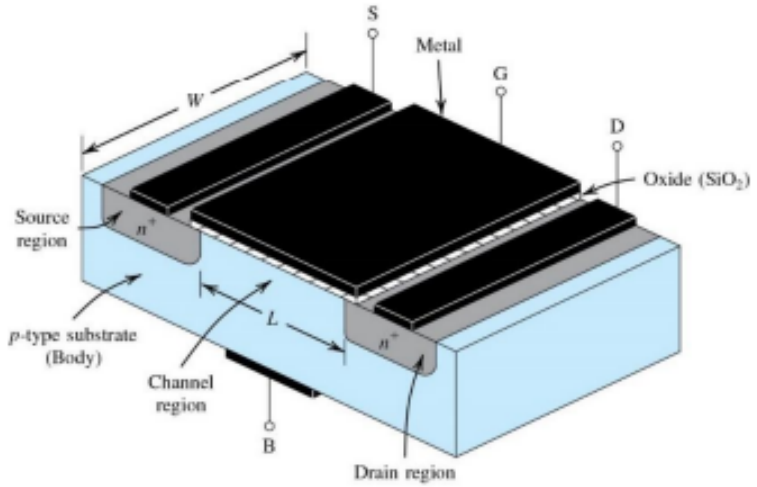
N-Channel (NMOS):

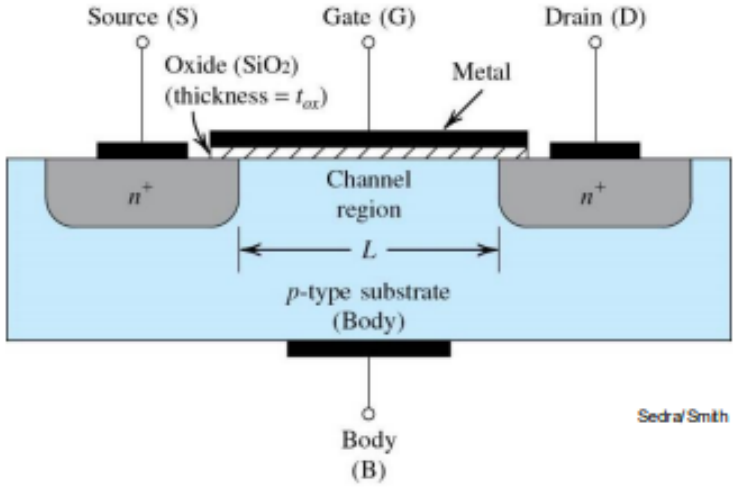


P-Channel (PMOS):



Review of MOSFETs





- P-type substrate
- N+ source and drain
- ***Metal gate electrode***, and source/drain/body contacts
- Thin ***oxide*** insulates the gate from the rest of the device
- Region of substrate between the drain and source is the ***channel***
  - Channel dimensions: W and L

Review of MOSFETs

- Terminal voltages and currents named as shown
  - Again, lower-case v/i and upper-case subscript represents ***total*** (AC and DC) voltage and current
- For an NMOS device in typical operation:

$$v_{GS} \geq 0$$

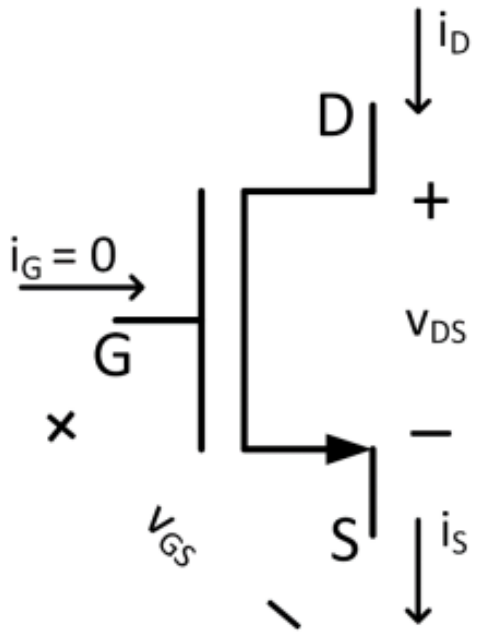
$$v_{DS} \geq 0$$

- Gate oxide does not allow current to flow, so

$$i_G = 0$$

and

$$i_D = i_S$$



Review of MOSFETs

Cut-Off Region

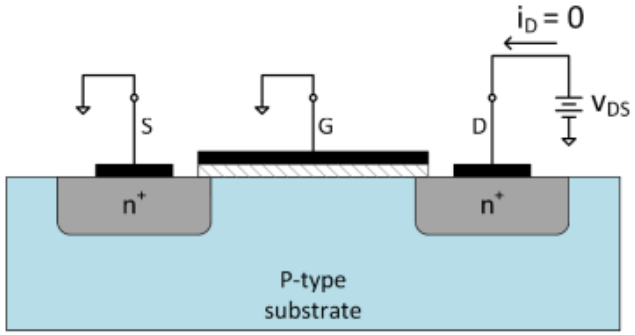
- Gate and source both grounded

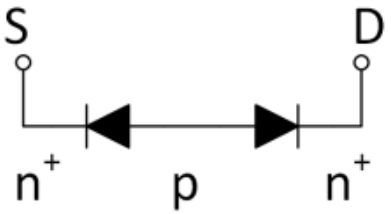
$$v_{GS} = 0$$

- Drain-to-source pathway looks like two back-to-back diodes
  - Very high drain-source resistance ($r_{DS} = \infty$)
- Even for $v_{DS} > 0$, no current will flow

$$i_D = 0$$

- Looks like an open switch

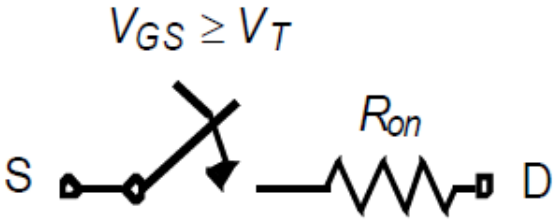


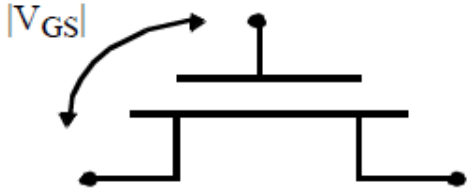


Review of MOSFETs

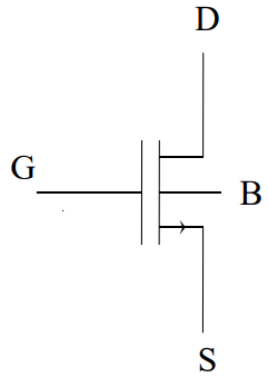
What is a Transistor?

A Switch! ⟷ An MOS Transistor

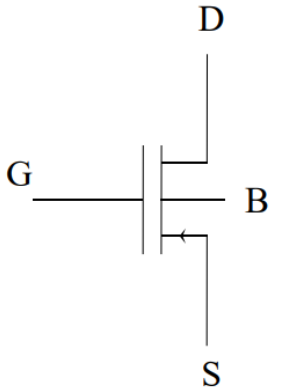




n-channel MOS Transistor



p-channel MOS Transistor



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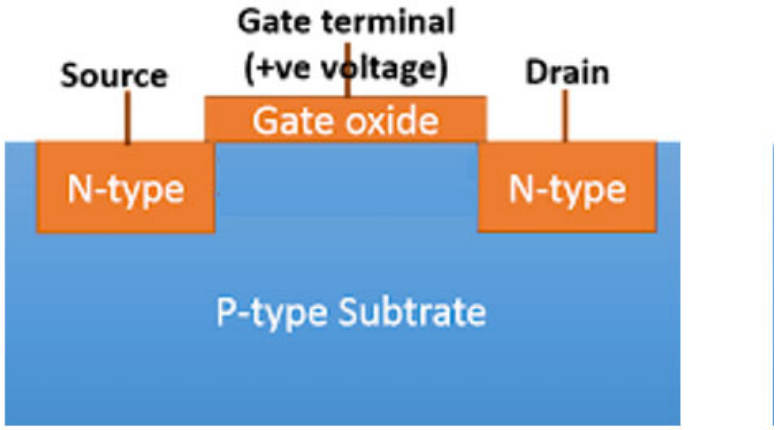
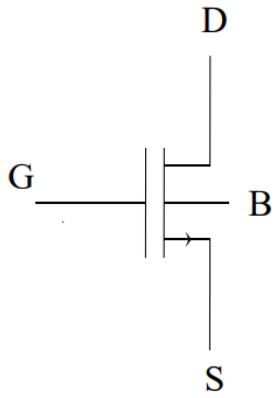
Review of MOSFETs



n-channel MOS
Transistor



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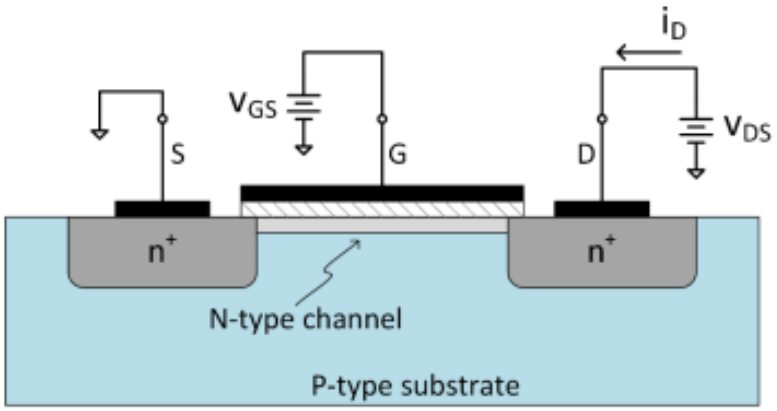
Review of MOSFETs

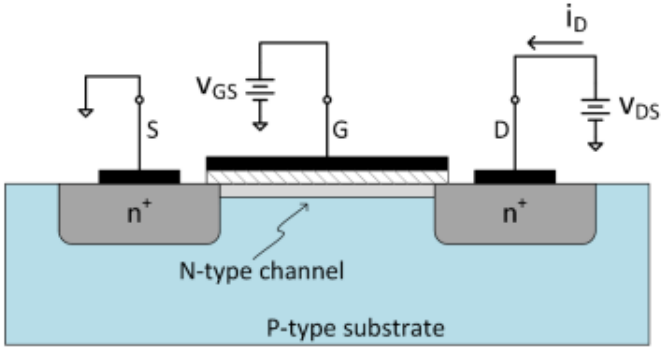
Inversion



- Now, v_{GS} is increased, while v_{DS} is kept small
  - Electric field established across gate oxide
  - Holes in p-type substrate repelled deeper into substrate
  - Electrons from drain and source attracted to region below the gate
- For large enough v_{GS}, p-type material below the gate is ***inverted*** to n-type
  - An ***inversion layer***
  - ***Induced n-type channel connects drain to source***
  - Now, current can flow in response to v_{DS}, $i_D > 0$

Review of MOSFETs

Threshold Voltage



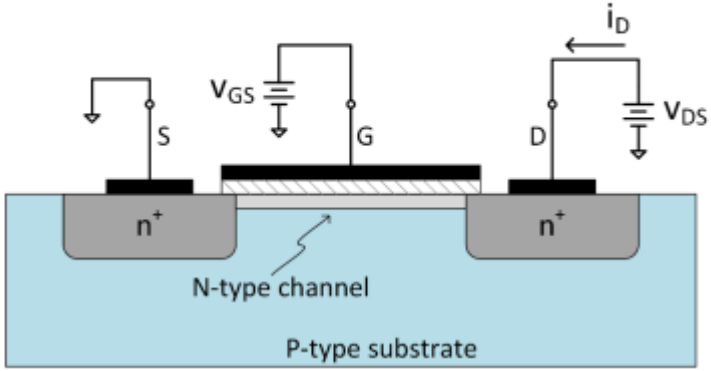
- Channel is induced once v_{GS} exceeds a certain voltage:
  - The ***threshold voltage***

$$v_{GS} \geq V_t$$

  - A device parameter
  - Typically, $V_t = 300\ mV \ldots 1\ V$
- As v_{GS} increases beyond V_t, the induced channel gets deeper
- As long as v_{DS} is small ($v_{DS} \ll V_t$), channel depth is uniform

Review of MOSFETs

Overdrive Voltage

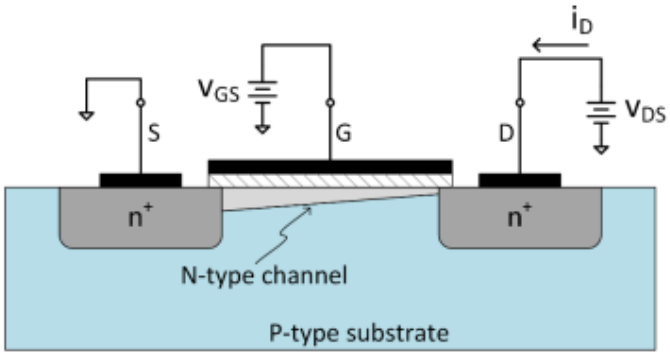


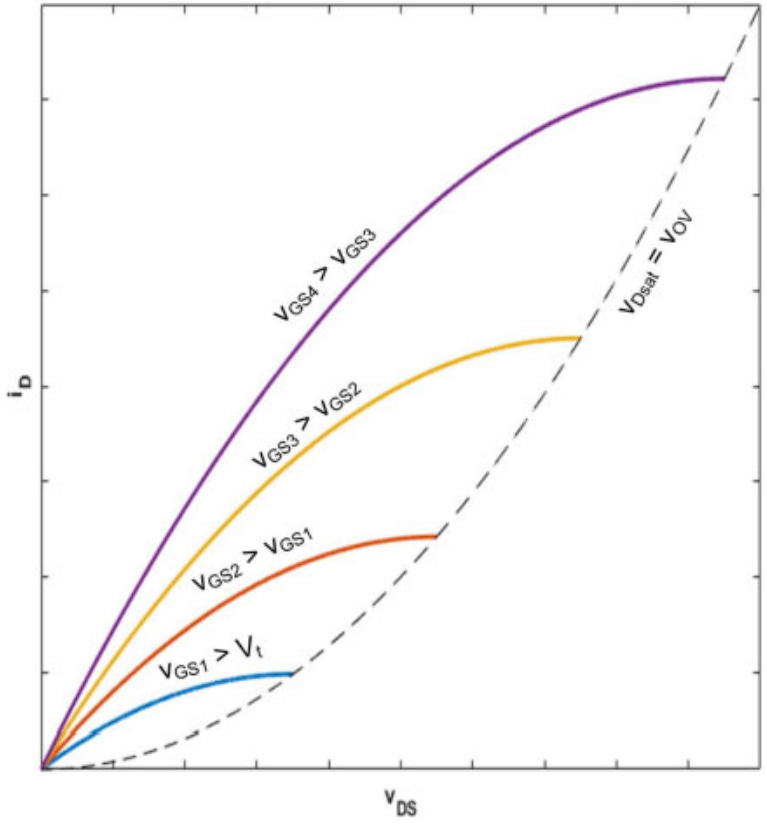
- A channel is induced once v_{GS} exceeds the threshold voltage
- v_{GS} in excess of the threshold voltage is called the ***overdrive voltage*** or ***effective voltage***:

$$v_{OV} = v_{GS} - V_t$$

- As we will soon see, v_{OV} plays an important role in determining device behavior

Review of MOSFETs- Linear Region





- As v_{DS} increases:
  - Voltage varies along the channel
    - v_S near the source, v_D near the drain
  - Gate-to-channel voltage decreases closer to the drain
  - Channel depth decreases closer to the drain
    - Channel is tapered
- More current flows with increasing v_{DS}, but channe. resistance increases as channel becomes more tapered

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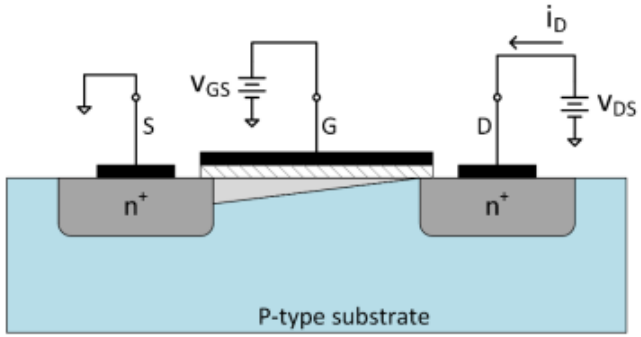
Review of MOSFETs- Linear Region

Channel Pinch-Off



- Eventually, for large enough v_{DS}
  - Gate-to-channel voltage near the drain no longer exceeds V_t
  - Channel ***pinch-off*** occurs
  - Channel disappears at the edge of the drain
- Pinch-off occurs when:

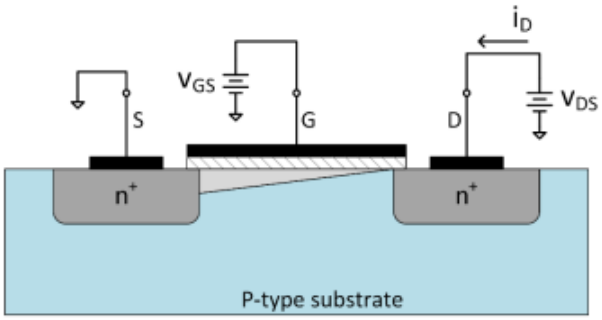
$$v_{GD} = V_t = v_{GS} - v_{DS}$$

$$v_{DS} = v_{GS} - V_t$$

Review of MOSFETs- Linear Region

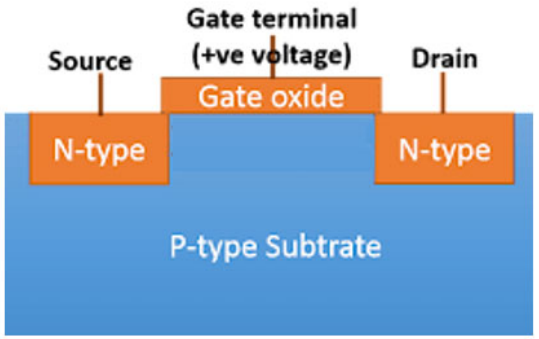
Saturation Region

- Once channel pinch-off occurs:
  - Voltage at the drain-end of the channel remains v_{OV}, even as v_{DS} increases
  - Any increase in v_{DS} beyond v_{OV} is dropped across the depletion region surrounding the drain



  - Voltage across the length of the channel is fixed at v_{OV}
  - Pinched-off channel shape does not change with v_{DS}
  - Drain current ***saturates*** at a constant value for constant v_{GS}

Review of MOSFETs



Channel formation basics

- A channel forms when

$$V_{GS} > V_T$$

because inversion charge appears under the gate.

- Along the channel, the local inversion charge is

$$Q_n(x) \;\propto\; V_{GS} - V_T - V(x),$$

where $V(x)$ is the channel potential at position x.

- At the source end, $V(0) = 0 \implies Q_n(0) \propto V_{GS} - V_T$ (strong channel).
- At the drain end, $V(L) = V_{DS} \implies Q_n(L) \propto V_{GS} - V_T - V_{DS}$.

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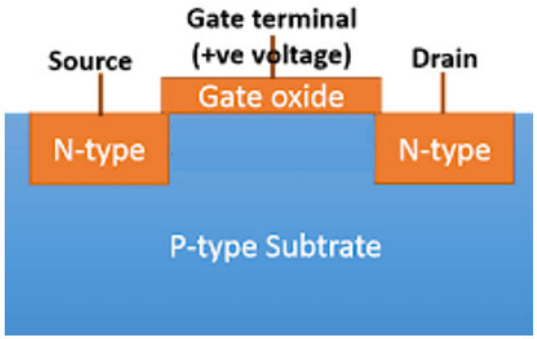
Review of MOSFETs

Condition for pinch-off



- If $V_{DS} < V_{GS} - V_T$:
  Channel charge is positive all along the channel → continuous inversion path from source to drain. MOSFET is in **linear/triode region**.
- If $V_{DS} = V_{GS} - V_T$:
  At the **drain end**,

$$Q_n(L) = 0$$

  → the inversion channel just disappears at the drain edge → **onset of pinch-off**.
- If $V_{DS} > V_{GS} - V_T$:
  No inversion possible near the drain. Instead:
  - Channel terminates at a "pinch-off point" before the drain.
  - Beyond this, a depletion region carries the extra potential drop.
  - Current saturates since the effective voltage across the channel is clamped at $V_{GS} - V_T$.

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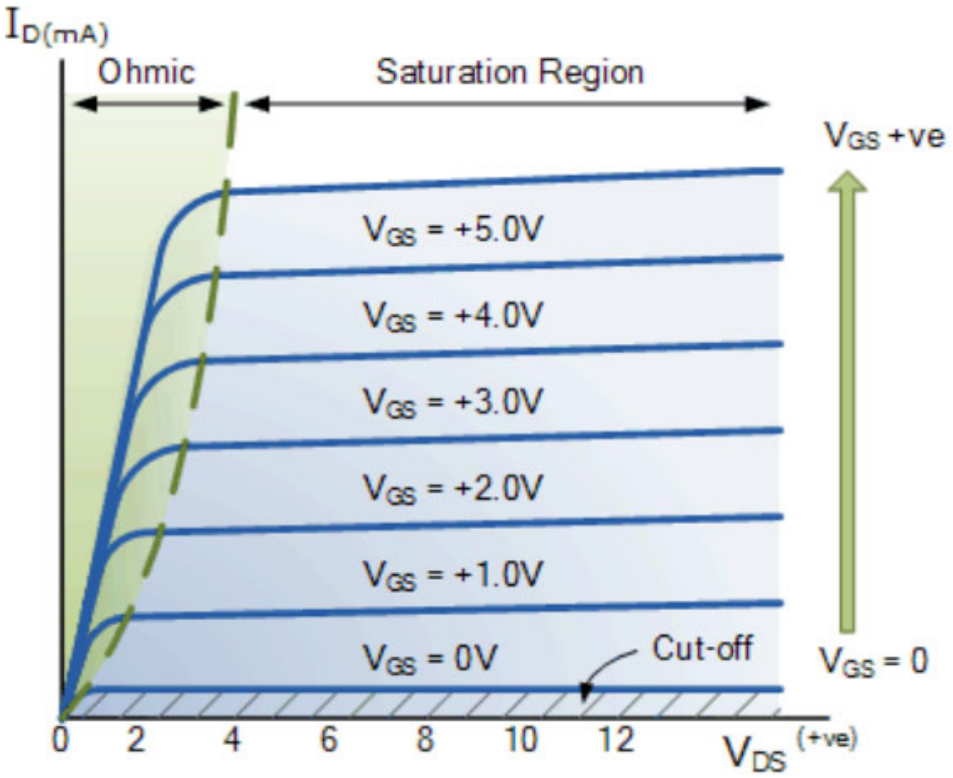

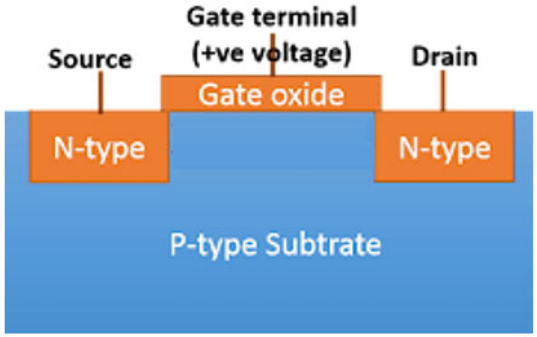

Relation between V_{DS} & V_{GS}

Case	V_T	Channel condition
Linear region	$V_{DS} < V_{GS} - V_T$	Continuous inversion from source to drain
Pinch-off onset	$V_{DS} = V_{GS} - V_T$	Channel just disappears at drain end
Saturation	$V_{DS} > V_{GS} - V_T$	Pinch-off near drain, depletion region forms, current saturates

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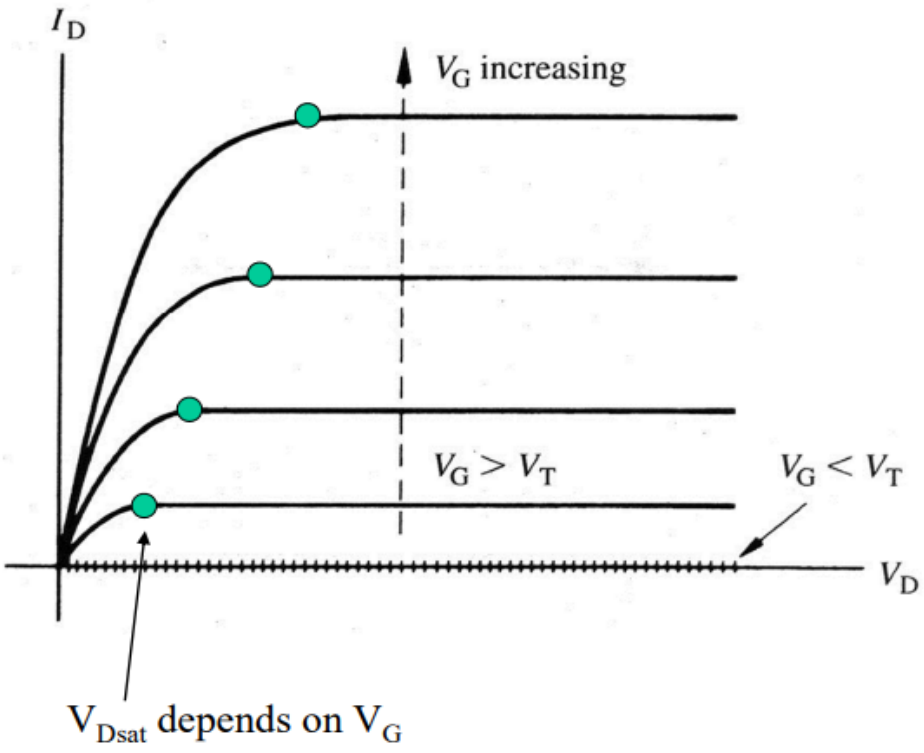
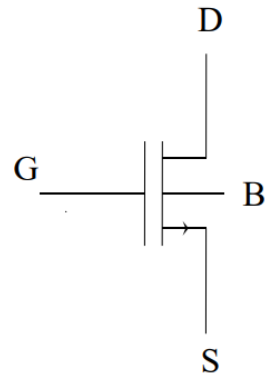
I_D-V_{DS} curves for various V_{GS}:



$$\beta = \mu C_{ox} \frac{W}{L}$$

n-channel MOS Transistor



$$_s = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

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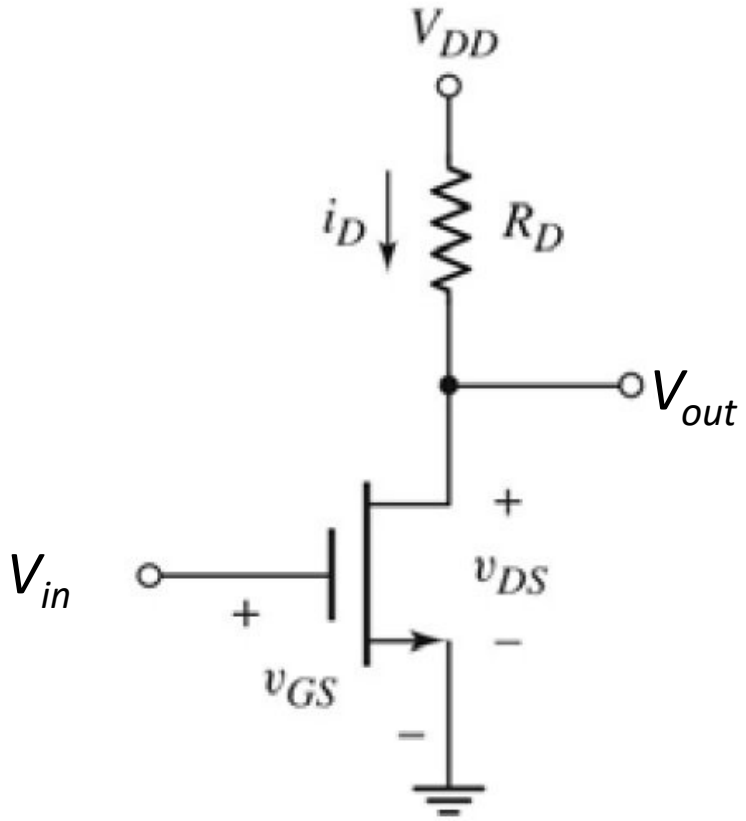
Review of MOSFETs: DC load line of n-MOSFET



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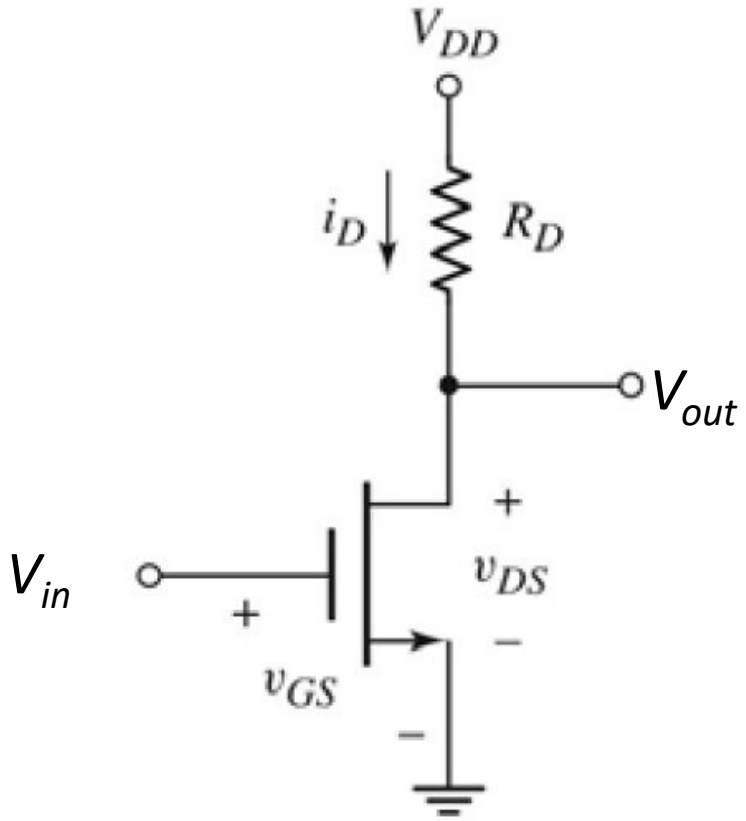
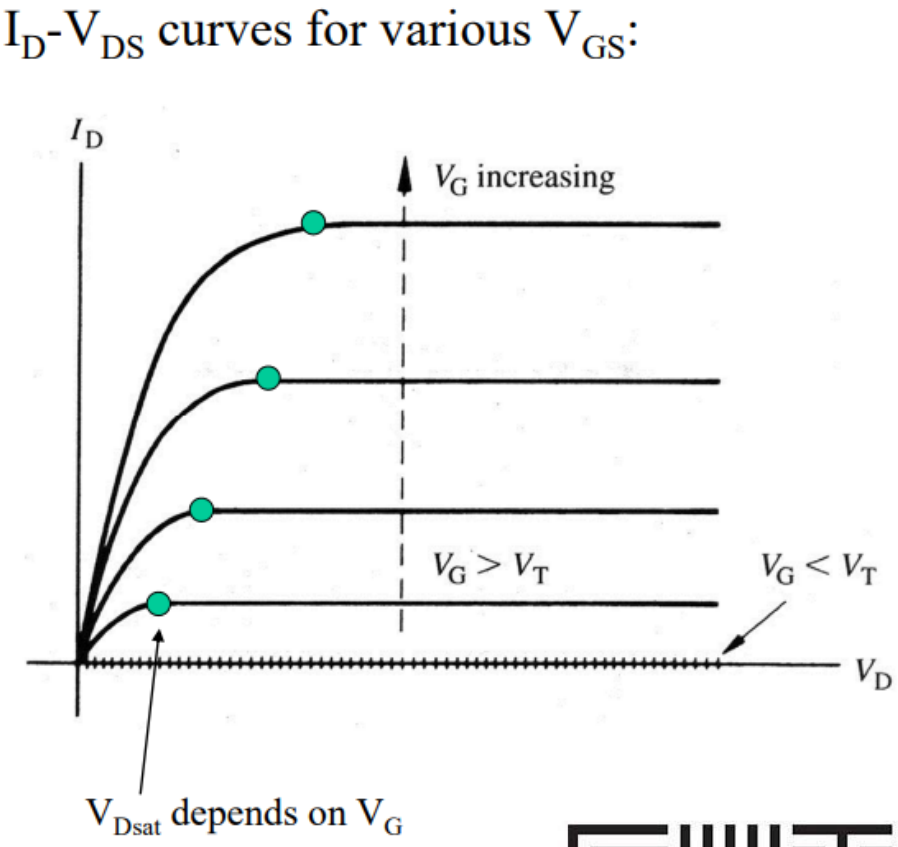
Review of MOSFETs: DC load line of n-MOSFET





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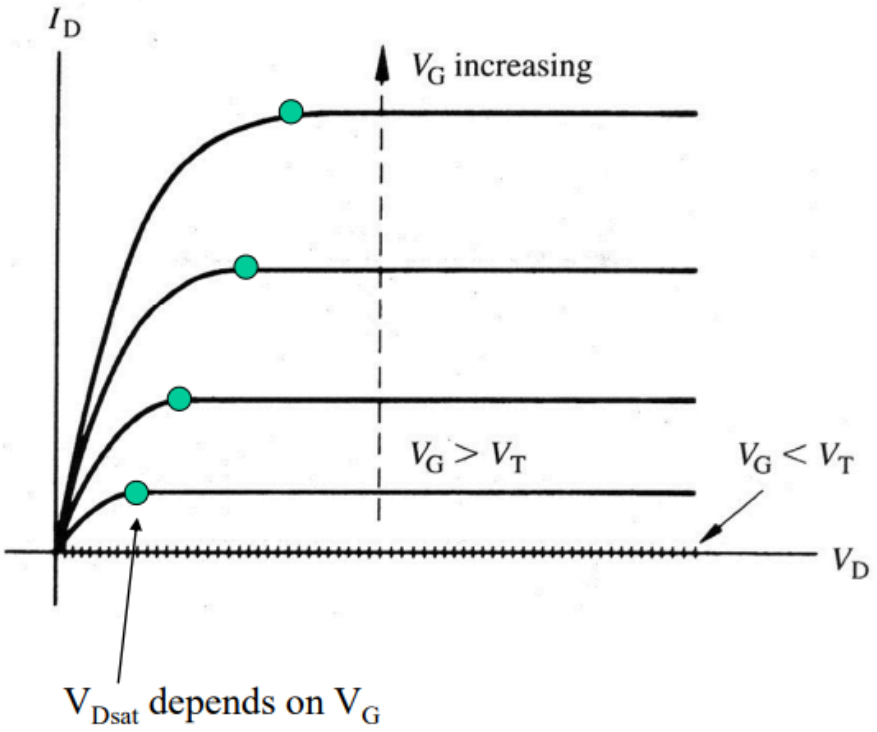
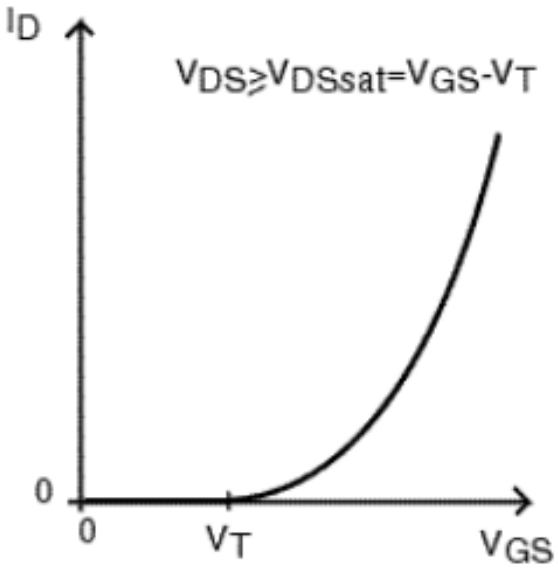


Transfer characteristics:



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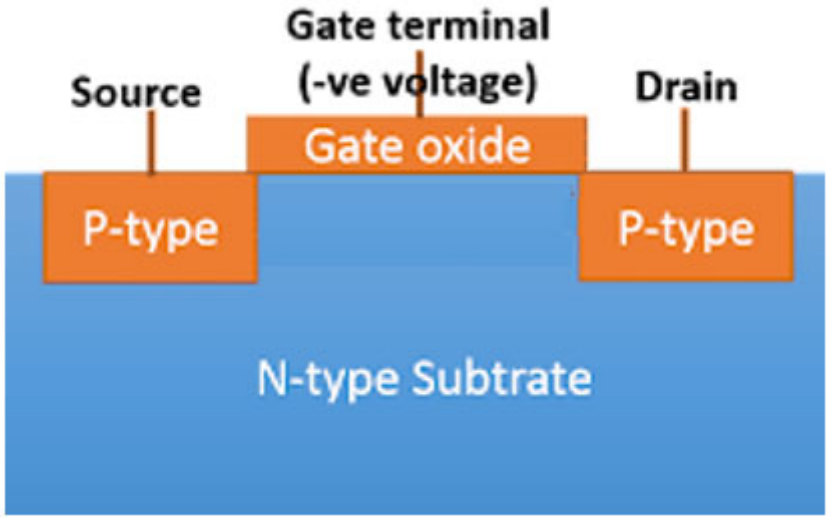
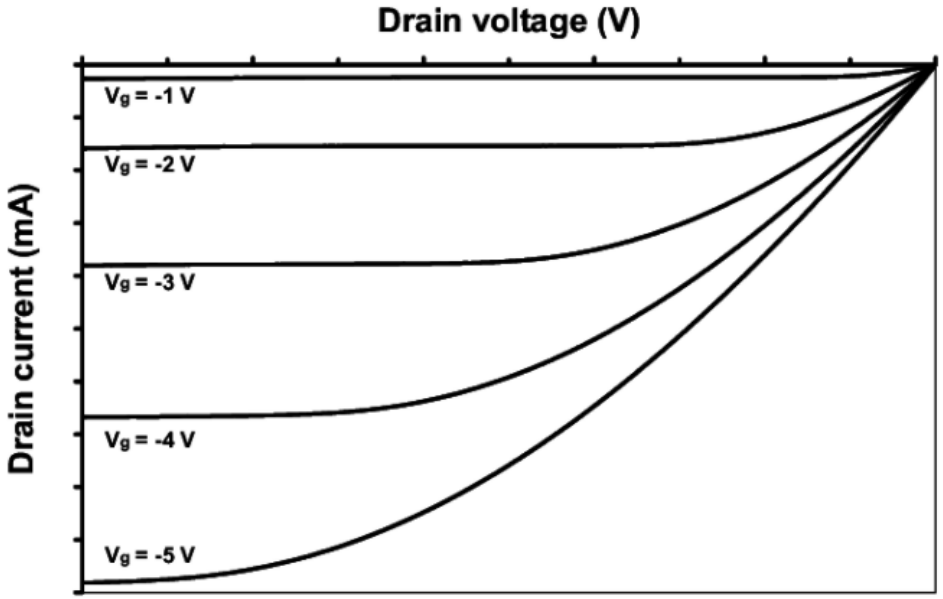
p-MOSFET





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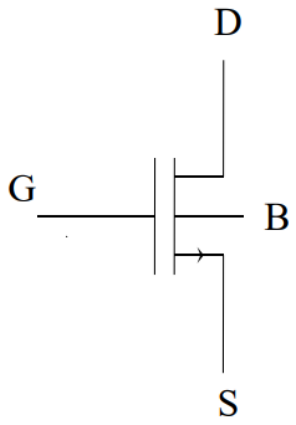
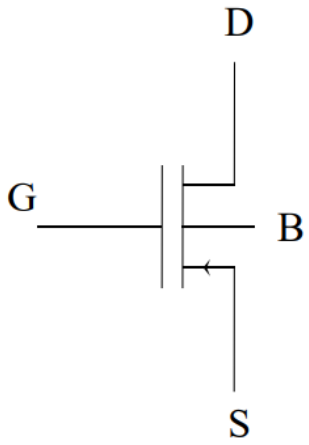
Review of MOSFETs

n-channel MOS Transistor

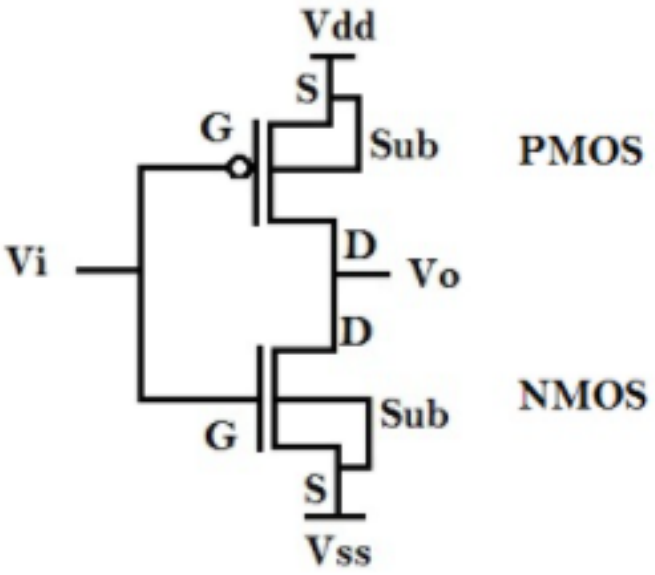


p-channel MOS Transistor



MOSFET type	V_{GS} = +ve	V_{GS} = 0	V_{GS} = -ve
N-Channel	ON	OFF	OFF
P-Channel	OFF	OFF	ON

CMOS circuit



G = Gate Terminal
S = Source Terminal
D = Drain Terminal
Sub = Substrate Terminal

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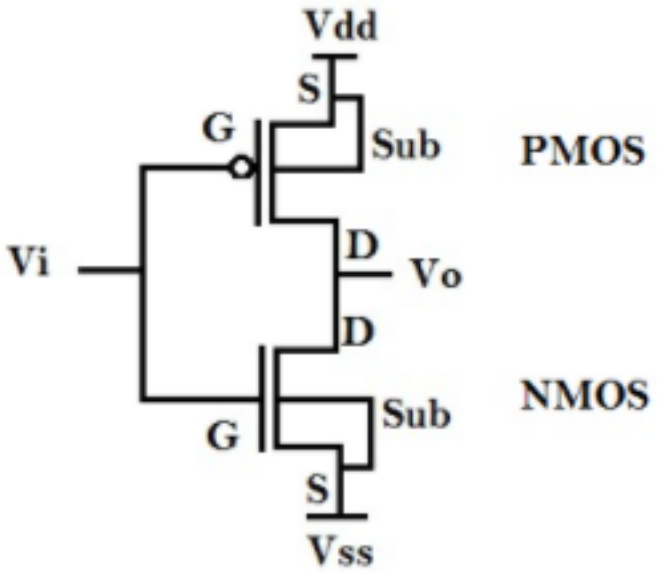
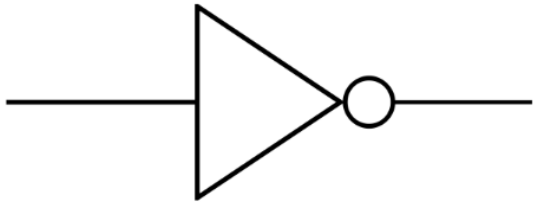
CMOS circuit





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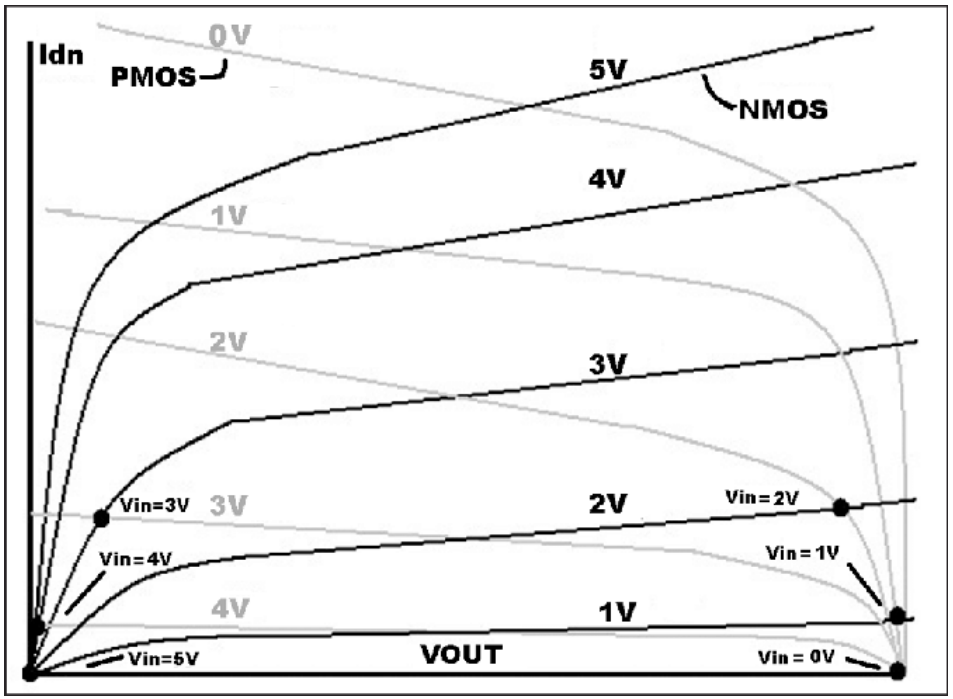

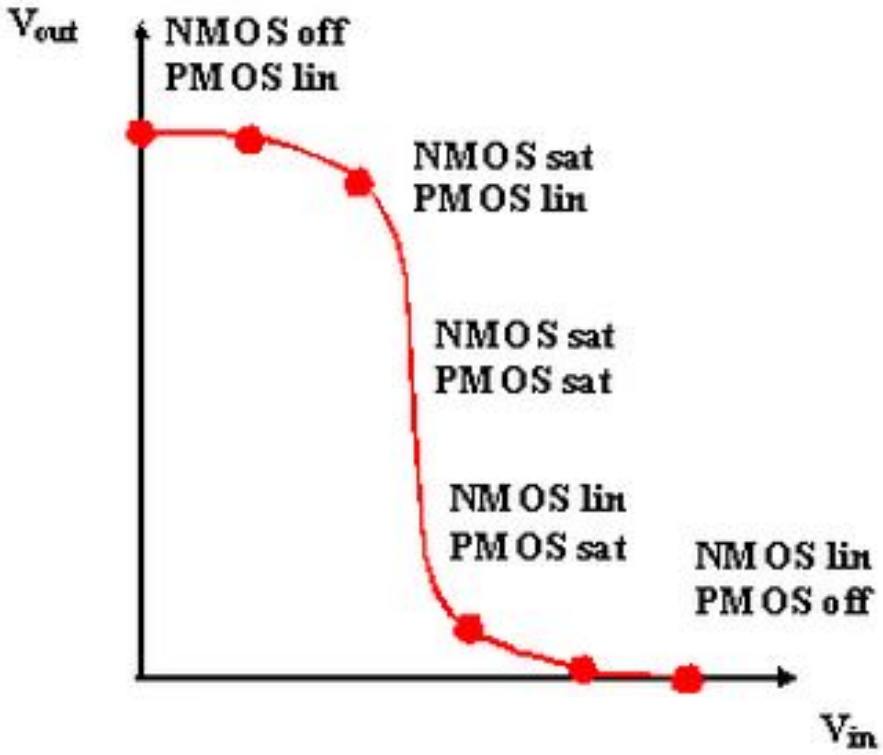

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CMOS circuit: Noise Margin

- Noise margin is the ratio by which the signal exceeds the minimum acceptable amount.
- It explains up to what extent IC allows noise in the transmission of logic ‘0’ and logic ‘1’.
- Logic ‘0’ and ‘1’ – represent the range of input values
- Hence, for error free digital signal transmission noise margin is required

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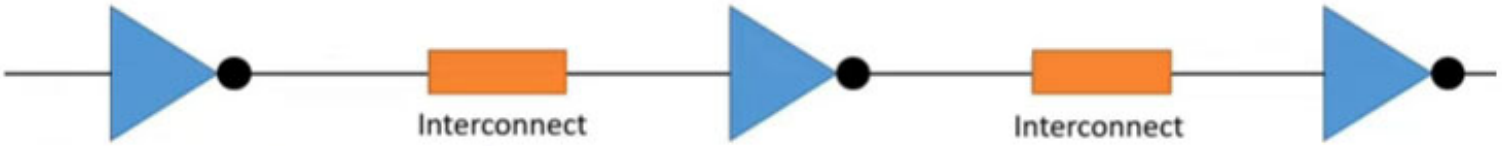

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