

Demonstration of fault-tolerant universal quantum gate operations

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Quantum computers can be protected from noise by encoding the logical quantum information redundantly into multiple qubits using error correcting codes. When manipulating the logical quantum states, it is imperative that errors caused by imperfect operations do not spread uncontrollably through the quantum register. This requires that all operations on the quantum register obey a fault-tolerant circuit design which, in general, increases the complexity of the implementation. Here, we demonstrate a fault-tolerant universal set of gates on two logical qubits in a trapped-ion quantum computer. In particular, we make use of the recently introduced paradigm of flag fault tolerance, where the absence or presence of dangerous errors is heralded by usage of few ancillary ‘flag’ qubits. We perform a logical two-qubit CNOT-gate between two instances of the seven qubit color code, and we also fault-tolerantly prepare a logical magic state. We then realize a fault-tolerant logical T-gate by injecting the magic state via teleportation from one logical qubit onto the other. We observe the hallmark feature of fault tolerance, a superior performance compared to a non-fault-tolerant implementation. In combination with recently demonstrated repeated quantum error correction cycles these results open the door to error-corrected universal quantum computation.

I. INTRODUCTION

Quantum computers promise to efficiently solve important computational tasks that are beyond the capabilities of classical computers, such as prime factorization or the simulation of complex quantum systems [1, 2]. A digital quantum computer will offer a native gate set, which is comprised of the operations that can be physically executed in hardware. Remarkably, finite sets of native gates are sufficient to compose *any* operation to an arbitrary desired precision, rendering such gate sets *universal* [3]. A fundamental challenge is to keep the quantum computation coherent, while all components of the quantum computer such as physical qubits, gate operations and measurements are inherently prone to errors. This roadblock towards large-scale quantum computation can be lifted with the tools of *quantum fault tolerance* [4–7]. The central idea is to use quantum error correction (QEC) codes, where many physical qubits together comprise so-called logical qubits such that the logical information is distributed non-locally and thereby protected from decoherence and errors due to finite control accuracy. By ingenuity of code design, it thus becomes possible to suppress logical decoherence arbitrarily by adding redundancy, once the physical noise level falls below some threshold [8]. Arbitrary logical quantum computation demands that a universal logical gate set has to be synthesized from physical gates, which presents new challenges: to prevent previously localized errors from spreading over the entire qubit register and destroying the computation, logical gates have to be designed with fault tolerance guarantees: For QEC codes with the po-

tential to correct at least one arbitrary single error, this means that a single error occurring at any location (initialization, gate or measurement) in a particular circuit may under no circumstances turn into a non-correctable error on two or more qubits. When assuming for simplicity that every location has some error probability p , the logical failure rate without fault tolerance will scale as $p_L \propto Np$ with N the number of error locations in the circuit that lead to a logical error. While adding further gates and qubits for fault tolerance increases the number of circuit locations, the logical failure rate will now scale with $p_L \propto N'p^2$, i.e. it is quadratically suppressed in p , where N' now denotes the number of pairs of locations where two errors lead to a logical error. This entails one of the hallmark features of fault-tolerant (FT) implementations: despite adding more (noisy) qubit and gates, the quality of the encoded information can be improved, if the physical noise level is sufficiently low. Certain QEC codes facilitate a fault-tolerant implementation of some gates by acting on all physical qubits individually – called a transversal logical gate. However, a universal gate set with all gates having a transversal unitary implementation is forbidden by a no-go theorem [9]. This leads to the difficulty that to reach universal fault-tolerant computation at least one logical gate must be implemented by other means, such as magic state injection [10] or code switching [11]. Fulfilling fault tolerance requirements for these approaches typically implies a substantial resource overhead [12].

The growing experimental effort towards fault-tolerant quantum computation has seen tremendous advances: Non-fault-tolerant logical state preparation and transver-

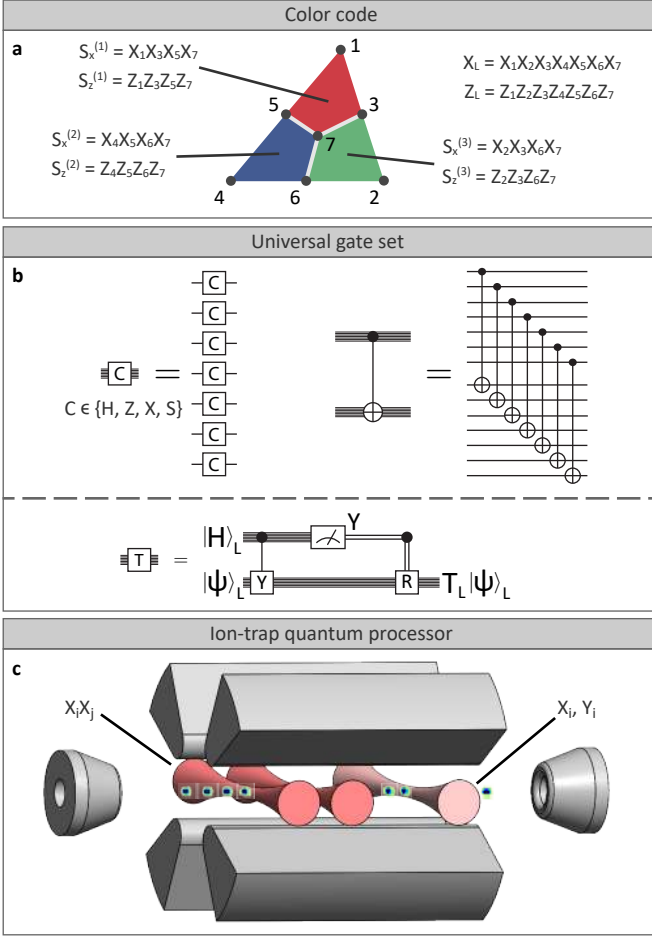


FIG. 1. QEC code, logical gates and experimental system. (a) Seven-qubit color code encoding one logical qubit in seven physical qubits. The six weight-4 operators $\{S_x^{(i)}, S_z^{(i)}\}$, $i = 1, 2, 3$, are the stabilizer generators and the weight-7 operators are logical operators Z_L and X_L . (b) Universal gate set consisting of Clifford gates (above dashed line) and the T-gate. Whereas the Clifford group is transversal in the color code, magic state injection can be used to realize the fault-tolerant T-gate. The magic state $|H\rangle_L$ is prepared fault-tolerantly and subsequently teleported onto the target qubit in an arbitrary state $|\psi\rangle_L$, effectively implementing a T-gate on the target qubit. (c) Schematic 3D model of the ion-trap quantum processor. Single and any pair i, j of ions can be addressed simultaneously by steerable tightly focused laser beams. This enables entangling (darker shaded beams) but also single-qubit (lighter) gates.

sal single-qubit logical gate operations were shown in a seven qubit experiment with trapped ions [13]. State preparation of a topological surface code state [14], repetitive stabilizer measurements in an error-detecting surface code [15, 16] and exponential error suppression in a repetition code [17] have been demonstrated in superconducting architectures. Shortly following a theory proposal towards demonstrations of fault tolerance in small systems [18], experiments showed state preparation using

error detection codes and post-selection [19–21], and recently error correction for fault-tolerant state preparation and a fault-tolerant logical single-qubit Clifford gate [22]. Theory works have substantially reduced the resource requirements for fault tolerance by the concept of flag fault tolerance [23–27]. Here, dedicated auxiliary qubits are introduced, which signal the presence of dangerous errors. This concept was used to demonstrate fault-tolerant operation of the five-qubit code in an NV center-based quantum processor [28], and fault-tolerant parity check measurements [29] and repetitive rounds of fault-tolerant QEC cycles [30] with trapped ions. In the present work, alongside the operation of single-qubit logical Clifford gates, we demonstrate the fault-tolerant implementation of a logical CNOT-gate between two logical color code qubits, thereby realizing the entire Clifford group fault-tolerantly. Since this is all one can hope for regarding transversal implementations, to obtain the non-Clifford gate required for universality, we amend the gate set by a T-gate. For this, in a first step we prepare a magic state fault-tolerantly by the use of flag qubits, as proposed in [25]. Finally, using this fault-tolerantly prepared magic state and the transversal logical CNOT-gate, we perform fault-tolerant magic state injection, thus demonstrating a universal fault-tolerant gate set.

Matching experimental capabilities on the one hand with fault tolerance requirements on the other hand makes the seven-qubit color code an attractive candidate system for the FT operation of a logical qubit. This QEC code, illustrated in Fig. 1a, is the smallest member of the code family of topological 2D color codes [31] and is also known as the Steane code [32]. It hosts one logical qubit and can be formulated as a stabilizer code on seven physical qubits, with logical states encoded in the joint $+1$ -eigenspace of six weight-4 Pauli operators. The logical operators are $X_L = X^{\otimes 7}$ and $Z_L = Z^{\otimes 7}$, which are stabilizer-equivalent to weight three operators, e.g. $Z_L \simeq Z_1 Z_2 Z_3$, rendering it a distance 3 code. This entails that all single-qubit errors can be corrected, but weight-2 errors on the code will lead to logical failures. Besides a transversal CNOT-gate, which is common to all QEC codes of the CSS (Calderbank-Shor-Steane) code family, remarkably it also admits the transversal implementation of the Hadamard gate H and the phase gate S . Consequently the entire Clifford group can be implemented transversally (see Fig. 1b) [3]. The required magic resource state to enable T-gate injection can be prepared fault-tolerantly thanks to a recently proposed protocol [25].

The experiments presented in this work have been performed in a 16-qubit ion-trap quantum information processor [33] shown schematically in Fig. 1c. The native gate set supported by this architecture is composed of entangling Mølmer-Sørensen operations [34] effectively implementing XX -rotations with an error rate of $p_2 = 2.5 \times 10^{-2}$, single-qubit rotations around an arbitrary axis in the equatorial plane of the Bloch sphere with an error rate of $p_1 = 5 \times 10^{-3}$ and Z -rotations in software.

Error rates for state initialization and measurement are estimated at $p_i, p_m = 3 \times 10^{-3}$. A more detailed discussion on experimental methods can be found in Sec. VI. For better readability, all circuits shown in this work are provided in standard CNOT-gates, as these are equivalent to XX-gates up to local Clifford operations [35]. Experimental results are accompanied by Monte Carlo simulations, for which we model imperfections as uniform depolarizing noise on single-qubit gates, initialization and measurement as well as two-qubit gates with independent physical error rates p_1, p_i, p_m, p_2 , respectively, as described in Sec. VII.

II. INITIALIZING AND CHARACTERIZING THE LOGICAL QUBIT

We start by experimentally preparing the logical state $|0\rangle_L$ as the +1-eigenstate of the logical Z-operator Z_L by implementing the circuit shown in Fig. 2a. The first part of the circuit encodes a logical qubit in a non-FT fashion: A single error, e.g. a bit flip on qubit 1, can propagate to other qubits, here qubit 3, resulting in an uncorrectable weight-2 error and therefore causing a logical error. To render this encoding circuit fault-tolerant, a verification step is added (see Fig. 2a) [36, 37]. An additional ancilla qubit is used to herald a successful logical qubit initialization, meaning that for an ancilla measurement outcome of +1 no single error anywhere in the encoding circuit can have led to uncorrectable errors on the data qubit register. This *flag* qubit will be triggered by any potentially detrimental error, as illustrated for the weight two error on qubits 1 and 3. For a measurement outcome of -1 of the flag qubit the initialization is aborted and repeated.

We analyze the quality of the information encoded in a logical qubit in terms of logical operator expectation values. After a projective measurement, the outcome of the logical operators is corrected according to the measured error syndrome, effectively performing a Pauli frame update [38, 39] described in Sec. VIII A. The updated measurement outcomes are categorized by different error patterns: (i) The outcome of all three measured stabilizer generators is +1, meaning that the error syndrome is trivial, and the logical operator exhibits the expected outcome. (ii) After the correction suggested by the non-trivial syndrome, the expected logical state is recovered. This case corresponds to a single correctable error. (iii) The syndrome is again non-trivial, but after error correction the logical state is flipped, indicating an uncorrectable error. (iv) The logical state is flipped despite the syndrome being trivial, meaning a logical error occurred directly. These categories correspond to states that have a minimum Hamming distance to any constituent state of the logical zero state (see Sec. VIII B, Eq. 10) of 0, 1, 2 and 3, respectively. For outcomes in the categories (i) and (ii) the logical state is recoverable, whereas for (iii) and (iv) an uncorrectable logical error is induced.

The relative occurrence of outcomes associated to those four categories for the initialization of $|0\rangle_L$ is shown in Fig. 2b. The verification circuit significantly suppresses the occurrence of errors leading to logical errors, resulting in decreased relative occurrences for error patterns (iii) and (iv) by a factor of more than 7. A figure of merit describing the quality of the encoded state is the logical state fidelity, i.e. the overlap of the measured with the target logical Bloch vector. A detailed discussion of the logical fidelity, not to be confused with the standard quantum state fidelity, can be found in Sec. VII. The logical infidelity is decreased from 0.090(4) to 0.012(1) by introducing the verification of the initialization, showing a clear signature that a FT implementation outperforms its non-FT counterpart despite the increased circuit complexity of one additional flag qubit and an increase from 8 to 11 entangling gates. The acceptance rate heralded by a +1 outcome of the flag measurement is 78.9(5)%. This behavior is in good qualitative agreement with numerical simulations which yield infidelities of 0.0538(2) and 0.0101(1) for the non-FT and FT circuits respectively, and an acceptance rate of 84.42(4)%.

III. TRANSVERSAL FAULT-TOLERANT OPERATIONS

The transversality of the Clifford group as a property of the color code allows for the preparation of the six cardinal states on the Bloch sphere, referred to as Pauli eigenstates herein, by applying single-qubit rotations corresponding to the respective logical gate to all qubits in the data register (see Fig. 1b). For both experimental data but also results of numerical simulations, the verification of the initialization reduces the logical infidelity of all six Pauli eigenstates, as can be seen in Fig. 2c (see also Sec. VII for definition of the logical fidelity). Due to miscalibration of experimental parameters the non-FT preparation of $|0\rangle_L$ and $|1\rangle_L$ exhibit an increased infidelity, while the infidelity is comparable for all six states for the FT scheme. The imperfections introduced by the single-qubit rotations constituting the Clifford operation are negligible compared to those originating from the initialization of the logical qubit. The average logical infidelity for the FT circuit is 0.011(1) with an acceptance rate of 80.6(2)%, while simulations suggest an average infidelity of 0.01203(4). The six stabilizer generators were measured projectively to verify the preparation of the correct encoded states for the Pauli states. The averaged expectation value of the X-(Z-)type stabilizers is 0.826(3) (0.760(3)) for the FT and 0.842(3) (0.790(3)) for the non-FT preparation scheme. Further details on the measured stabilizer generators can be found in Sec. VIII B.

The experimental implementation of the CNOT-gate acting on two logical qubits encoded in the color code is noticeably more challenging in terms of register size and circuit complexity, requiring 29 entangling gates applied to 16 qubits. As shown in Fig. 3, we first prepare

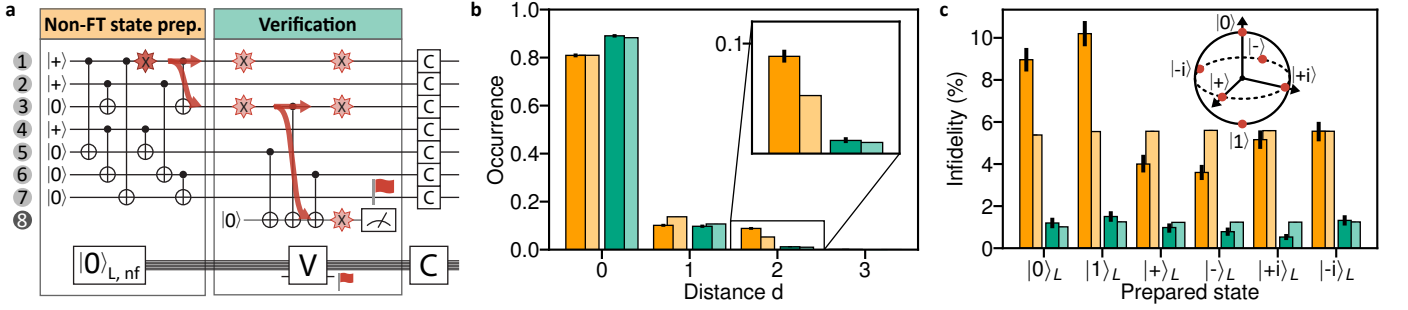


FIG. 2. Fault-tolerant (FT) preparation of a logical basis state $|0\rangle_L$ and logical Clifford operations. (a) Logical Pauli states are prepared fault-tolerantly in three steps: First $|0\rangle_L$ is prepared by a non-fault-tolerant circuit. fault tolerance is ensured through verification (V) of the state by coupling to an additional flag ancilla qubit. This qubit, when measured as $|0\rangle$, signals that the correct state has been prepared fault-tolerantly, i.e. up to single-qubit errors. To prepare a logical Pauli eigenstate other than $|0\rangle_L$ an additional transversal Clifford gate needs to be applied. (b) Relative occurrence rates of logical output states of distance d to the target state $|0\rangle_L$ for non-FT (orange) and FT (turquoise) initialization. Example states of $d = 1, 2, 3$ are $X_0|0\rangle_L, X_0X_1|0\rangle_L, X_0X_1X_2|0\rangle_L$. Simulation results are depicted by lighter colored bars. as described in the main text, all circuit elements are subject to depolarizing noise in numerical simulations. (c) Logical infidelities of all six logical Pauli eigenstates (red markers on Bloch sphere) including an ideal round of error correction performed in post-processing (experimental/simulation results depicted darker/lighter).

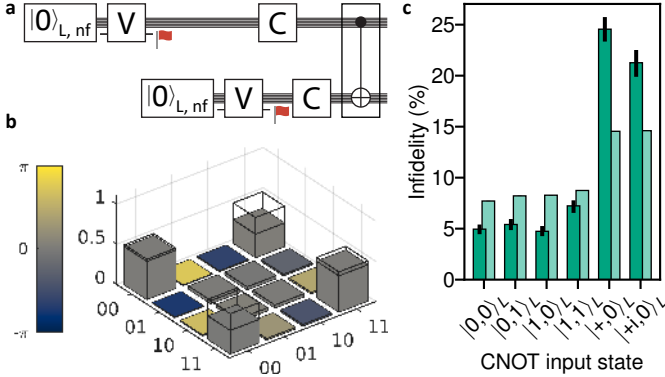


FIG. 3. FT implementation of a logical entangling gate. (a) To estimate the performance of the logical CNOT-gate we fault-tolerantly prepare six different logical two-qubit input states and apply the transversal CNOT-gate (framed gate at the end of the circuit). (b) Logical state tomography after applying the CNOT-gate to the $|+, 0\rangle$ state. The phase of the complex amplitudes is encoded in the color of the 3D bar plot and the wireframes depict ideal results. (c) Logical infidelities for six different input states of the CNOT-gate (experimental/simulation results depicted darker/lighter).

the two logical $|0\rangle_L$ states, then apply single-qubit rotations to prepare six different logical Pauli input states. The transversal logical CNOT-gate is implemented by sequentially applying CNOT-gates to corresponding pairs of physical qubits of the two logical qubits (see also Fig. 1b). A single error on any of the physical qubits propagates to at most one error on each of the logical qubits and therefore remains correctable, thereby ensuring fault tolerance of the gate realization. Applying the logical CNOT-gate to the input state $|+, 0\rangle_L$ yields the logical Bell state $\frac{1}{\sqrt{2}}(|0, 0\rangle_L + |1, 1\rangle_L)$ depicted in Fig. 3b.

This logical density matrix is retrieved from measurements of all nine twofold combinations of the logical observables X_L, Y_L and Z_L on the two logical qubits, followed by a maximum likelihood state reconstruction of the two-qubit state [40]. The logical fidelity of the logical Bell state is 0.754(9), consequently the correlations of the logical operator outcomes correspond to those of a Bell state with clear two-partite entanglement. Figure 3c shows the logical infidelity for six different input states. It reveals that the infidelity of output states is higher if the control qubit is in a superposition state, thus leading to an entangled outcome, compared to cases in which the outcome is a basis state of the logical two-qubit computational basis. This increased error rate is well-described by numerical simulations based on the circuit noise model: The average logical infidelity is 0.110^{+3}_{-4} and $0.1035(1)$ for the experimental implementation and the numerical simulation, respectively.

IV. UNIVERSAL FAULT-TOLERANT OPERATIONS

A universal set of logical gates allows to implement any logical unitary operation to arbitrary precision. The ability to perform a $\pi/4$ -rotation about any axis is known to be sufficient to augment the set of Clifford gates, which are transversal in the color code, to a universal gate set. The logical T-gate

$$T_L = e^{-i\frac{\pi}{8}Y_L} \quad (1)$$

performs a $\pi/4$ -rotation about the Y-axis and can be implemented by magic state injection as shown in Fig. 1b. It consists of the logical CNOT-operation we have demonstrated in the preceding section, a logical measurement and single-qubit Clifford operation conditioned on the

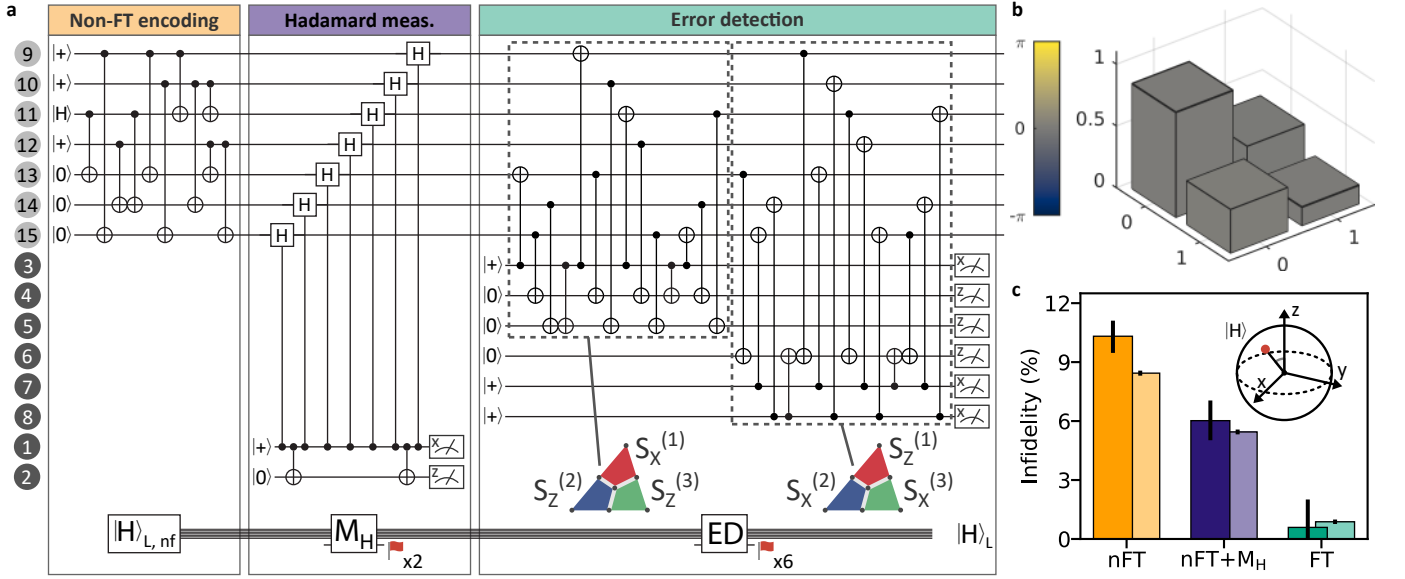


FIG. 4. Fault-tolerant generation of a logical magic state $|H\rangle_L$ (see Eqn. 2). (a) The magic state is prepared non-fault-tolerantly in a first step, where a physical magic state $|H\rangle$ is mapped to the logical state $|H\rangle_{L,nf}$ encoded in the data qubits at positions 9 to 15 in the ion string (see labels at left of circuit). Thereafter, a FT measurement of the Hadamard operator (M_H) is carried out. Two ancilla qubits herald that the prepared state is a $+1$ -eigenstate of the Hadamard operator but also that no dangerous error occurred during the measurement. The magic state preparation is concluded with an error detection block that measures the three X- and Z-type stabilizers each in a fault-tolerant fashion. The first part of the error detection circuit (first dashed box), measures $S_X^{(1)}, S_Z^{(2)}$ and $S_Z^{(3)}$, whereas the second part measures $S_Z^{(1)}, S_X^{(2)}$ and $S_X^{(3)}$. The magic state preparation is discarded and repeated in case of a non-trivial syndrome of the eight ancilla qubits 1 to 8. (b) Logical state tomography (see Sec. III) after FT magic state preparation. The phase of the complex amplitudes is encoded in the color of the 3D bar plot and the wireframes depict ideal results. Phase deviations from the ideal density matrix are smaller than 50 mrad while amplitude deviations are smaller than 0.07. (c) The decrease in infidelity of the logical magic state (red marker on Bloch sphere) after each step of the FT preparation procedure is observed experimentally and captured by depolarizing noise simulations (experimental/simulation results depicted darker/lighter).

logical measurement outcome. First preparing and then injecting the logical magic state

$$|H\rangle_L = \cos(\pi/8) |0\rangle_L + \sin(\pi/8) |1\rangle_L \quad (2)$$

enables gate teleportation of the logical non-Clifford T-gate. The logical magic state in Eq. (2) is the $+1$ -eigenstate of the logical Hadamard operator. Its corresponding -1 -eigenstate is $|-H\rangle_L = Y_L |H\rangle_L$, related to $|H\rangle_L$ via a logical Y-flip.

Recently, a resource-efficient procedure to prepare a magic state using FT circuits following the flag fault tolerance paradigm has been proposed [25]. The procedure consists of the following steps, depicted in Fig. 4a: we begin with a non-FT preparation of the magic state $|H\rangle_{L,nf}$, as recently demonstrated also in [30] (shown in subbox "Non-FT encoding"). Next, a measurement of the logical Hadamard operator is performed, which projects input states onto the $+1$ -eigenspace and discards states that are eigenstates with eigenvalue -1 (subbox "Hadamard meas."). The latter may be caused by single faults in the circuit (e.g. faults in the initial state preparation of $|H\rangle$ for physical qubit 11), thus rendering the circuit non-FT if -1 -eigenstates are not discarded in this step. Here both ancillas (qubits 1 and 2) are utilized as flag qubits.

The syndrome measurement ancilla flags when the -1 -eigenstate has erroneously been prepared, the second ancilla flags when a dangerous fault has occurred that may corrupt the state. The last step is a complete error correction (EC) cycle, consisting of fault-tolerantly measuring all six stabilizers of the color code using one flag qubit per stabilizer as suggested in [23]. The EC block is used to sort out faulty states whenever any flag qubit is measured as -1 and thus enables error detection (ED) (subbox "Error detection"). The resulting states after performing all three steps are guaranteed to be the correct logical magic state $|H\rangle_L$ up to correctable single-qubit errors provided at most one fault has occurred anywhere in the circuit. In total the protocol requires eight ancilla qubits that act as flags. The generated state is accepted as valid if all flag qubits indicate that no harmful error has happened.

We implement all steps for the magic state preparation and estimate the logical infidelities of the generated magic state. We compare the results to numerical simulations of depolarizing noise on all circuit operations. In Fig. 4b the reconstructed density matrix of the fault-tolerantly prepared magic state is shown and its ideal numerical values can be found in Eq. (35). Fig. 4c shows

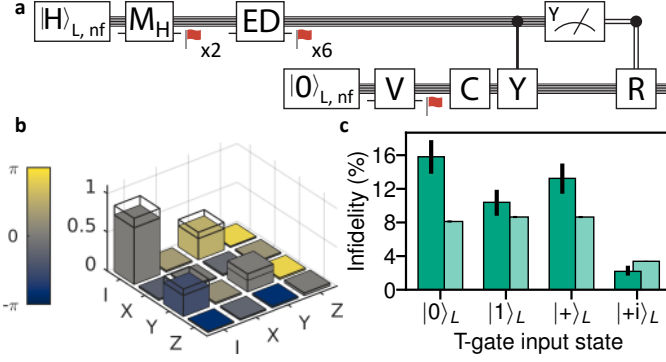


FIG. 5. FT T-gate injection. (a) After performing the fully fault-tolerant three step procedure of preparing the logical magic state, the logical T-gate is applied via logical gate teleportation onto a second register that has a logical Pauli state prepared. Conditional application of $R \equiv R_Y(\pi/2)$ is done in post-processing. (b) Logical process matrix of the experimental logical T-gate. The phase of the complex amplitudes is encoded in the color of the 3D bar plot and the wireframes depict ideal results. (c) Infidelities of the data qubit state when applying the logical T-gate to several logical Pauli input states (experimental/simulation results depicted darker/lighter). Infidelity is the lowest for the $|+i\rangle_L$ state since it is an eigenstate of the T-gate. Infidelity is slightly larger for $|1\rangle_L$ and $|+\rangle_L$ than for $|0\rangle_L$ since preparation contains an additional transversal Clifford operation prone to errors.

the logical infidelity of the magic state, which clearly decreases after each preparation step in both experiment and simulation. Each step of the magic state initialization process improves the quality of the generated logical state. After the full FT initialization procedure, a logical infidelity of 0.006^{+14}_{-5} for the magic state $|H\rangle_L$ with an acceptance rate of 13.7(3)% is found in the experimental realization, whereas numerical simulations predict approximately 27%, see Sec. VIII E for discussion.

Next, the fault-tolerant magic state initialization is followed by transversal Clifford operations to fault-tolerantly teleport the logical magic state, thereby resulting in a realization of a FT logical T-gate. For this, we perform an in-sequence measurement of the flag qubits for the magic state generation as sketched in Fig. 5a. In the case of heralded successful magic state generation, the ancilla qubits are in a well-defined state after the measurement and can directly be re-used to encode a second logical qubit in $|0\rangle_L$ using the FT protocol from Fig. 2a. We then apply a transversal Clifford operation on this second logical qubit to prepare one of the logical initial states $|0\rangle_L, |1\rangle_L, |+\rangle_L, |+i\rangle_L$. Finally, the transversal controlled-Y operation is applied on the second register and all physical qubits are measured. The measurement outcome for the logical Y-operator of the control qubit in the first register is then extracted and the conditional $Y(\pi/2)$ -rotation R to the target qubit in the second register is applied in post-processing, see Sec. VII

for details. By measuring the logical state of the target register for the four different initial states, it is possible to reconstruct the logical process matrix, shown in Fig. 5b with the ideal values explained in Sec. VIII D. Fig. 5c shows the logical infidelities for the different input states, yielding a mean infidelity of 0.10(1). It is expected and indeed observed experimentally that the best fidelity is achieved for the logical Y-eigenstate $|+i\rangle_L$ as it is an eigenstate of the T-gate. Infidelities for the three other logical input states are slightly higher, which qualitatively agrees with the numerical simulations.

V. DISCUSSION AND OUTLOOK

In this work we have demonstrated the first fault-tolerant implementation of a universal set of single- and two-qubit logical gates. We were able to witness a hallmark feature of fault-tolerant circuit design, namely an improvement of the performance of encoded qubits, despite the FT implementations of encoding and manipulation requiring an increased gate count and complexity of the underlying circuits. The resource-efficient implementation of these FT operations is enabled by the all-to-all qubit connectivity in the present trapped ion architecture, allowing for entangling operations between arbitrary pairs of qubits. Predictions from numerical simulations based on a relatively simple, generic and architecture-agnostic depolarizing circuit noise model, only informed by estimated experimental error rates, approximate the experimental findings well. The largest deviations between experimental behavior and numerical predictions were observed for the logical CNOT-gate. A more extensive characterization of this logical entangling gate and the other fault-tolerant gadgets, together with more sophisticated and validated theoretical noise models will be subject to future investigations, and is imperative for designing future QEC architectures and procedures.

On the way towards error-protected universal quantum computation on even more robust logical qubits, further milestones ahead are the incorporation of repetitive QEC cycles [30] into the FT logical gate operations demonstrated in our work. Another hurdle to be taken is the demonstration of error correction and FT gate operations for larger-distance logical qubits [25].

VI. EXPERIMENTAL METHODS

The experiments described in this work are performed on a trapped ion quantum computer. $^{40}\text{Ca}^+$ ions are trapped in a macroscopic Paul trap and the optical qubit is encoded in two Zeeman sublevels of the $4S_{1/2}$ and $3D_{5/2}$ electronic states. Further details on the experimental setup can be found in the recent publication [33].

A. Trapping and cooling

For this work, the ion crystal is configured to consist of 16 ions with an axial center-of-mass (COM) mode frequency $\omega_{\text{ax, COM}} = 2\pi \times 400 \text{ kHz}$ and radial COM mode frequencies of $\omega_{\text{rad1, COM}} = 2\pi \times 3270 \text{ kHz}$ and $\omega_{\text{rad2, COM}} = 2\pi \times 3100 \text{ kHz}$. Before executing any gate sequence, the radial motional modes of the ion chain are cooled nearly to the ground state via Doppler cooling for 2 ms, followed by resolved sideband cooling for 15 ms. Subsequently, the qubits are initialized via optical pumping to the $4S_{1/2, m_j=-1/2}$ ground state.

B. Qubit manipulation

Coherent qubit manipulation is performed by individually addressable laser pulses at a wavelength of 729 nm. Pulses resonant with the $4S_{1/2, m_j=-1/2}$ to $3D_{5/2, m_j=-1/2}$ transition enable rotations around an arbitrary axis in the equatorial plane of the Bloch sphere, where the angle between the rotation axis and the X-axis is determined by the phase ϕ of the light pulse. Those operations are described by $R_\phi^{(i)}(\theta) = \exp(-i\frac{\theta}{2}(\sigma_x^{(i)} \cos \phi - \sigma_y^{(i)} \sin \phi))$, where $\sigma_x^{(i)}$ and $\sigma_y^{(i)}$ are single-qubit Pauli matrices acting on qubit i . Rotations around the X-axis R_x (Y-axis R_y) can be implemented by setting ϕ to 0 ($-\pi/2$). A pulse length of 15 μs is required to implement a $\pi/2$ -pulse on a single qubit. Randomized benchmarking for single-qubit gates in the 16-ion chain yields an average fidelity of a $\pi/2$ -gate of $99.51 \pm 0.05\%$. Additionally, rotations around the Z-axis of the Bloch sphere for a specific ion can be implemented *virtually* by introducing a phase shift to all subsequent pulses applied to the ion.

Two-qubit gates are realized by the Mølmer-Sørensen interaction [34] described by $\text{MS}_{ij}(\theta) = \exp(-i\frac{\theta}{2}\sigma_x^{(i)}\sigma_x^{(j)})$. An arbitrary pair of ions is addressed with bichromatic beams slightly detuned from the radial COM mode $\omega_{\text{rad1, COM}}$. Gate time $t_{\text{gate}} = 270 \mu\text{s}$ and detuning from the COM mode $\Delta \approx 2\pi \times 3.7 \text{ kHz}$ are chosen to allow for simultaneous decoupling of the two closest radial modes $\omega_{\text{rad1, COM}}$, $\omega_{\text{rad1, 2}}$ at the end of the interaction. An additional (third) frequency tone, 1.05 MHz blue-detuned from the carrier transition, compensates the AC Stark shift induced by the bichromatic light field. For $\theta = \pi/2$ this results in an XX-gate which is equivalent to a CNOT-gate up to single-qubit rota-

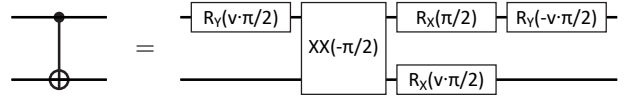


FIG. 6. Decomposition of a CNOT-gate into gates native to the experimental architecture used in this work. The parameter $v = \pm 1$ can be varied arbitrarily.

tions [41], as depicted in Fig. 6. The average Bell state fidelity in a chain of 16 ions is about 97.5% for entangling gates between neighbouring ions.

C. State readout

Qubit state readout is performed by illuminating the ions with a light field resonant to the $4S_{1/2}$ to $4P_{1/2}$ transition and collect scattered photons. Due to technical limitations imposed by the EMCCD camera, site-resolved state readout is only possible after the coherent evolution. In-sequence detection events utilizing an avalanche photodiode (APD) can only reveal the number of excitations present in the ion string. A subset of qubits can be read out in-sequence by shelving the population in the $4S$ state of all other ions to the $3D_{5/2, m_j=-3/2}$ Zeeman sublevel prior to the illumination of the ion string with the detection light field. This technique is used for the measurements presented in Sec. IV. For the FT initialization of the magic state the ancilla qubits are measured via the APD. If there are no excited ions detected, the protocol is continued by reusing the measured ions for encoding a second logical qubit state and injecting the magic state. After an illumination time of 2 ms for the EMCCD measurement and 0.5 ms for the APD measurement a readout fidelity of $> 99.7\%$ is achieved, where this number refers to the single-qubit readout fidelity for EMCCD measurements and the discrimination between 0 and > 0 excited qubits for APD measurements.

D. Error estimation

The errors given throughout this work solely account for statistical errors. For the estimation of the statistical fluctuations all measured outcomes are resampled from a multinomial distribution according to their respective probabilities. The stated errors in the text but also errorbars given in figures correspond to 68% confidence intervals extracted from the resampled datasets.

VII. SIMULATION METHODS

Theoretical simulation results presented in the main text are obtained using stabilizer simulations and state-vector simulations for the logical Pauli states and magic

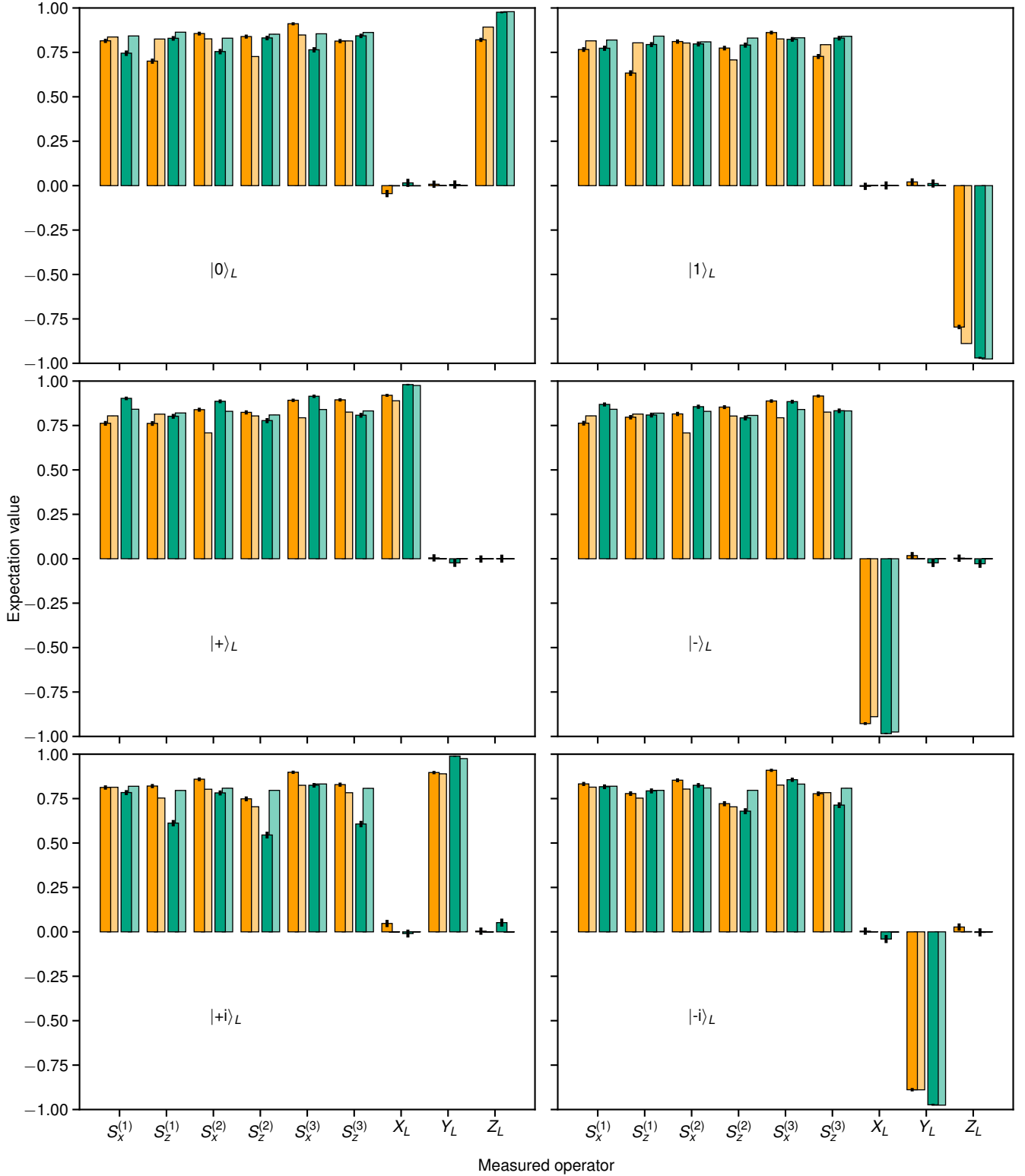


FIG. 7. Expectation values of the stabilizer generators and the logical operators of the seven-qubit color code for the six cardinal states of the Bloch sphere. Results for the non-FT and FT preparation scheme are depicted in orange and turquoise respectively, whereas results from numerical simulations are shown in lighter colored bars. 2500 and 10^6 runs were performed in the experiment and for simulations for each prepared state, respectively. For the calculation of the expectation values of the logical operators a round of perfect error correction is applied. For the measurements corresponding to the data presented in this figure but also in Fig. 2 the sign of the rotation angle of physical Y-rotations is flipped, effectively implementing an additional deterministic π phase flip on qubit 6 and a π bit flip on qubit 7 at the end of the circuit depicted in Fig. 2a. The effects of this redefinition do not amount in a change of measurement bases and can be readily accounted for in post-processing.

state preparation and injection circuits, respectively. We use the "Performance Estimator of Codes On Surfaces" (PECOS) package due to its flexibility in analyzing error propagation in different error models through Monte Carlo (MC) simulation (publicly available at <https://github.com/PECOS-packages/PECOS>) [42]. In these simulations any ideal circuit element is replaced by a faulty element, consisting of the ideal operation followed by an error operator, with a given probability.

We model circuit errors as depolarizing errors, which reproduces well the experimentally observed infidelities despite its conceptual simplicity which does not take the microscopic physical processes underlying noisy gates and operations in the ion trap into account explicitly. Noise is applied in simulations by randomly placing Pauli errors E according to the experimental physical error rates after every single-qubit operation, i.e. single-qubit gates, initializations and measurements, as well as two-qubit gates, each with their respective error rates p_1 , p_i , p_m and p_2 . These errors can be

$$E_x \in \{\sigma_k, \forall k \in \{1, 2, 3\}, x \in \{1, i, m\}\} \quad (3)$$

$$E_2 \in \{\sigma_k \otimes \sigma_l, \forall k, l \in \{0, 1, 2, 3\} \setminus \{I \otimes I\}\} \quad (4)$$

where $\sigma_k = \{I, X, Y, Z\}$ with $k = 0, 1, 2, 3$ are the Pauli matrices. The error channels for our depolarizing noise model read

$$\mathcal{E}_x(\rho) = (1 - p_x)\rho + \frac{p_x}{3}(X\rho X + Y\rho Y + Z\rho Z) \quad (5)$$

$$\mathcal{E}_2(\rho) = (1 - p_2)\rho + \frac{p_2}{15} \left[\sum_{i,j=0}^3 (\sigma_i \rho \sigma_j) - \rho \right] \quad (6)$$

so that any single-qubit error is applied uniformly to the ideal operation with equal probability $p_x/3$ and the single-qubit operation is executed ideally with probability $1 - p_x$; two-qubit errors are applied uniformly after the ideal two-qubit gates with equal probability $p_2/15$ and any two-qubit gate is executed ideally with probability $1 - p_2$. In all simulations we used physical error rates of

$$\begin{aligned} p_1 &= 0.005 \\ p_2 &= 0.025 \\ p_i &= p_m = 0.003 \end{aligned} \quad (7)$$

for the corresponding operations.

The logical Pauli state encoding circuits (Fig. 2a) and logical CNOT circuit (Fig. 3a) are simulated efficiently using stabilizer simulations. This is possible since we are preparing eigenstates of Pauli operators, measuring exclusively in one of three possible Pauli bases here and these circuits only contain Clifford gates.

This description as stabilizer states breaks down when arbitrary single-qubit rotations are to be performed by the circuit, especially with regards to the magic state, Eq. (2), that generates the non-Clifford T-gate. The circuits that fault-tolerantly prepare the logical magic state

(Fig. 4a) and perform the gate teleportation (Fig. 5a) contain non-Clifford operations and thus we are required to run full statevector simulations.

In the teleportation circuit (Fig. 5a), the logical controlled-Y is followed by measurement of all data qubits of the first register in the Y-basis and application of a classically controlled Y-rotation

$$R \equiv R_Y(\pi/2) \quad (8)$$

depending on the measurement result of the first register where the logical magic state has been prepared previously. The logical gate $R_L \simeq R^{\otimes 7}$ is applied to the second register which carries a logical Pauli state, e.g. $|+\rangle_L$. The resulting output state is the logical T-gate applied to the logical Pauli state, e.g. $T_L |+\rangle_L$. Both in simulation and experiment the effect of the R-gate is taken into account by altering the destructive final data qubit measurements. Since R is a $\pi/2$ -rotation about the Y-axis, it maps Z-basis states onto X-basis states and vice versa.

VIII. CHARACTERIZATION METHODS

A. Ideal error correction

Whenever performing destructive measurements on encoded data qubits we may reinterpret the measurement result according to the color code look-up table decoder. For example, from measuring the bitstring 0000001 on a seven-qubit register we may conclude for low physical error rates present in our setup that the likeliest error on those qubits has been a single X-flip on the first qubit and reinterpret the measurement result as 0000000. This process of ideal or in-software error correction (EC) is commonly used and possible whenever one aims not to keep running further quantum circuits on the error-corrected state. In general the corrected bitstring is determined by extracting the syndrome from the overlap of the measured bitstring with the stabilizer generators in binary notation and applying the respective correction. For CSS codes such as the color code the X- and Z-sectors can be treated distinctly. So when measuring the bitstring 0000001 in the Z-basis, the overlap with Z-stabilizers in binary notation $s_Z^{(1)} = 1010101$, $s_Z^{(2)} = 1111000$, $s_Z^{(3)} = 1100110$ yields the syndrome $[-1, +1, +1]$. Here binary 1s correspond to a Pauli Z-operator for the single qubit at the respective position and binary 0s represent the identity operation. Reinterpreting the measured bitstring as 0000000 is equivalent to applying a X_1 correction operator based on the syndrome information which would correctly recover the original state. Since in this work we are demonstrating FT operations, all final quantum states may only be correct up to an arbitrary single Pauli error. These errors are accounted for via ideal error correction.

B. Logical Pauli states

When fault-tolerantly encoding logical Pauli states we characterize the output state by categories of errors present after executing the circuit in Fig. 2a. The categories of errors given in Fig. 2b refer to the states of distance d to the desired $|0\rangle_L$ -state which determines whether or not we can correctly identify the state as $|0\rangle_L$ after ideal EC.

We obtain the distance d to the desired $|0\rangle_L$ -state by destructively measuring the data qubit register and finding the minimal Hamming distance D_H of the measurement bitstring m to the bitstrings that label the basis states of

$$\begin{aligned} |0\rangle_L = \frac{1}{\sqrt{8}} & \left(|0000000\rangle + |1010101\rangle + |0110011\rangle \right. \\ & + |1100110\rangle + |0001111\rangle + |1011010\rangle \\ & \left. + |0111100\rangle + |1101001\rangle \right) \end{aligned} \quad (9)$$

in post-processing:

$$d \equiv \min \left(D_H(m, 0000000), D_H(m, 1010101), \dots, D_H(m, 1101001) \right). \quad (10)$$

Ideal EC will trivially correct the exact $|0\rangle_L$ state, i.e. $d = 0$, and correct all states with single Pauli errors, e.g. $X_2|0\rangle_L$ ($d = 1$). It will yield the logically flipped $|1\rangle_L$ result when acting on a state of distance $d = 2$ or $d = 3$ from $|0\rangle_L$, i.e. $|0\rangle_L$ carrying two X-errors or directly a weight-3 logical bit flip X_L .

For arbitrary logical Pauli states destructive measurements must be performed in their respective basis. However, only Pauli-X (Pauli-Z) errors are visible in the preparation of logical Pauli-Z (Pauli-X) basis states $|0\rangle_1, |1\rangle_L$ ($|\pm\rangle_L$).

Note that for all measurements on the characterization of logical Pauli states shown in Fig. 2 and Fig. 7 an accidental redefinition of the rotation direction of physical single-qubit Y-rotations is accounted for in post-processing. See Fig. 7 for more details.

C. Logical fidelities

Single-qubit logical states. – The logical fidelities presented in the main text are obtained by reconstructing the logical Bloch vector of the prepared state ρ and determining the overlap with the Bloch vector of a logical target state. Within the code space, the projector onto an ideal single-qubit logical target state $\rho_t = |t\rangle\langle t|_L$ is given by

$$P_t = \frac{1}{2} (I + O_t) \quad (11)$$

with O_t the logical operator that the target state $O_t|t\rangle_L = |t\rangle_L$ is the +1-eigenstate to. For the Pauli states considered in this work the projectors are

$$P_{0/1} = \frac{1}{2} (I \pm Z_L) \quad (12)$$

$$P_{\pm} = \frac{1}{2} (I \pm X_L) \quad (13)$$

$$P_{\pm i} = \frac{1}{2} (I \pm Y_L) \quad (14)$$

and logical fidelity of a prepared state ρ follows as

$$\mathcal{F}_t(\rho) = \langle P_t \rangle = \text{tr}(P_t \rho). \quad (15)$$

We emphasize that these logical fidelities are *not* equivalent to the full quantum state fidelities $\mathcal{F} = \text{tr}(\rho_t \rho)$ but are the probabilities to be able to correctly conclude which logical state was intended to be prepared or stored.

Combining Eqs. (12)-(14) with the expression for the logical fidelity in Eq. (15), we can see that expectation values of logical Pauli operators O_t need to be determined in order to find the logical fidelities

$$\mathcal{F} = \frac{1}{2} (1 \pm \langle O_t \rangle) \quad \text{with } O_t \in \{X_L, Y_L, Z_L\}, \quad (16)$$

which e.g. evaluates to $\mathcal{F}_0 = \frac{1}{2} (1 + \langle Z_L \rangle)$ for the logical Pauli state $|0\rangle_L$. All six cardinal state logical fidelities are shown in Fig. 2c. We sample the expectation values of the logical Pauli operators by running stabilizer simulations of the respective preparation circuit $N = 10^6$ times followed by destructive measurement of all data qubits and ideal EC in the respective Pauli basis. The measurement result for a logical operator before EC is determined as $(-1)^{|m|}$ by the number of 1s in the measurement bitstring m modulo 2. Then a round of ideal EC as described in Sec. VIII A is performed to obtain the final measurement result. Measurement results from each run are averaged to obtain the expectation value of the respective logical operator.

Two-qubit logical states. – In order to characterize the logical CNOT-gate through stabilizer simulations we first list its action on various logical input states in the table below:

input	output
$ 0, 0\rangle_L$	$ 0, 0\rangle_L$
$ 0, 1\rangle_L$	$ 0, 1\rangle_L$
$ 1, 0\rangle_L$	$ 1, 1\rangle_L$
$ 1, 1\rangle_L$	$ 1, 0\rangle_L$
$ +, 0\rangle_L$	$ \beta\rangle_L$
$ +i, 0\rangle_L$	$ \gamma\rangle_L$

where $|x, y\rangle_L = |x\rangle_L \otimes |y\rangle_L$. Single logical qubit states $|x\rangle_L$ and $|y\rangle_L$ are prepared distinctly in two seven-qubit registers. The CNOT-gate, acting $|x, y\rangle_L \mapsto |x, y \oplus x\rangle_L$, flips the second bit (target) if the first bit (control) is in the 1-state. Thus, $|+, 0\rangle_L$ is mapped to the maximally entangled Bell state

$$|\beta\rangle_L = \frac{1}{\sqrt{2}} (|0, 0\rangle_L + |1, 1\rangle_L), \quad (17)$$

which can equivalently be expressed by the logical density operator

$$\rho_\beta = |\beta\rangle\langle\beta|_L \simeq \frac{1}{2} \begin{pmatrix} 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 \end{pmatrix} \quad (18)$$

where the matrix representation is in the logical two-qubit computational basis. Quantum state tomography has been performed to quantify experimental capabilities to obtain the logical Bell state described by this density matrix as shown in Fig. 3b. Expectation values of all logical two-qubit Pauli matrices including the identity are measured and subsequently maximum likelihood techniques are used to reconstruct the logical density operator [40]. The Bell state is stabilized by the logical operators $Z_L^1 Z_L^2$ and $X_L^1 X_L^2$ where superscripts ^{1,2} refer to the two logical qubits. Analogously, the CNOT maps input $|+i, 0\rangle_L$ to the Y-basis maximally entangled state

$$|\gamma\rangle_L = \frac{1}{\sqrt{2}}(|0, 0\rangle_L + i|1, 1\rangle_L). \quad (19)$$

Its stabilizers can be obtained by realizing that both states are related via a phase gate

$$|\gamma\rangle = S_1 |\beta\rangle \quad (20)$$

so by transforming the stabilizer generators of $|\beta\rangle$ as

$$S_1 Z_1 Z_2 S_1^\dagger = Z_1 Z_2 \quad (21)$$

$$S_1 X_1 X_2 S_1^\dagger = X_1 Y_2 \quad (22)$$

we obtain the stabilizer generators of $|\gamma\rangle$.

The projectors onto the logical two-qubit output states we wish to characterize is now given by the product of the projectors onto the simultaneous +1-eigenspace of the logical operators in both registers

$$P_{00} = (P_0 \otimes I)(I \otimes P_0) = \frac{1}{2} (I + Z_L^1) \frac{1}{2} (I + Z_L^2) \quad (23)$$

$$P_{01} = (P_0 \otimes I)(I \otimes P_1) = \frac{1}{2} (I + Z_L^1) \frac{1}{2} (I - Z_L^2) \quad (24)$$

$$P_{11} = (P_1 \otimes I)(I \otimes P_1) = \frac{1}{2} (I - Z_L^1) \frac{1}{2} (I - Z_L^2) \quad (25)$$

$$P_{10} = (P_1 \otimes I)(I \otimes P_0) = \frac{1}{2} (I - Z_L^1) \frac{1}{2} (I + Z_L^2) \quad (26)$$

$$P_\beta = \frac{1}{2} (I + X_L^1 X_L^2) \frac{1}{2} (I + Z_L^1 Z_L^2) \quad (27)$$

$$P_\gamma = \frac{1}{2} (I + Z_L^1 Z_L^2) \frac{1}{2} (I + X_L^1 Y_L^2) \quad (28)$$

Employing Eq. (15), the logical fidelities for the output states of the logical CNOT-gate follow as expectation

values of the logical two-qubit state projectors as

$$\mathcal{F}_{00} = \frac{1}{4} (1 + \langle Z_L^1 \rangle + \langle Z_L^2 \rangle + \langle Z_L^1 Z_L^2 \rangle) \quad (29)$$

$$\mathcal{F}_{01} = \frac{1}{4} (1 + \langle Z_L^1 \rangle - \langle Z_L^2 \rangle - \langle Z_L^1 Z_L^2 \rangle) \quad (30)$$

$$\mathcal{F}_{11} = \frac{1}{4} (1 - \langle Z_L^1 \rangle - \langle Z_L^2 \rangle + \langle Z_L^1 Z_L^2 \rangle) \quad (31)$$

$$\mathcal{F}_{10} = \frac{1}{4} (1 - \langle Z_L^1 \rangle + \langle Z_L^2 \rangle - \langle Z_L^1 Z_L^2 \rangle) \quad (32)$$

$$\mathcal{F}_\beta = \frac{1}{4} (1 + \langle X_L^1 X_L^2 \rangle - \langle Y_L^1 Y_L^2 \rangle + \langle Z_L^1 Z_L^2 \rangle) \quad (33)$$

$$\mathcal{F}_\gamma = \frac{1}{4} (1 + \langle Z_L^1 Z_L^2 \rangle + \langle X_L^1 Y_L^2 \rangle + \langle Y_L^1 X_L^2 \rangle) \quad (34)$$

and are shown in Fig. 3b as results of $N = 10^6$ stabilizer simulation runs of the logical CNOT circuit followed by destructive measurement of all data qubits and ideal EC in the respective Pauli basis. Averaging over measurement results for the logical operators yields their expectation value.

The logical magic state $|H\rangle_L$ may be denoted by the logical density operator

$$\rho_H = |H\rangle\langle H|_L \simeq \frac{1}{2} \begin{pmatrix} 1 + 1/\sqrt{2} & 1/\sqrt{2} \\ 1/\sqrt{2} & 1 - 1/\sqrt{2} \end{pmatrix} \quad (35)$$

where the matrix representation is in the logical computational basis. Quantum state tomography of the experimentally prepared logical magic state is shown in comparison to the theoretical values in Eq. (35) in Fig. 4b. The fidelity of the logical magic state as shown in Fig. 4c is given by

$$\mathcal{F}_H = \frac{1}{2} \left(1 + \frac{\langle X_L \rangle + \langle Z_L \rangle}{\sqrt{2}} \right) \quad (36)$$

since the logical magic state is the +1-eigenstate of the logical Hadamard operator $H_L |H\rangle_L = |H\rangle_L$ and its projector reads

$$P_H = \frac{1}{2} (I + H_L) = \frac{1}{2} \left(I + \frac{X_L + Z_L}{\sqrt{2}} \right). \quad (37)$$

When we inject the logical magic state onto logical Pauli states the result is the logical T-gate applied to the previously prepared logical Pauli state

$$|\psi\rangle_{L,\text{out}} = T_L |t\rangle_{L,\text{in}}. \quad (38)$$

For the four different input logical Pauli states $|0\rangle_L$, $|1\rangle_L$, $|+\rangle_L$ and $|+i\rangle_L$ the output states are

$$|H\rangle_L = T_L |0\rangle_L \quad (39)$$

$$|-H\rangle_L = T_L |1\rangle_L \quad (40)$$

$$X_L |H\rangle_L = T_L |+\rangle_L \quad (41)$$

$$|+i\rangle_L = T_L |+i\rangle_L \quad (42)$$

and their projectors read

$$P_{0/1} = \frac{1}{2} (I \pm H_L) = \frac{1}{2} \left(1 \pm \frac{X_L + Z_L}{\sqrt{2}} \right) \quad (43)$$

$$P_+ = X_L P_0 X_L = \frac{1}{2} \left(1 + \frac{X_L - Z_L}{\sqrt{2}} \right) \quad (44)$$

$$P_{+i} = \frac{1}{2} (I + Y_L). \quad (45)$$

The respective logical T-gate output state fidelities \mathcal{F}_t for input Pauli state $|t\rangle_L$ are then given by

$$\mathcal{F}_0 = \frac{1}{2} \left(1 + \frac{\langle X_L \rangle + \langle Z_L \rangle}{\sqrt{2}} \right) \quad (46)$$

$$\mathcal{F}_1 = \frac{1}{2} \left(1 - \frac{\langle X_L \rangle + \langle Z_L \rangle}{\sqrt{2}} \right) \quad (47)$$

$$\mathcal{F}_+ = \frac{1}{2} \left(1 + \frac{\langle X_L \rangle - \langle Z_L \rangle}{\sqrt{2}} \right) \quad (48)$$

$$\mathcal{F}_{+i} = \frac{1}{2} (1 + \langle Y_L \rangle). \quad (49)$$

To estimate the expectation values of the logical operators occurring in the expressions for the fidelities given above, we run $N = 10^5$ statevector simulations of the FT preparation and injection circuits. Each run is followed by destructive measurement in the respective Pauli basis and ideal EC that determines a measurement outcome of the logical Pauli operator. The expectation value is then calculated as the mean over all measurement outcomes.

The sampling uncertainty ε_L when sampling the expectation value of a logical Pauli operator O_L is $\varepsilon_L = \sqrt{\frac{\text{Var}(\langle O_L \rangle)}{N}}$ and is propagated to their respective fidelities by Gaussian error propagation.

D. Logical process matrix

Process matrices can be used to parameterize quantum channels

$$\mathcal{E}(\rho) = \sum_{n=0}^3 \sum_{m=0}^3 \chi_{mn} E_m \rho E_n^\dagger \quad (50)$$

in the quantum operations formalism. The process matrix χ_{mn} for the logical T-gate that we show in Fig. 5b is described by the quantum channel

$$\mathcal{E}(\rho) = T \rho T^\dagger = \sum_{n=0}^3 \sum_{m=0}^3 \chi_{mn} \sigma_m \rho \sigma_n \quad (51)$$

where we expand the channel in terms of the logical Pauli matrices. The matrix representation of χ in the logical Pauli basis reads

$$\chi = \frac{1}{2} \begin{pmatrix} 1 + 1/\sqrt{2} & 0 & i/\sqrt{2} & 0 \\ 0 & 0 & 0 & 0 \\ -i/\sqrt{2} & 0 & 1 - 1/\sqrt{2} & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix}. \quad (52)$$

Measurements of expectation values of the logical Pauli basis for the T-gate input states $|0\rangle_L$, $|1\rangle_L$, $|+\rangle_L$ and $|+i\rangle_L$ form a tomographically complete set and allow for the reconstruction of the process matrix χ_{mn} [40].

E. Acceptance rates

We define the *acceptance rate* as ratio of circuit runs where all flag qubits are measured as +1. The logical Pauli $|0\rangle_L$ -state is fault-tolerantly encoded ($|0\rangle_{L,\text{ft}}$) using the circuit given in Fig. 2a, the logical magic state is prepared both by using the non-FT circuit followed by only the transversal Hadamard measurement ($|H\rangle_{L,\text{nf}}$ & M_H) and by using the full FT protocol ($|H\rangle_{L,\text{ft}}$) as given in Fig. 4a. Approximate acceptance rates in simulation and experiment are shown in the table below for these three different encoding circuits alongside with the respective number of qubits acting as flags as well as circuit depth:

encoding	depth	#flags	simulation	experiment	$\Delta\varepsilon$
$ 0\rangle_{L,\text{ft}}$	25	1	85%	79%	7%
$ H\rangle_{L,\text{nf}}$ & M_H	32	2	72%	57%	21%
$ H\rangle_{L,\text{ft}}$	75	8	27%	14%	48%

We observe that the relative error $\Delta\varepsilon$ between MC simulation and experimentally measured acceptance rates for the respective circuits increases with larger circuit depth and number of flag qubits involved.

IX. DATA AVAILABILITY

The data underlying the findings of this work and the quantum circuits are available at <https://doi.org/10.5281/zenodo.5725062>.

X. CODE AVAILABILITY

All codes used for data analysis are available from the corresponding author upon reasonable request.

XI. AUTHOR CONTRIBUTIONS

L.P., I.P. and T.F. carried out the experiments. L.P., I.P., T.F., M.Meth, C.D.M., R.S., M.Ringbauer, P.S. and T.M. contributed to the experimental setup. L.P. analyzed the data. S.H. performed the numerical simulations. S.H., M.Rispler and M.Müller performed circuit analysis, characterization and theory modelling. L.P., S.H., I.P., M.Rispler, P.S. and M.Müller wrote the manuscript, with contributions from all authors. R.B., P.S., M.Müller and T.M. supervised the project.

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