Project 6.6 Classiq: Implement a Multi-Control-X

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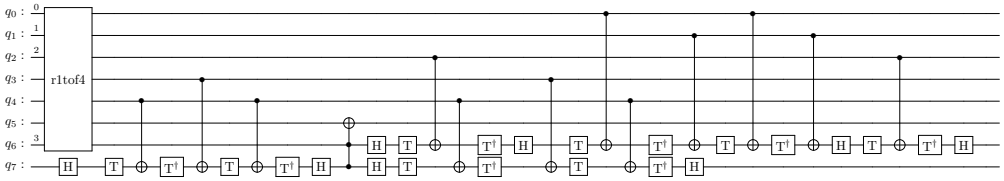
1 Task A

Synthesize 3 different implementations of an MCX (multi-control-x) with 5 control qubits and 1 target qubit (you should use the control quantum operation for implementing an MCX, follow thisLinks to an external site. tutorial that can be open in the IDE). One implementation should be optimized for minimized depth, the other for minimized width, and the third somewhere in between (choose yourself what is the maximal width / depth you apply). Explain the key differences.

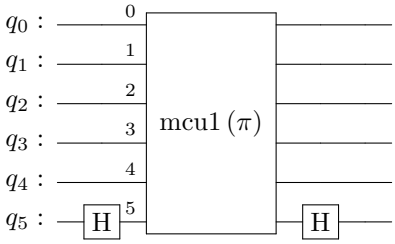
1.1 Optimize for *depth*

Model has been synthesized by specifying Optimization "*depth*". No backend was selected.
Program depth: 47 & width: 8. Gate count: H:14, T:16, Cx: 24, TDG: 15
Transpiled circuit depth: 34 & width: 8. Gate count: U:28, CX:24



1.2 Optimize for *width*

Model has been synthesized by specifying Optimization "*width*". No backend was selected.
Program depth: 63 & width: 6. Gate count: H:2, CU1:31, CX: 30
Transpiled circuit depth: 117 & width: 6. Gate count: U:91, CX:80

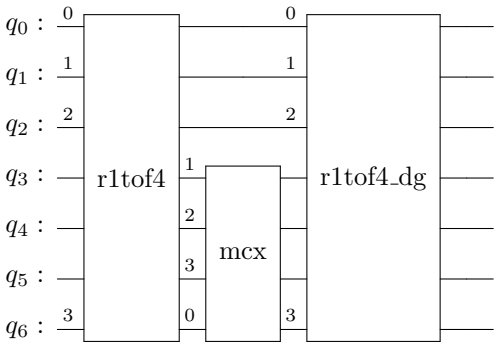


1.3 *In between* case

Model has been synthesized by specifying the constraint "Width=7" while using Optimization "*width*". No backend was selected.

Program depth: 63 & width: 7. Gate count: H:10, T:8, CX: 26. TDG: 8, P: 15.

Transpiled circuit depth: 51 & width: 7. Gate count: U:29, CX:26



1.4 Discussion

The data for program depth and width, along with circuit depth and width, for all three cases mentioned above is summarized in the table below.

Option	Program Width	Program Depth	Circuit Width	Circuit Depth	Circuit Gate Count U	Circuit Gate Count CX
Minimum Width	6	63	6	117	91	80
In Between	7	63	7	51	29	26
Minimum Depth	8	47	8	34	28	24

The MCX (Multiple-Control Toffoli) gate, also known as the multi-controlled NOT gate, performs a NOT operation (flips the target qubit) only when all control qubits are in the $|1\rangle$ state.

Program Width is the number of qubits in the high-level program, whereas Transpiled Circuit Width is the number of qubits after transpilation, potentially higher due to additional requirements like error correction; similarly, Program Depth is the number of gate layers in the high-level program, while Transpiled Circuit Depth is the number of gate layers after transpilation, often decreased due to hardware-specific optimizations.

For our specifications, Program Width and Circuit Width remained the same in each of the cases analysed, Minimum Width, Minimum Depth and In between.

In general, the program/circuit depth decreases dramatically with each additional qubit (Width increase), although the Program Depth is the same for 6 and 7 qubits, respectively. Increasing the width by 1 qubit from 6 to 7 decreases the Circuit Depth from 117 to 51 (about 56% decrease); by increasing the Program/Circuit Width from 7 to 8 qubits decreases the Circuit Depth from 51 to 34 (about 33% decrease).

These numbers also reflect the dynamic of the number of Circuit Gates, with a significant decrease in the case of increasing the number of qubits from 6 to 7 (the total gate count decreases from 171 to 55, or about 67% decrease), and a less dramatic decrease for the case of increasing the number of qubits from 7 to 8 (the total gate count decreases from 55 to 52, or about 5% decrease).

Overall and for our problem of implementing the MCX gate, the *In Between* case looks like a good compromise between keeping the number of qubits low (qubits are expensive) and using fewer gates in the Transpiled Quantum Circuits.

2 Task B

Synthesize 2 different implementations of an MCX (multi-control-x) with 20 control qubits and 1 target qubit. Compare the circuit width and circuit depth required for each implementation. Strategy: Use optimization on each of Width and Depth, and then constrain on the number of qubits and optimize on Depth (in-between cases).

2.1 Implementation 1

For an optimal (minimum) Depth of 119 Program Gate Layers and 66 Transpiled Circuit Gate Layers, the Width was 30 qubits.

2.2 Implementation 2

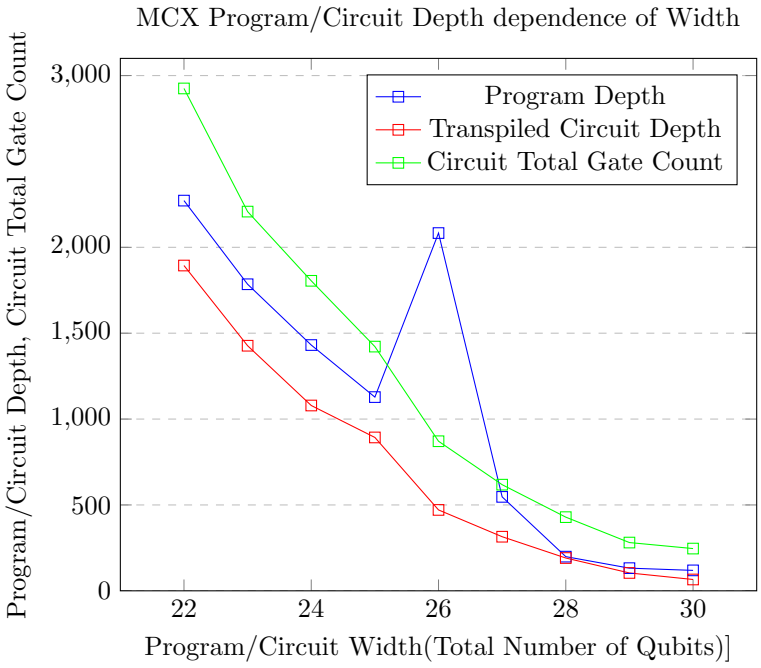
For an optimal (minimum) Width of 22 qubits, the Depth was 2,272 for Program Gate Layers and 1,894 for Transpiled Circuit Gate Layers.

2.3 Discussion

All qubit values between 22 (optimal/minimum Width) and 30 (optimal/minimum Depth) were used as constraints to synthesize 9 circuits. Tabular data is presented below:

Total number of Qubits	Program Depth	Circuit Depth	Circuit Total Gate Count
22	2,272	1,894	2,925
23	1,785	1,427	2,208
24	1,431	1,079	1,805
25	1,128	893	1,422
26	2,083	471	871
27	547	315	618
28	199	191	429
29	132	104	281
30	119	66	246

Plotting from data:



With a notable exception of one data point, Program Depth for 26 qubits, all graphs are consistent with an exponential decay. The decrease in Circuit Depth Due to hardware optimization is relevant for number of qubits between 22 and 26, there is no significant decrease for number of qubits between 26 and 30.

I do not have enough expertise to add some smart commentary; however, I can assume the sweet spot will be a compromise between adding another expensive qubit (add in Width) to decrease the total number of Gate Layers (Circuit Depth) and Gates.

3 Final Thoughts and One Question

I learned a lot from working on this project about Quantum circuits and their hardware implementation using Classiq. Is the Program Depth off-reading at n=26 total qubits a bug or a correct value, and if it is correct, what is the reason?

Thank you!