Exercise-6

June 30, 2024

1 TASK A

[1]:
```
from classiq import *


@qfunc
def main(cntrl: Output[QArray[QBit]], target: Output[QBit]) -> None:
    allocate(5, cntrl)
    allocate(1, target)
    control(ctrl=cntrl, operand=lambda: X(target))
```

[2]:
```
qmod = create_model(main)
```

[3]:
```
write_qmod(qmod, "mcx_example")
qprog = synthesize(qmod)
```

[4]:
```
qmod_depth = set_constraints(
    qmod, Constraints(optimization_parameter="depth")
)
```

[5]:
```
qmod_width = set_constraints(
    qmod, Constraints(optimization_parameter="width")
)
```

[6]:
```
qmod_mix = set_constraints(
    qmod, Constraints(optimization_parameter="width", max_width=50,␣
 ↪max_depth=500)
)
```

[7]:
```
qprog_width = synthesize(qmod_width)
qprog_depth = synthesize(qmod_depth)
qprog_mix = synthesize(qmod_mix)
```

Here, the circuit is applied with the desired optimization parameters for the mcx gate, The first circuit optimizes depth, the second optimizes width and the last optimizes a mix the depth with a max filter on the depth and height as parameters for the circuit construction. The execution/ synthesis is done in the main site.

2 TASK B

[8]:
```
from classiq import *


@qfunc
def main(cntrl: Output[QArray[QBit]], target: Output[QBit]) -> None:
    allocate(20, cntrl)
    allocate(1, target)
    control(ctrl=cntrl, operand=lambda: X(target))
```

[9]:
```
mcx_model = create_model(main)
mcx_mix = set_constraints(
    mcx_model, Constraints(optimization_parameter="width", max_width=50,␣
 ↪max_depth=500)
)
```

[10]:
```
program1 = synthesize(mcx_model)
program2 = synthesize(mcx_mix)
```

[ ]:
```

```

For **Task B** we take the mcx example as given in the example guide. Our circuit has 20 control qubit and 1 target qubit and so has been given in the code. The first implementation is the trivial implementation of the same while for the second one we have a mix optimized circuit with optimization constraints in the form of width and depth as the previous task. Both of these implementations are different primarily due to the optimization operation and yield uniquely different circuit parameters.