# Ronit Nagarapu

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## EDUCATION

**University of California, Berkeley** **Berkeley, CA**
*M.S. Electrical Engineering and Computer Sciences* *Expected Graduation: May 2026*
*B.S. Electrical Engineering and Computer Sciences* **(GPA: 4.00)** *Graduated: May 2025*

Coursework: Computer Architecture, Digital Design & Integrated Circuits, FPGA Design, ASIC Design, Cryptography, Microelectronic Devices, Analog Circuits, Data Structures and Algorithms, Control Systems, and Artificial Intelligence

Extracurriculars:

- TA for CS152: Computer Architecture — Developed assignments for architectural modeling and programming
- President of Big Data at Berkeley — Managed 60+ members to execute DS/ML contract projects for companies
- EE Team at Formula Electric at Berkeley — Designed electronics systems for braking and accelerator control
- 2nd place at UC Berkeley's AI Hackathon for Best Knowledge Intensive LLM App
- 3rd place at Cal Hacks 9.0: InterSystems API Division
- 2nd place Data Visualization Award: Data Science Research at UC Berkeley

## SKILLS

- Programming: Python, Java, C, C++, Scala, SQL, Assembly, Rust
- Digital Design: Verilog, Chisel, Chipyard, Cadence (Indago, Genus, Innovus, Spectre, Virtuoso), Synopsys VCS
- Electronics: Altium, LTSpice, EasyEDA, Microcontrollers, Embedded Systems, Networking, Data Protocols
- Software Engineering: AWS, Bash, Linux, Git, Flask, React, PostgreSQL, Docker, REST APIs, Bootstrap
- Data Science: Numpy, PyTorch, Pandas, Matplotlib, Seaborn, Scikit-learn, Scipy, Plotly

## EXPERIENCE

**Amazon (Annapurna Labs):** *ML Chip Architect Intern* *May 2025 - August 2025*

- Prototyped architectural changes to Trainium accelerators to optimize performance for dynamic ML workloads
- Developed hardware and software solutions to boost performance for efficient control flow in MoE kernels
- Applied hardware-software co-design to coordinate requests between software, compiler, and hardware teams

**Amazon (Annapurna Labs):** *ML Chip Architect Intern* *September 2024 - December 2024*

- Analyzed novel hardware features for optimizing collective communication algorithms in ML workloads
- Designed monitoring tools for FPGA platforms to extract bandwidth & latency metrics of dataflow emulations
- Collaborated with users of AWS Neuron Kernel Interface to deploy LLM workloads on Tranium devices

**Apple:** *Design Verification Intern* *May 2024 - August 2024*

- Developed automated scripts using Cadence Indago to verify unique static properties in hardware security
- Researched optimal algorithms to explore and validate connectivity in cross-chip communication systems
- Prototyped visualization tools for DV workflows using Tableau and integrated static verification test pipelines

**UC Berkeley SLICE Lab:** *Hardware Design Researcher* *September 2023 - Current*

- Investigating profile-guided optimization techniques on ML accelerator hardware (AWS Tranium)
- Implemented UCIe 1.1 (Universal Chiplet Interface Express) in Scala and Chisel to optimize VLSI research
- Designed CRC module generator to validate data transfer, parameterizing for throughput and area

## PROJECTS

**Spot Micro Robot Dog:**

- Prototyped robotic quadruped dog for autonomous surveillance and search & rescue in disaster relief scenarios
- Developed embedded system with Raspberry Pi Zero, implemented dynamic control system with gyroscopes

**8-Bit Computer:**

- Enhanced open-source 8-bit TTL logic gate computer design with bus output multiplexing, active programming
- Designed Intel 6502 equivalent processor using CMOS logic chips with 50+ ISA, I/O ports, 64kB RAM/ROM

**Barker Code Light Barrier:**

- Developed visible light barrier circuit with Barker-7 code, multiprocessing Arduino Nano MCUs
- Applied autocorrelation property and signal analysis to filter ambient 60Hz interference with non-IR sensor