

PH3204: Electronics Laboratory

Experiment 04: Study of Boolean algebra truth tables for Logic Gate functions using AND, OR, NAND, NOR etc. ICs

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1 Theory

Boolean algebra deals with variables only two possible output, 0 and 1 (false and true). A Boolean function takes in one or more boolean inputs and produces a boolean output. A boolean function can be implemented in the form of a boolean circuit using logic gates. Some of the most common logic gates along with their truth tables are given below:

- NOT Gate

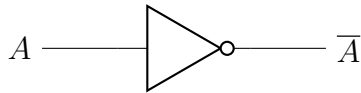
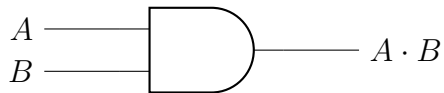


Figure 1: Symbol of NOT Gate

A	\overline{A}
0	1
1	0

Table 1: Truth Table for NOT Gate

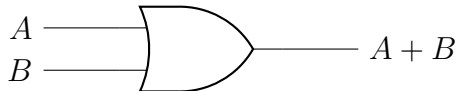
- AND Gate



A	B	$A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

Table 2: Truth Table for AND Gate

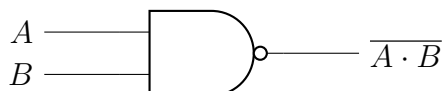
- OR Gate



A	B	$A + B$
0	0	0
0	1	1
1	0	1
1	1	1

Table 3: Truth Table for OR Gate

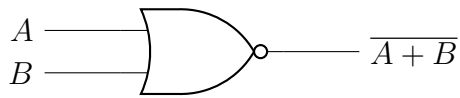
- NAND Gate



A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Table 4: Truth Table for NAND Gate

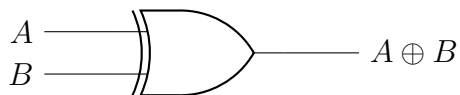
- NOR Gate



A	B	$\overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

Table 5: Truth Table for NOR Gate

• XOR Gate

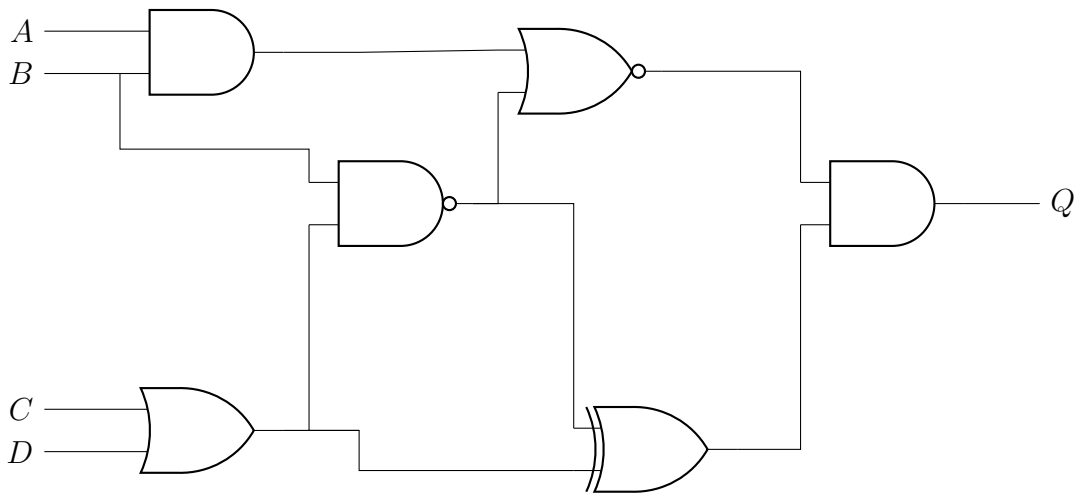


A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Table 6: Truth Table for XOR Gate

2 Boolean Circuit Verification

2.1 Example 1

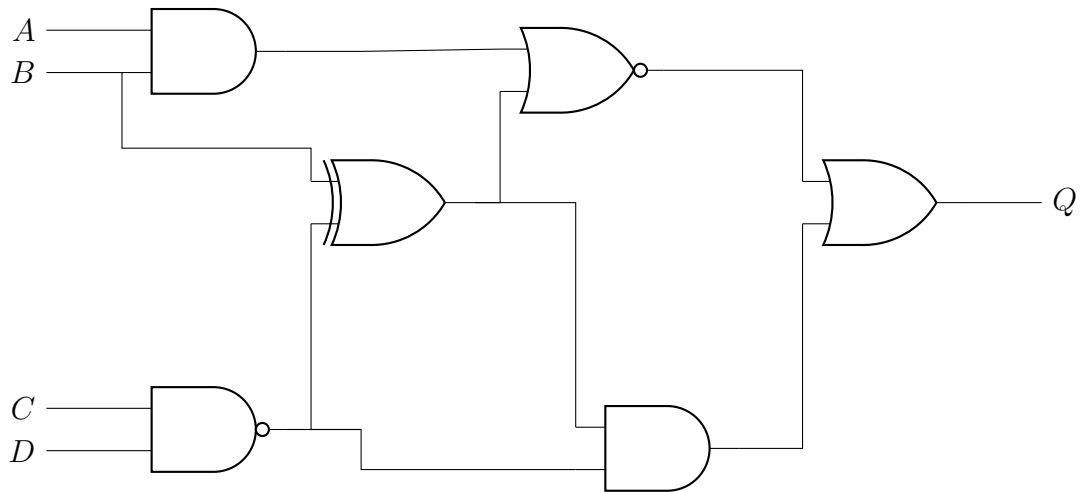


A	B	C	D	Q
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1

A	B	C	D	Q
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Table 7: Truth Table for Example 1

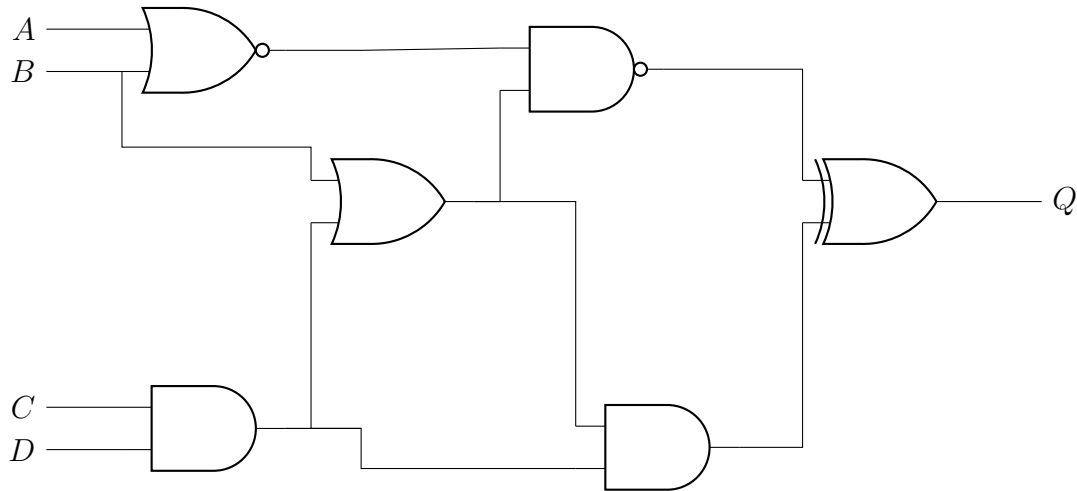
2.2 Example 2



A	B	C	D	Q
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Table 8: Truth Table for Example 2

2.3 Example 3



A	B	C	D	Q
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Table 9: Truth Table for Example 3

3 Conclusion

In this experiment, we studied three different boolean circuits and verified the truth tables for each of the circuit. In each case, the truth tables were verified to be correct.

4 Sources of Error