CECS 225

Lab 2

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Section 1: RCA8 Verilog module source

```
`timescale 1ns / 1ps

module RCA8(A_8, B_8, Cin, Cout, S_8 );
   input [7:0] A_8;
        input [7:0] B_8;
   input Cin;
   output Cout;
   output [7:0] S_8;

        wire c0, c1, c2, c3, c4, c5, c6;

        FullAdder fa0( .FA_A(   A_8[0]   ),
                                        .FA_B(   B_8[0]   ),
                                        .Cin(    Cin      ),
                                        .FA_S(   S_8[0]   ),
                                        .Cout(   c0       )
                                        );

        FullAdder fa1( .FA_A(   A_8[1]   ),
                                        .FA_B(   B_8[1]   ),
                                        .Cin(    c0       ),
                                        .FA_S(   S_8[1]   ),
                                        .Cout(   c1       )
                                        );

        FullAdder fa2( .FA_A(   A_8[2]   ),
                                        .FA_B(   B_8[2]   ),
```

```
                                .Cin(    c1      ),
                                .FA_S(   S_8[2]  ),
                                .Cout(   c2      )
                                );

FullAdder fa3( .FA_A(   A_8[3]  ),
                                .FA_B(   B_8[3]  ),
                                .Cin(    c2      ),
                                .FA_S(   S_8[3]  ),
                                .Cout(   c3      )
                                );

FullAdder fa4( .FA_A(   A_8[4]  ),
                                .FA_B(   B_8[4]  ),
                                .Cin(    c3      ),
                                .FA_S(   S_8[4]  ),
                                .Cout(   c4      )
                                );

FullAdder fa5( .FA_A(   A_8[5]  ),
                                .FA_B(   B_8[5]  ),
                                .Cin(    c4      ),
                                .FA_S(   S_8[5]  ),
                                .Cout(   c5      )
                                );

FullAdder fa6( .FA_A(   A_8[6]  ),
                                .FA_B(   B_8[6]  ),
                                .Cin(    c5      ),
                                .FA_S(   S_8[6]  ),
```

```
                                        .Cout(   c6      )
                                        );

        FullAdder fa7( .FA_A(   A_8[7]   ),
                                        .FA_B(   B_8[7]   ),
                                        .Cin(    c6       ),
                                        .FA_S(   S_8[7]   ),
                                        .Cout(   Cout     )
                                        );



endmodule
```

Section 2: RCA8 Verilog Test Fixture

```
`timescale 1ns / 1ps

module RCA8_Tester;

	// Inputs
	reg [7:0] A_8;
	reg [7:0] B_8;
	reg Cin;

	// Outputs
	wire Cout;
	wire [7:0] S_8;

	// Instantiate the Unit Under Test (UUT)
	RCA8 uut (
		.A_8(A_8),
		.B_8(B_8),
		.Cin(Cin),
		.Cout(Cout),
		.S_8(S_8)
	);

	initial begin
		// test case 0
		Cin = 0;
		A_8 = 12;
		B_8 = 34;
		#10;
```

```
// test case 1
Cin = 0;
A_8 = 55;
B_8 = 170;
#10;

// test case 2
Cin = 0;
A_8 = 72;
B_8 = 27;
#10;

// test case 3
Cin = 0;
A_8 = 80;
B_8 = 08;
#10;

// test case 4
Cin = 1;
A_8 = 12;
B_8 = 34;
#10;

// test case 5
Cin = 1;
A_8 = 55;
B_8 = 170;
#10;
```

```
        // test case 6
        Cin = 1;
        A_8 = 72;
        B_8 = 27;
        #10;

        // test case 7
        Cin = 1;
        A_8 = 80;
        B_8 = 08;
        #10;
        $stop;
    end

endmodule
```

Section 3:


60.569 ns
66.667 ns
Name
Value
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80 ns
Cout
0
S_8[7:0]
100
46
225
99
88
47
226
100
89
A_8[7:0]
72
12
55
72
80
12
55
72
80
B_8[7:0]
27
34
170
27
8
34
170
27
8
Cin
1